U_FPGA
FPGA.SchDoc

C_SODIMM
SODIMM.SchDoc

U_CLOCK
CLOCK.SchDoc

C_POWER
POWER.SchDoc

U_CONN
CONN.SchDoc

U_CPLD
CPLD.SchDoc

PM1
FIDU-DOT - small

PM2
FIDU-DOT - small

PM3
FIDU-DOT - small

PM4
FIDU-DOT - small

PM5
FIDU-DOT - small

PM6
FIDU-DOT - small

LOGO1
TE Logo PRINT Layer

Serial
Serialnumber 6.3 x 6.3mm

LOGOPRINT
null
DDR3 CK1 and DDR3_CLK were swapped
CHANGES REV01 to REV02:

1) added C87, C88 4.7\(\mu\)F
2) C154 increment from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)