Overview

The FPGA Micromodule integrates a leading edge Spartan-3 FPGA, an USB2.0 transceiver, EEPROM, configuration Flash and power supply on a tiny footprint. A large number of configurable I/Os are provided via B2B mini-connectors. The majority of I/O voltages can be user-defined (16 x 3.3V / 6 x 2.5V / 98 x user configurable 1.2 to 3.3V). Thus, the Micromodule is ideally suited for battery-powered and small-sized Applications.

For using as an OEM module, Trenz Electronic provides support to integrate the Micromodule with your application.

In combination with our carrier boards, it serves as a powerful system widely used for educational and research activities.

Specification

- Xilinx Spartan-3 FPGA XC3S400-4FT256C or XC3S1000-4FT256C
- user accessible Xilinx Platform-Flash XCF02 or XCF04 for configuration
- USB 2.0 UTMI USB3250
- serial EEPROM 16kBit
- Single 5V power supply input via USB, or from a carrier board
- 120 I/Os available on B2B connectors
- Evenly spread GND Pins on B2B connectors, for good EMC characteristics
- 1 LED
- 1 Pushbutton
- Programming is implemented via JTAG.

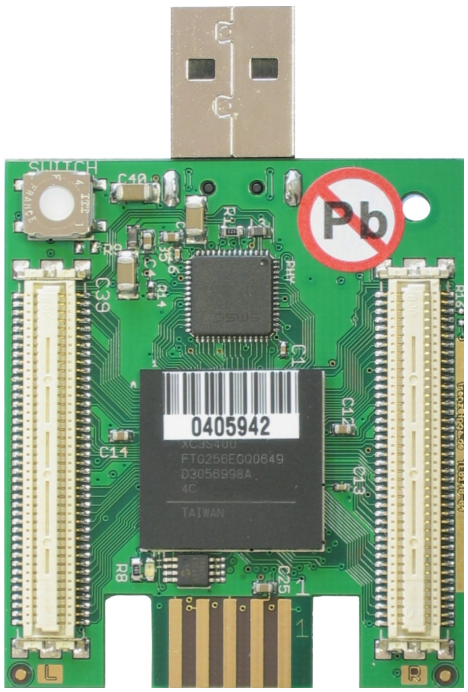

Figure 1: Micromodule Front Side

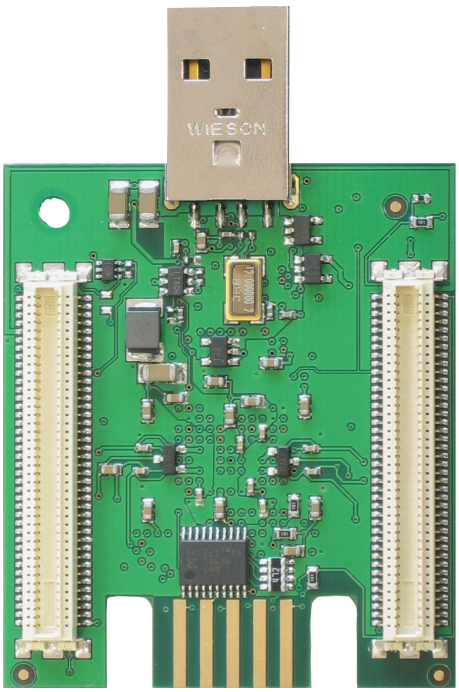

Figure 2: Micromodule Bottom Side

Details

Board Dimensions

- Connector spacing: 34mm
- PCB size: 50,7mm x 43,6mm

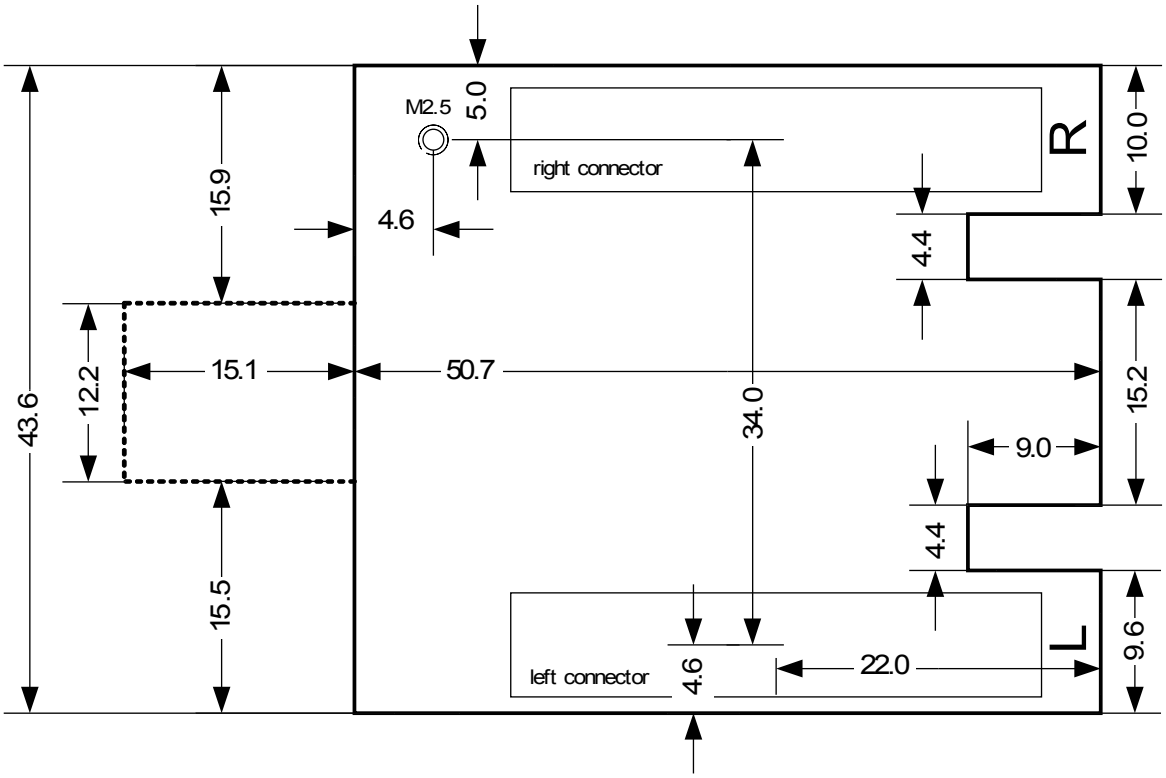

Figure 3: Dimensions in mm

Board Stacks

Two or more boards of revision 4.0 can be stacked for projects that require more than one FPGA. In the JTAG chain the bottom board appears first. The pins RL1 and RL2 are crossed between top or bottom connectors so are pins LR1 and LR2. This can be used by the FPGA to detect if it is on the top or bottom board that one of these pins are connected to different values by the base boards.

Alternatively an FPGA can use this to select between a device on the base board

and the other FPGA when communicating with shared pins.

Power supply

5V DC-powered:

A single 5V DC power supply is necessary. The power is usually supplied over the 5V pins on the B2B connectors (See Table 8). Minimum input voltage is 3.6V.

USB-powered:

If the module is equipped with an USB connector, and the module is connected to the USB Bus, power is supplied via the USB connector. In this case, other components (e.g. extension or carrier boards) may also use USB power via the B2B con-

nectors.

Attention: The USB Power pins, and the 5V pins on the B2B connectors are directly connected. Never apply 5V to the B2B connector, if the USB powered option is used. Special care must be taken to limit currents with respect to the USB specification.

Onboard voltage regulators provide the necessary supply rails for all components of the Micromodule.

The following voltages and currents are available for the FPGA and can be shared with a baseboard. Please note, that power consumption of the FPGA is highly dependent on the design actually loaded. So please use a tool like Xilinx Xpower to determine the expected power consumption.

- 1,2V, 600mA
- 1,8V see Figure 4
- 2,5V see Figure 5
- 3,3V see Figure 6

If more power is required for the FPGA core, the 1,2V regulator can be shut off by pulling the ENABLE12 signal low. Then an alternative 1,2V supply must be provided on the expansion connectors.

Even if the provided voltages of the module are not used on a baseboard, it is recommended to bypass them with 100nF capacitors.

Stacked Boards

Each Board supplies itself by its own voltage regulators, so only one 5V source is required for the whole stack. The other voltage lines are not connected between the separate boards.

The 1.2V core voltage of the first board can be driven externally by tying pin LL2 to ground. But all other Boards have to use their own regulators.

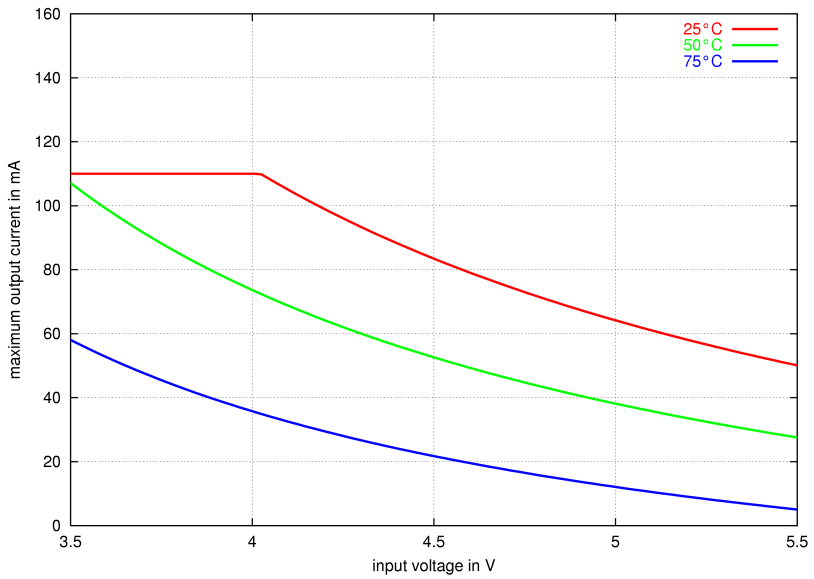

Figure 4: Available 1.8V power

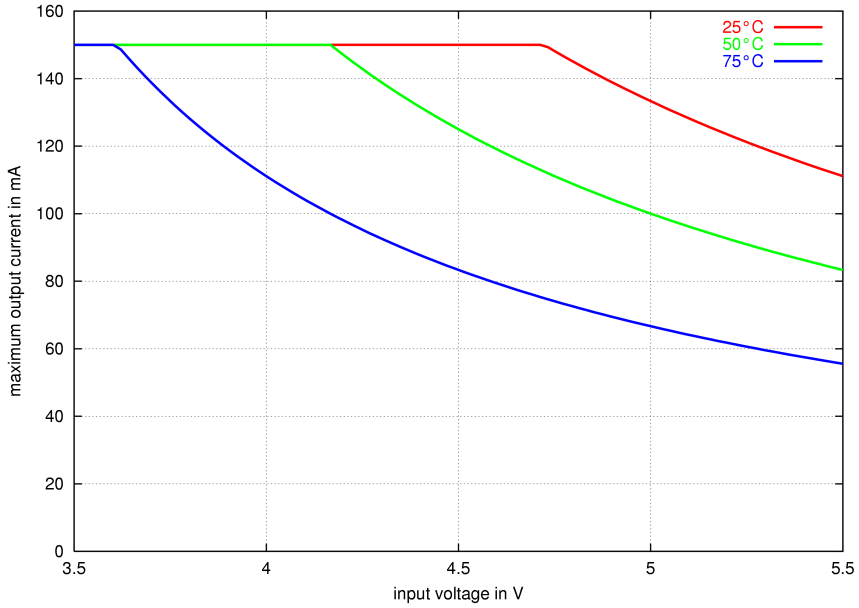

Figure 5: Available 2.5V power

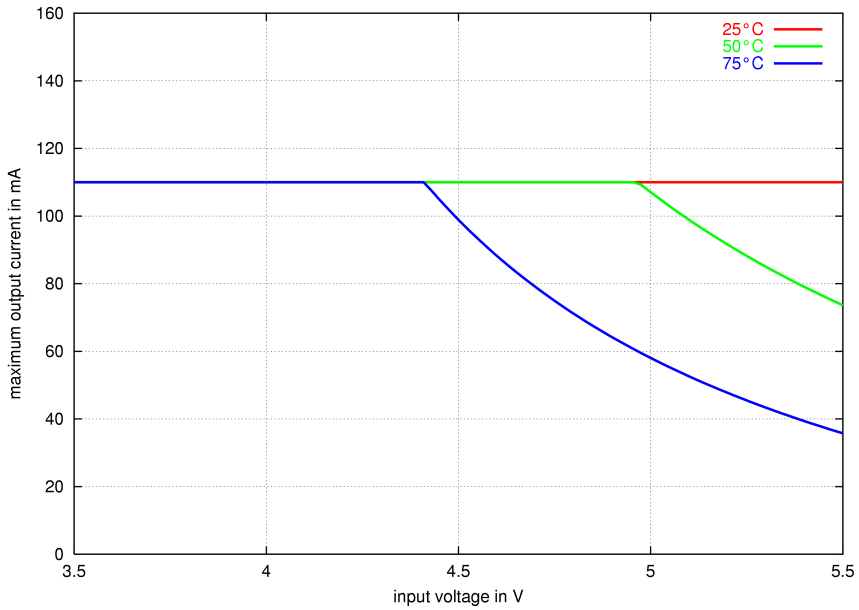

Figure 6: Available 3.3V power

IO Banks Power Supply

VCCIO for the different FPGA IO Banks are fixed for Banks 0,1,4 and 5. VCCIO for Banks 2,3,6 and 7 can be connected externally over the B2B connectors. If certain banks are not needed, the corresponding VCCIO can be left open.

Bank	Supply Voltage
0	3,3V
1	3,3V
2	VCCIO2
3	VCCIO3
4	3,3V
5	2,5V
6	VCCIO6
7	VCCIO7

Table 1: IO Banks Power Supply

IO Signals

120 IO signals are available on B2B connectors:

- 18 x 3.3V
- 8 x 2.5V
- 92 x configurable from 1.2V to 3.3V in four banks

Warning: Spartan-III IO's are not 5V tolerant. Applying more than 3.6V to any Pin, results in a damaged FPGA.

Differential Pairs

There are 35 differential pairs routed to adjacent pins on the connectors and routed pairwise. These can be used for high speed signaling. There are additional differential pairs that are either not routed in pairs or not routed to adjacent connector pins. These can be used to reduce EMI with medium speed signals.

Table 2 lists the differential pairs. They belong to three groups.

Differential pairs marked as "top" are routed as 0.12mm wires on the top layer over a contiguous supply layer. These signals have a maximum length of 16mm. The impedance is mostly around 130 ohms but there can be sections of up to 5mm with an impedance as high as 170 ohms.

Pairs marked as L3 are routed as 0.13mm wires on layer 3 along a contiguous supply layer. These signals have a length of up to 20mm. Because they are additionally partially adjacent to supply planes on layer 4 the impedance of these signals is less controlled. The impedance is in the range of 90 ohms to 150 ohms but mostly falls into the lower end of this range.

The other signals runs partially on top but contain a layer change to layer 3. They are referenced to the same supply plane but change their impedance at the layer change which makes them less desirable for high speed signaling.

Termination Resistors on Bank5

On Bank 5 VRP is connected with a reference resistor to GND and VRN to 2.5V. The resistors are 100 Ohm each.

Pair	P	N	Group	Mismatch ca. [mm]	Comment
17_2	RL8	RL7	Top	1	
20_2	RL12	RL11	Top	<1	
22_2	RL14	RL13	Top	<1	
24_2	RL16	RL15	Top	<1	
39_2	RL20	RL19	Top	1	
40_2	RL21	RL22	Top	1	
22_3	RL28	RL29	Top	<1	
20_3	RL32	RL33	Top	<1	
21_3	RL35	RL34	Top	<1	
17_3	RL38	RL37	Top	2	
30_1	RR8	RR7	L3	2	
21_2	RR13	RR14	L3	1	
23_2	RR15	RR16	L3	1	
39_3	RR18	RR19	L3	2	
23_3	RR22	RR21	L3	1	
16_3	RR26	RR27		3	5mm on top
32_4	RR38	RR37		1	GCLK, 8mm on top
29_0	LL8	LL9	L3	2	
21_7	LL13	LL14	L3	1	
23_7	LL15	LL16	L3	3	2mm spacing
39_6	LL19	LL18	L3	2	
23_6	LL22	LL21	L3	1	
27_5	LL29	LL30	L3	<1	
32_5	LL37	LL38	L3	1	GCLK
17_7	LR7	LR8	Top	2	
20_7	LR11	LR12	Top	2	
22_7	LR13	LR14	Top	2	
24_7	LR15	LR16	Top	2	
39_7	LR22	LR21	Top	1	
40_6	LR24	LR25	Top	2	
22_6	LR29	LR28	Top	<1	
20_6	LR33	LR32	Top	<1	
21_6	LR34	LR35	Top	2	
17_6	LR37	LR38	Top	2	

Table 2: Differential Pairs

LED

The LED is lit when 28N_5 (Pin N6) is pulled low.

Pushbutton

The function of the pushbutton is configurable by two solder jumpers. See Figure 7 for location of these Jumpers (actually resistors).

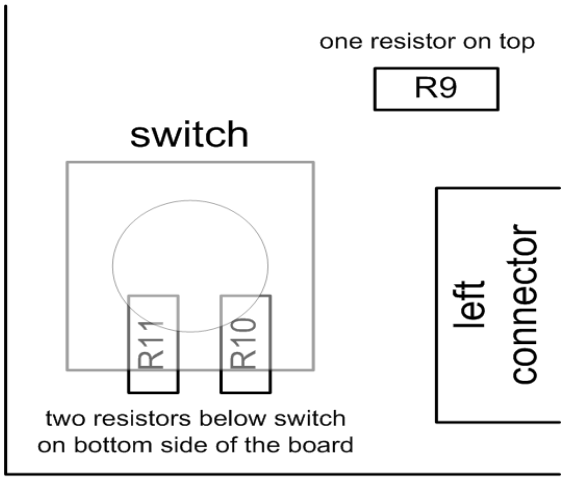

Figure 7: Location of resistors

In the default configuration the button pulls pin 31N_0 low when pressed. The same signal is also connected to pin L7 on the left connector. See Figure 8 for details.

In the alternative configuration the PROGRAM pin is pulled down by the button. See Figure 9 for details.

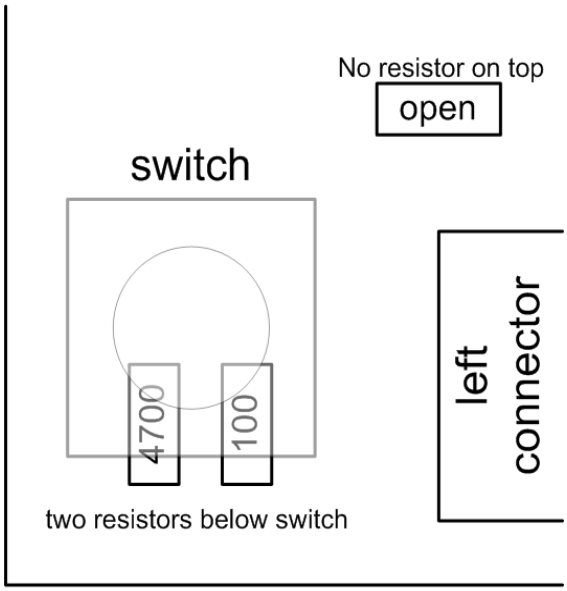

Figure 8: Default configuration

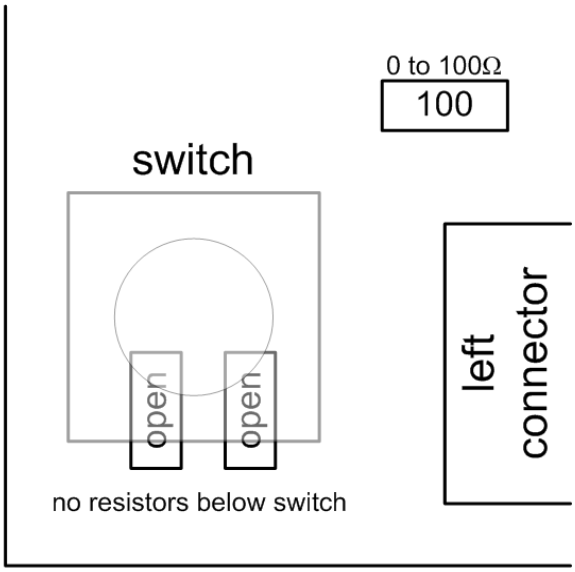

Figure 9: Alternate configuration

JTAG chain and configuration

The first device in the JTAG chain is the configuration Flash followed by the FPGA.

JTAG signals are available on the dedicated edge connector.

Pin	Signal
1	GND
2	Mode
3	2.5V (Vref)
4	TCK
5	GND
6	TMS
7	3.3V (VCC)
8	TDI
9	GND
10	TDO

Table 3: JTAG Connector

All JTAG signal levels are 2.5V LVTTL. Therefore the 2.5V Vref on the connector can be used to power the output drivers of the JTAG cable. 3.3V VCC can be used to power the remaining circuitry of the download cable.

The MODE input should be pulled to 2.5V by the download cable to select JTAG configuration.

To improve the signal quality both the 2.5V and the 3.3V pins should be bypassed to ground by the download cable even if they are not used by the cable. All GND pins should be connected.

The serial Flash for storing configuration data is accessible from the FPGA. It can be read out over the lines shown in Table 4.

To connect the JTAG Programmer see Figure 10.

Signal	Pin	Direction (FPGA)
Flash_CLK	P13	Out
Flash_OE/RESET	N9	Out
Flash_DO	M11	IN

Table 4: Flash Signals

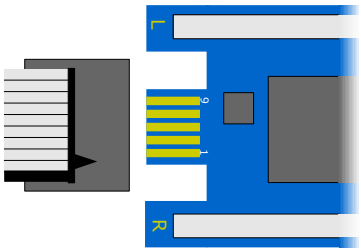

Figure 10: Connecting the Programmer

EEPROM

A serial EEPROM with 64kBit memory is added in revision 01 and higher. Table 5 shows the available signals.

Signal	Pin	Direction (FPGA)
EEPROM_CS	T3	Out
EEPROM_CLK	R3	Out
EEPROM_DI	T5	Out
EEPROM_DO	T7	IN

Table 5: EEPROM Signals

USB2.0 UTMI Interface

The FPGA is connected to an USB2.0 physical layer interfaces chip USB3250 by SMSC. Use the LVCMOS33 IO standard on the FPGA to interface with these signals. When USB is not used, the control signals should always be driven to their default values from the FPGA.

Stacked Boards

The USB signals are not routed to the upper B2B connector, so a baseboard can connect only to the bottommost board in a stack.

Signal	Pin	Direction (FPGA)	Default
DATABUS16_8	B14	Out	0
RESET	B4	Out	0
XCVRSELCT	D6	Out	1
TERMSELECT	B6	Out	1
OPMODE1	C6	Out	0
LINESTATE0	A3	In	
LINESTATE1	A5	In	
CLKOUT	D9	In	
TXVALID	B12	Out	0
TXREADY	A14	In	
VALIDH	B13	Bidir	
RXVALID	A12	In	
RXACTIVE	C11	In	
RXERROR	C12	In	
D0	A13	Bidir	
D1	B11	Bidir	
D2	C10	Bidir	
D3	B10	Bidir	
D4	A10	Bidir	
D5	C9	Bidir	
D6	A9	Bidir	
D7	B8	Bidir	
D8	A8	Bidir	
D9	C8	Bidir	
D10	C7	Bidir	
D11	A7	Bidir	
D12	B7	Bidir	
D13	B5	Bidir	
D14	C5	Bidir	
D15	A4	Bidir	
OPMODE0	T10	OUT	0
SUSPENDN	3.3V		

Table 6: UTMI Interface connection

Clock supply

The USB interface chip can provide a 60MHz clock signal to pin D9 of the FPGA. In order to use this clock the USB3250 control signals must be driven according to the previous section. DATABUS16_8 can also be set to '1' to provide a 30MHz clock instead.

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from this signal.

B2B connectors

The following connector pinouts are valid for the connectors on the top of the board.

The bottom side differs in that Pins L2 and L1 are swapped on the right connector. Also some signals are not available on the upper connector.

Likewise pins R2 and R1 are swapped on the left connector.

This way these signals can be used to select boards connected to the top or bottom.

See Figure 1 for location and orientation of the B2B connectors.

FPGA	Left	Pin	right	FPGA
B16	01N_VRP_2	1	TDO	A15
D14	16P_2	2	TDI	A2
C15	16N_2	3	TCK	C14
C16	01P_VRN_2	4	TMS	C13
-	GND	5	5V	-
E13	19N_2	6	5V	-
D15	17N_2	7	30N_1	D10
D16	17P_VREF_2	8	30P_1	E10
E14	19P_2	9	28N_1	D11
-	GND	10	IO_D12_VREF_1	D12
E15	20N_2	11	GND	-
E16	20P_2	12	28P_1	E11
F14	22N_2	13	21P_2	F13
F15	22P_2	14	21N_2	F12
G14	24N_2	15	23P_2	G13
G15	24P_2	16	23N_VREF_2	G12
-	GND	17	3,3V[1]	-
G16	IO_G16_2	18	39P_3	J13
H13	39N_2	19	39N_3	J14
H14	39P_2	20	VCCIO2	-
H16	40P_VREF_2	21	23N_3	K12
H15	40N_2	22	23P_VREF_3	L12
-	GND	23	24P_3	K13
J16	40N_VREF_3	24	1,8V[1]	-
K14	24N_3	25	01P_VRN_3	R16
K15	IO_K15_3	26	16P_3	P14
K16	40P_3	27	16N_3	P15
L14	22P_3	28	VCCIO3	-
L15	22N_3	29	IO_T14_4	T14
-	2.5V[1]	30	01N_VRP_4	R13
M14	19N_3	31	3,3V[1]	-
M15	20P_3	32	01P_VRN_4	T13
M16	20N_3	33	25P_4	R12
L13	21N_3	34	IO_T12_4	T12
M13	21P_3	35	GND	-
-	GND	36	28P_4	R11
N16	17N_3	37	32N_GCLK1_4	R9
N15	17P_VREF_3	38	32P_GCLK0_4	T9
N14	19P_3	39	1,2V[1]	-
P16	01N_VRP_3	40	1,2V[1]	-

Table 7: Right connector (1)- only available on the bottom connector

FPGA	Left	Pin	right	FPGA
P3/P4	MODE	1	01P_VRN	B1
-	ENABLE12[1]	2	16P_VREF	C3
-	USB_DM[1]	3	16N_7	C2
-	USB_DP[1]	4	01N_VRP_7	C1
-	5V	5	GND	-
-	5V	6	19P_7	D3
D8	31N_0	7	17P_7	D2
D7	29P_0	8	17N_7	D1
E7	29N_0	9	19N_VREF_7	E3
D5	IO_D5_VREF_0	10	PROGRAM	B3
-	GND	11	20P_7	E2
E6	27N_0	12	20N_7	E1
E4	21P_7	13	22P_7	F3
F4	21N_7	14	22N_7	F2
F5	23P_7	15	24P_7	G4
G5	23N_7	16	24N_7	G3
-	3,3V[1]	17	GND	-
J4	39N_6	18	40P_7	G1
J3	39P_6	19	IO_G2_7	G2
-	VCCIO7	20	40N_VREF_7	H1
K5	23N_6	21	39N_7	H3
K4	23P_6	22	39P_7	H4
K3	24N_VREF_6	23	GND	-
-	1,8V[1]	24	40P_VREF_6	J1
M4	19N_6	25	40N_6	J2
P2	16N_6	26	24P_6	K2
R1	01N_VRP_6	27	IO_K1_6	K1
-	VCCIO6	28	22N_6	L3
P5	27P_5	29	22P_6	L2
R5	27N_VREF_5	30	2.5V[1]	-
-	3,3V[1]	31	19P_6	M3
P6	29P_5	32	20N_6	M2
R6	29N_5	33	20P_6	M1
P7	IO_P7_5	34	21P_6	L4
-	GND	35	21N_6	L5
T8	IO_T8_VREF_5	36	GND	-
N8	32P_GCLK2_5	37	17P_VREF_6	N1
P8	32N_GCLK3_5	38	17N_6	N2
-	1,2V[1]	39	16P_6	N3
-	1,2V[1]	40	01P_VRN_6	P1

Table 8: Left connector (1)- only available on the bottom connector

Changes to Revision 00

- Spartan-III devices with more logic cells available
- Stackable up to two devices
- Serial EEPROM
- Access to serial Flash
- RR17 and RR31 are now connected to 3.3V
- PROGRAM pin is available on LR10
- MicroMatch connector for JTAG is removed to provide stackability

Changes to Revision 01

- Screw hole added
- Voltage Regulator for 1.2V provides 600 mA
- On the upper B2B connector, the following signals are no longer connected:
  - 3.3V
  - 1.8V
  - 2.5V
  - 1.2V
  - Enable12
  - USB_DM
  - USB_DP
- More than two boards can be stacked
- USB-Softconnect is provided by routing the signal OPMODE0 to the FPGA

Changes to Revision 2.01

- New USB Chip: USB3250

Ordering Details

Scope of Supply

- Micromodule

Order number

The Order Number is:

TE0140-04 for XC3S400-4 2MBit Flash

TE0140-04B for XC3S1000-4 4MBit Flash

History

Rev	Date	Who	Description
0.9	2004-06-09	TT	Created
0.91	2004-09-10	TT	B2B Connectors swapped
0.92	2004-11-02	TT	SUSPEND corrected
1.0	2004-12-20	TS	HW Rev. 01
1.01	2005-01-12	TS	Edge connector description
1.02	2005-01-17	TT	USB2.0 section revised
2.0	2005-05-30	TS	HW Rev. 02
2.01	2005-06-17	TT	Minor changes
4.0	2007-10-10	JS	HW Rev. 04
4.01	2008-01-21	TT	EEProm size

Table 9: History