Overview

The Prototyping Carrier Board provides low-cost connection and extension of the Spartan-3 Micromodule.

The Micromodule's signals, which are available on high-density, surface mount connectors, are routed to standard headers by the Prototyping Carrier Board.

Various JTAG connectors for compatibility with Xilinx parallel cable III and IV, as well as with the low cost Trenz Electronic JTAG Programmer are made available for easy attachment.

Flexible power supply, either via USB, or via a dedicated DC jack is possible.

Features

- All signals available on header w. 2.54mm (100mil) pitch
- Board supply via DC jack or USB
- JTAG header compatible to TE JTAG Programmer, Xilinx parallel cable III and IV
- Small form factor: 115x72mm (2,83 x 4,53 inch)

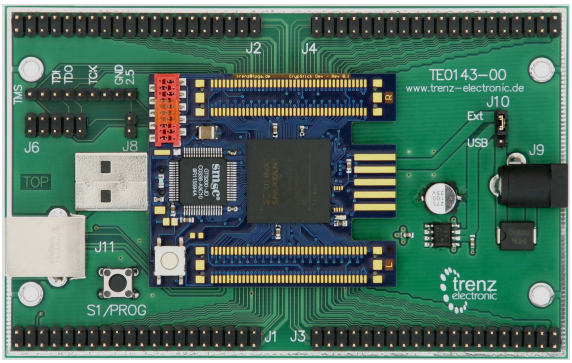

Figure 1: Board with Micromodule

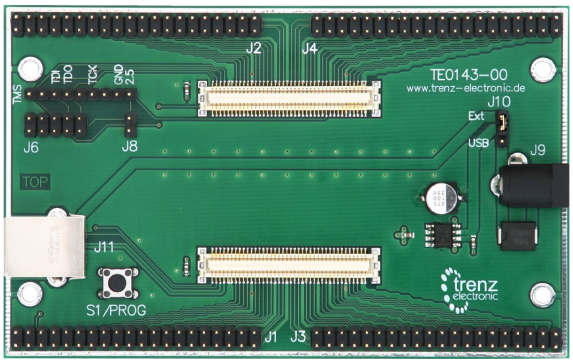

Figure 2: Board without Micromodule

Details

To locate the jumper and connectors see Figure 3.

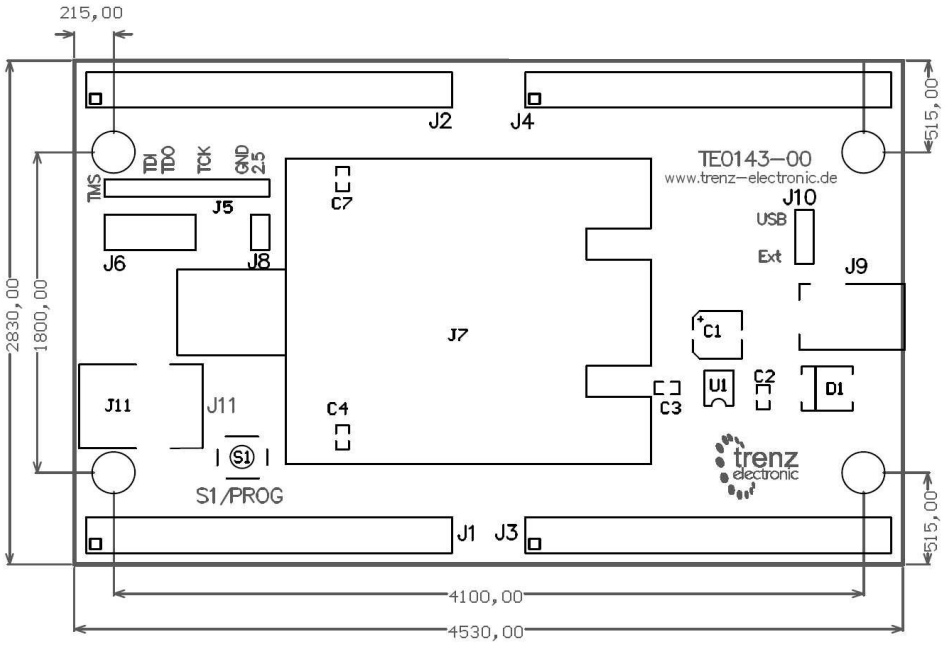

Figure 3: Component Side (dimensions in mil)

Power Supply

There are two option to supply power to the board. In either case there is a current limiting power switch in the path. Total current is limited to 700mA max. Further, the ramp-up time of the voltage is well defined. This is neccessary to meet the VCCIO ramp-up time needed by the FPGA. For more information see the Spartan-3 datasheet.

5V-DC powered

Set the Jumper J10 to EXT, and connect a 5V DC supply to the DC-Jack (J9).

USB powered

Set the Jumper J10 to USB, and connect a a standard USB cable.

Header Power Pins

Power pins on the IO headers can provide power to external circuits. The following voltages are generated by the Micromodule:

- 1.2V
- 1.8V
- 2.5V
- 3.3V

For more details of available power ratings, see the Micromodule's user's manual.

The 1.2V FPGA core supply pin can also be used to power the core external, if more current is neccessary than delivered by the onboard regulator. Again, see the Micromodule user's manual for more details.

IO BANKS Power Supply

VCCIO for Banks 2,3,6 and 7 can be connected externally over the connectors J1-J4. If certain banks are not needed, the corresponding VCCIO can be left open.

Bank	Pin	Voltage
J1	9,11	+5V
J1	33	+3.3V
J1	10, 21, 34	GND
J1	39	VCCIO7
J2	10,12	+5V
J2	34	+3.3V
J2	9, 19, 22 ,33	GND
J2	40	VCCIO2
J3	21	+3.3V
J3	20	+2.5V
J3	7	+1.8V
J3	37,39	+1.2V
J3	6, 29, 32	GND
J3	15	VCCIO6
J4	22	+3.3V
J4	19	+2.5V
J4	8	+1.8V
J4	40,38	+1.2V
J4	5, 30, 31	GND
J4	16	VCCIO3

Table 1: Power Supply Pins

Warning: Spartan-3 IO's are not 5V tolerant. Applying 5V to any pin, may cause damage to the FPGA.

JTAG Programming

There are two JTAG connectors available. J5 supports the older 9 pin Xilinx header. Table 2 shows the pin assignments.

Pin	Signal
1	VREF
2	GND
3	-
4	TCK
5	-
6	TDO
7	TDI
8	-
9	TMS

Table 2: 9 Pin JTAG Connector

For easy to use with Trenz Electronic JTAG Programmer a 10 pin header (J6) is added. By using it, the Prototyping Carrier Board supplies the JTAG Programmer with power over an additional voltage line (pin 7).

Pin	Signal
1	GND
2	MODE
3	VREF
4	TCK
5	GND
6	TMS
7	VCC
8	TDI
9	GND
10	TDO

Table 3: 10 PIN JTAG Connector

During programming, jumper J8 can be bridged, to switch the FPGA in JTAG only mode. If you use the 10 pin header with Trenz Electronic JTAG Programmer, the connection is made on the programmer by default. (see Table 3, pin 2.)

Please note, that the Micromodule won't

configure from Flash, if the jumper is set, or if the Trenz Electronic JTAG Programmer is connected.

USB Connector

The data lines are direct connected to the USB interface chip on the Micromodule.

Pushbutton

The pushbutton is connected to the prog line on module revision 01 (TE0140-01) and above. By pressing the button, the FPGA configuration will be loaded again from Flash. It has no function, when used with module Revision 00 (TE0140-00).

Note: If the Micromodule is stackable and owns high-density connectors on both solder and component side, you have the revision TE0140-01 and up.

PIN Assignments

PIN (J1)	Label	Signal	FPGA	PIN (J2)	Label	Signal	FPGA
1	-	-	-	1	RL1	16P 2	D14
2	LR1	16P VREF	C3	2	-	-	-
3	LL2	ENABLE12	-	3	RL2	01N VRP 2	B16
4	LR2	01P VRN 7	B1	4	-	-	-
5	-	-	-	5	RL3	16N 2	C15
6	LR3	16N 7	C2	6	-	-	-
7	-	-	-	7	RL4	01P VRN 2	C16
8	LR4	01N VRP 7	C1	8	-	-	-
9	+5V	-	-	9	GND	-	-
10	GND	-	-	10	+5V	-	-
11	+5V	-	-	11	RL6	19N 2	E13
12	LR6	19P 7	D3	12	+5V	-	-
13	LL7	31N 0	D8	13	RL7	17N 2	D15
14	LR7	17P 7	D2	14	RR7	30N 1	D10
15	LL8	29P 0	D7	15	RL8	17P VREF 2	D16
16	LR8	17N 7	D1	16	RR8	30P 1	E10
17	LL9	29N 0	E7	17	RL9	19P 2	E14
18	LR9	19N VREF 7	E3	18	RR9	28N 1	D11
19	LL10	IO D5VREF 0	D5	19	GND	-	-
20	LR10	Reserved	-	20	RR10	IO D12 VREF 1	D12
21	GND	GND	-	21	RL11	20N 2	E15
22	LR11	20P 7	E2	22	GND	-	-
23	LL12	27N 0	E6	23	RL12	20P 2	E16
24	LR12	20N 7	E1	24	RR12	28P 1	E11
25	LL13	21P 7	E4	25	RL13	22N 2	F14
26	LR13	22P 7	F3	26	RR13	21P 2	F13
27	LL14	21N 7	F4	27	RL14	22P 2	F15
28	LR14	22N 7	F2	28	RR14	21N 2	F12
29	LL15	23P 7	F5	29	RL15	24N 2	G14
30	LR15	24P 7	G4	30	RR15	23P 2	G13
31	LL16	23N 7	G5	31	RL16	24P 2	G15
32	LR16	24N 7	G3	32	RR16	23N VREF 2	G12
33	+3.3V LL17	3.3V	-	33	GND	-	-
34	GND	-	-	34	+3.3V RR17	3.3V	-
35	LL18	39N 6	J4	35	RL18	IO G16 2	G16
36	LR18	40P 7	G1	36	RR18	39P 3	J13
37	LL19	39P 6	J3	37	RL19	39N 2	H13
38	LR19	IO G2 7	G2	38	RR19	39N 3	J14
39	VCCIO7 LL20	VCCIO7	-	39	RL20	39P 2	H14
40	LR20	40N VREF 7	H1	40	VCCIO2 RR20	VCCIO2	-

Table 4: Connector J1 and J2

PIN (J3)	Label	Signal	FPGA	PIN (J4)	Label	Signal	FPGA
1	LL21	23N 6	K5	1	RL21	40P VREF 2	H16
2	LR21	39N 7	H3	2	RR21	23N 3	K12
3	LL22	23P 6	K4	3	RL22	40N 2	H15
4	LR22	39P 7	H4	4	RR22	23P VREF 3	L12
5	LL23	24N VREF 6	K3	5	GND	-	-
6	GND	-	-	6	RR23	24P 3	K13
7	+1.8V LL24	1.8V	-	7	RL24	40N VREF 3	J16
8	LR24	40P VREF 6	J1	8	+1.8V RR24	1.8V	-
9	LL25	19N 6	M4	9	RL25	24N 3	K14
10	LR25	40N 6	J2	10	RR25	01P VRN 3	R16
11	LL26	16N 6	P2	11	RL26	IO K15 3	K15
12	LR26	24P 6	K2	12	RR26	16P 3	P14
13	LL27	01N VRP 6	R1	13	RL27	40P 3	K16
14	LR27	IO K1 6	K1	14	RR27	16N 3	P15
15	VCCIO6 LL28	VCCIO6	-	15	RL28	22P 3	L14
16	LR28	22N 6	L3	16	VCCIO3 RR28	VCCIO3	-
17	LL29	27P 5	P5	17	RL29	22N 3	L15
18	LR29	22P 6	L2	18	RR29	IO T14 4	T14
19	LL30	27N VREF 5	R5	19	+2.5V RL30	2.5V	-
20	+2.5V LR30	2.5V	-	20	RR30	01N VRP 4	R13
21	+3.3V LL31	3.3V	-	21	RL31	19N 3	M14
22	LR31	19P 6	M3	22	+3.3V RR31	3.3V	-
23	LL32	29P 5	P6	23	RL32	20P 3	M15
24	LR32	20N 6	M2	24	RR32	01P VRN 4	T13
25	LL33	29N 5	R6	25	RL33	20N 3	M16
26	LR33	20P 6	M1	26	RR33	25P 4	R12
27	LL34	IO P7 5	P7	27	RL34	21N 3	L13
28	LR34	21P 6	L4	28	RR34	IO T12 4	T12
29	GND	-	-	29	RL35	21P 3	M13
30	LR35	21N 6	L5	30	GND	-	-
31	LL36	IO T8 VREF 5	T8	31	GND	-	-
32	GND	-	-	32	RR36	28P 4	R11
33	LL37	32P GCLK2 5	N8	33	RL37	17N 3	N16
34	LR37	17P VREF 6	N1	34	RR37	32N GCLK1 4	R9
35	LL38	32N GCLK3 5	P8	35	RL38	17P VREF 3	N15
36	LR38	17N 6	N2	36	RR38	32P GCLK0 4	T9
37	+1.2V LL39	1.2V	-	37	RL39	19P 3	N14
38	LR39	16P 6	N3	38	+1.2V RR39	1.2V	-
39	+1.2V LL40	1.2V	-	39	RL40	01N VRP 3	P16
40	LR40	01P VRN 6	P1	40	+1.2V RR40	1.2V	-

Table 5: Connector J3 and J4

Ordering Details

Package contents

- Prototyping Carrier Board
- Documentation CD-ROM including schematics

Order number

The order number is: TE0143-00

History

Rev	Date	Who	Description
0.9	2004-09-20	TS	created
0.10	2007-10-11	JS	Minor Changes

Table 3: History