Overview

The FPGA Micromodule integrates a leading-edge Spartan-3 FPGA, an USB2.0 transceiver, configuration Flash, SDRAM and power supply on a tiny footprint. A large number of configurable I/Os are provided via B2B mini-connectors.

For using as an OEM module, Trenz Electronic provides support to integrate the Micromodule with your application.

Specification

- Xilinx Spartan-3 FPGA XC3S1000-4FT256C
- user accessible Xilinx Platform-Flash XCF04 for configuration
- USB 2.0 UTMI GT3200
- MT48LC2M32B2P-7 SDRAM
- Single 5V power supply input via USB, or from a carrier board
- 55 I/Os available on B2B connectors
- Evenly spread GND Pins on B2B connectors, for good EMC characteristics
- 1 LED
- Programming is implemented via JTAG.

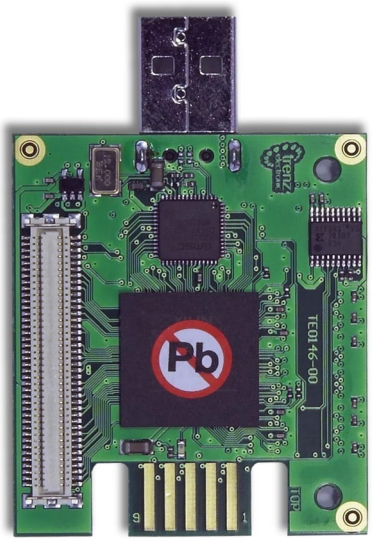

Figure 1: Micromodule Front Side

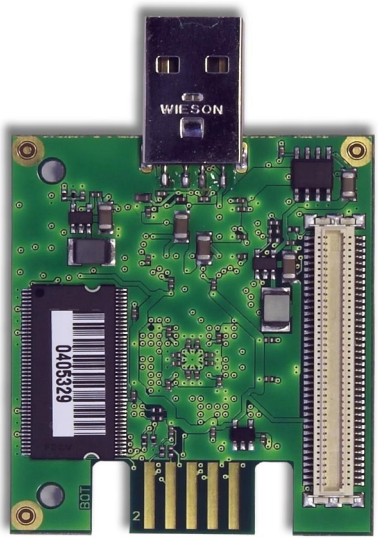

Figure 2: Micromodule Bottom Side

Details

Board Dimensions

- PCB size: 50,7mm x 43,6mm

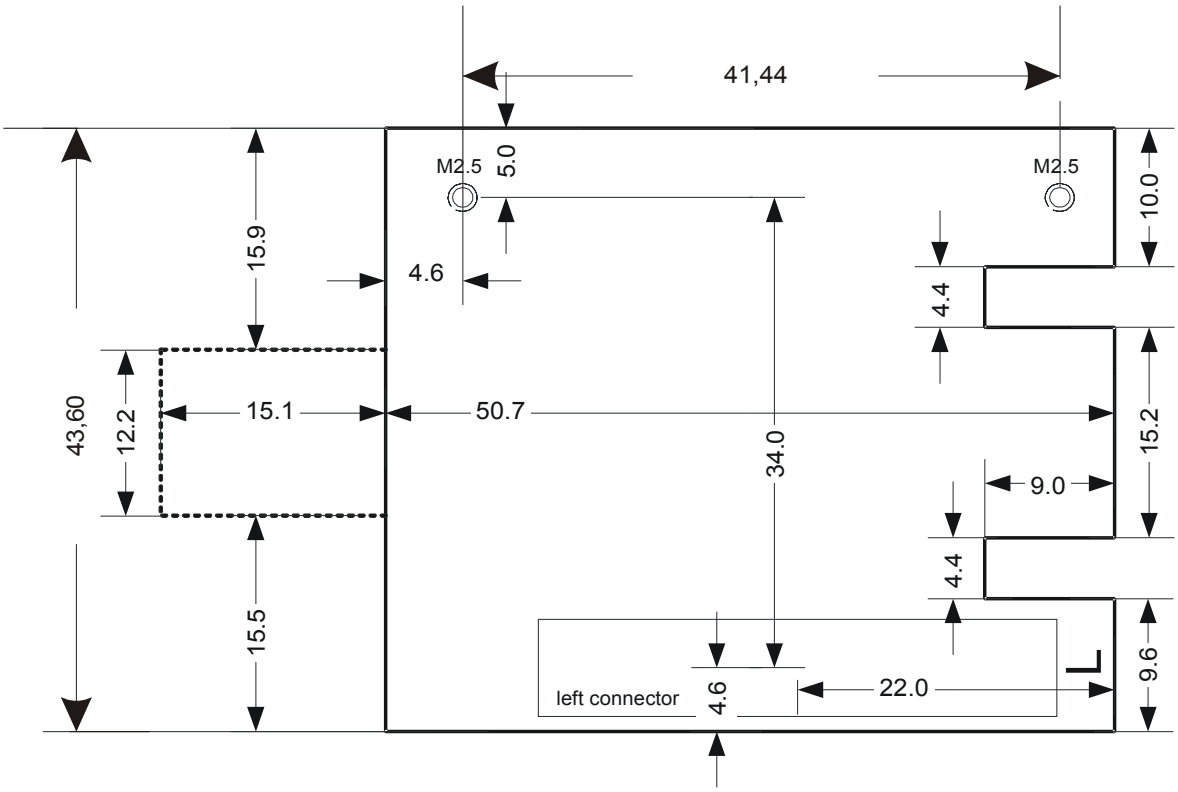

Figure 3: Dimensions in mm

Power supply

5V DC-powered:

A single 5V DC power supply is necessary. The power is usually supplied over the +VB (5V) pins on the B2B connectors (See Table 5). Minimum input voltage is 3.6V.

USB-powered:

If the module is equipped with an USB connector, and the module is connected to the USB Bus, power is supplied via the USB connector. In this case, other components (e.g. extension or carrier boards) may also use USB power via the B2B connectors.

Attention: The USB Power pins, and the +VB pins on the B2B connectors are directly connected. Never apply 5V to the B2B connector, if the USB powered option is used. Special care must be taken to limit currents with respect to the USB specification.

Onboard voltage regulators provide the necessary supply rails for all components of the Micromodule.

The following voltages and currents are available for the FPGA and can be shared with a baseboard. Please note, that power consumption of the FPGA is highly dependent on the design actually loaded. So please use a tool like Xilinx Xpower to determine the expected power consumption.

- 1.2V, 600mA
- 1.8V see Figure 4
- 2.5V see Figure 5
- 3.3V, 600mA

If more power is required for the FPGA core, the 1.2V regulator can be shut off by pulling the V12_EN signal low. Then an alternative 1.2V supply must be provided on the expansion connectors.

Even if the provided voltages of the module are not used on a baseboard, it is recommended to bypass them with 100nF capacitors.

IO Banks Power Supply

VCCIO for the different FPGA IO Banks are fixed to 3.3V for all banks.

IO Signals

55 IO signals are available on B2B connectors.

Warning: Spartan-III IO's are not 5V tolerant. Applying more than 3.6V to any Pin, results in a damaged FPGA.

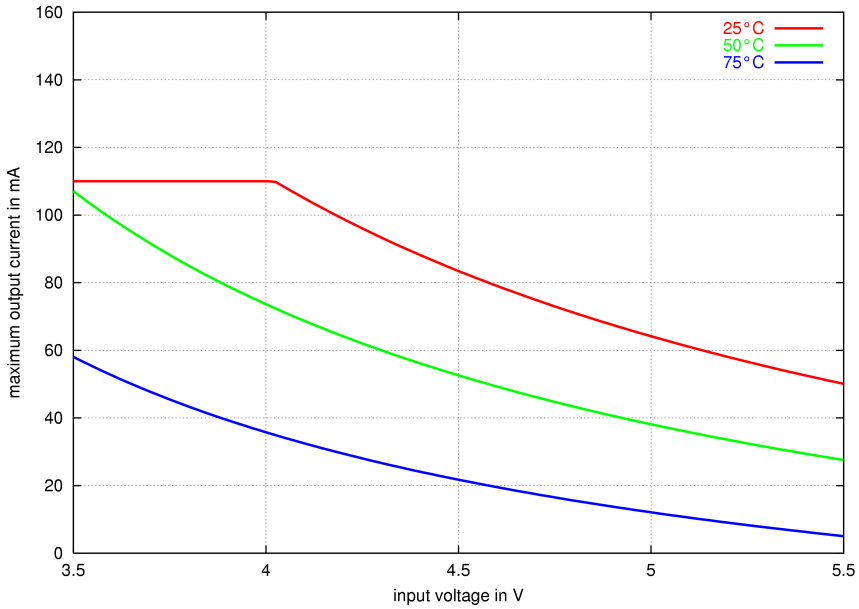

Figure 4: Available 1.8V power

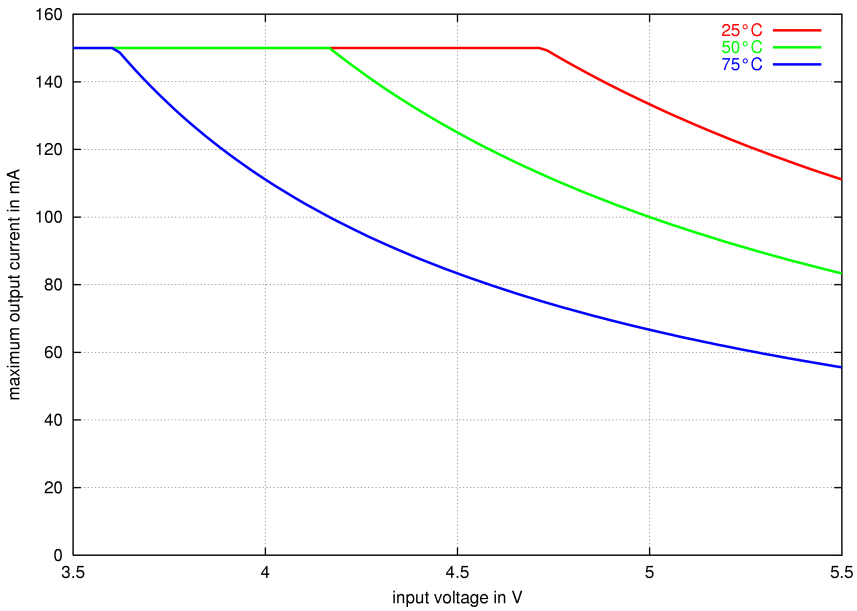

Figure 5: Available 2.5V power

Differential Pairs

There are 10 differential pairs routed to adjacent pins on the connectors and routed pairwise. These can be used for high speed signaling. There are additional differential pairs that are either not routed in pairs or not routed to adjacent connector pins. These can be used to reduce EMI with medium speed signals.

Table 1 lists the high speed differential pairs.

They are routed as 0.12 mm wires on the top layer over a contiguous supply layer. These signals have a maxim length of 20 mm. The impedance is mostly around 130 ohms but there can be sections of up to 5 mm with an impedance as high as 170 ohms.

Termination Resistors

On Banks 2, 3 and 4 VRP is connected with a reference resistor to GND and VRN to 3.3V. The resistors are 50 Ohm each.

Pair	P	N	Group	Mismatch ca. [mm]	Comment
19_7	LR8	LR9	TOP	2	Variable spacing
20_7	LR11	LR12	TOP	1	
22_7	LR13	LR14	TOP	1	
24_7	LR15	LR16	TOP	1	
29_7	LR22	LR21	TOP	3	
40_6	LR24	LR25	TOP	1	
22_6	LR29	LR28	TOP	2	
20_6	LR33	LR32	TOP	2	
21_6	LR34	LR35	TOP	1	
17_6	LR37	LR38	TOP	3	

Table 1: Differential Pairs

LED

The LED is lit when 28N_5 (Pin N6) is pulled low.

JTAG chain and configuration

The first device in the JTAG chain is the configuration Flash followed by the FPGA.

JTAG signals are available on the dedicated edge connector.

Pin	Signal
1	GND
2	Mode
3	2.5V (Vref)
4	TCK
5	GND
6	TMS
7	3.3V (VCC)
8	TDI
9	GND
10	TDO

Table 2: JTAG Connector

All JTAG signal levels are 2.5V LVTTL. Therefore the 2.5V Vref on the connector can be used to power the output drivers of the JTAG cable. 3.3V VCC can be used to power the remaining circuitry of the download cable.

The MODE input should be pulled to 2.5V by the download cable to select JTAG configuration.

To improve the signal quality both the 2.5V and the 3.3V pins should be bypassed to ground by the download cable even if they are not used by the cable. Alls GND pins should be connected.

The serial Flash for storing configuration data is accessible from the FPGA. It can be read out over the lines shown in Table 3.

Signal	Pin	Direction (FPGA)
Flash_CLK	P13	Out
Flash_OE/RESET	N9	Out
Flash_DO	M11	IN

Table 3: Flash Signals

To connect the JTAG Programmer see Figure 6.

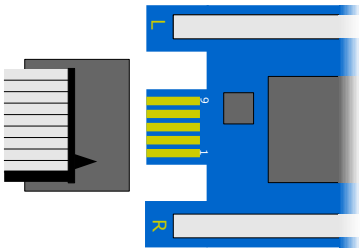

Figure 6: Connecting the Programmer

USB2.0 UTMI Interface

The FPGA is connected to an USB2.0 physical layer interfaces chip USB3250 by SMSC. Use the LVCMOS33 IO standard on the FPGA to interface with these signals. When USB is not used, the control signals should always be driven to their default values from the FPGA.

Note: The signals USB_DM and USB_DP of the USB PHY are normally connected to the USB Connector and not to the B2B Connector. Therefore if you want to connect these signals to the B2B connector, then you will need to solder two zero Ohm 0402 (1005) resistors (R13 and R14) as shown in Figure 7.

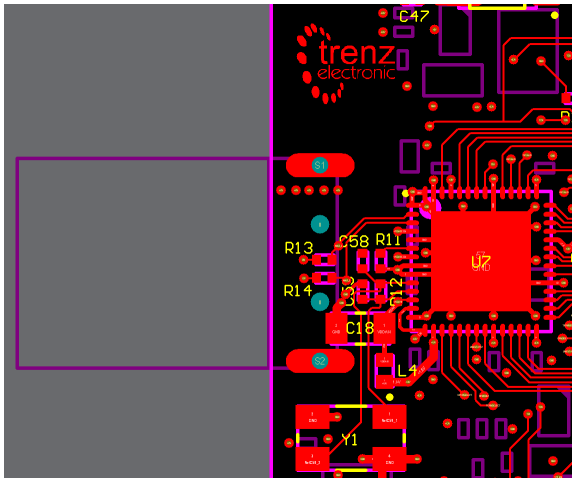

Figure 7: R13 and R14 resistors

Clock

The USB interface chip can provide a 60MHz clock signal to pin D9 of the FPGA. In order to use this clock the USB3250 control signals must be driven according to the previous section. DATABUS16_8 can also be set to '1' to provide a 30MHz clock instead.

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from this signal.

SDRAM

A Micron MT48LC2M32B2P-7, 64MB SDRAM, organized in 512K x 32 x 4 banks is connected directly to the FPGA.

B2B connectors

The following connector pinouts are valid for the connectors on the top and bottom of the board.

See Figure 1 for location and orientation of the B2B connectors.

Signal	Pin	Direction (FPGA)	Default
DATABUS16_8	B14	Out	0
RESET	B4	Out	0
XCVRSELCT	D6	Out	1
TERMSELECT	B6	Out	1
OPMODE1	C6	Out	0
LINESTATE0	A3	In	
LINESTATE1	A5	In	
CLKOUT	D9	In	
TXVALID	B12	Out	0
TXREADY	A14	In	
VALIDH	B13	Bidir	
RXVALID	A12	In	
RXACTIVE	C11	In	
RXERROR	C12	In	
D0	A13	Bidir	
D1	B11	Bidir	
D2	C10	Bidir	
D3	B10	Bidir	
D4	A10	Bidir	
D5	C9	Bidir	
D6	A9	Bidir	
D7	B8	Bidir	
D8	A8	Bidir	
D9	C8	Bidir	
D10	C7	Bidir	
D11	A7	Bidir	
D12	B7	Bidir	
D13	B5	Bidir	
D14	C5	Bidir	
D15	A4	Bidir	
OPMODE0	T10	OUT	0
SUSPENDN	3.3V		

Table 4: UTMI Interface connection

Pin	B2B	FPGA	Pin	B2B	FPGA
1	TDO	A15	2	MODE	P3/P4
3	TDI	-	4	V12_EN	-
5	TCK	C14	6	USB_DM	-
7	TMS	C13	8	USB_DP	-
9	GND	-	10	+VB (5V)	-
11	LR6 01P/VRN	B1	12	+VB (5V)	-
13	LR7 16P/VREF	C3	14	LL7 31N	D8
15	LR8 19P	D3	16	LL8 29P	D7
17	LR9 19N/VREF	E3	18	LL9 29N	E7
19	PROG	B3	20	LL10 01N/VRP	C1
21	LR11 20P	E2	22	GND	-
23	LR12 20N	E1	24	LL12 27N	E6
25	LR13 22P	F3	26	LL13 21P	E4
27	LR14 22N	F2	28	LL14 21N	F4
29	LR15 24P	G4	30	LL15 23P	F5
31	LR16 24N	G3	32	LL16 23N	G5
33	GND	-	34	+3.3V	-
35	LR18 40P	G1	36	LL18 39N	J4
37	LR19 IO_G2	G2	38	LL19 39P	J3
39	LR20 40N/VREF	H1	40	+3.3V	-
41	LR21 39N	H3	42	LL21 23N	K5
43	LR22 39P	H4	44	LL22 23P	K4
45	GND	-	46	LL23 24N/VREF	K3
47	LR24 40P/VREF	J1	48	+1.8V	-
49	LR25 40N	J2	50	LL25 19N	M4
51	LR26 24P	K2	52	LL26 16N	P2
53	LR27 IO_K1	K1	54	LL27 01N/VRP	R1
55	LR28 22N	L3	56	+3.3V	-
57	LR29 22P	L2	58	LL29 27P	P5
59	+2.5V	-	60	LL30 27N/VREF	R5
61	LR31 19P	M3	62	+3.3V	-
63	LR32 20N	M2	64	LL32 29P/VREF	P6
65	LR33 20P	M1	66	LL33 29N	R6
67	LR34 21P	L4	68	LL34 IO_P7	P7
69	LR35 21N	L5	70	GND	-
71	GND	-	72	LL36 IO/VREF	T8
73	LR37 17P/VREF	N1	74	LL37 32P/GCLK2	N8
75	LR38 17N	N2	76	LL38 32N/GCLK3	P8
77	LR39 16P	N3	78	+1.2V	-
79	LR40 01P/VRN	P1	80	+1.2V	-

Table 5: B2B connector

Ordering Details

Scope of Supply

- Micromodule
- CD-Rom with schematics, datasheets, this Document, and all available application notes

Order number

The Order Number is:

TE0146-00

History

Rev	Date	Who	Description
0.9	2006-02-21	TT	Created
1.0	2007-10-11	JS	Minor changes

Table 6: History