Prototyping Carrier Board for Industrial Micromodule

Overview

The Prototyping Carrier Board provides low-cost connection and extension of the Spartan-3E Industrial Micromodule.

The Micromodule signals, which are available on high-density, surface mount connectors, are routed to the standard headers of the Prototyping Carrier Board with a differential impedance of 100 ohm.

Three JTAG connectors are made available for easy attachment: a 6-pin connector for Xilinx flying leads cable, a 10-pin connector for the low cost Trenz Electronic JTAG Programmer TE0149, a 14-pin connector for Xilinx parallel cable III, IV and USB cable HW-USB.

Flexible power supply is possible through USB bus, dedicated DC jack or screw terminals.

Features

- All signals available on headers J1 to J4 with 2.54 mm (100 mil) pitch
- 42 differential pairs (for high-speed signals)
- 26 single-ended lines (for low- / medium-speed signals)
- Board supply via DC jack, USB bus or screw terminals
- JTAG header compatible to Xilinx flying leads cable, low cost Trenz Electronic JTAG Programmer TE0149, Xilinx parallel cable III, IV and USB cable HW-USB
- Small form factor: 115 x 70 mm

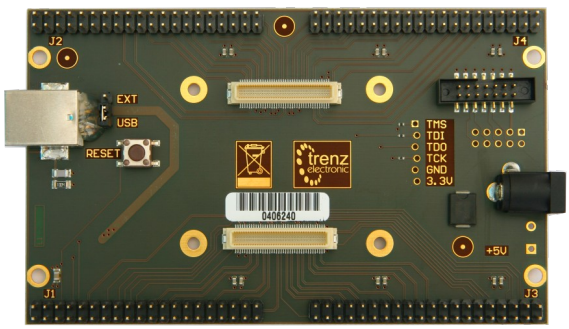


Figure 1: prototyping carrier board: top view without module.

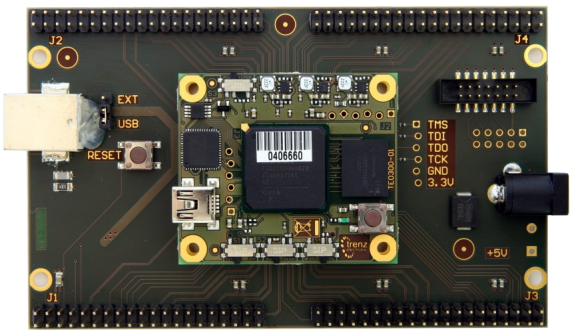


Figure 2: prototyping carrier board: top view with module.

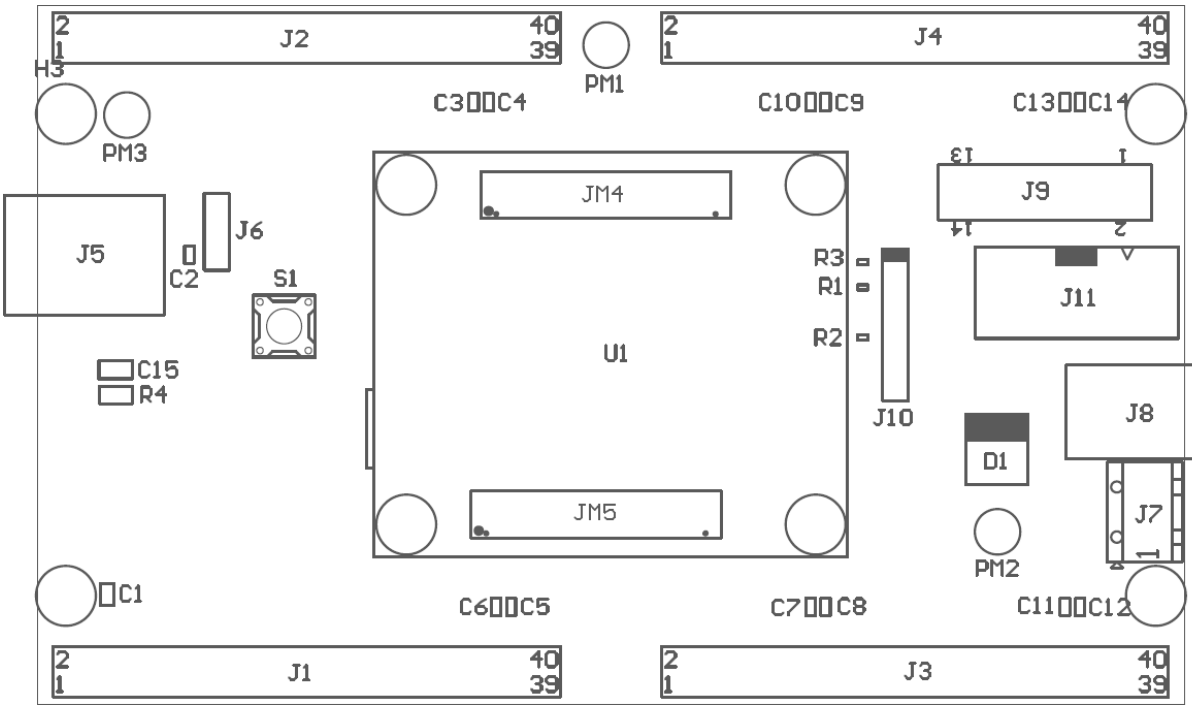


Figure 3: assemby diagram

Details

To locate the jumper and the connectors see Figure 3.

Warning! Take care to install the module only in the way shown in Figure 3.

Two quick ways to check this are to make sure that

- USB receptacles of both micromodule and carrier board are on their respective left side;
- mounting holes of the micromodule are in line with their respective ones on the carrier board.

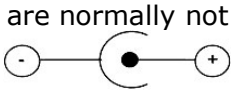
Power Supply

There are three mutually exclusive options to supply power to the board:

- 5 V DC via DC jack;
- 5 V DC via DC screw terminals;
- USB bus power supply.

5 V DC power supply

Set the Jumper J6 to EXT, and connect a 5 V DC supply to either the the 2.5 mm DC-Jack J8 (center positive) or the DC screw terminals J7 (lower terminal positive as hinted by the "+5V" label). Screw terminals J7 are normally not populated.



Both inputs are protected against polarity inversion by a cross bar diode D1.

USB powered

Set the Jumper J6 to USB and connect a standard USB cable to receptacle J5.

Header Power Pins

Power pins on the IO mating headers can provide power to external circuits. The following voltages are generated on the micromodule:

- 1.2 V,
- 2.5 V,

- 3.3 V.

For more details of available power ratings, see the Industrial Micromodule User Manual.

IO Banks Power Supply

VccIO for bank 0 can be connected externally through connector J2, pins 1-4. If bank 0 is not needed, VccIO can be left open.

Warning! If VccIO line is internally supplied, do NOT apply any voltage externally.

Warning! Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see Xilinx Answer AR#19146).

Single-ended lines

The prototyping carrier board has a total of 26 single ended lines routed to header connectors J1 to J4. These lines can be used for low-speed and medium-speed signals.

Differential Pairs

The prototyping carrier board has a total of 42 differential signal pairs routed with a differential impedance of 100 ohm to header connectors J1 to J4. These lines can be used for high speed signaling up to 666 Mbit/s per differential pair (see Xilinx Application Note XAPP485).

JTAG Programming

There are three JTAG connectors available: J9, J10, J11.

JTAG connector J9

Connector J9 is a 14-pin JTAG connector for Xilinx parallel cable III, IV and USB cable HW-USB. Vref is about 3.3 V.

Signal	Pin	Pin	Signal
GND	1	2	Vref
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	n.c.
GND	13	14	n.c.

Table 1: 14-pin JTAG connector J9.

JTAG connector J10

Connector J10 is a 6-pin JTAG connector for Xilinx flying leads cable.

Pin	Signal
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	Vref (3.3 V)

Table 2: 6-pin JTAG connector J10.

JTAG connector J11

For ease of use with the low-cost Trenz Electronic JTAG Programmer TE0149, 10-pin header J11 has been added. By using it, the Prototyping Carrier Board supplies power to the JTAG Programmer over an additional voltage line (pin 7).

Pin	Signal
1	GND
2	n.c.
3	Vref (3.3 V)
4	TCK
5	GND
6	TMS
7	Vcc (3.3 C)
8	TDI
9	GND
10	TDO

Table 3: 10 PIN JTAG Connector

USB Connector

The data lines are directly connected to the USB interface chip on the micromodule.

Pushbutton

The pushbutton is connected to the master reset line of the module. By pressing the button, the EZ-USB FX2 USB microcontroller and the FPGA are reset. The value of the master reset is overridden by switch S2 of the micromodule when it is set to "Reset (off)".

Order numbers

The order number for the standard carrier board is TE0303-01

The order number for the carrier board with unsoldered headers J1-J4 is TE0303-01NC.

For other kind of headers J1-J4, or for other header mounting options, please contact Trenz Electronic.

Document Change History

Rev	Date	Who	Description
1.00	2008-08-01	FDR	created
1.01	2009-02-19	FDR	fixed figure 2
1.02	2009-06-25	FDR	added differential pairs and single-ended lines details
1.03	2009-09-01	FDR	new assembly diagram and some minor changes
1.04	2011-11-28	FDR	revision from -00 to -01
1.05	2012-04-11	AIK	Added TE0630 pin-out

Table 3: document change history

Appendix

The following tables reports pin-out information of the multi-pin connectors J1, J2, J3 and J4 for TE0300 and TE0630 modules.

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	+Vb2b	-	I	I	-	+Vb2b	2
3	+Vb2b	-	I	I	-	+Vb2b	4
5	5Vout	-	O	I	-	/MR	6
7	RESET	-	O	O	-	/RESET	8
9	B3_L21_N	P1	IO	IO	P2	B3_L21_P	10
11	GND	-	-	-	-	GND	12
13	B2_IP_V4	V4	I	IO	T2	B3_IO_T2	14
15	B2_IO_L03	U4	IO	IO	M3	B3_IO_L18 N	16
17	B2_IO_V7	V7	IO	IO	U5	B2_IO_U5	18
19	GND	-	-	-	-	GND	20
21	B3_L22_N	P4	IO	IO	P3	B3_L22_P	22
23	B3_L20_N	N5	IO	IO	N4	B3_L20_P	24
25	B3_L23_P	R3	IO	IO	R2	B3_L23_N	26
27	GND	-	-	-	-	GND	28
29	B2_L06_N	V6	IO	IO	V5	B2_L06_P	30
31	B2_L04_P	R5	IO	IO	T5	B2_L04_N	32
33	B2_L05_N	P6	IO	IO	R6	B2_L05_P	34
35	3.3 V	-	O	O	-	3.3 V	36
37	B2_L07_P	N7	IO	IO	P7	B2_L07_N	38
39	B3_L17_P	L6	IO	IO	L5	B3_L17_N	40

Table 4: TE0300 J1 header pin-out

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	+Vb2b	-	I	I	-	+Vb2b	2
3	+Vb2b	-	I	I	-	+Vb2b	4
5	5Vout	-	O	I	-	/MR	6
7	RESET	-	O	O	-	/RESET	8
9	V3_IO_17	U3	IO	IO	V1	V3_IO_18	10
11	GND	-	-	-	-	GND	12
13	V2_IO_01	V15	I	IO	U1	V3_IO_16	14
15	V3_IO_22	AB3	IO	IO	Y2	V3_IO_21	16
17	V3_IO_27	U8	IO	IO	Y3	V3_IO_23	18
19	GND	-	-	-	-	GND	20
21	V3_IO_13	T1	IO	IO	T2	V3_IO_12	22
23	V3_IO_15	AB2	IO	IO	AA2	V3_IO_14	24
25	V3_IO_20	Y1	IO	IO	V2	V3_IO_19	26
27	GND	-	-	-	-	GND	28
29	V3_IO_25	AA4	IO	IO	AB4	V3_IO_24	30
31	V2_IO_01_P	AA6	IO	IO	AB6	V2_IO_01_N	32
33	V2_IO_02_N	AB7	IO	IO	Y7	V2_IO_02_P	34
35	3.3 V	-	O	O	-	3.3 V	36
37	V2_IO_03_P	AA8	IO	IO	AB8	V2_IO_03_N	38
39	V2_IO_10_N	Y6	IO	IO	W6	V2_IO_10_P	40

Table 6: TE0630 J1 header pin-out

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	VccIO	-	I	I	-	VccIO	2
3	VccIO	-	I	I	-	VccIO	4
5	B0_IO_C3	C3	IO	IO	C4	B0_IO_C4	6
7	B0_L24_N	B4	IO	IO	A4	B0_L24_P	8
9	B0_L23_N	D5	IO	IO	C5	B0_L23_P	10
11	B0_L20_P	B6	IO	IO	A6	B0_L20_N	12
13	GND	-	-	-	-	GND	14
15	GCLK_L13_N	B9	I	I	B8	GCLK_L13_P	16
17	B3_L02_N	D2	IO	IO	D1	B3_L02_P	18
19	B3_L01_P	C1	IO	IO	C2	B3_L01_N	20
21	B3_L07_P	G6	IO	IO	G5	B3_L07_N	22
23	GND	-	-	-	-	GND	24
25	B3_L03_N	E1	IO	IO	E2	B3_L03_P	26
27	B0_L19_P	F7	IO	IO	E7	B0_L19_N	28
29	B0_L21_N	E6	IO	IO	D6	B0_L21_P	30
31	B0_L18_N	D7	IO	IO	C7	B0_L18_P	32
33	3.3 V	-	O	O	-	3.3 V	34
35	B0_L17_N	F8	IO	IO	E8	B0_L17_P	36
37	B0_IO_A8	A8	IO	IO	A7	B0_IO_A7	38
39	GCLK_L14_N	D9	IO	IO	C9	GCLK_L14_P	40

Table 7: TE0300 J2 header pin-out

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	VccIO	-	I	I	-	VccIO	2
3	VccIO	-	I	I	-	VccIO	4
5	V3_IO_05	F7	IO	IO	C5	V0_IO_01_P	6
7	V0_IO_01	A4	IO	IO	A5	V0_IO_01_N	8
9	V0_IO_02_N	C6	IO	IO	D6	V0_IO_02_P	10
11	V0_IO_03_P	D7	IO	IO	C8	V0_IO_03_N	12
13	GND	-	-	-	-	GND	14
15	V0_CLK_03_N	A12	I	I	B12	V0_CLK_03_P	16
17	V3_IO_04	E5	IO	IO	F5	V3_IO_03	18
19	V3_IO_01	G6	IO	IO	G4	V3_IO_02	20
21	V3_IO_06	C4	IO	IO	D3	V3_IO_07	22
23	GND	-	-	-	-	GND	24
25	V3_IO_08	E6	IO	IO	D5	V3_IO_09	26
27	V0_IO_11_P	B6	IO	IO	A6	V0_IO_11_N	28
29	V0_IO_12_N	A7	IO	IO	C7	V0_IO_12_P	30
31	V0_IO_13_N	A8	IO	IO	B8	V0_IO_13_P	32
33	3.3 V	-	O	O	-	3.3 V	34
35	V0_IO_14_N	A9	IO	IO	C9	V0_IO_14_P	36
37	V3_IO_10	M7	IO	IO	D9	V0_IO_04_P	38
39	V0_CLK_04_N	C12	IO	IO	D11	V0_CLK_04_P	40

Table 8: TE0630 J2 header pin-out

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	B2_GCLK13	M9	IO	IO	U6	B2_IO_U6	2
3	GND	-	-	-	-	GND	4
5	B2_L10_N	T8	IO	IO	R8	B2_L10_P	6
7	B2_GCLK_L13_N	V9	IO	IO	U9	B2_GCLK_L13_P	8
9	B2_L18_N	N11	IO	IO	P11	B2_L18_P	10
11	B3_L19_P	M5	IO	IO	M6	B3_L19_N	12
13	2.5 V	-	O	O	-	2.5 V	14
15	B2_L20_N	R12	IO	IO	T12	B2_L20_P	16
17	B2_L19_N	V13	IO	IO	V12	B2_L19_P	18
19	B2_L22_N	R13	IO	IO	P13	B2_L22_P	20
21	B2_L24_P	T14	IO	IO	R14	B2_L24_N	22
23	GND	-	-	-	-	GND	24
25	B2_L09_P	P8	IO	IO	N8	B2_L09_N	26
27	B2_L21_N	P12	IO	IO	N12	B2_L21_P	28
29	B2_IO_P9	P9	IO	I	V14	B2_IP_V14	30
31	B2_IO_U13	U13	IO	IO	R9	B2_IO_R9	32
33	1.2 V	-	O	O	-	1.2 V	34
35	B2_IO_P10	P10	IO	IO	R11	B2_IO_R11	36
37	B2_IP_U8	U8	I	I	T7	B2_IP_T7	38
39	GND	-	-	-	-	GND	40

Table 9: TE0300 J3 header pin-out

pin	B2B name	FPGA pin	dir	dir	FPGA pin	B2B name	pin
1	V2_IO_02	AB12	IO	IO	Y4	V3_IO_26	2
3	GND	-	-	-	-	GND	4
5	V2_CLK_01_N	AB11	IO	IO	Y11	V2_CLK_01_P	6
7	V2_IO_04_P	W15	IO	IO	Y16	V2_IO_04_N	8
9	V2_IO_05_N	U14	IO	IO	T14	V2_IO_05_P	10
11	V2_IO_12_P	Y9	IO	IO	AB9	V2_IO_12_N	12
13	2.5 V	-	O	O	-	2.5 V	14
15	V2_IO_06_P	AA14	IO	IO	AB14	V2_IO_06_N	16
17	V2_IO_07_N	AB15	IO	IO	Y15	V2_IO_07_P	18
19	V2_IO_08_P	AA16	IO	IO	AB16	V2_IO_08_N	20
21	V2_IO_09_N	AB18	IO	IO	AA18	V2_IO_09_P	22
23	GND	-	-	-	-	GND	24
25	V2_CLK_02_N	AB10	IO	IO	AA10	V2_CLK_02_P	26
27	V2_IO_15_P	Y13	IO	IO	AB13	V2_IO_15_N	28
29	V2_IO_13_P	W11	IO	I	Y14	V2_IO_16_N	30
31	V2_IO_16_P	W14	IO	IO	W12	V2_IO_14_P	32
33	1.2 V	-	O	O	-	1.2 V	34
35	V2_IO_14_N	Y12	IO	IO	Y10	V2_IO_13_N	36
37	V2_IO_11_P	W9	I	I	Y8	V2_IO_11_N	38
39	GND	-	-	-	-	GND	40

Table 10: TE0630 J3 header pin-out

Pin	B2B name	FPGA pin	Dir	Dir	FPGA pin	B2B name	Pin
1	GCLK_L11_P	D10	IO	IO	E10	GCLK_L11_N	2
3	B0_L09_P	C11	IO	IO	D11	B0_L09_N	4
5	GND	-	-	-	-	GND	6
7	B0_IO_A11	A11	IO	IO	G9	B0_IO_G9	8
9	GCLK_L12_N	A10	IO	IO	B10	GCLK_L12_P	10
11	B0_L15_N	F9	IO	IO	E9	B0_L15_P	12
13	2.5 V	-	O	O	-	2.5 V	14
15	B0_IO_A12	A12	IO	IO	B11	B0_IO_B11	16
17	B0_L06_N	E12	IO	IO	F12	B0_L06_P	18
19	B0_IO_E13	E13	IO	IO	D13	B0_IO_D13	20
21	B0_L08_N	F11	IO	IO	E11	B0_L08_P	22
23	GND	-	-	-	-	GND	24
25	B0_L05_N	B13	IO	IO	A13	B0_L05_P	26
27	B0_L01_N	A16	IO	IO	B16	B0_L01_P	28
29	B0_L03_N	C14	IO	IO	D14	B0_L03_P	30
31	B0_L04_N	A14	IO	IO	B14	B0_L04_P	32
33	1.2 V	-	O	O	-	1.2 V	34
35	n.c.	-	-	-	-	n.c.	36
37	n.c.	-	-	-	-	n.c.	38
39	GND	-	-	-	-	GND	40

Table 11: TE0300 J4 header pin-out

Pin	B2B name	FPGA pin	Dir	Dir	FPGA pin	B2B name	Pin
1	V0_CLK_01_P	B10	IO	IO	A10	V0_CLK_01_N	2
3	V0_IO_15_P	C15	IO	IO	A15	V0_IO_15_N	4
5	GND	-	-	-	-	GND	6
7	V3_IO_11	M8	IO	IO	D8	V0_IO_04_N	8
9	V0_CLK_02_N	A11	IO	IO	C11	V0_CLK_02_P	10
11	V0_IO_05_N	A13	IO	IO	C13	V0_IO_05_P	12
13	2.5 V	-	O	O	-	2.5 V	14
15	V0_IO_16_N	A16	IO	IO	B16	V0_IO_16_P	16
17	V0_IO_17_N	A17	IO	IO	C17	V0_IO_17_P	18
19	V0_IO_18_N	A18	IO	IO	B18	V0_IO_18_P	20
21	V0_IO_06_N	C10	IO	IO	D10	V0_IO_06_P	22
23	GND	-	-	-	-	GND	24
25	V0_IO_07_N	E10	IO	IO	F10	V0_IO_07_P	26
27	V0_IO_10_N	C16	IO	IO	D17	V0_IO_10_P	28
29	V0_IO_09_N	C14	IO	IO	D15	V0_IO_09_P	30
31	V0_IO_08_N	A14	IO	IO	B14	V0_IO_08_P	32
33	1.2 V	-	O	O	-	1.2 V	34
35	n.c.	-	-	-	-	n.c.	36
37	n.c.	-	-	-	-	n.c.	38
39	GND	-	-	-	-	GND	40

Table 12: TE0630 J4 header pin-out