



## Product Change Notification

*Trenz Electronic TE0600 modules*

### Notification Title

Trenz Electronic TE0600 module, new board revision.

### Notification Type

Hardware Revision

### Notification Entity

minor change	major change
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### Products Affected

Trenz Electronic TE0600 series.

New 02 revision will completely replace 01 revision. To buy 01 revision modules, contact Trenz Electronic representative.

### Description of Change

New board revision with new capabilities and features:

- More powerful regulators for 1.2V and 1.5V rails
- VCCAUX separated from 2.5V power rail
- 128Mbit SPI Flash
- Additional secure 1Kbit EEPROM
- Optional B2B connection to bank 2 differential clock input
- New memory options

### Reason for Change

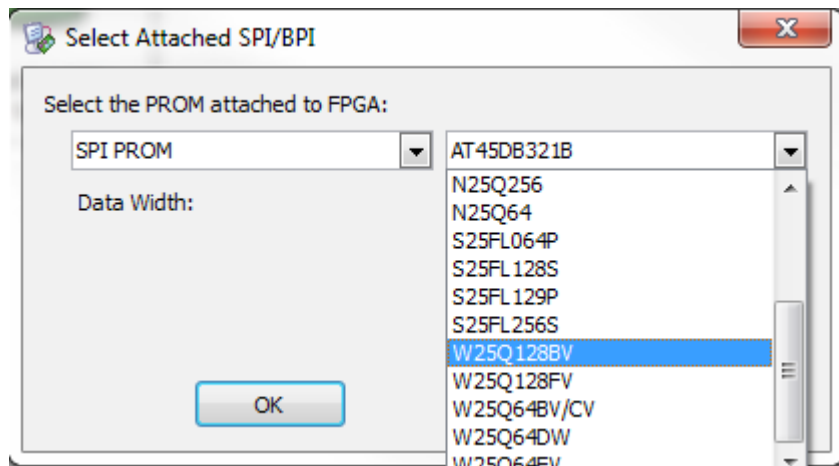
Increasing product power characteristics. New connectivity and security features for user projects.

### Impact

As new SPI Flash used in new board revision, flash related operation should be changed.

## ISE iMPACT Software

For indirect SPI flash programming W25Q128BV SPI PROM should be selected.



## User firmware

### New SPI Flash have differ Device ID

Module revision	Manufacturer ID	Device ID
Revision 01	0xEF (Winbond)	0x16 (W25Q64CV)
Revision 02	0xEF (Winbond)	0x17 (W25Q128BV)

Table 1: SPI Device ID

### Additional chip on 1-Wire bus

To work with multiple chips on 1-Wire bus firmware should perform search algorithm <http://www.maximintegrated.com/app-notes/index.mvp/id/187> to find address of each chip and use MACH\_ROM commands to work with selected chip.

## Revision encoding

Module revision coded by 4 FPGA BR[3:0] pins, which can be read by FPGA firmware. All these pins should be configured to have internal PULLUP.

Signal FPGA pin	BR3 R19	BR2 P18	BR1 N16	BR0 P17
Revision 01	1	1	1	1
Revision 02	1	1	1	0

Table 2: Board revisions pin coding

## New revision advantages

- Projects with higher power consumption possible
- More convenient eFUSE usage
- More Flash memory for user data

- Security option for devices without eFUSE
- Differential clock input option for FPGA bank 2

For complete module information refer [TE0600 user manual](#).

## **Expected Sample Availability Date**

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First Availability of Post-Conversion Product November 2012.

## **Expected Production Availability Date**

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First Availability of Post-Conversion Product January 2013.

## **PCN Representative**

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