Module board corresponding to industrial network module
Industrial Grade SOM (System On Module)

[ TB-7Z-IAE ]

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Tokyo Electron Device's electronic component business has been certified for ISO14001 by Japan Audit and Certification Organization for Environment and Quality (JACO).

Tokyo Electron Device markets proprietary information, technology and services under our original 'inrevium' brand name. The name was created by combining the first letters of the words 'intellectual' and 'revolutionary', with the suffix '-ium' ('element') added. It signifies our ongoing mission to help solve customer problems and aid their business activities through our groundbreaking proprietary information, technology and services.
Providing world-class, leading-edge products and solutions to the world.

Since 1965, TOKYO ELECTRON DEVICE LIMITED (TED) has been focused on the semiconductor distribution business. Leveraging 40 years of industry experience, in 2004, TED began offering FPGA solutions under the “inrevium” brand name. Today, inrevium offers FPGA platform solutions, market-specific IP, technical support, and design services to customers worldwide. inrevium’s domain-specific expertise, market knowledge, and pre-qualified solutions, resulted in inrevium being adorned with the prestigious Xilinx Alliance Program Premier Design Services Member designation.

With design and development centers in Japan, China, and Canada, and a global network of sales offices, inrevium remains uniquely positioned to provide high-value design services to its customers. In addition to services, the development centers also create market-specific multi-million gate LSI devices, FPGA evaluation boards, FMC option cards, ASIC prototyping boards, drivers, firmware, and IP, to support a wide range of worldwide applications.

Corporate Profile

Company Name: TOKYO ELECTRON DEVICE LIMITED
Headquarters: Yokohama East Square 1-4, Kinko-cho, Kanagawa-ku, Yokohama City, Kanagawa 221-0056, Japan
Established: March 3, 1986
Capital: 2,495 million yen (March 31, 2014)
Common Stock Listings: 1st Section of the Tokyo Stock Exchange (reg.no.2760)
Net Sales: 101,801 million yen (FY2014)
Employees: 999 (as of September 30, 2014)

Description of Business: Electronic Components Business:
- Distribution, design and development of Semiconductor Products, Boards, software, and Other electronic components.

Group Company:
- Tokyo Electron Device ASIA PACIFIC LIMITED
- Tokyo Electron Device Shanghai Limited
- Tokyo Electron Device Singapore Pte. Limited
- inrevium America Inc.
- Shanghai inrevium Solutions Limited
- WUX inrevium Solutions Limited
- PAN ELECTRON Limited
- Fidus Systems, Inc.

inrevium Solution

About inrevium
Design Service

Development abilities to meet customer needs

Drawing on the technology and experience accumulated from many years of association with the Tokyo Electron Device Group, our Design & Development Center provides outsourced design/development support and Self-developed products (inrevium).

Manufacturing Services (OEM / ODM)

From experimental production development, consistent service to mass production

Stage : Design and Prototype

- Design Proposal
- Prototype
- Prototype Evaluation

Stage : Production

- Pre Production
- Mass Production
- Support

GAP

Same Engineer will be managing Prototype and production process

Smoothly moving from Prototype to Production

Major Action Items of Mass Production Process.
- Evaluate Pre-Production.
- Factory Test Arrangement.
- Failure Analysis.
- Managing discontinue parts.

About Fidus Systems, Inc

www.fidus.com

FSF-AD8200A
8-Channel, 185Msps 14-bit, JESD204B
Analog-to-Digital Converter FMC

Fidus System, Inc FMC Cards ➤ http://www.fidus.com/fmc-by-fidus/
Kintex UltraScale 8K4K Image Evaluation Platform

The platform accelerate development Super-High Definition 8K image Processing

Part Number: TB-KU-060-ACDC-8K / TB-KU-085-ACDC-8K

Features
- 20nm Kintex UltraSCALE XCKU060/085-2FFVA1517
- 2 x DDR4 SDRAM (2,400Mops) 32bit
- Provides the extensibility with GTH transceiver
- FMC card connect

Description
- Device: XCKU060/085-2FFVA1517
- Memory: DDR4-SDRAM (64bit) x2
- Interface:
  - FMC
  - SFP + Socket
  - RS-232C (Connector is USB-B type)
  - PMOD (Digilent module interface)
  - 10pin header for Xilinx cable
  - General pin header
- Push switch, DIP switch, LED
- Clock:
  - 200MHz for DDR4
  - 148.5MHz for image processing
  - 156.25MHz for high speed Serdes
- PLL for general purpose
- Configuration: QUAD Dual-SPI Flash
- Power (AC adopter)

Reference Design
- DDR4 memory controller (MIG)
- FMC Connection: Chip2Chip design

Note: This product is under development. The specification may change without notice.

Virtex-7 FPGA Large-Scale PCI Express Gen3 Evaluation Platform

Flexibility and extensible for Hi-Speed and Hi-Density application

Part Number: TB-7VX-690T-PCIEXP / TB-7VX-980T-PCIEXP / TB-7VX-1140T-PCIEXP

Features
- The 7VX-xxxT-PCIEXP series also provides x8-lane PCI Express Gen3 (using FPGA integrated block for PCI Express) and the high-speed memory interface 1,600 Mbps DDR3 SDRAM SO-DIMM 2 system as standard. Connecting the optional fiber solution TB-FMCH-OPT10 FMC card with optical cable interface to TB-7VX-xxxT-PCIEXP enables 10ch of 10G optical modules to be mounted on each FMC connector. This achieves an optical interface configuration of up to 400Gbps.

Device:
- XC7VX690T-2FFG1926
- XC7VX980T-2FFG1926
- XC7VX1140T-2FLG1926

Memory:
- DDR3-SDRAM SO-DIMM Connector x2 (with 4GB module)
- SPI Flash 128Mbit

Interface:
- FMC HPC x4*1
- PCI Express x8 (Gen3)
- USB3.0 Device
- MMCX Clock input
- PMOD (Digilent module interface)
- 15pin header for Xilinx cable
- General 10pin header
- Push switch, DIP switch, LED
- Power
- Board size: H140 x W312 (mm)

Reference Design
- PCI Express DMA Design with Time limitation
- DDR3 memory controller (MIG)
**Features**
- Business Card sized small module with Zynq-7000 All Programmable SoC and peripherals.
- Enables to implement multiple industrial network on single platform
- 2ch Giga Ethernet for supporting flexible topology
- Mass Production usage

**Description**
- Device : Xilinx Zynq-7000 Zynq-7020
- Memory : DDR3 SDRAM 512MByte
- QSPI Flash 16MByte
- 64Kbit Non-volatile F-RAM
- Expansion IO Connector : 120 Position Connector 0.80mm Pitch (PL IO:60 / PS IO:10)
- General Purpose Interface : Gigabit Ethernet x 2
- Socket for microSD card
- Debug Interface : JTAG, LED
- Clock : Processing System, Programmable Logic
- RTC Device
- Power Supply : Single DC5V operation
- Board size : H60 x W85(mm) * Protruding parts are not included
- Operating Temperature : 0℃ ~ +50℃

**Use Case**
This reference design enables greater development time shortening for machine vision systems.

**Reference Design**
- Daughter board : TB-7Z-IAE
- Mother board : Device : Xilinx XC6SLX45-FGG484
- Memory : DDR2 SDRAM 1Gbit
- QSPI Flash 64Mbit
- Interface : USB2.0 (Host), DVI TX, CameraLink Base
- 10/100Mbit Ethernet (RJ45), CAN (D-SUB9), RS-232C (D-SUB9)
- PMOD x2, XADC (Pin header)
- Debug Interface : ARM JTAG 20 pin header, 10pin header for XILINX Cable
- Push Switch, DIP Switch, LED, Rotary Switch
- Power (AC adopter)
- Board size : H110 x W185(mm)
Virtex-7 FPGA ASIC Development Test Platform

Part Number: TB-7V-2000T-LSI

Reducing development schedule for SoC emulation and ASIC development

Features:
- Shortens development time by providing an ASIC emulation platform
- Provision of high-speed interfaces including high-speed I/O connectors and expansion FPGA results in an ASIC development platform with excellent flexibility and expandability
- Use of supplied reference designs allows testing to be performed under actual operating conditions with high clock speed

Block Diagram

Description:
- Device:
  - XC7V2000T-2FLG1925
  - XC7K25T-2FFG900
- Memory:
  - DDR3 SDRAM 2Gbit x8
- Interface:
  - Connectors for FMC cards: High-speed I/O connector (120 pin) x 5
  - PCI Express Gen 2 8-lane
  - USB 2.0/3.0 (device) Type-B
  - MMICX clock input/output
  - DVI (Tx, Rx), Full HD supported
  - 10pin header for XILINX cable
  - General 24pin header
  - Push switch, DIP switch, LED
- Configuration:
  - microSD Card (Virtex-7 FPGA Only)
  - NAND Flash (Virtex-7 FPGA Only)
  - QSPI Flash (Kintex-7 FPGA)
- Power Supply
  - Board size: H300 x W400 (mm)

Reference Design:
- DDR3 memory controller (MIG)
- DVI, USB3.0/2.0 Interface design

Zynq-7000 All Programmable SoC Extension Microcontroller Card

Part Number: TB-7Z-020-EMC

Individual software development platform with level extensible for any application

Features:
- TB-7Z-020-EMC has excellent connectivity with the main development system such as the TB-7V-2000T-LSI or any other inrevium platform. By featuring Zynq-7000 All Programmable SoC, small size and wide range of interfaces, the TB-7Z-020-EMC goes far beyond just connection ability with FPGA evaluation platform. Software engineers can use the TB-7Z-020-EMC to perform repeated testing on real hardware during the development process.

Block Diagram

Description:
- Device: XC7Z020-1CLG484
- Memory:
  - DDR3 SDRAM 1GByte
  - microSD Card socket and media
  - 128Mbit QSPI flash memory
- Expansion Interface:
  - FMC (LPC) x 2*1
  - LPC (Mezzanine)
  - LPC (Carrier)
- General Purpose Interface:
  - Gigabit Ethernet
  - USB2.0 (Host Device)
  - UART (RS-232C)
  - CAN
  - DVI TX
- Push switch, DIP switch, LED
- Debug Interface:
  - MIC33TR-36 for ARM
  - 10pin header for XILINX cable
  - Clock: Multi-clock generator
  - - ARM 333MHz
  - - Logic 148.5MHz
- Power Supply
  - Board size: H69 x W130 (mm)

Reference Design:
- FPGA Board Connection: chip2chip design
- DIV output Reference Design
- Linux boot Reference Design

Veriﬁcation Technology
Embedded Performance Veriﬁcation IP, VARON
http://www.vtech-inc.co.jp/product/v01_02_e.html
### Evaluation Board

#### ACDC (Acquisition, Contribution, Distribution and Consumption) 1.0 Base board

**Part Number:** TB-7K-325T-IMG

**Description**

The ACDC 1.0 base board is a revolutionary platform suited for evaluation, test and debug, and development of video designs. With GTX transceivers and 64bit x 1,800Mbps DDR3 memory, the board meets the high-bandwidth, high-performance requirements of ultra-realistic, high-definition display technology such as 4K2K and OLED. The ACDC 1.0 base board also provides the best power-to-performance optimization in designs compared to competitive offerings.

**Features**

- **Device:** XC7K325T-2FFG900
- **Memory:** DDR3 SDRAM 2Gbit x4
- **Interface**
  - FMC
  - HPC (High Pin Count) x2
  - LPC (Low Pin Count) x2
  - GTX Transceiver 5.4Gbps 8ch x2 (HPC)
  - MMCX for External Clock
  - UART (RS-232/232 D-sub 9pin)
  - XADC pin header
  - 10pin header XILINX for cable
  - Push switch, DIP switch, LED
- **Clock**
  - 74.25MHz OSC (via Socket)
  - 135MHz OSC
  - 200MHz OSC
  - PLL
- **Configuration:** QUAD SPI Flash
- **Power Supply**
- **Board size:** H175 x W240 (mm)

*Not all VITA57.1 signals are populated.*

**Reference Design**

- HDMI Frame Buffer Design
- HDMI frame Buffer Design with TB-FMC6-HDMI2 (sold separately)
- Memory controller: Generated by Memory Interface Generator (MIG)
- EDK Base System Builder Design
- XBD file for EDK base system builder
- MicroBlaze softcore CPU and peripherals

### Evaluation Board

#### ACDC A7 Evaluation Board

**Part Number:** TB-A7-200T-IMG

**Description**

The ACDC A7 Evaluation Board is an ideal video processing platform for 4K video applications. inrevium recognizes its strong design expertise in 4K video, imaging and multimedia products have made available a video development package that targets video processing development using an Artix-7 FPGA device.

The package includes an Artix-7 FPGA development board (TB-A7-200T-IMG) featuring the leading system performance per watt Artix-7 family to allow additional functionality and connectivity via FMC option cards. The ACDC A7 development board delivers a complete 4K development platform with various reference designs for Display Port1.2, HDMI2.0, V-by-OneHS, and 6GSDI. Furthermore, the board has a DDR3 SODIMM, creating a complete integrated memory interface solution for memory-intensive applications.

**Features**

- Develop audio applications with S/PDIF interface
- Develop networking applications with 10/100/1000 Mbps Ethernet (RGMII)
- Enabling high-performance serial connectivity with 8 GTP transceivers per FMC connector (16 total)
- Expand I/O with the FPGA Mezzanine Card (FMC) interface x 2 *
- Hardware and pre-verified reference designs
- Optimized for quickly prototyping 4K applications using Artix-7 FPGAs
- Reference designs for Display Port1.2, HDMI2.0, V-by-One HS, and 6G-SDI
- Supports embedded processing with MicroBlaze, soft 32bit RISC
- Advanced memory interface with 1GB 64bit DDR3 SODIMM up to 800Mbps
- Power Supply

*1) Not all VITA57.1 signals are populated.*

**Reference Design**

- Targeted Reference Design featuring Xilinx Display Port, 6G SDI and HDMI (V-by-One HS reference design is optional)
**FMC Card**

**FMC Mezzanine Card (FMC) Standard**
Developed by a consortium of companies ranging from FPGA vendors to end users, the FMC Mezzanine Card is an ANSI standard that provides a standard Mezzanine Card form factor, connectors and modular interface to an FPGA located on a base board. Decoupling the I/O interfaces from the FPGA simplifies I/O interface module design while maximizing carrier card reuse.

### Connector User IO (High Speed Serial IO) Pin
- High Pin Count (HPC)
  - 400 pin
  - 18 pins (10 channels)
- Low Pin Count (LPC)
  - 160 pin
  - 72 pin (3 channels)

**FMC Card**

**FMC HPC (High Pin Count)**

**Display Port 1.2 Card**
- Part Number: TB-FMCH-D P2
- NEW
- SMA TX/RX 4CH
- 156.5MHz OSC & SMA IN for reference clock
- Supports LVDS connector.
- X148.5MHz / 74.25MHz for reference clock
- On board PLL
- 51pin connector (4pin mounting option)
- Supports LVDS connector:
  - X148.5MHz / 74.25MHz for reference clock
- On board PLL
- SMA TX/RX - 4CH
- 156.5MHz OSC & SMA IN for reference clock
- Individual RX/TX Board
- 8x2, 7x2
- Uses ADI conversion chips to R/G/B or YUV
- Up to 1080P Full HD resolution
- 3D Format supported
- 1.8V IO requirement, please contact us

**HDMI 2.0 Card**
- Part Number: TB-FMCH-HD64K
- NEW
- HDMI2.0 Input x 1
- HDMI2.0 Output x 1
- Expansion connector for additional TB-FMCH-HD64K
- HDMI IP required
- DisplayPort 1.2 Standard
- Sink/Source - 1CH each
- Working with 44m x Displayport IP
- This product has limitation of environment. Please contact us.
- 75Ω HD-BNC, 1ch IN, 1ch OUT
- 3ch Bi-direction
- Expansion connector for additional TB-FMCH-12GSDI
- Analog B.S.P 512x512 input
- Supports FMC 1.8V IO
- Attached D-BNC-8N/8N convert cable
- 148.5MHz, 148.95165MHz clock

**12G SDI Card**
- Part Number: TB-FMCH-12GSDI
- NEW
- 12G SDI Card QSFP Module Card
- Supports FMC 1.8V IO
- Attached D-BNC-8N/8N convert cable
- 148.5MHz, 148.95165MHz clock

**HDMI 1.4 Card**
- Part Number: TB-FMCH-HDMI12
- NEW
- HDMI1.4 Card
- HDMI1.4 Card 1.8V IO modification version
- HDMI2.0 Input x 1
- HDMI2.0 Output x 1
- Expansion connector for additional TB-FMCH-HDMI4K
- HDMI IP required

**3G/HD/SDI Card**
- Part Number: TB-FMCH-3GSDI2A
- NEW
- 3G/HD/SDI 2x2 Input, 2x2 Output
- 3x2 Bi-direction
- Expansion connector for additional TB-FMCH-3GSDI2A
- Analog B.S.P 512x512 input
- Supports FMC 1.8V IO
- Attached D-BNC-8N/8N convert cable
- 148.5MHz, 148.95165MHz clock

**QSFP Module Card**
- Part Number: TB-FMCH-OPT10
- NEW
- QSFP Module x2
- SFP Module x2
- 156.25MHz OSC & MMCX IN for reference clock

**1000 Base-T Ethernet Card**
- Part Number: TB-FMCH-PH
- NEW
- Pin header Card
- 30pin, pin header x3
- Each Pin header connect 24 signals
- For LAN Communication
- 1000BASE-T PHY (Marvell):
  - 88E1111-B2-BAB1C00
- For developing LVDS interface
- LVDS Tx/Rx Loopback Design (Verilog HDL)
- USB Function only

**USB3.0 Device Card**
- Part Number: TB-FMCH-LVDS
- NEW
- LVDS Card
- USB3.0 Device Card
- CYUSB2104(CY314)
- USB Function only

**FMC LPC (Low Pin Count)**

**USB3.0 Device Card**
- Part Number: TB-FMCH-LVDS
- NEW
- LVDS Card
- USB3.0 Device Card
- CYUSB2104(CY314)
- USB Function only

**Pin Header Card**
- Part Number: TB-FMCH-LVDS
- NEW
- Pin header Card
- 30pin, pin header x3
- Each Pin header connect 24 signals
- For LAN Communication
- 1000BASE-T PHY (Marvell):
  - 88E1111-B2-BAB1C00
- For developing LVDS interface
- LVDS Tx/Rx Loopback Design (Verilog HDL)

**Displayport 1.2 Standard**
- Sink/Source - 1CH each
- Working with Xilinx’s Displayport IP
- This product has limitation of environment. Please contact us.
### Features
The FSF-AD15000A is a single channel, 5GSPS, 12-bit, JESD204B, ADC FMC. It is designed to be electrically and mechanically compatible with ANSI/VITA 57.1. Designed with two out-of-phase ADI AD9625, 2.5GSPS converters, an equivalent sample rate of 5GSPS is achieved. The JESD204B interface provides link alignment and minimizes the number of required FPGA I/O. Interleaving correction IP for the host FPGA is available.

### Description
- 5GSPS (equivalent), 12-bit, ADC FMC
- Analog Input
  - 1x SMA, AC-Coupled, 50Ω, xfrmr coupled
  - Bandwidth: 0.5 MHz - 3.3 GHz (-3dB)
  - Dual Analog Devices AD9625 ADC's
- Other interfaces
  - HPC FMC connectors, featuring 16x MGT, operating at 6.25Gbps
  - Ext. Clock Input: SMA, AC-Coupled, 50Ω
  - Ext. Trigger input: SMA, DC-Coupled
- Extremely low phase noise onboard oscillator, with analog clock distribution topology
- Physical
  - Designed for compatibility with ANSI/VITA 57.1
  - 0 to +45°C operating temperature range
  - JESD204B Subclass 1 feature set including deterministic latency
  - Designed for experimentation and integration
- Interleaving correction FPGA IP available

### Reference Design
- Reference design, demonstrates interleaving, interleaving correction, and data capture to Xilinx® ILA™
- VC707 targeted .bit file

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### Features
The FSF-AD8200A is an 8-Channel, 185MSPS, 14-bit, JESD204B, conduction cooled, ADC FMC. It is designed to be electrically and mechanically compatible with ANSI/VITA 57.1. The FSF-AD8200A has sufficient analog bandwidth for under-sampling systems. JESD204B enables channel alignment.

### Description
- 8-channel, 185MSPS, 14-bit, ADC FMC
- Analog Inputs
  - 8x SSMC, AC-Coupled, 50Ω, xfrmr coupled
  - Bandwidth: 4.5 MHz - 500 MHz (-3dB)
  - Ch-to-ch crosstalk < -75 dB @ 183 MHz
- Other interfaces
  - HPC FMC connector, featuring 8x MGT
  - Ext. Clock Input: SSMC, AC-Coupled, 50Ω
  - Ext. Trigger input: SSMC, DC-Coupled
- On-board clock generator capable of sub-100fs jitter
- Physical
  - Designed for compatibility with ANSI/VITA 57.1
  - 0 to +45°C operating temperature range (heat sink, natural convection)
  - JESD204B Subclass 1 feature set including deterministic latency
  - Designed for experimentation and integration

### Reference Design
- Reference design, enables 8-channel coherent sample capture to Xilinx® ChipScope
- VC707 targeted .bit file
**V-by-One HS IP Core**

**Part Number** TIP-VBY1HS-PROJ (Project License)

Supporting the higher frame rates and the higher resolutions required by advancing FPD technology

**Features**
- Targets high-speed video signal transmission based on internal connection of equipment.
- Up to 3.75Gbps data rate (effective data rate 3Gbps) per lane.
- Data scrambling and Clock Data Recovery (CDR) to reduce EMI.
- CDR solves the skew problem between clock and data in conventional transfer systems.

**Logic Resource**

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Refresh rate (Pixel Clock)</th>
<th>Color depth</th>
<th>No. of Data Lane</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD</td>
<td>60Hz (74.25MHz)</td>
<td>18/24/36/38 bit</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>120Hz (148.5MHz)</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>240Hz (297MHz)</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>Full-HD</td>
<td>60Hz (148.5MHz)</td>
<td>18/24/36/38 bit</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>120Hz (297MHz)</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>240Hz (594MHz)</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>4Kx2K</td>
<td>60Hz (594MHz)</td>
<td>18/24/36/38 bit</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>120Hz (1188MHz)</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>240Hz (2376MHz)</td>
<td></td>
<td>32</td>
</tr>
</tbody>
</table>

**Support FPGA**

- Virtex-7 FPGA / Kintex-7 FPGA / Artix-7 FPGA

**MECHATROLINK-III Master IP Core**

**Part Number** TIP-ML3MST-PROJ (Project License : Master)

Controlling 62 slaves in perfect synchronization

**Features**
- Master Function
- Maximum 65MHz Clock, High-speed, Synchronous host interface
- Flexible system configuration by FPGA Logic fabric
  - 16bit/32bit CPU bus, asynchronous bus
  - Zynq AP SoC or MicroBlaze base SoC

**Core Spec**
- 1, 2, 4, 8, 16-lane operation
- (Design service for 32 lanes is available.)
- Variable settings of driver swing, pre-emphasis and equalizer.
- Flexible implementation and package compatibility.

**Logic Resource**

<table>
<thead>
<tr>
<th>Core Resources (in case of Spartan-6 FPGA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
</tr>
<tr>
<td>Master</td>
</tr>
<tr>
<td>Slave</td>
</tr>
</tbody>
</table>

**Support FPGA**

- Spartan-6 FPGA
- Zynq-7000 All Programmable SoC (Under Development)