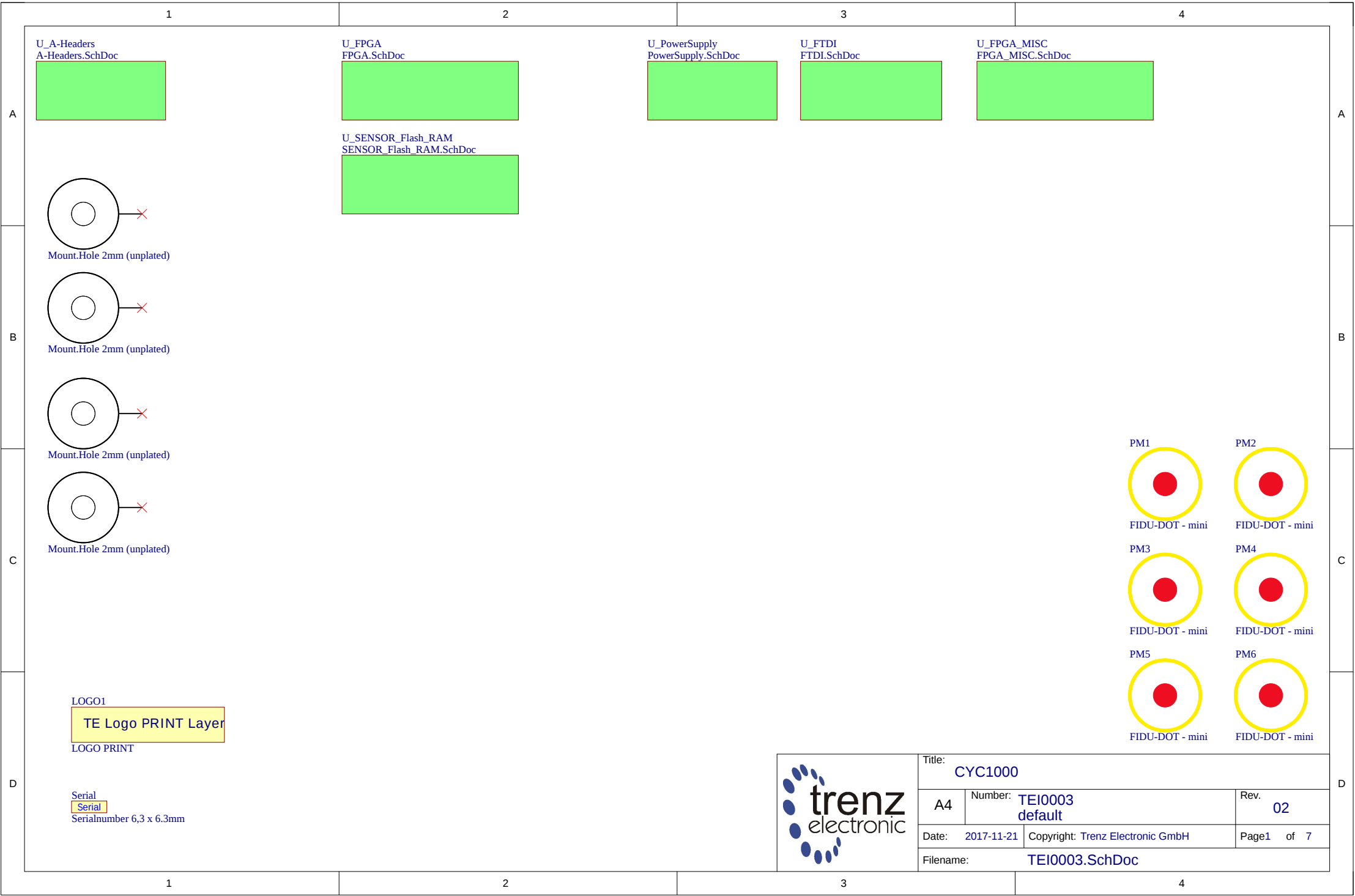


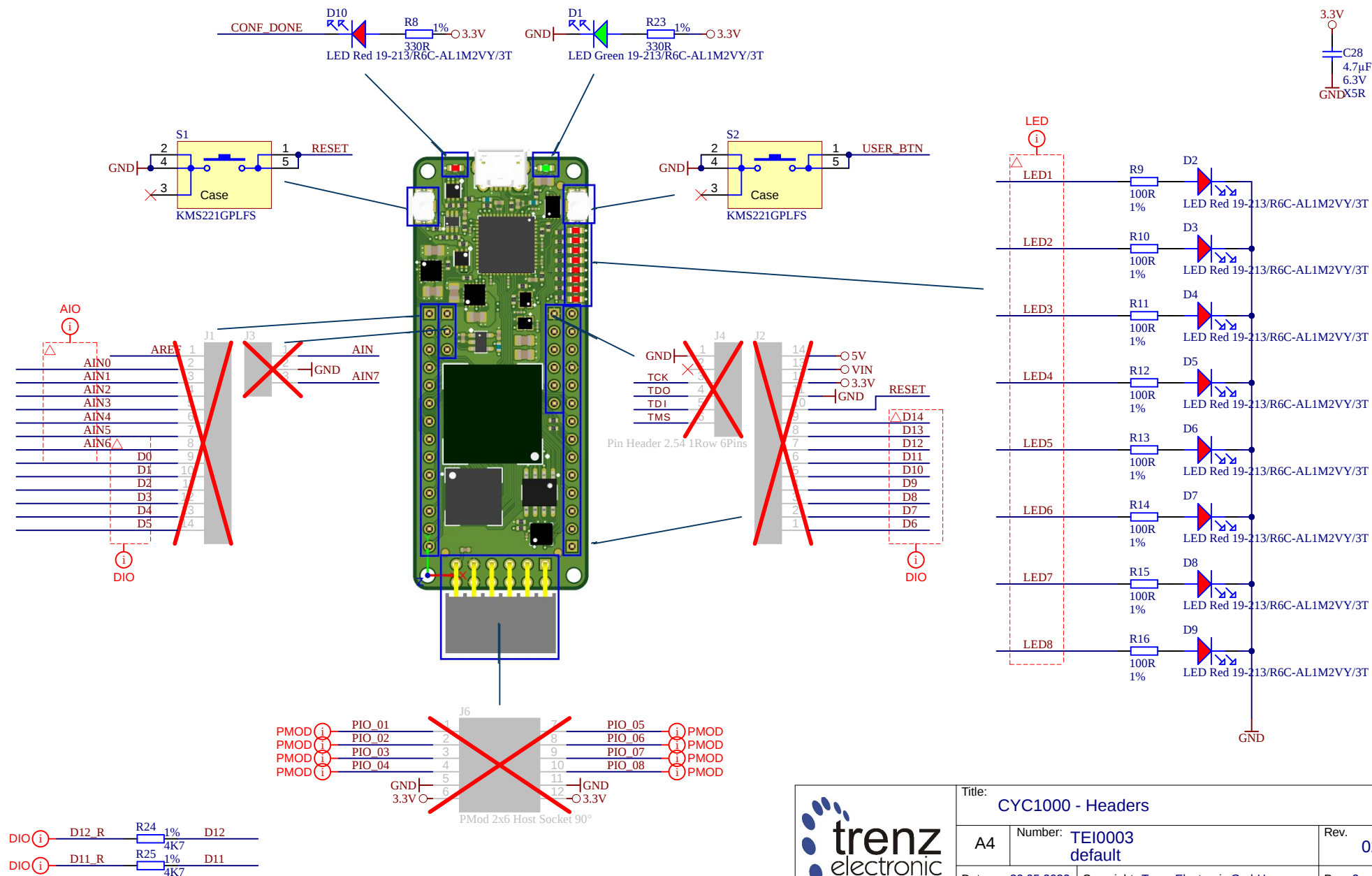


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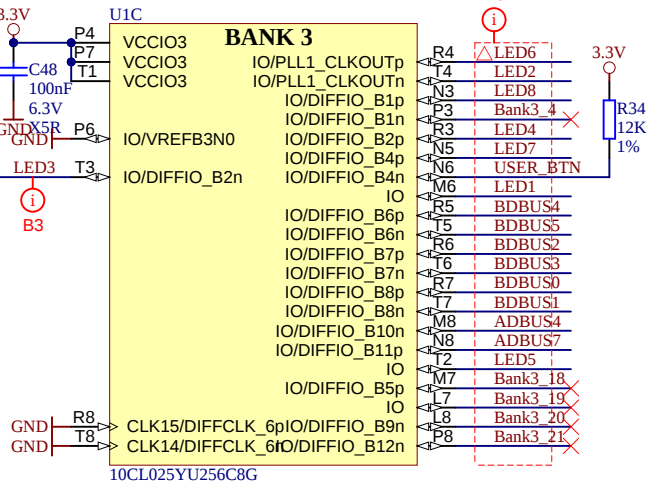
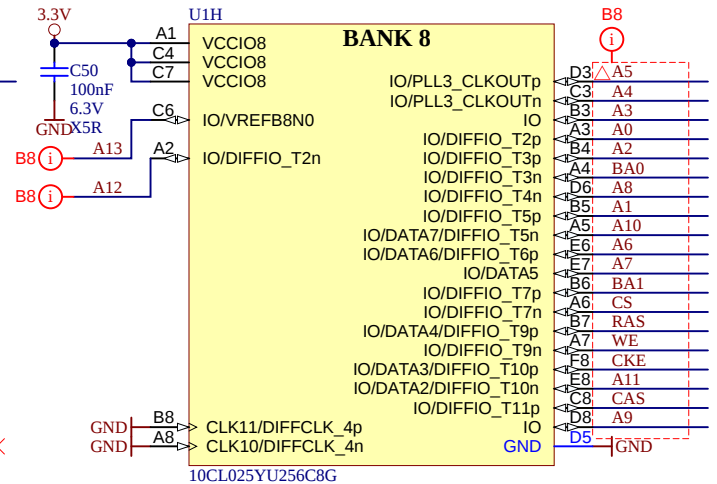
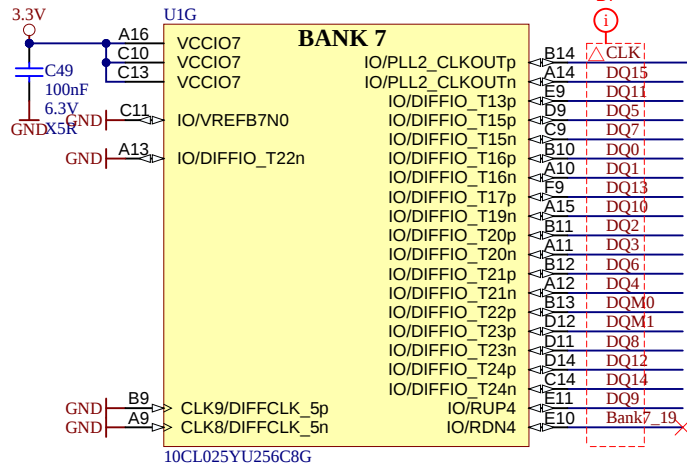
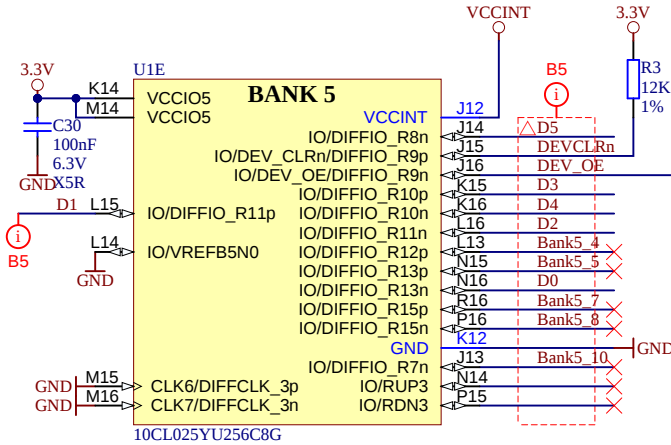
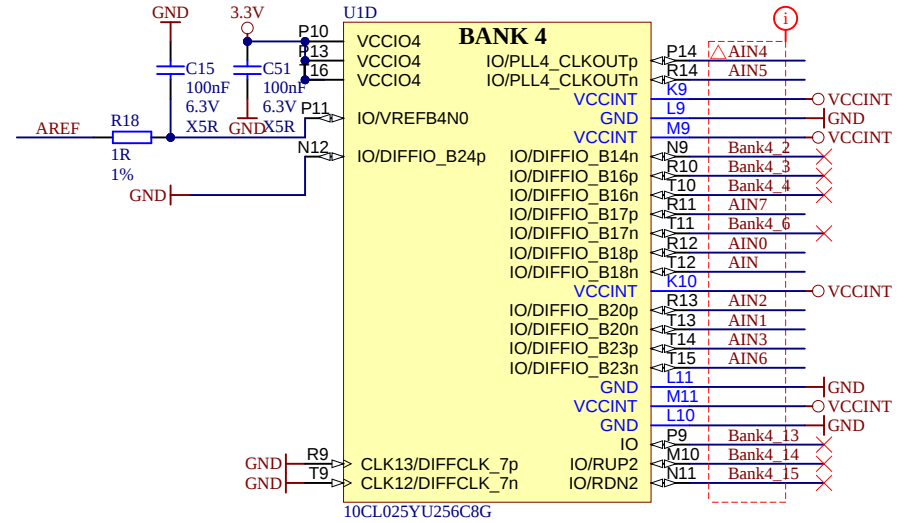
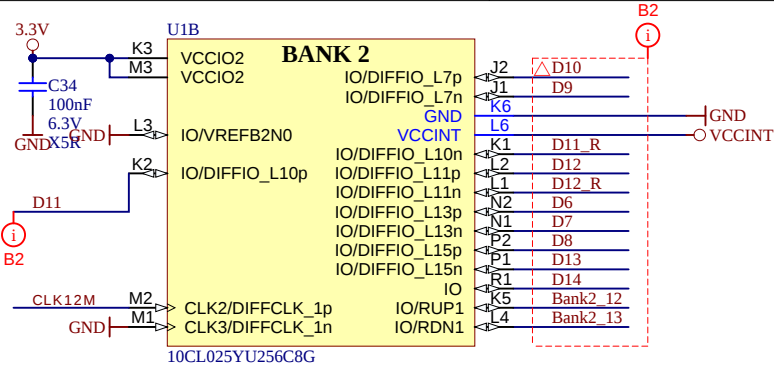
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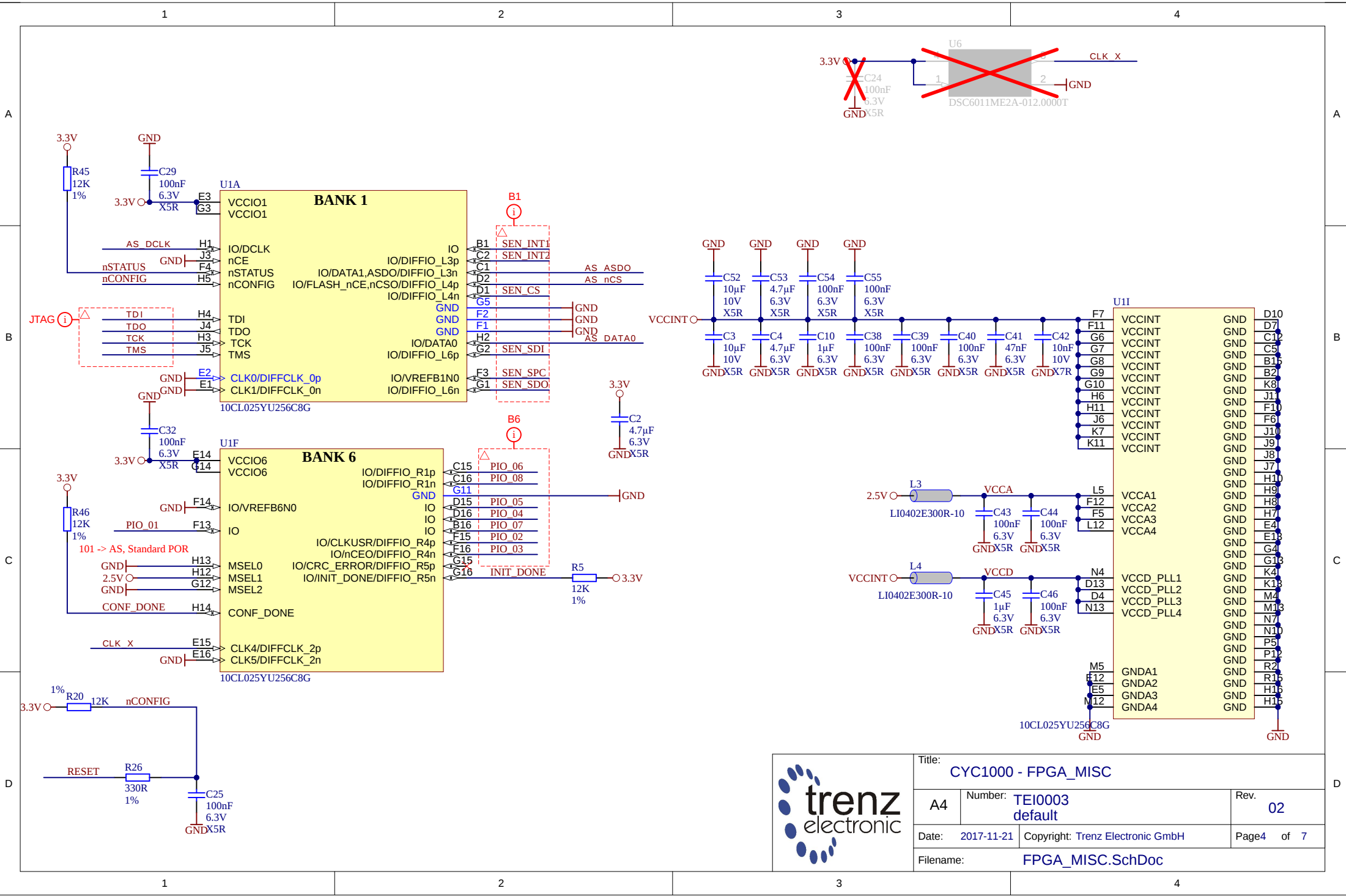
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Filename: FPGA.SchDoc		Page3 of 7

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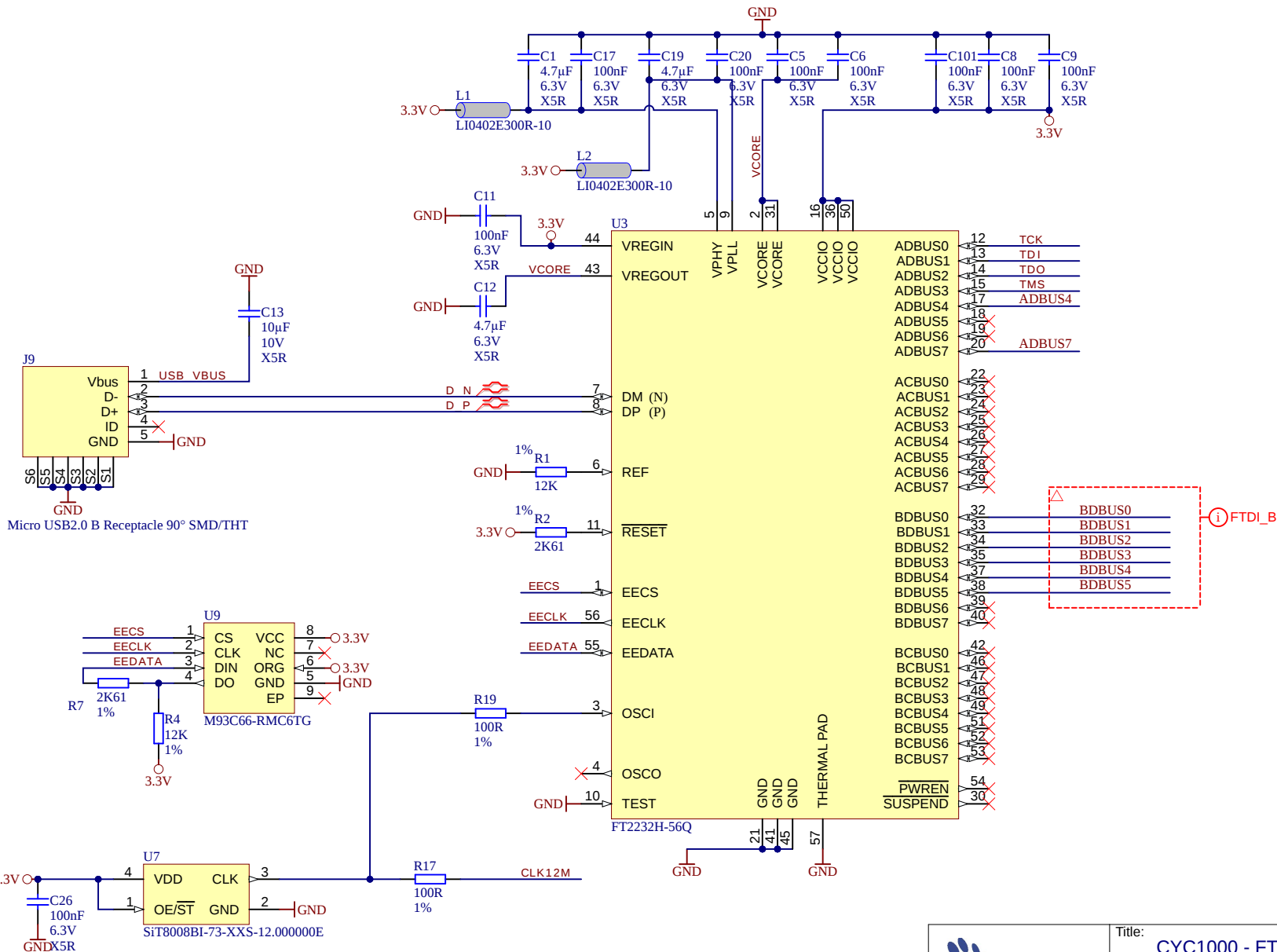


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FTDI_B



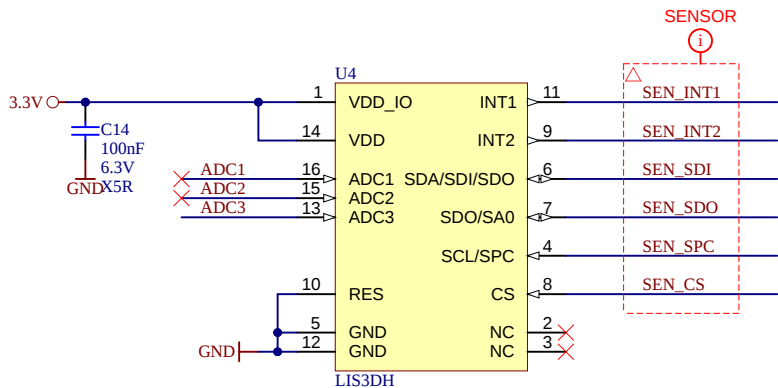
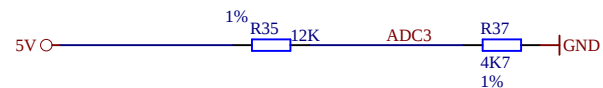
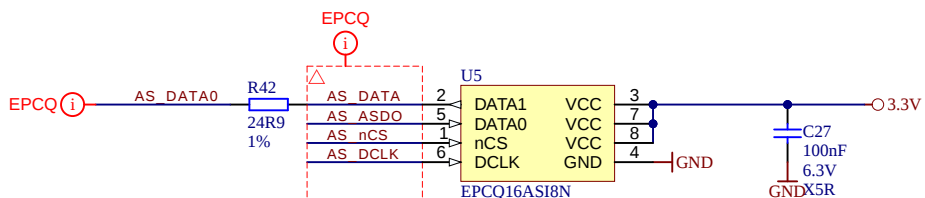
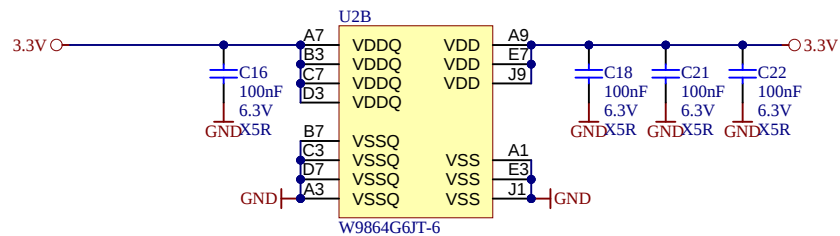
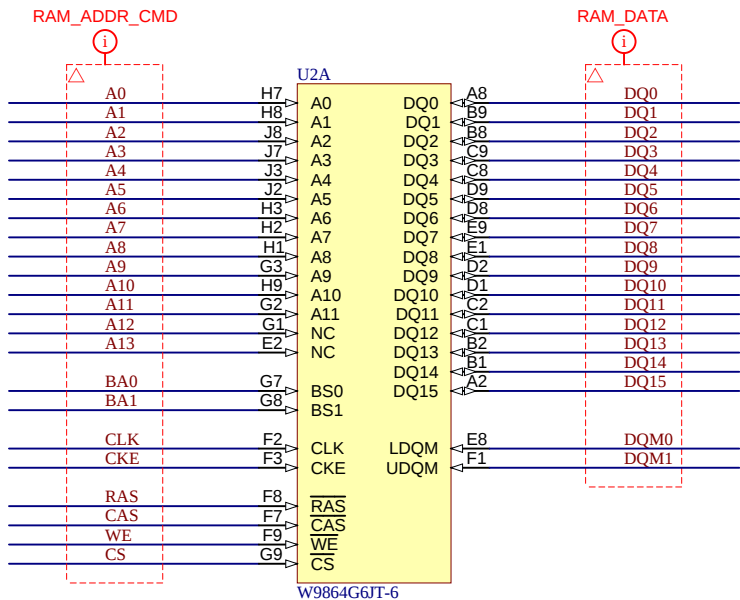
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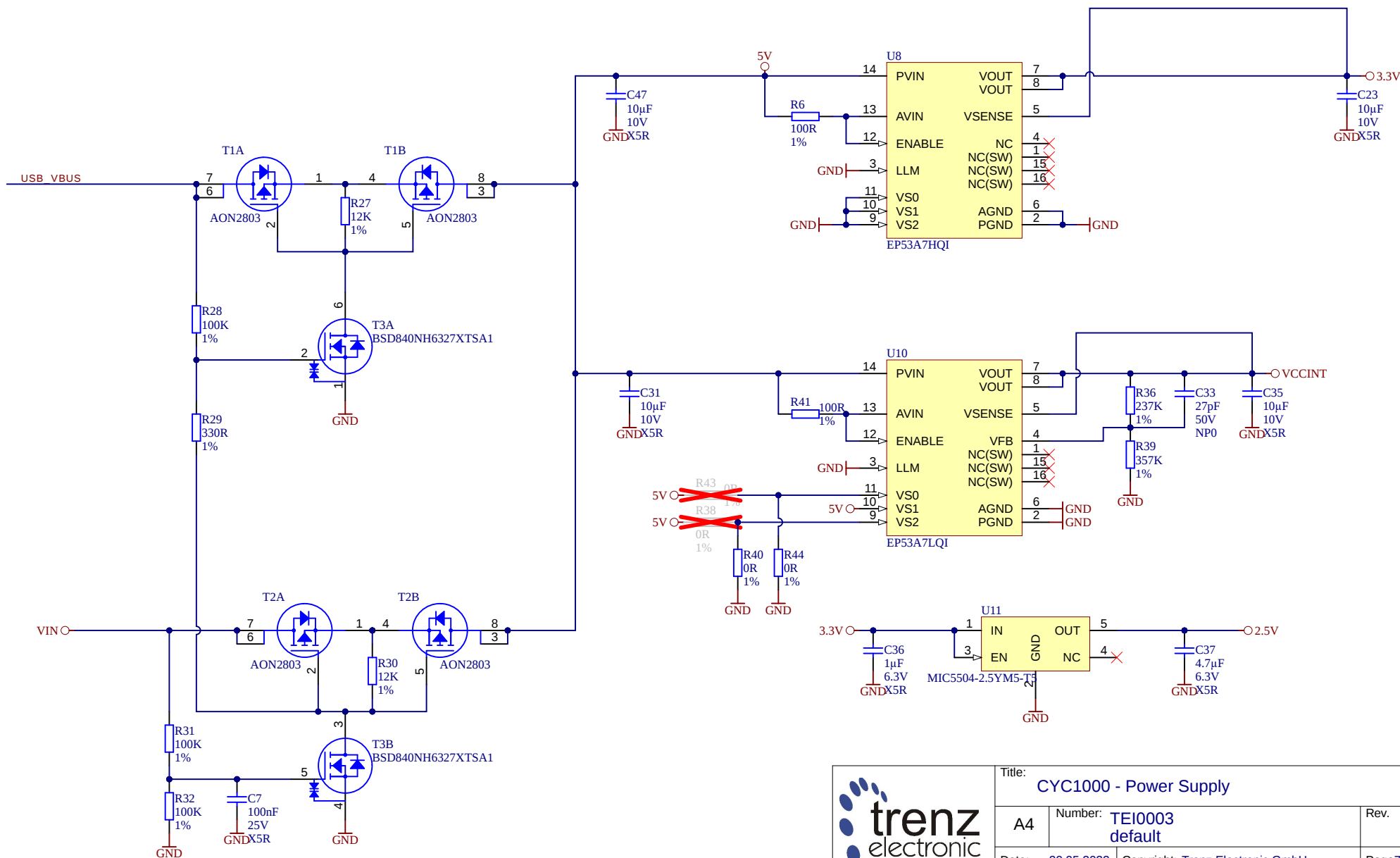
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Title: CYC1000 - Sensor_Flash_SDRAM		
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A	<table><tr><td>REV</td><td>Description</td><td></td></tr><tr><td>-01</td><td>Initial revision</td><td></td></tr><tr><td>-02</td><td>1. Bug fix 20.05.2022 1. Replaced obsolete parts: - Clock generator U7 DSC6011ME2A-012.0000T -> SiT8008BI-73-XXS-12.000000E; - Transisor T3 AO7800 -> BSD840NH6327XTSA1</td><td>VY</td></tr></table>				REV	Description		-01	Initial revision		-02	1. Bug fix 20.05.2022 1. Replaced obsolete parts: - Clock generator U7 DSC6011ME2A-012.0000T -> SiT8008BI-73-XXS-12.000000E; - Transisor T3 AO7800 -> BSD840NH6327XTSA1	VY
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D	 Title: Revision History <table><tr><td>A4</td><td>Number: TEI0003 default</td><td>Rev. 02</td></tr><tr><td>Date: 2019-10-02</td><td>Copyright: Trenz Electronic GmbH</td><td>Page of</td></tr><tr><td>Drawn by:</td><td colspan="2">Filename: Revision Changes.SchDoc</td></tr></table>				A4	Number: TEI0003 default	Rev. 02	Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page of	Drawn by:	Filename: Revision Changes.SchDoc	
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