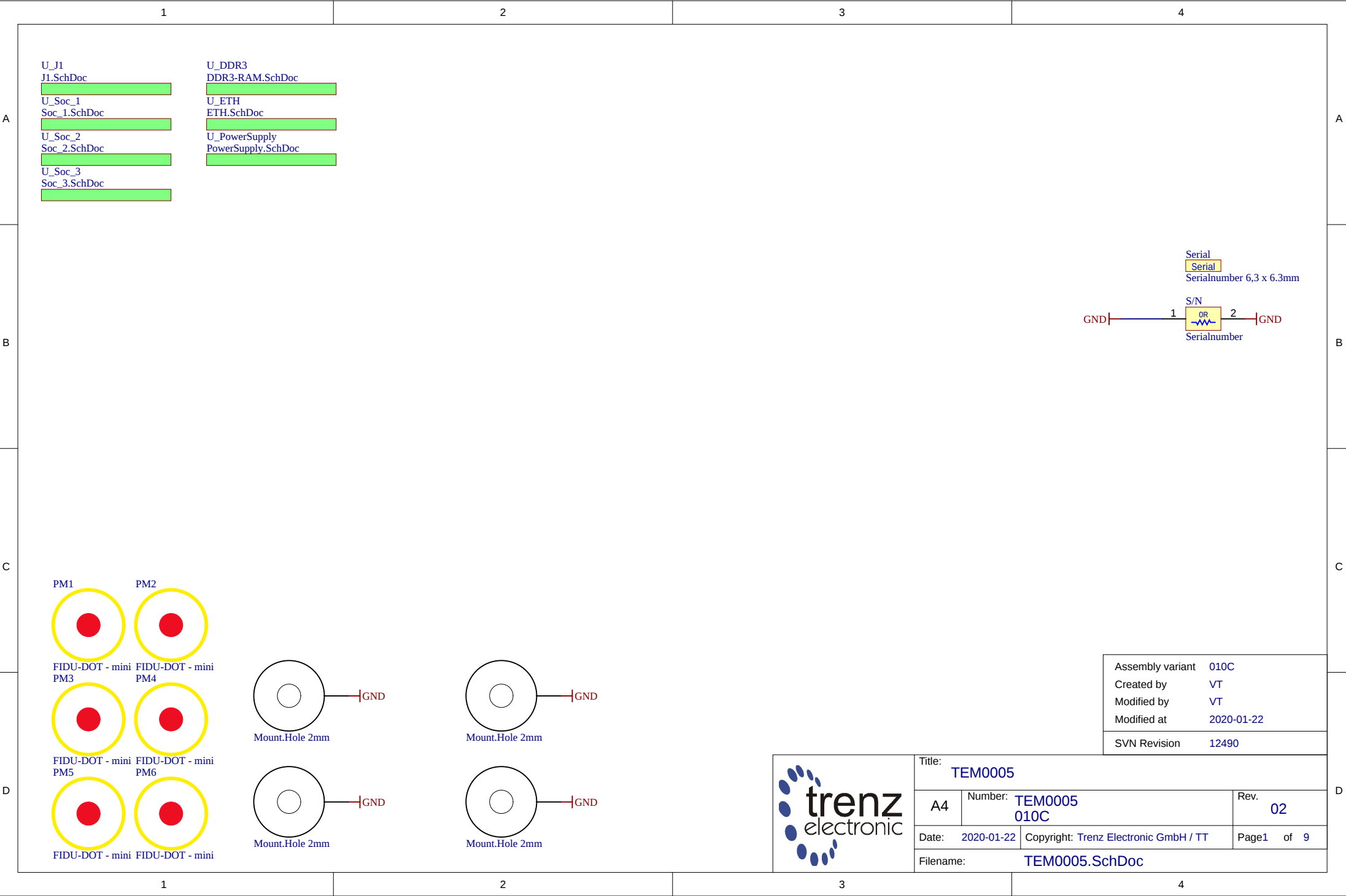




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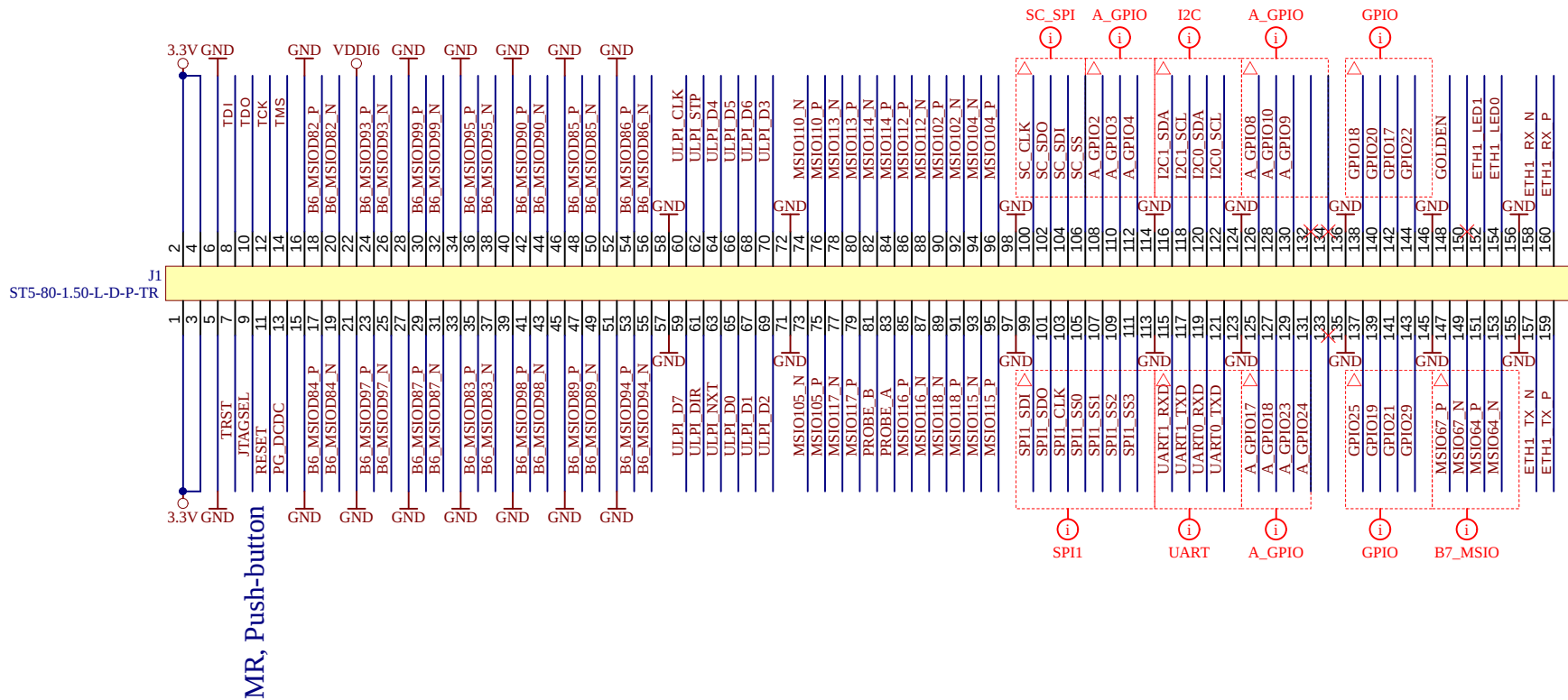
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				Title: TEM0005 - B2B_connector J1	
A4		Number: TEM0005 010C		Rev. 02	
Date: 2020-01-22		Copyright: Trenz Electronic GmbH / TT			Page2 of 9
Filename:		J1.SchDoc			

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U2A

BANK 0

A7 VDDIO
A17 VDDIO
B10 VDDIO
C3 VDDIO
D6 VDDIO
D16 VDDIO
E9 VDDIO
G8 VDDIO
G10 VDDIO
G12 VDDIO

DDRIO29PB0/MDDR_ADDR14
DDRIO29NB0/MDDR_ADDR15
DDRIO30PB0/MDDR_ADDR12
DDRIO30NB0/MDDR_ADDR13
DDRIO31PB0/MDDR_ADDR10
DDRIO31NB0/MDDR_ADDR11
DDRIO32PB0/MDDR_ADDR8
DDRIO32NB0/MDDR_ADDR9
DDRIO33PB0/MDDR_ODT
DDRIO33NB0/MDDR_ADDR7
DDRIO34PB0/MDDR_ADDR5
DDRIO34NB0/MDDR_ADDR6
DDRIO35PB0/MDDR_ADDR3
DDRIO35NB0/MDDR_ADDR4
DDRIO36PB0/MDDR_ADDR1
DDRIO36NB0/MDDR_ADDR2
DDRIO37PB0/MDDR_BA2
DDRIO37NB0/MDDR_ADDR0
DDRIO38PB0/MDDR_BA0
DDRIO38NB0/MDDR_BA1
DDRIO39PB0/MDDR_CLK
DDRIO39NB0/MDDR_CLK_N
DDRIO40PB0/MDDR_RESET_N
DDRIO40NB0/MDDR_CAS_N
DDRIO41PB0/MDDR_CKE
DDRIO41NB0/MDDR_CS_N
DDRIO42PB0/MDDR_RAS_N
DDRIO42NB0/MDDR_WE_N
*DDRIO43PB0/MDDR_DQ14
DDRIO43NB0/MDDR_DQ15
*DDRIO44PB0/MDDR_DQ12
DDRIO44NB0/MDDR_DQ13
DDRIO45PB0/MDDR_TMATCH_0_IN
DDRIO45NB0/MDDR_DM_RDQS1
*DDRIO46PB0/MDDR_DQS1_N
DDRIO46NB0/MDDR_DQS1_N
*DDRIO47PB0/MDDR_DQ10
DDRIO47NB0/MDDR_DQ11
DDRIO48PB0/MDDR_DQ8
DDRIO48NB0/MDDR_DQ9
DDRIO49PB0/MDDR_DQ7
DDRIO49NB0/MDDR_TMATCH_0_OUT
DDRIO50PB0/MDDR_DQ5
DDRIO50NB0/MDDR_DQ6
DDRIO51PB0/MDDR_DM_RDQS0
DDRIO51NB0/MDDR_DQ4
DDRIO52PB0/MDDR_DQS0
DDRIO52NB0/MDDR_DQS0_N
DDRIO53PB0/MDDR_DQ2
DDRIO53NB0/MDDR_DQ3
DDRIO54PB0/MDDR_DQ0
DDRIO54NB0/MDDR_DQ1
DDRIO55PB0/CCC_NE0_CLKI3
DDRIO55NB0
DDRIO56PB0/MDDR_DQ_ECC1
DDRIO56NB0/MDDR_DQ_ECC0
DDRIO57PB0/MDDR_TMATCH_ECC_IN
DDRIO57NB0/MDDR_DM_RDQS_ECC
DDRIO58PB0/MDDR_DQS_ECC
DDRIO58NB0/MDDR_DQS_ECC_N
DDRIO59PB0/GB0
DDRIO59NB0/GB4
DDRIO60PB0/MDDR_TMATCH_ECC_OUT
DDRIO60NB0/CCC_NE1_CLKI3

A18 DDR3-A14
B18 DDR3-A15
D17 DDR3-A12
C17 DDR3-A13
D15 DDR3-A10
E15 DDR3-A11
A16 DDR3-A8
B17 DDR3-A9
B16 DDR3-ODT
C16 DDR3-A7
B14 DDR3-A5
A15 DDR3-A6
C14 DDR3-A3
C15 DDR3-A4
A13 DDR3-A1
A14 DDR3-A2
D13 DDR3-BA2
D14 DDR3-A0
E13 DDR3-BA0
F13 DDR3-BA1
B13 DDR3-CLK_P
B12 DDR3-CLK_N
F11 DDR3-RESET
E12 DDR3-CAS
C12 DDR3-CKE
C11 DDR3-CS
D12 DDR3-RAS
E11 DDR3-WE
A11 DDR3-D14
B11 DDR3-D15
D10 DDR3-D12
E10 DDR3-D13
E8 TMATCH
F9 DDR3-DM1
C9 DDR3-DQS1_P
B9 DDR3-DQS1_N
D9 DDR3-D10
C10 DDR3-D11
A9 DDR3-D8
A10 DDR3-D9
D7 DDR3-D7
D8
A8 DDR3-D5
B8 DDR3-D6
B6 DDR3-DM0
B7 DDR3-D4
C6 DDR3-DQS0_P
C7 DDR3-DQS0_N
A5 DDR3-D2
A6 DDR3-D3
E7 DDR3-D0
F8 DDR3-D1
E6 NC
D5 NC
A3 NC
A4 NC
D4 TMATCH_ECC
C5 NC
B3 NC
B4 NC
A1 NC
B1 NC
C4
D3 NC

*clock input in M2S025/50/60

M2S010-VFG400

U2C

BANK 2

H18 VDDI2
L17 VDDI2
M20 VDDI2
N14 VDDI2
P16 VDDI2
R19 VDDI2
V18 VDDI2

SC_CLK M18
SC_SDI L17
SC_SDO N17
SC_SS P17

SC_CLK M18
SC_SDI L17
SC_SDO N17
SC_SS P17

H18 VDDI2
L17 VDDI2
M20 VDDI2
N14 VDDI2
P16 VDDI2
R19 VDDI2
V18 VDDI2

SC_CLK M18
SC_SDI L17
SC_SDO N17
SC_SS P17

C87 470nF 470nF
6.3V 6.3V
GNDX5R GNDX5R

C89 470nF 470nF
6.3V 6.3V
GNDX5R GNDX5R

*clock input in M2S025/50/60

M2S010-VFG400



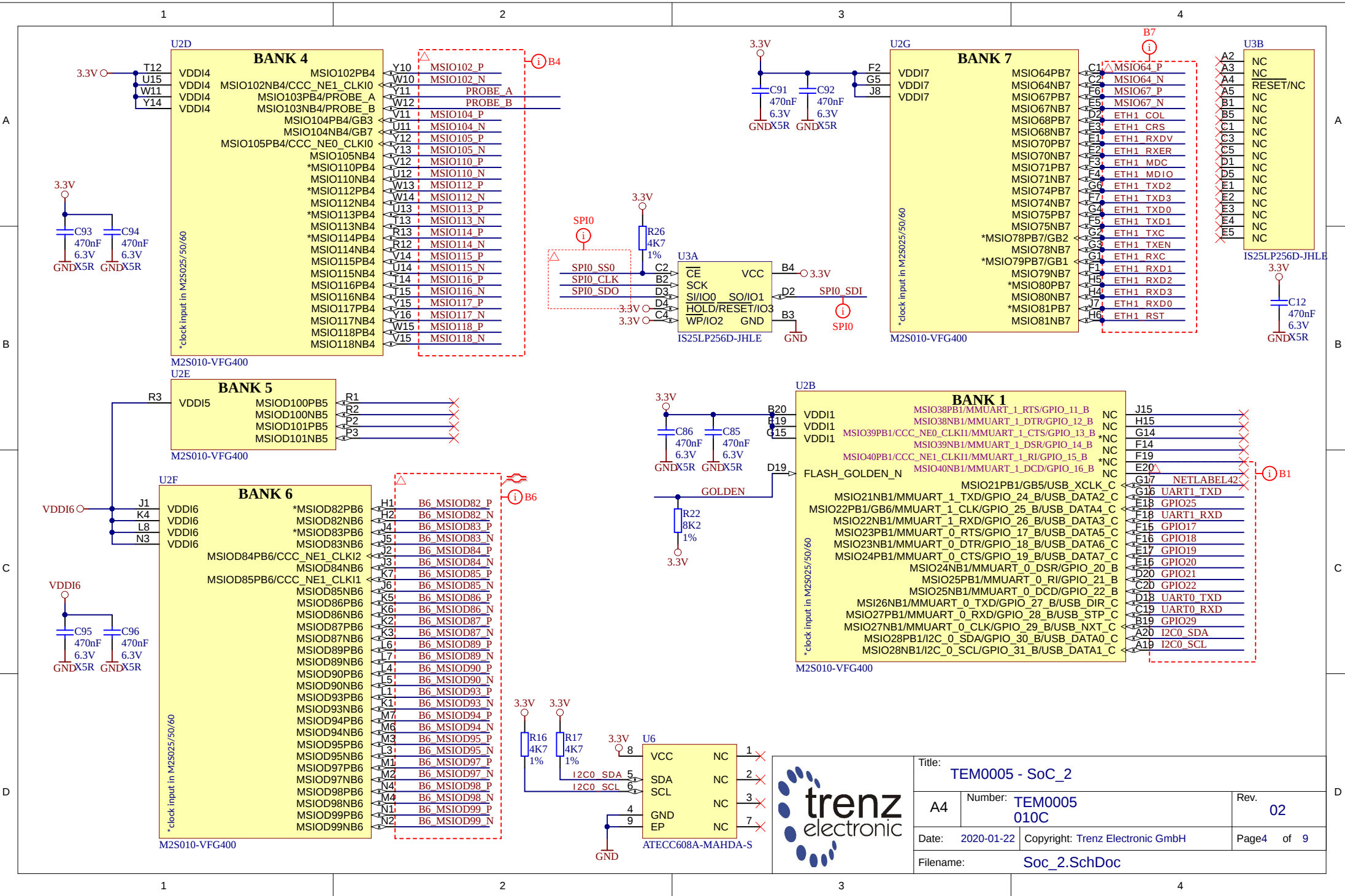
Title: TEM0005 - SoC_1		
A4	Number: TEM0005 010C	Rev. 02
Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page3 of 9
Filename: Soc_1.SchDoc		

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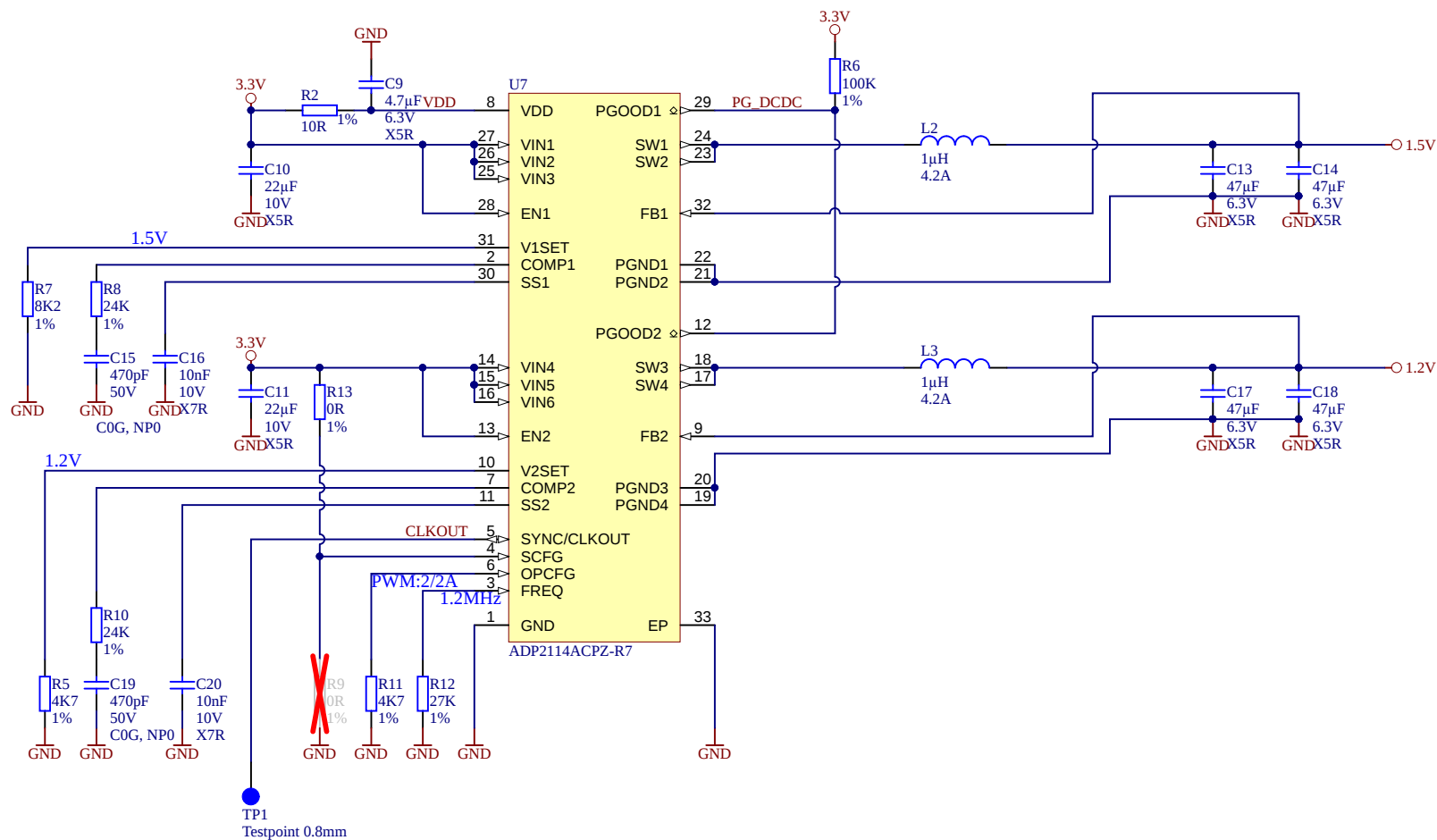
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Title: TEM0005 - SoC_2			
A4	Number: TEM0005 010C	Rev. 02	
Date: 2020-01-22	Copyright: Trenz Electronic GmbH		Page4 of 9
Filename: Soc_2.SchDoc			



	Title: TEM0005 - PowerSupply		
	A4	Number: TEM0005 010C	Rev. 02
	Date: 2020-01-22	Copyright: Trenz Electronic GmbH	Page8 of 9
	Filename: PowerSupply.SchDoc		

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VT: Initial Rev (07.2019)

REV02: (01.2020)

VT: 1) Support M2S050 -> added R29,R30, C24..C26,C31

VT: 2) Added resistor R32

VT: 3) Full upd LIB

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		Title: TEM0005 - Revision changes	
		A4	Rev. 02
		Date: 2020-01-22	Page9 of 9
		Filename: Revision_Changes.SchDoc	

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