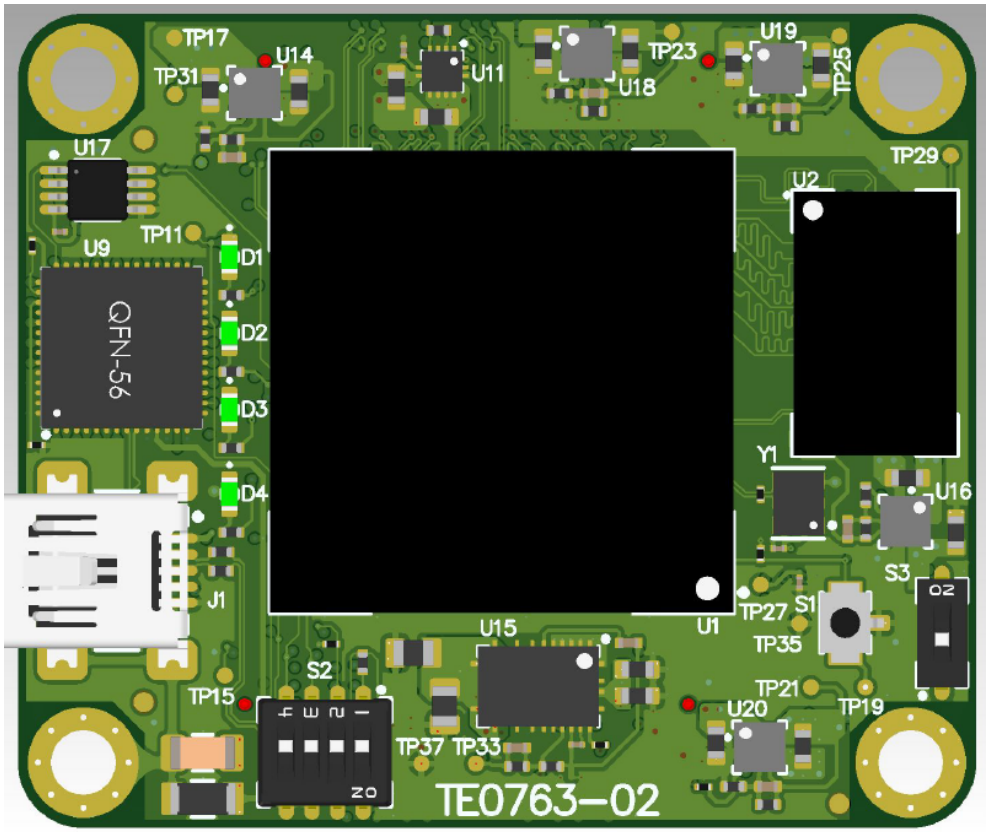

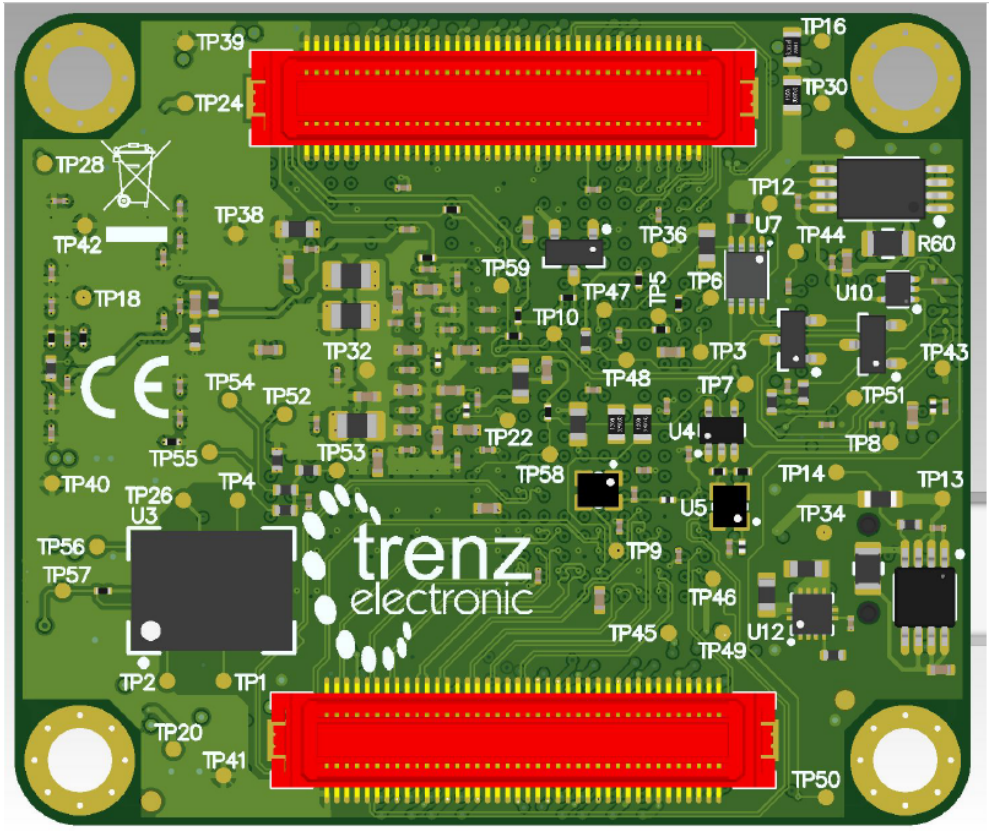

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices		
	A4	Number: TE0763 82I51-A	Rev. 02
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REV	Description	
-01	REV01 Initial revision ---------- Changes from TE0630-02 1) Changed FPGA to Artix 2) Changed PS DCDC to MPS parts	AL 24.01.2023
-02	1. Testpoint positions were corrected. 2. Added S3 (JTAG only mode). 3. CLK GEN DSC1123DL5-200.0000 (27130) replaced by SIT9121AI-2B1-XXE-200.00000 (33457). 4. Capacitor C47 330uF 1210 replaced by C47, C117, C118 100uF 0805.	IG 20.04.2023

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Title: Changes list

A4 | Number: TE0763 82I51-A | Rev. 02

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Filename: Revision_Changes.SchDoc

U_Power
Power_Diagram.SchDoc

U_FPGA_PWR
FPGA_PWR.SchDoc

U_DDR3_RAM
DDR3_RAM.SchDoc

U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc

U_FPGA_B13_B14
FPGA_B13_B14.SchDoc

U_FPGA_DDR3
FPGA_DDR3.SchDoc

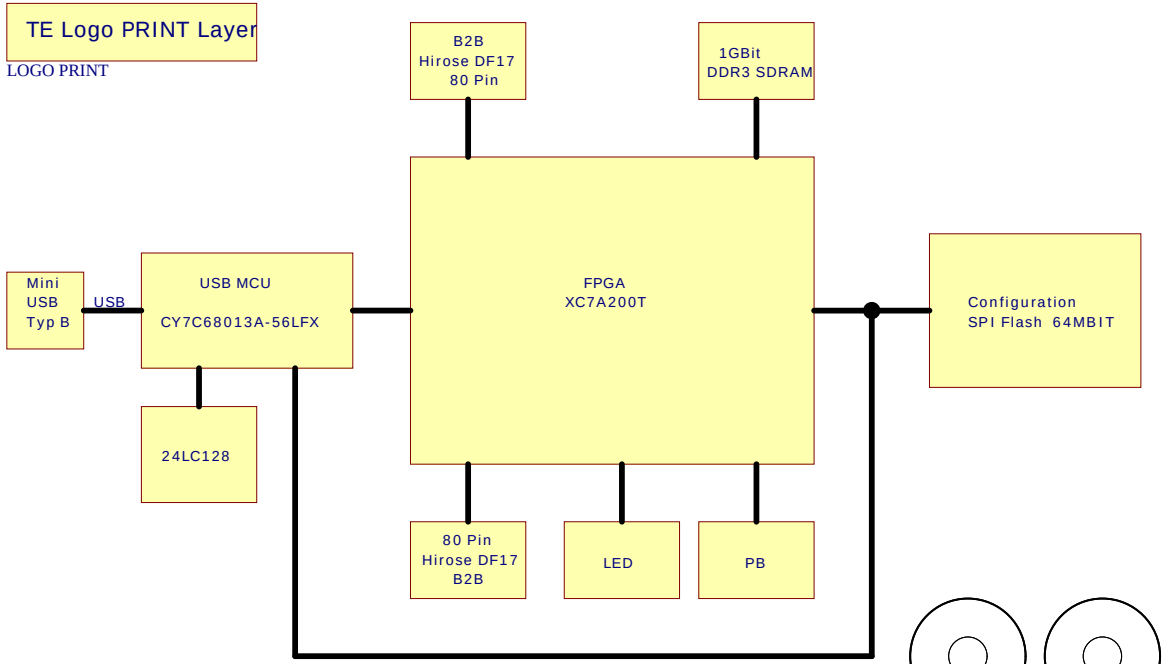
U_FPGA_B15
FPGA_B15.SchDoc

U_FPGA_B16
FPGA_B16.SchDoc

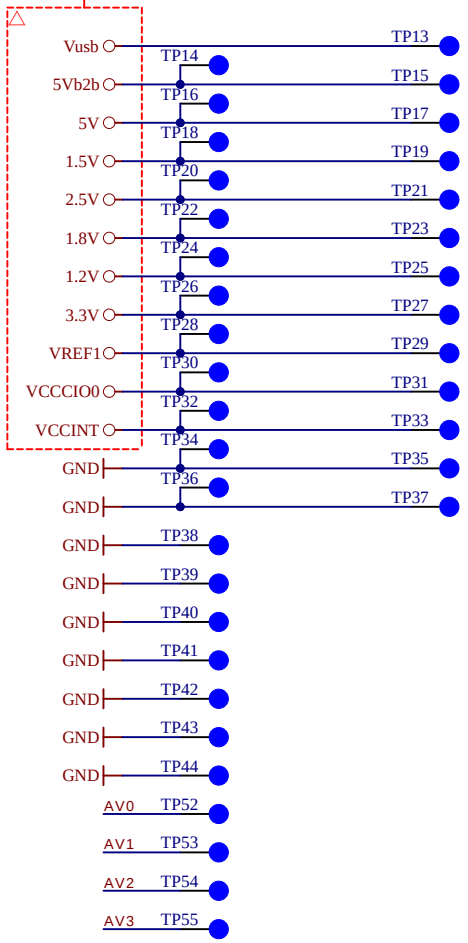
U_USB
USB.SchDoc

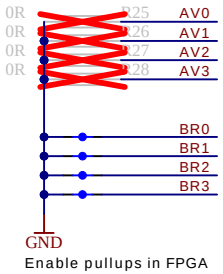
U_B2B_Connectors
B2B_Connectors.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



GlobalNet





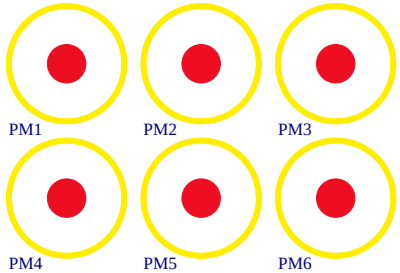
Enable pullups in FPGA

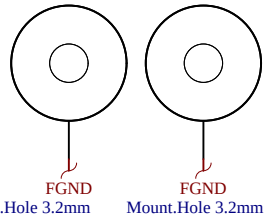
Assembly Variants

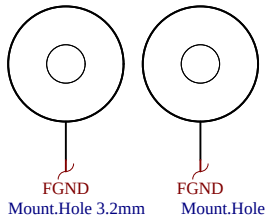
AV0	AV1	AV2	AV3	
1	1	1	1	TE0763-01-82I51-A
1	1	1	0	TE0763-01-82I51-B (MiniUSB - Not populated)

Board Revisions

BR0	BR1	BR2	BR3	
0	0	0	0	-01 Initial revision







Serial1
Serial
Serialnumber 6,3 x 6.3mm

Drawn by	IG
Checked by	IG
Assembly variant	82I51-A
Created by	IG
Modified by	-
Modified at	-

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Title: Overviev

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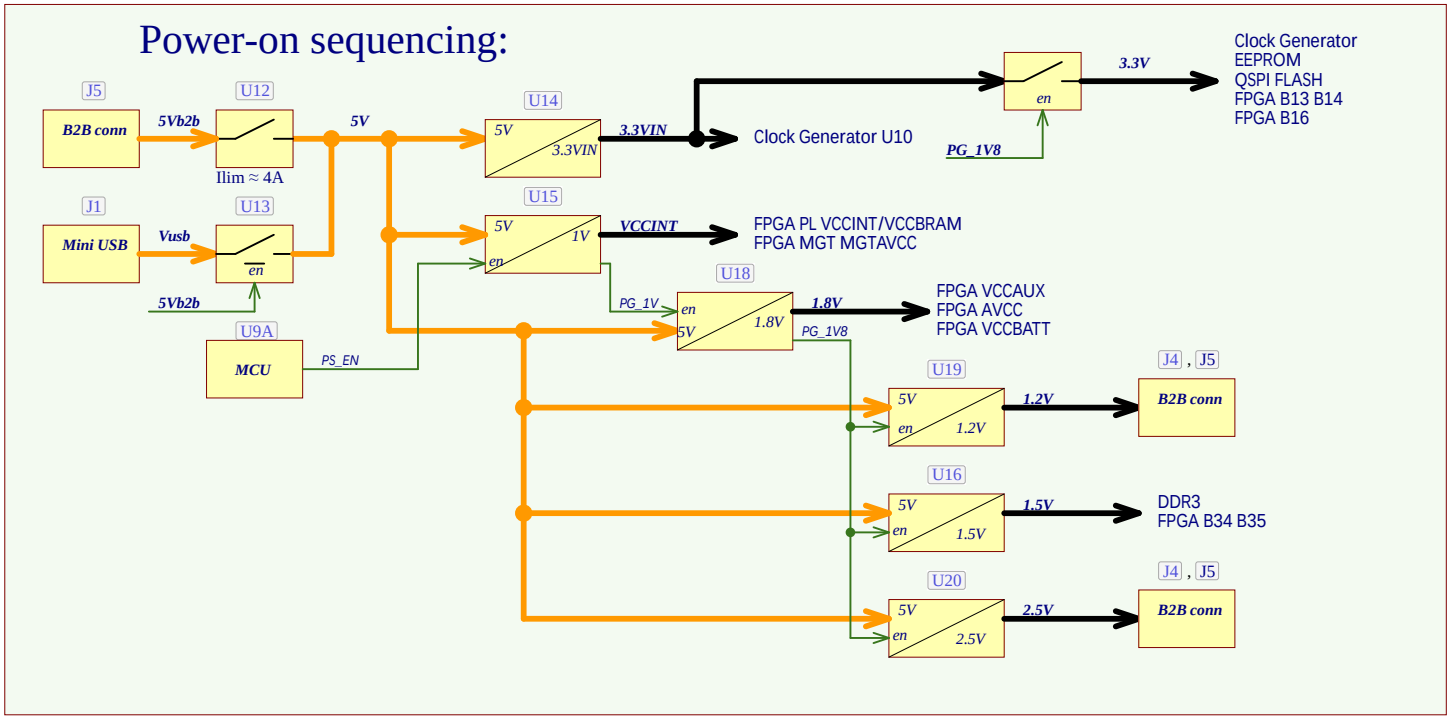
Power-on sequencing:



Supported Voltage Ranges:

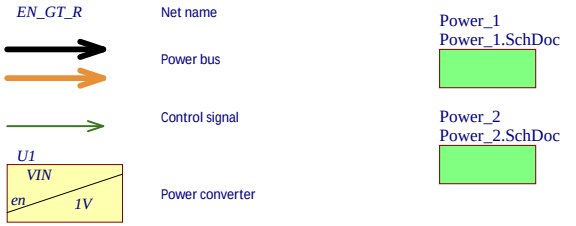
Power Rail	Direction	Range	Tolerance	Description	Note
5Vb2b	IN	5V	±5%	Micromodule Power	-
Vusb	IN	5V	±5%	Micromodule Power	-
3.3VIN		3.3V	±3%	Internal Power	-
3.3V		3.3V	±3%	Internal Power	FPGA B13, B14, B16
VCCIO0		3.3V or 2.5V	±3%	Internal Power	3.3V (Default) FPGA B15
VCCINT		1.0V	±2%	Internal Power	FPGA CORE
1.8V		1.8V	±3%	Internal Power	FPGA VCCAUX, AVCC, VCCBAT
1.2V	OUT	1.2V	±3%	Power Supply for External load	Current rating ≤ 1A
1.5V		1.5V	±3%	DDR Power	FPGA B34, B35, DDR3
2.5V	OUT	2.5V	±3%	Power Supply for External load	Current rating ≤ 1A

Programmable Logic, supplied by power rail

Low-Power Domain, supplied by power rail

GTH/GTY Transceiver, supplied by power rail

Full-Power Domain and GTR, supplied by power rail



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Title: Power_Diagram			
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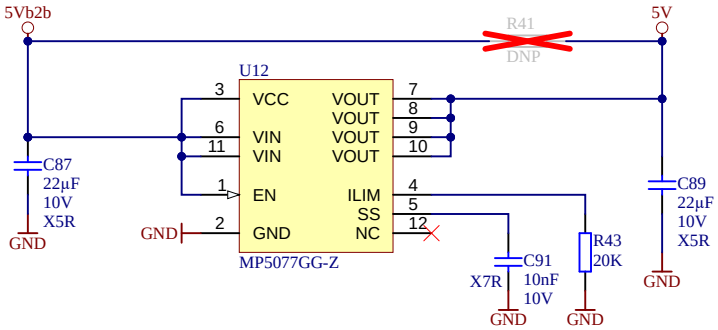
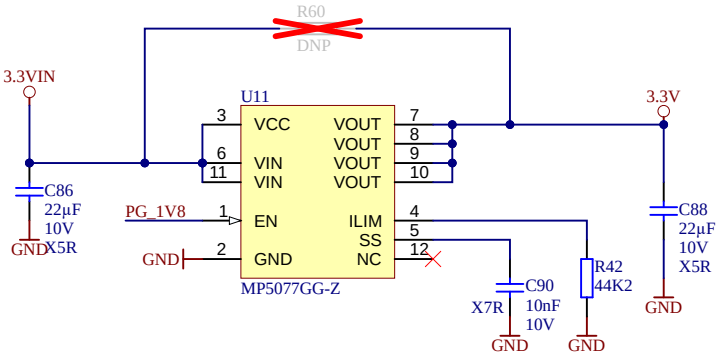
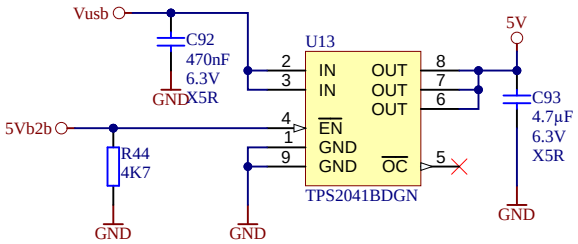
Date: 22.11.2023	Copyright: Trenz Electronic GmbH		Page 4 of 15
Filename: Power_Diagram.SchDoc			







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	Date: 22.11.2023	Copyright: Trenz Electronic GmbH	Page 5 of 15
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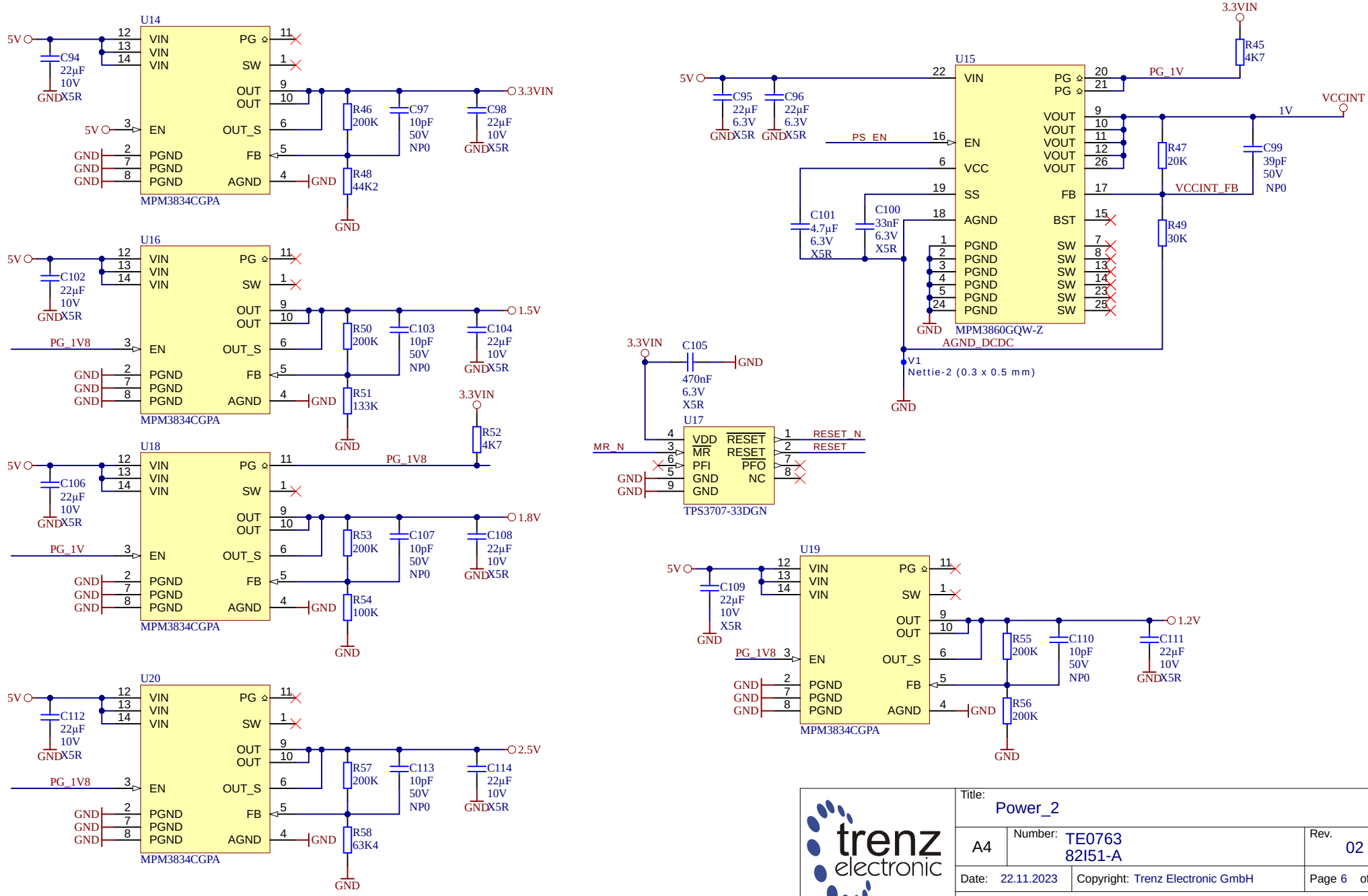

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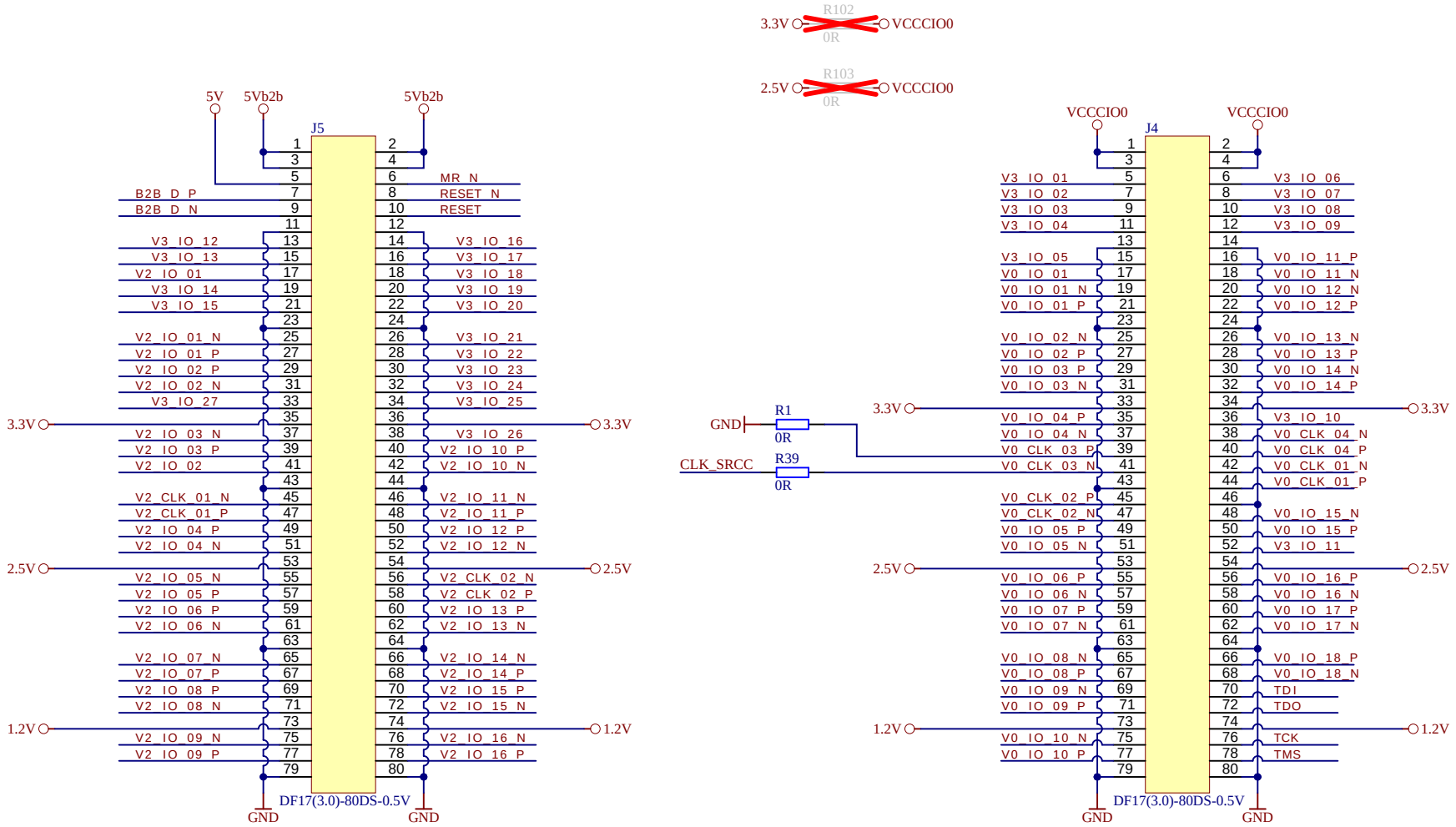
Filename: Power_2.SchDoc			



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Date: 22.11.2023	Copyright: Trenz Electronic GmbH		Page 7 of 15
Filename: B2B_Connectors.SchDoc			

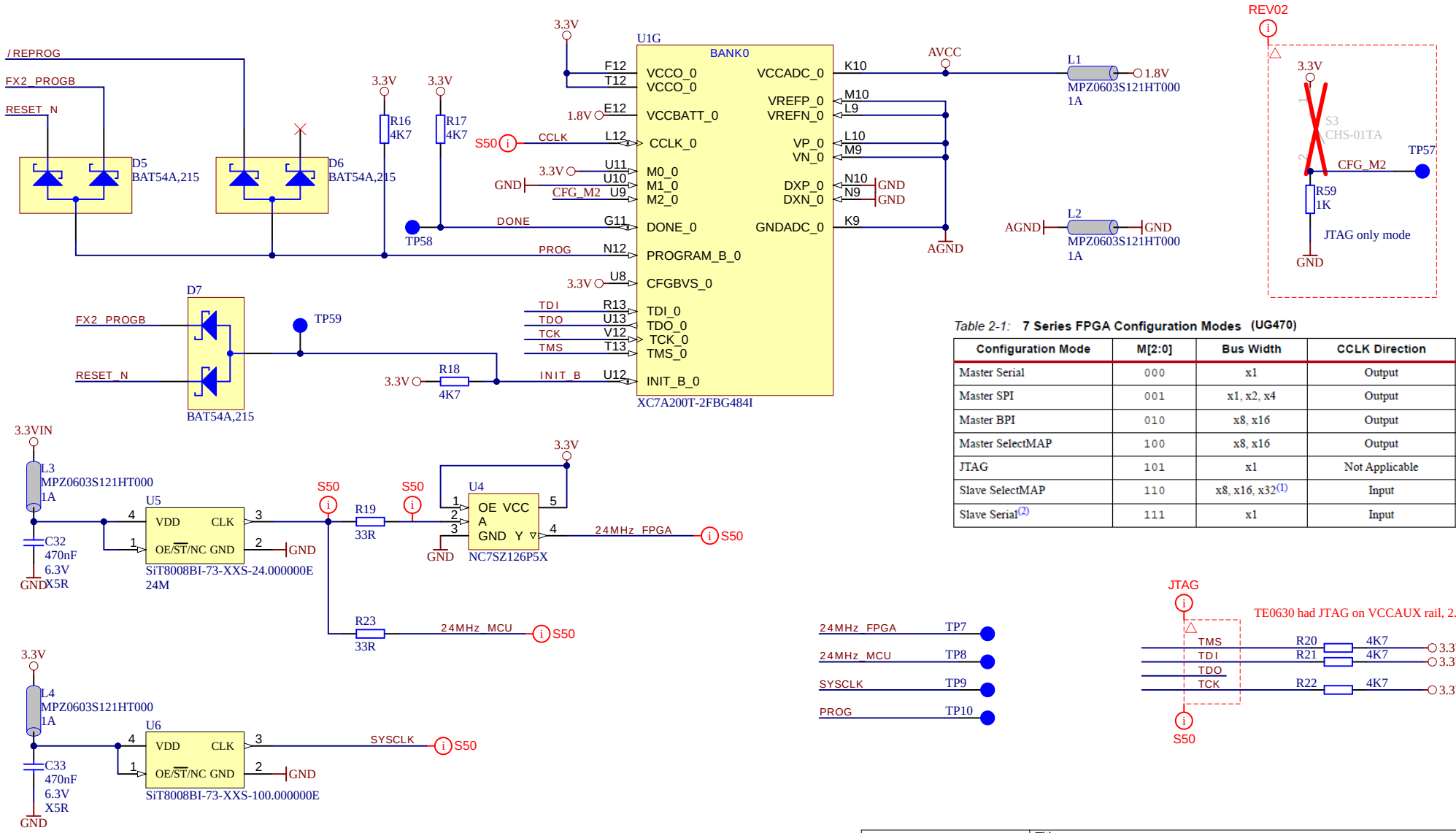

Table 2-1: **7 Series FPGA Configuration Modes (UG470)**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input

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Title: FPGA_CFG_CLK		
A4	Number: TE0763 82I51-A	Rev. 02
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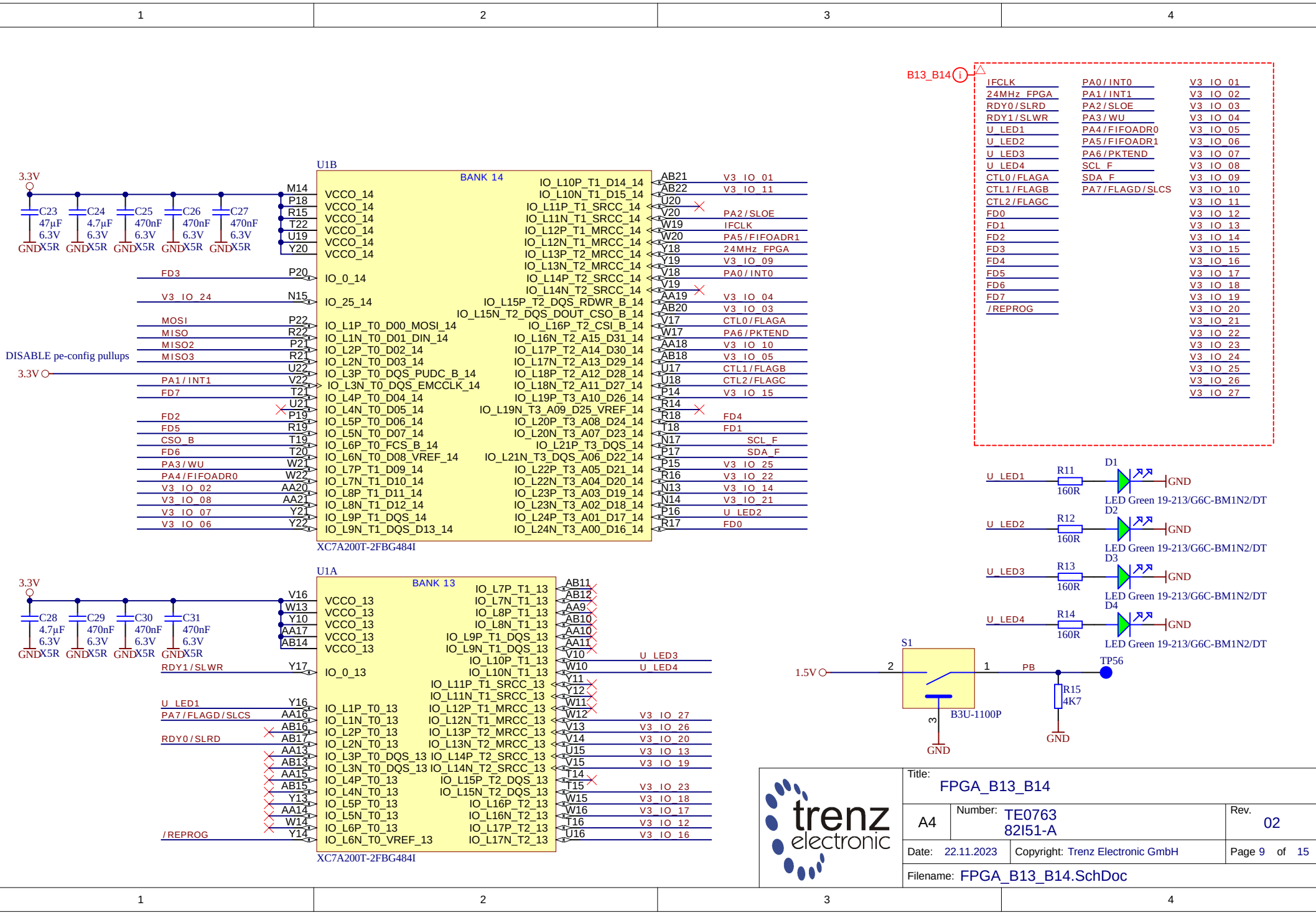
Filename: FPGA_CFG_CLK.SchDoc		



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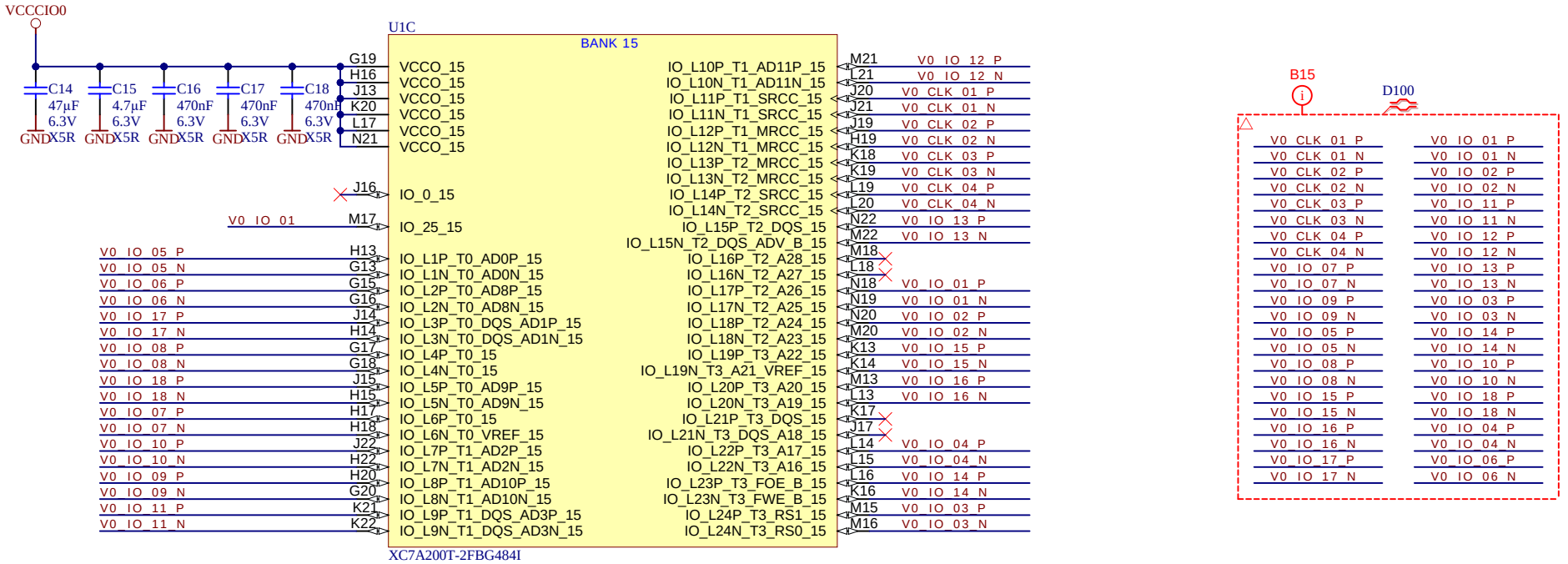
Filename: FPGA_B13_B14.SchDoc		



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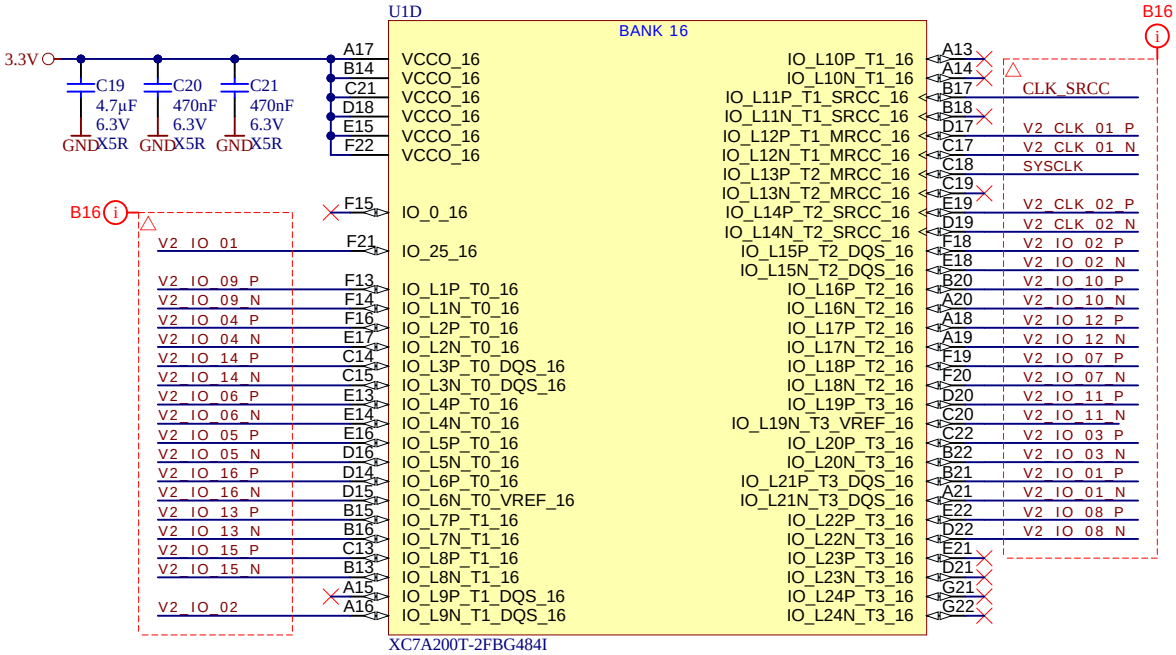

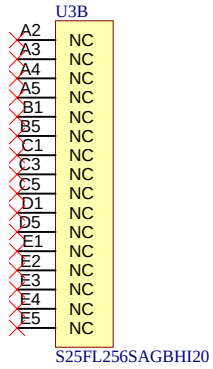

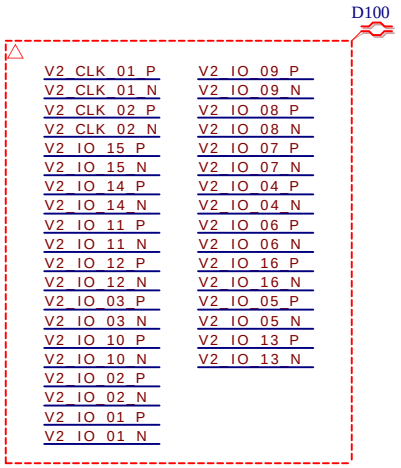

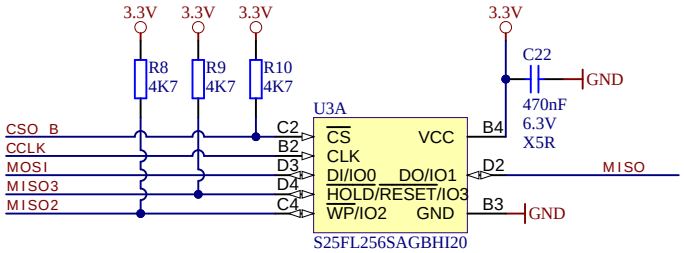

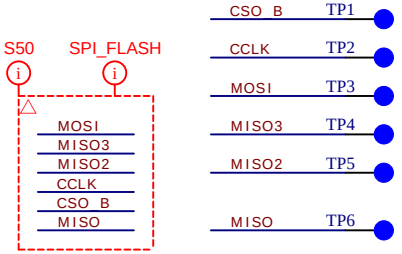

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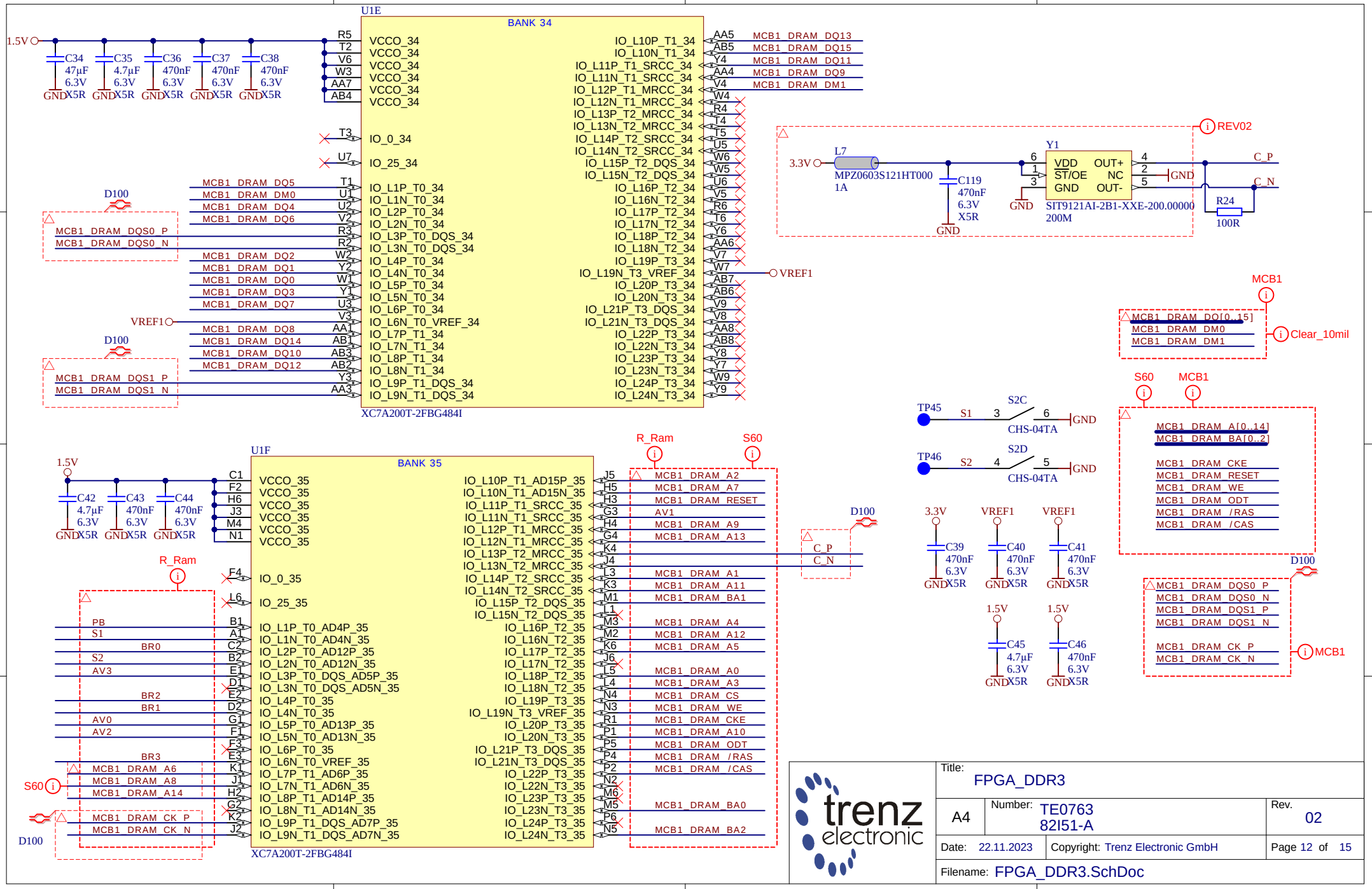
Date: 22.11.2023	Copyright: Trenz Electronic GmbH		Page 11 of 15
Filename: FPGA_B16.SchDoc			



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Date: 22.11.2023	Copyright: Trenz Electronic GmbH		Page 12 of 15
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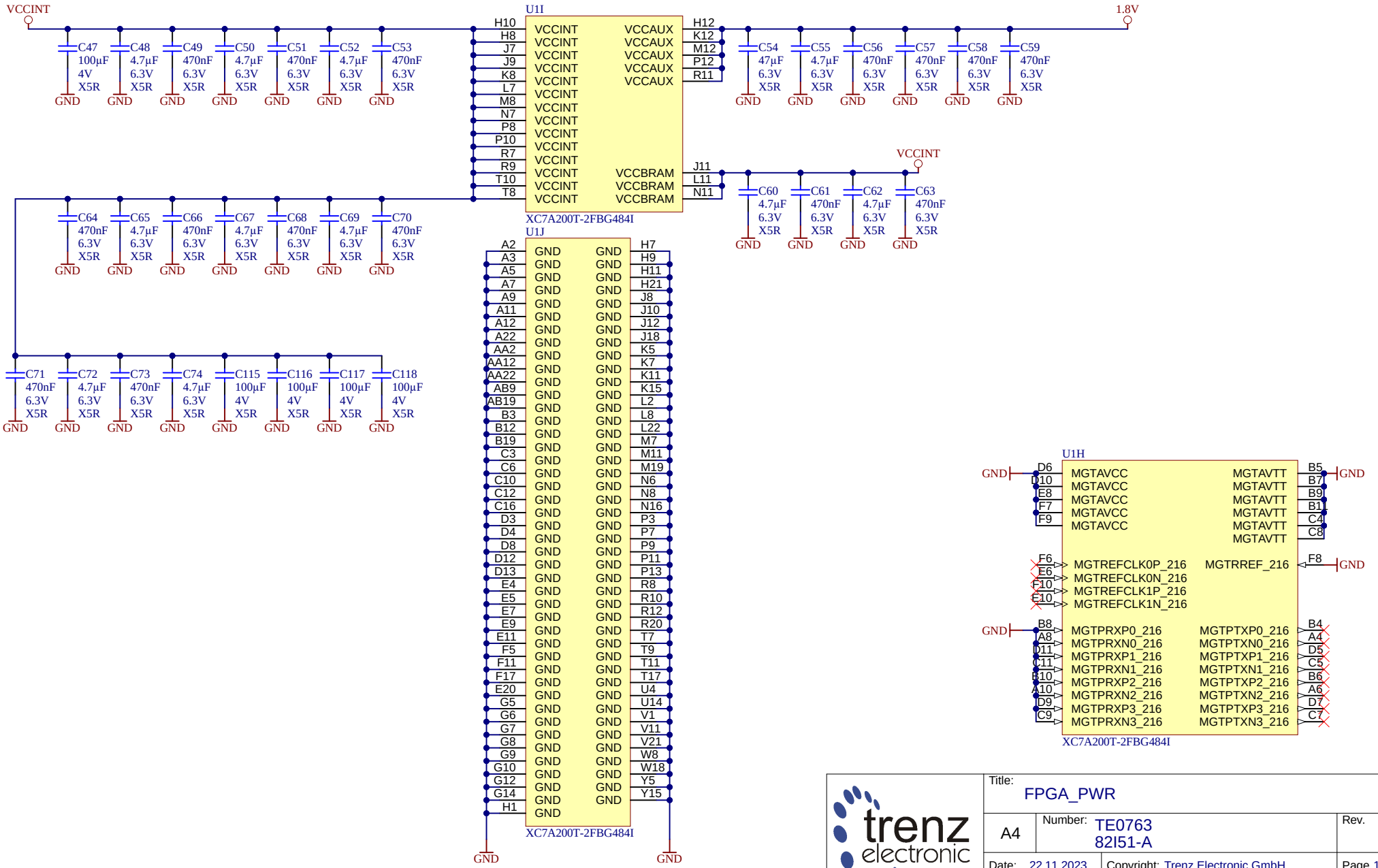

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Title: FPGA_PWR		
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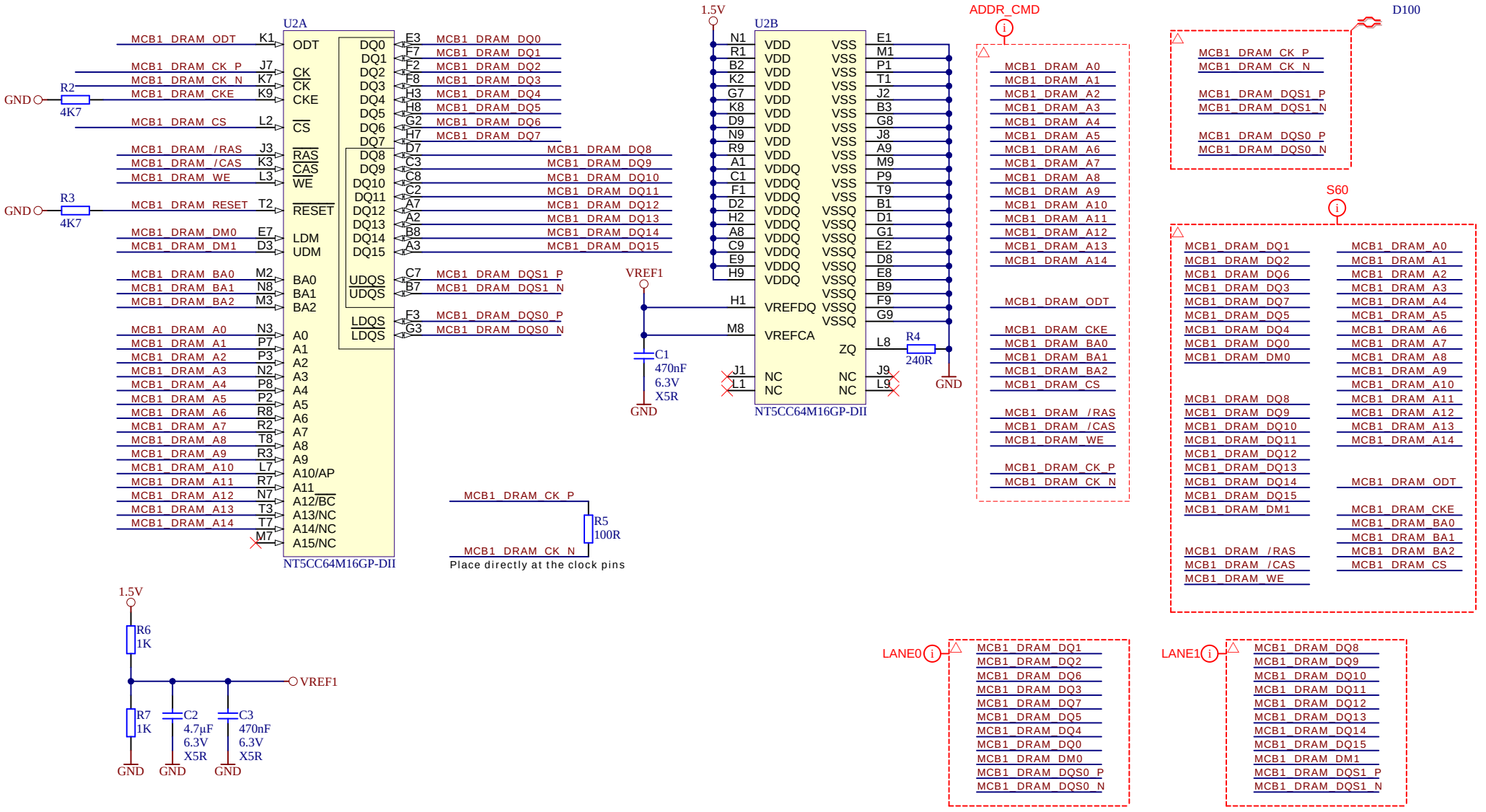
Filename: FPGA_PWR.SchDoc		



Title: DDR3_RAM			
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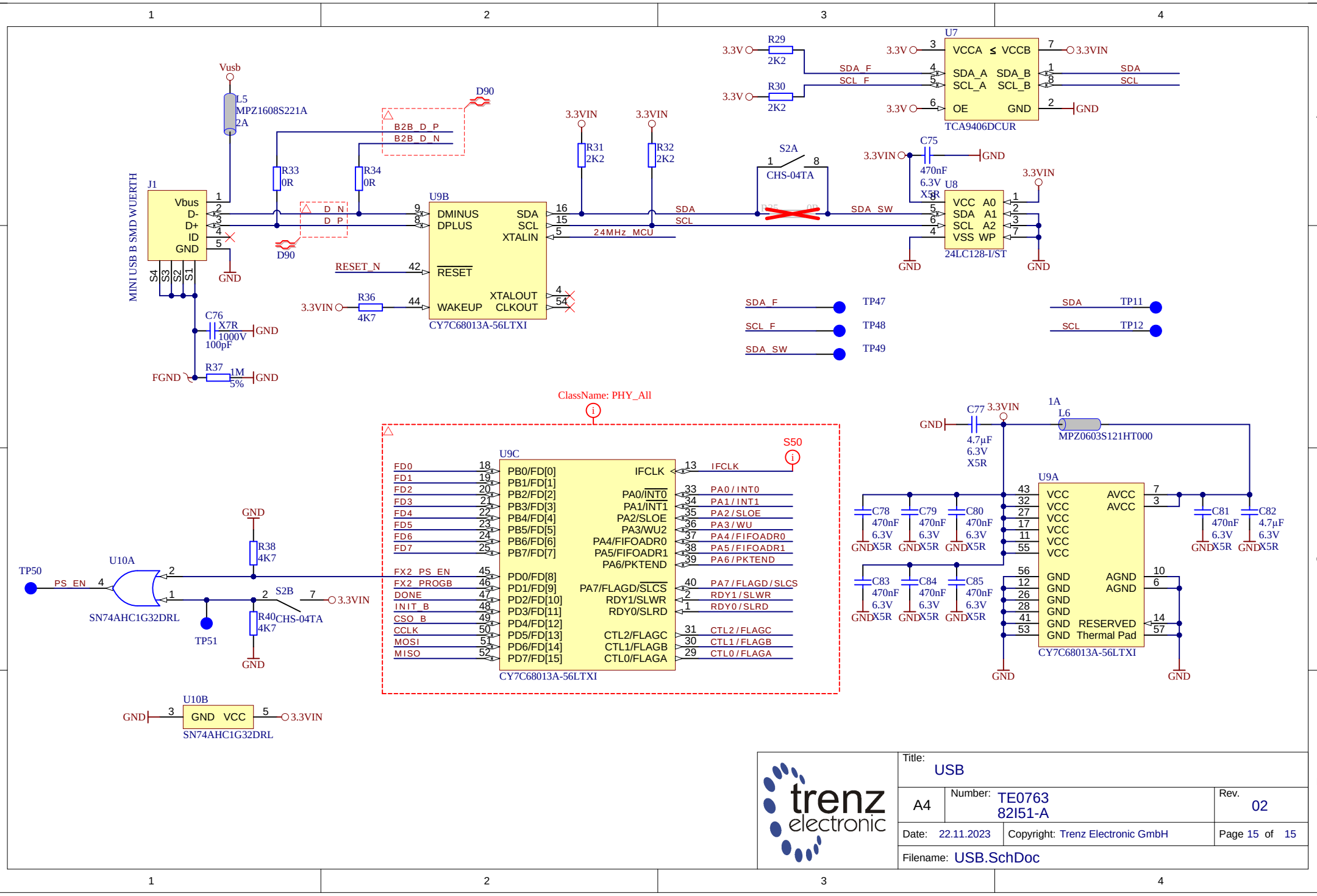
Date: 22.11.2023	Copyright: Trenz Electronic GmbH		Page 14 of 15
Filename: DDR3_RAM.SchDoc			



trenz electronic	Title: USB		
A4	Number: TE0763 82I51-A		Rev. 02
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Filename: USB.SchDoc			