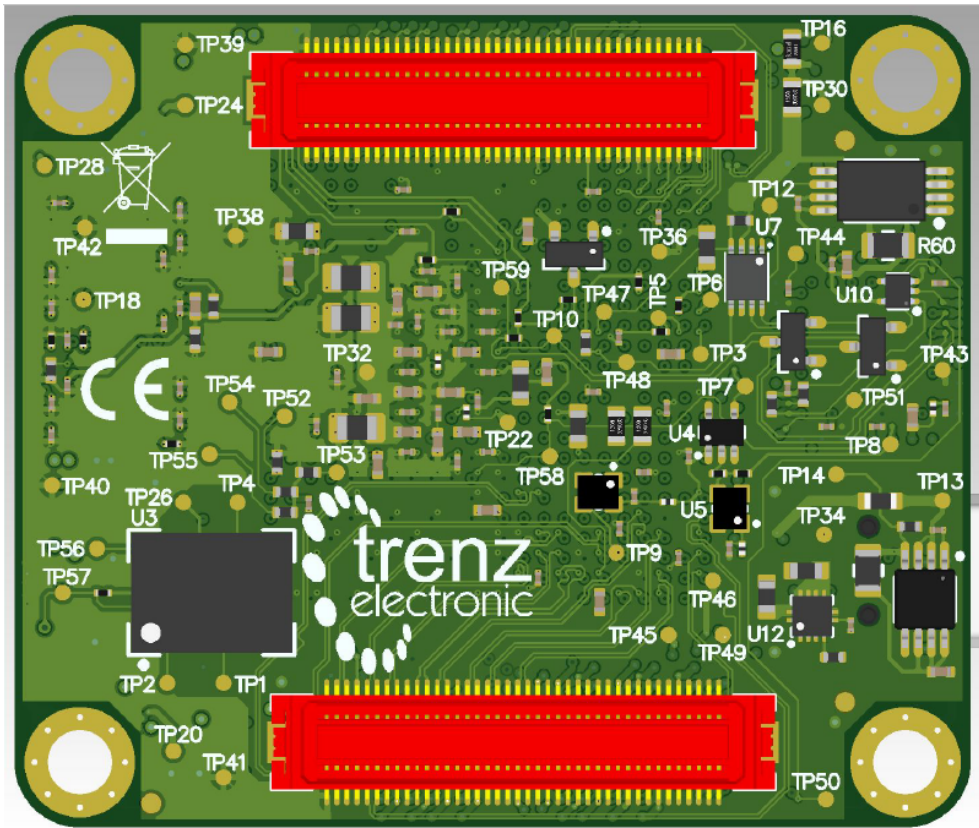
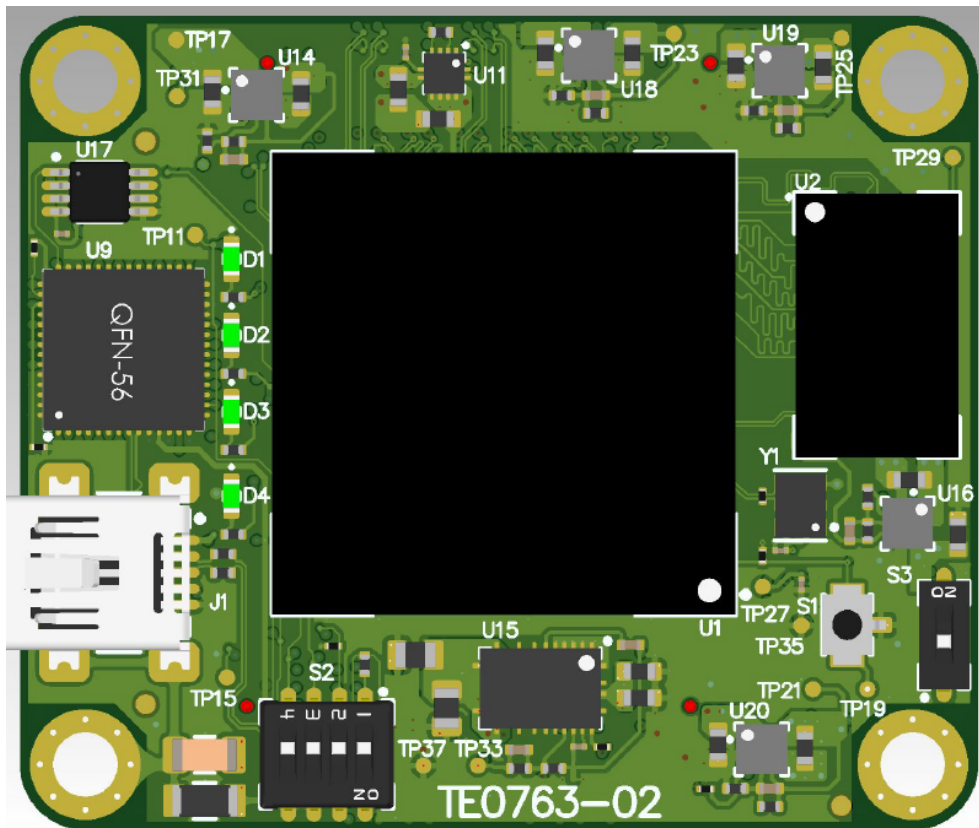




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		Title: Legal Notices	
		A4	Number: TE0763 82I51-A
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Filename: Legal Notices Modules.SchDoc		Page 1 of 15	

	1	2	3	4									
A	<table><tr><td>REV</td><td>Description</td><td></td></tr><tr><td>-01</td><td>REV01 Initial revision ----- Changes from TE0630-02 1) Changed FPGA to Artix 2) Changed PS DCDC to MPS parts</td><td>AL 24.01.2023</td></tr><tr><td>-02</td><td>1. Testpoint positions were corrected. 2. Added S3 (JTAG only mode). 3. CLK GEN DSC1123DL5-200.0000 (27130) replaced by SIT9121AI-2B1-XXE-200.00000 (33457). 4. Capacitor C47 330uF 1210 replaced by C47, C117, C118 100uF 0805.</td><td>IG 20.04.2023</td></tr></table>				REV	Description		-01	REV01 Initial revision ----- Changes from TE0630-02 1) Changed FPGA to Artix 2) Changed PS DCDC to MPS parts	AL 24.01.2023	-02	1. Testpoint positions were corrected. 2. Added S3 (JTAG only mode). 3. CLK GEN DSC1123DL5-200.0000 (27130) replaced by SIT9121AI-2B1-XXE-200.00000 (33457). 4. Capacitor C47 330uF 1210 replaced by C47, C117, C118 100uF 0805.	IG 20.04.2023
REV	Description												
-01	REV01 Initial revision ----- Changes from TE0630-02 1) Changed FPGA to Artix 2) Changed PS DCDC to MPS parts	AL 24.01.2023											
-02	1. Testpoint positions were corrected. 2. Added S3 (JTAG only mode). 3. CLK GEN DSC1123DL5-200.0000 (27130) replaced by SIT9121AI-2B1-XXE-200.00000 (33457). 4. Capacitor C47 330uF 1210 replaced by C47, C117, C118 100uF 0805.	IG 20.04.2023											
B													
C													
D	 Title: Changes list A4 Number: TE0763 82I51-A Rev. 02 Date: 22.11.2023 Copyright: Trenz Electronic GmbH Page 2 of 15 Filename: Revision_Changes.SchDoc												
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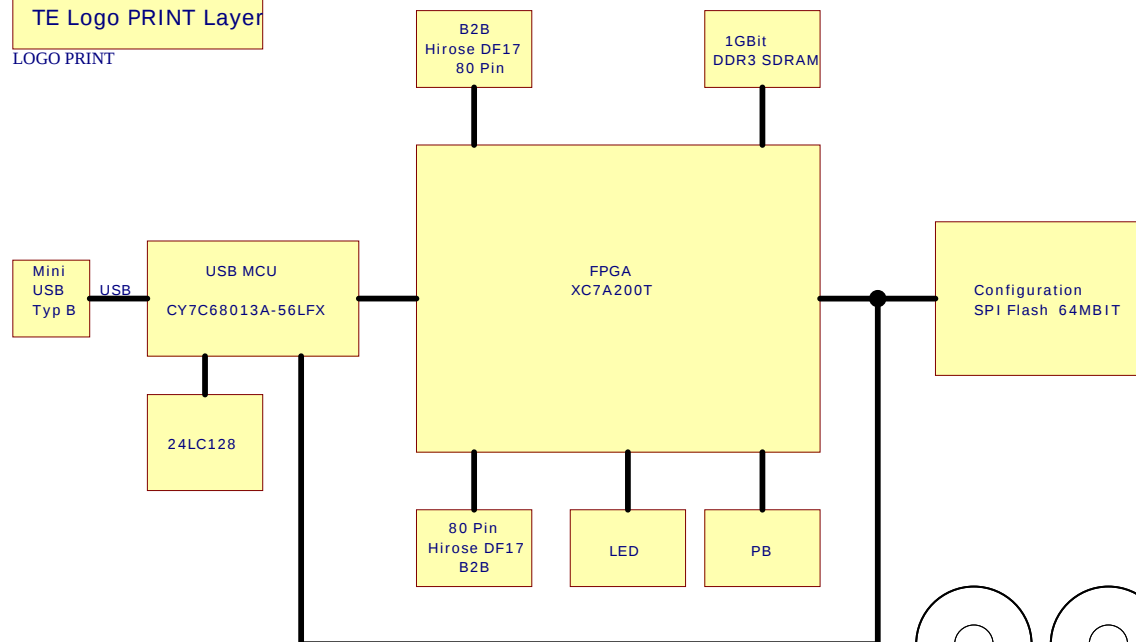
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U_Power
Power_Diagram.SchDoc
U_FPGA_PWR
FPGA_PWR.SchDoc
U_DDR3_RAM
DDR3_RAM.SchDoc
U_FPGA_CFG_CLK
FPGA_CFG_CLK.SchDoc
U_FPGA_B13_B14
FPGA_B13_B14.SchDoc
U_FPGA_DDR3
FPGA_DDR3.SchDoc
U_FPGA_B15
FPGA_B15.SchDoc
U_FPGA_B16
FPGA_B16.SchDoc
U_USB
USB.SchDoc
U_B2B_Connectors
B2B_Connectors.SchDoc

LOGO1

TE Logo PRINT Layer

LOGO PRINT



Assembly Variants

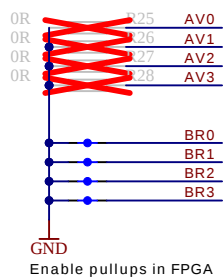
AV0 AV1 AV2 AV3

AV0	AV1	AV2	AV3	Part
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1	1	1	0	TE0763-01-82I51-B (MiniUSB - Not populated)

Board Revisions

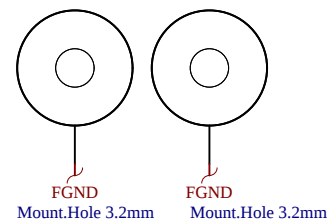
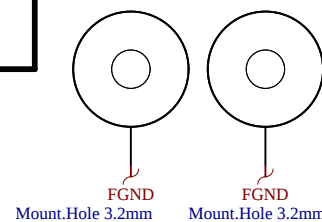
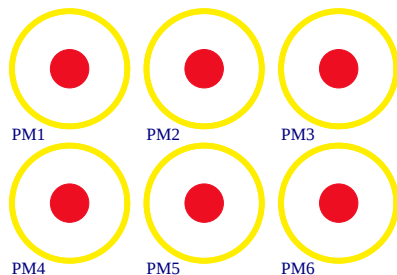
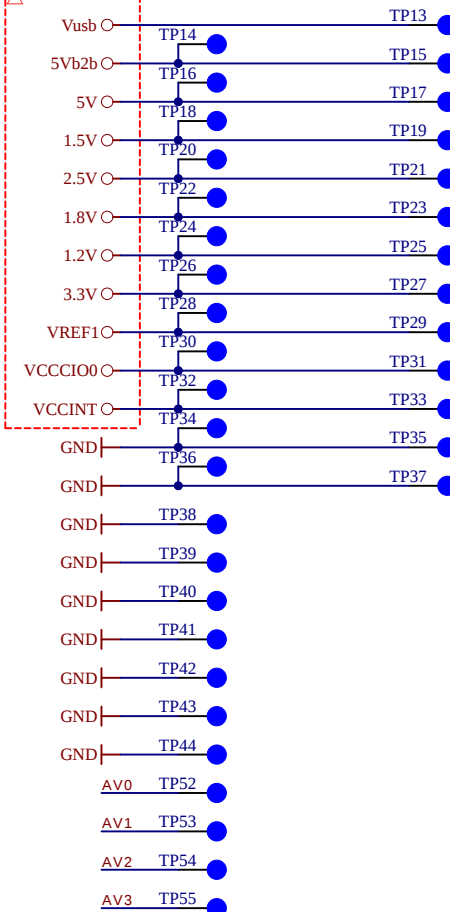
BR0 BR1 BR2 BR3

BR0	BR1	BR2	BR3	Revision
0	0	0	0	-01 Initial revision



Enable pullups in FPGA

Serial1
Serial
Serialnumber 6,3 x 6.3mm

GlobalNet
i

Drawn by IG
Checked by IG
Assembly variant 82I51-A
Created by IG
Modified by -
Modified at -

Title:
Overview

A4

Number: TE0763
82I51-ARev.
02

Date: 22.11.2023

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Filename: TE0763.SchDoc

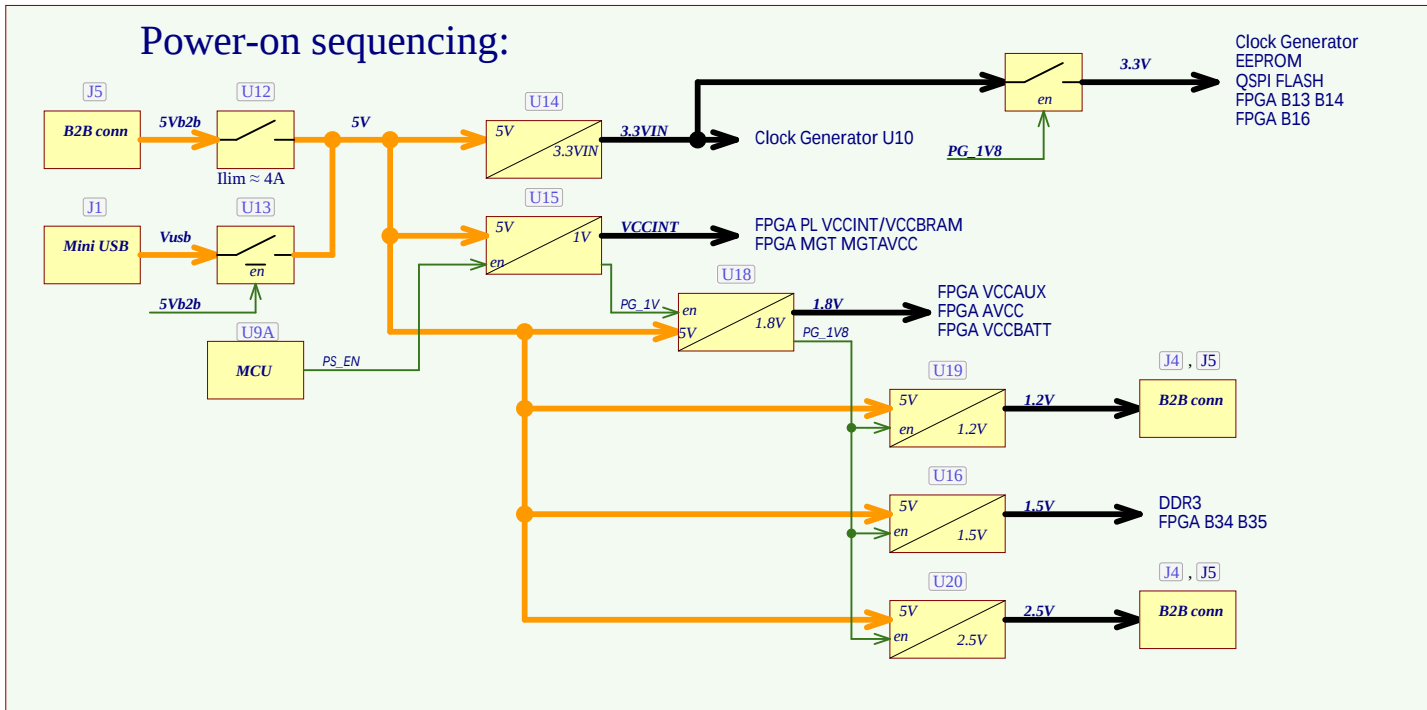
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Power-on sequencing:



Supported Voltage Ranges:

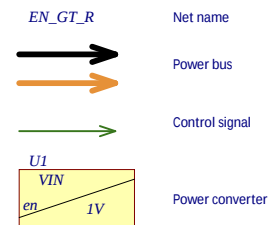
Power Rail	Direction	Range	Tolerance	Description	Note
5Vb2b	IN	5V	±5%	Micromodule Power	-
Vusb	IN	5V	±5%	Micromodule Power	-
3.3VIN		3.3V	±3%	Internal Power	-
3.3V		3.3V	±3%	Internal Power	FPGA B13, B14, B16
VCCIO0		3.3V or 2.5V	±3%	Internal Power	3.3V (Default) FPGA B15
VCCINT		1.0V	±2%	Internal Power	FPGA CORE
1.8V		1.8V	±3%	Internal Power	FPGA VCCAUX, AVCC, VCCBAT
1.2V	OUT	1.2V	±3%	Power Supply for External load	Current rating ≤ 1A
1.5V		1.5V	±3%	DDR Power	FPGA B34, B35, DDR3
2.5V	OUT	2.5V	±3%	Power Supply for External load	Current rating ≤ 1A

Programmable Logic, supplied by power rail

Low-Power Domain, supplied by power rail

GTH/GTY Transceiver, supplied by power rail

Full-Power Domain and GTR, supplied by power rail

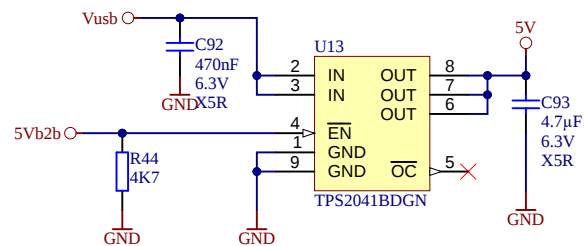
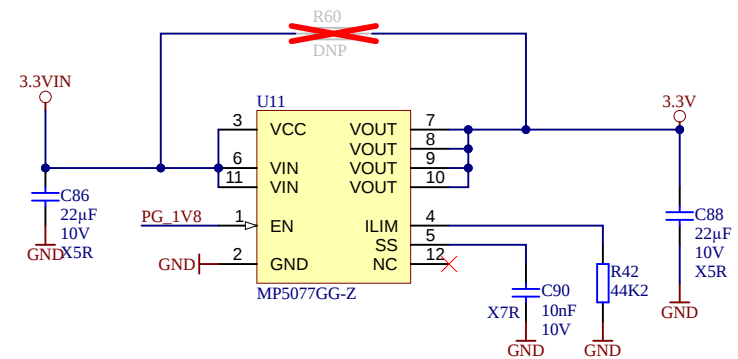


Power_1
Power_1.SchDoc

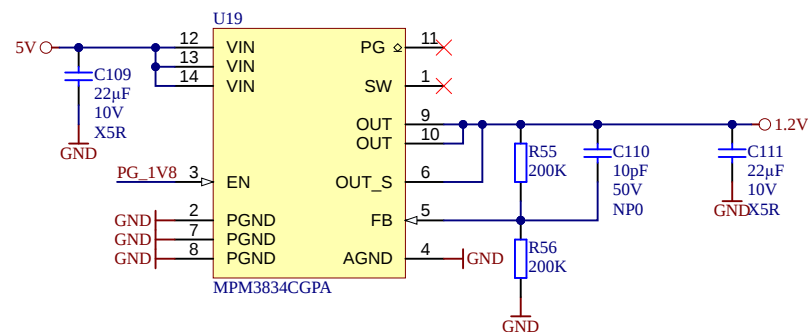
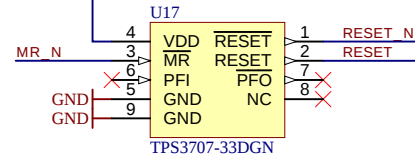
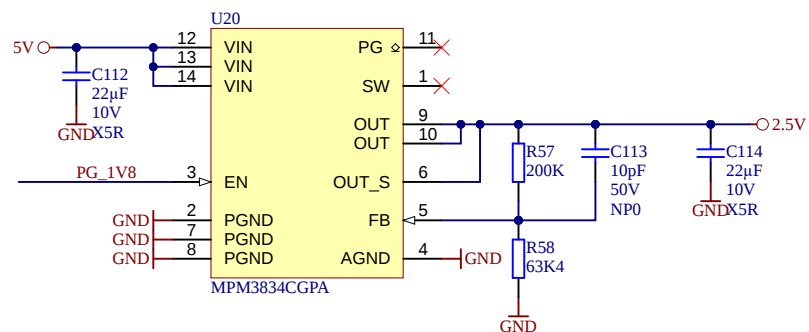
Power_2
Power_2.SchDoc

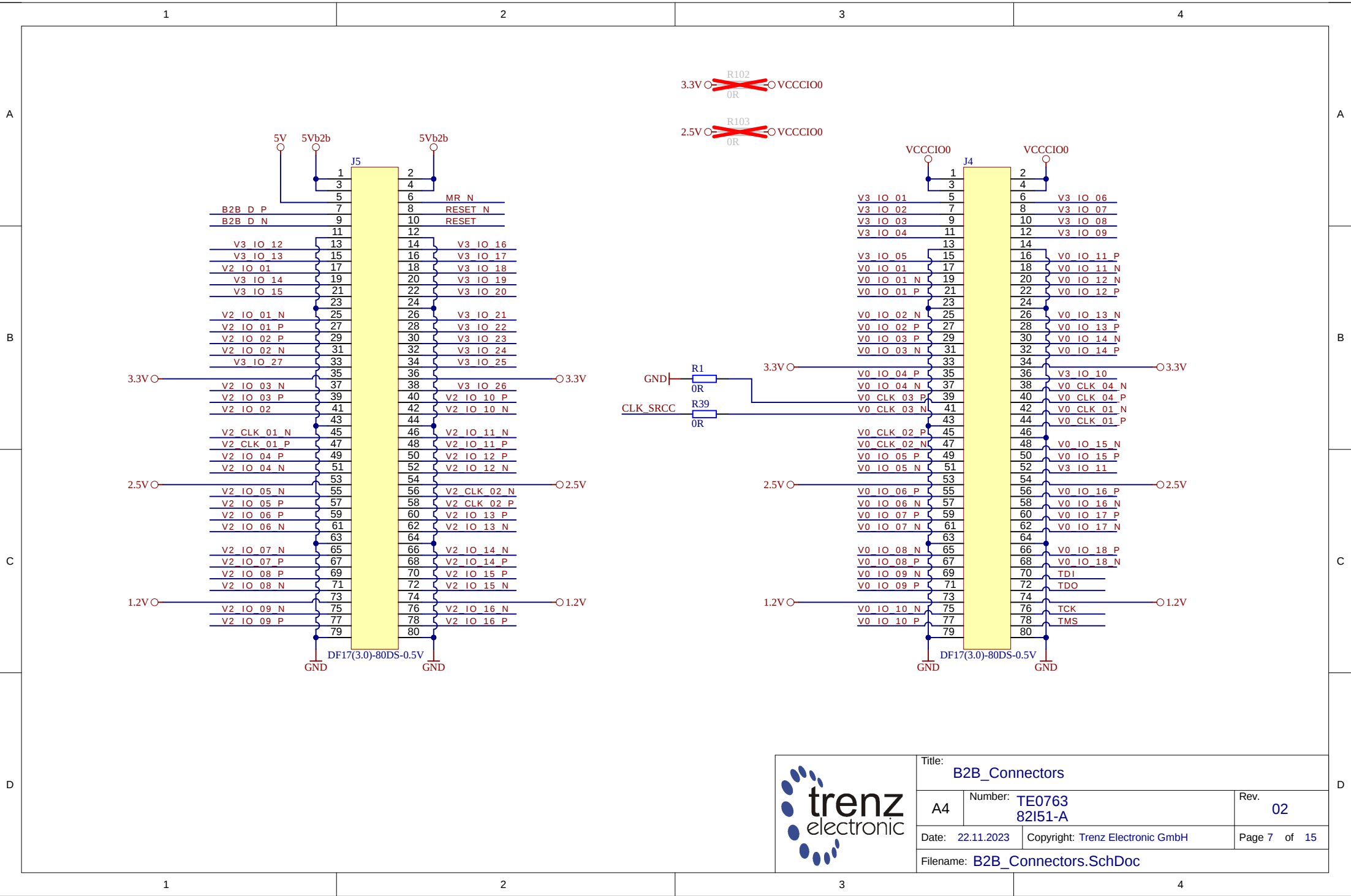


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Date: 22.11.2023	Copyright: Trenz Electronic GmbH	Page 4 of 15
Filename: Power_Diagram.SchDoc		



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A4	Number: TE0763 82I51-A	Rev. 01
Date: 22.11.2023	Copyright: Trenz Electronic GmbH	Page 5 of 15
Filename: Power_1.SchDoc		





Title: B2B_Connectors			
A4	Number: TE0763 82I51-A		Rev. 02
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Filename: B2B_Connectors.SchDoc			

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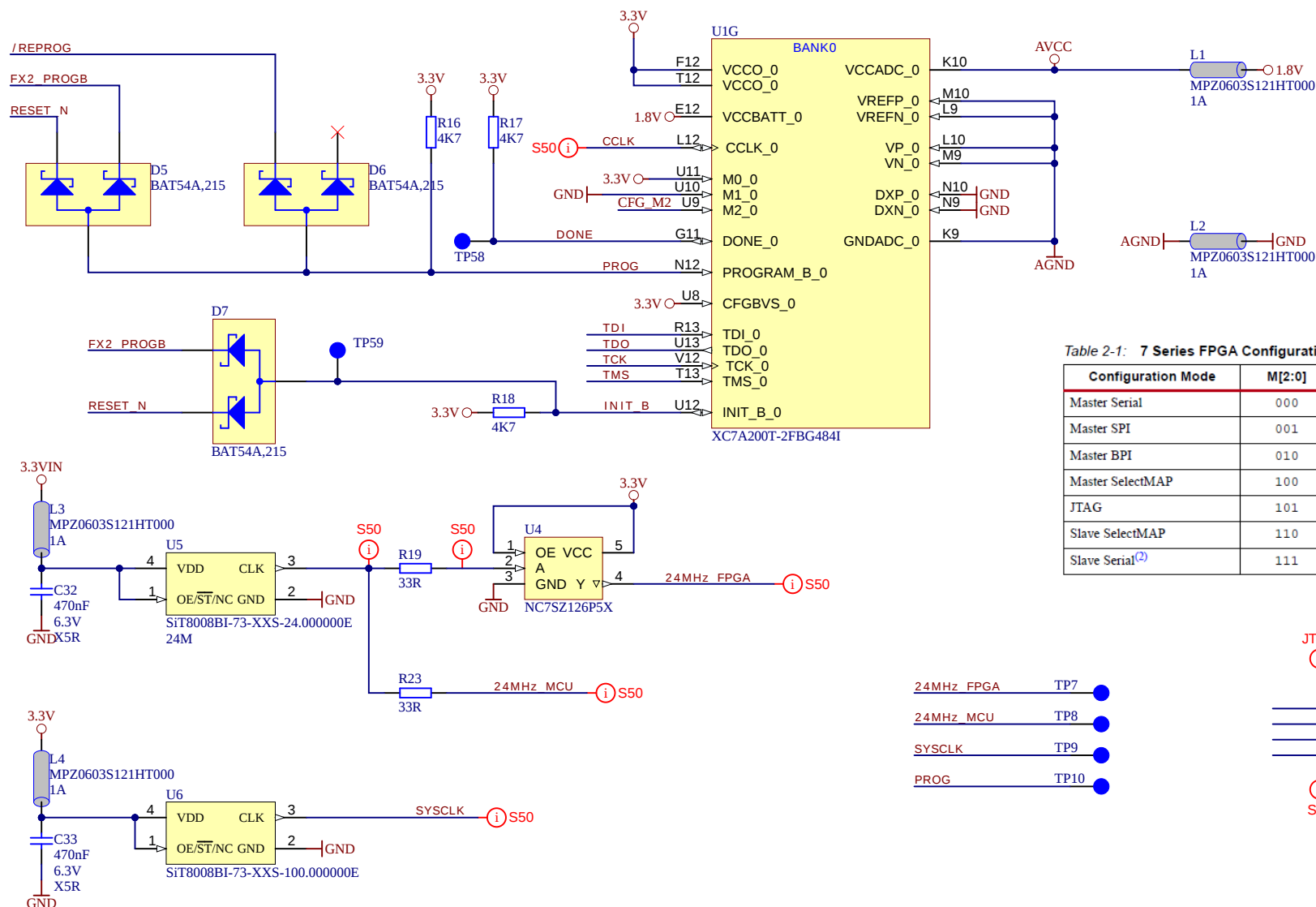
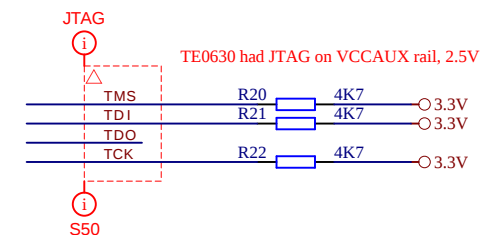
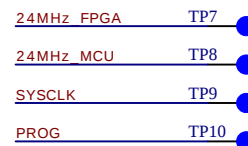


Table 2-1: 7 Series FPGA Configuration Modes (UG470)

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input



Title: FPGA_CFG_CLK		
A4	Number: TE0763 82I51-A	Rev. 02
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Filename: FPGA_CFG_CLK.SchDoc		

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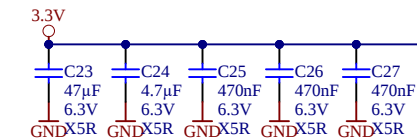
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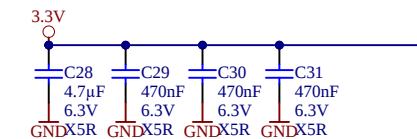


U1B

BANK 14

VCCO_14	IO_L10P_T1_D14_14	AB21	V3 IO_01
VCCO_14	IO_L10N_T1_D15_14	AB22	V3 IO_11
VCCO_14	IO_L11P_T1_SRCC_14	U20	PA2/SLOE
VCCO_14	IO_L11N_T1_SRCC_14	W19	IFCLK
VCCO_14	IO_L12P_T1_MRCC_14	W20	PA5/FIFOADR1
VCCO_14	IO_L12N_T1_MRCC_14	Y18	24MHz FPGA
VCCO_14	IO_L13P_T2_MRCC_14	Y19	V3 IO_09
VCCO_14	IO_L13N_T2_MRCC_14	V18	PA0/INT0
VCCO_14	IO_L14P_T2_SRCC_14	V19	
VCCO_14	IO_L14N_T2_SRCC_14	AA19	V3 IO_04
IO_0_14	IO_L15P_T2_DQS_RDWR_B_14	AB20	V3 IO_03
IO_25_14	IO_L15N_T2_DQS_DOUT_CS0_B_14	V17	CTL0/FLAGA
IO_L1P_T0_D00_MOSI_14	IO_L16P_T2_CSI_B_14	W17	PA6/PKTEND
IO_L1N_T0_D01_DIN_14	IO_L16N_T2_A15_D31_14	AA18	V3 IO_10
IO_L2P_T0_D02_14	IO_L17P_T2_A14_D30_14	AB18	V3 IO_05
IO_L2N_T0_D03_14	IO_L17N_T2_A13_D29_14	U17	CTL1/FLAGB
IO_L3P_T0_DQS_PUDC_B_14	IO_L18P_T2_A12_D28_14	U18	CTL2/FLAGC
IO_L3N_T0_DQS_EMCCLK_14	IO_L18N_T2_A11_D27_14	P14	V3 IO_15
IO_L4P_T0_D04_14	IO_L19P_T3_A10_D26_14	R14	
IO_L4N_T0_D05_14	IO_L19N_T3_A09_D25_VREF_14	R18	FD4
IO_L5P_T0_D06_14	IO_L20P_T3_A08_D24_14	T18	FD1
IO_L5N_T0_D07_14	IO_L20N_T3_A07_D23_14	N17	SCL_F
IO_L6P_T0_FCS_B_14	IO_L21P_T3_DQS_14	P17	SDA_F
IO_L6N_T0_D08_VREF_14	IO_L21N_T3_DQS_A06_D22_14	P15	V3 IO_25
IO_L7P_T1_D09_14	IO_L22P_T3_A05_D21_14	R16	V3 IO_22
IO_L7N_T1_D10_14	IO_L22N_T3_A04_D20_14	N13	V3 IO_14
IO_L8P_T1_D11_14	IO_L23P_T3_A03_D19_14	N14	V3 IO_21
IO_L8N_T1_D12_14	IO_L23N_T3_A02_D18_14	P16	U_LED2
IO_L9P_T1_DQS_14	IO_L24P_T3_A01_D17_14	R17	FD0
IO_L9N_T1_DQS_D13_14	IO_L24N_T3_A00_D16_14		

XC7A200T-2FBG484I



U1A

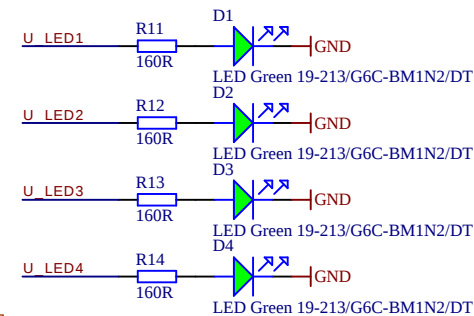
BANK 13

VCCO_13	IO_L7P_T1_13	AB11	
VCCO_13	IO_L7N_T1_13	AB12	
VCCO_13	IO_L8P_T1_13	AA9	
VCCO_13	IO_L8N_T1_13	AB10	
VCCO_13	IO_L9P_T1_DQS_13	AA10	
VCCO_13	IO_L9N_T1_DQS_13	AA11	
IO_0_13	IO_L10P_T1_13	V10	U_LED3
	IO_L10N_T1_13	W10	U_LED4
IO_L1P_T0_13	IO_L11P_T1_SRCC_13	Y11	
IO_L1N_T0_13	IO_L11N_T1_SRCC_13	Y12	
IO_L2P_T0_13	IO_L12P_T1_MRCC_13	W11	
IO_L2N_T0_13	IO_L12N_T1_MRCC_13	W12	V3 IO_27
IO_L3P_T0_DQS_13	IO_L13P_T2_MRCC_13	V13	V3 IO_26
IO_L3N_T0_DQS_13	IO_L13N_T2_MRCC_13	V14	V3 IO_20
IO_L4P_T0_13	IO_L14P_T2_SRCC_13	U15	V3 IO_13
IO_L4N_T0_13	IO_L14N_T2_SRCC_13	V15	V3 IO_19
IO_L5P_T0_13	IO_L15P_T2_DQS_13	T14	
IO_L5N_T0_13	IO_L15N_T2_DQS_13	T15	V3 IO_23
IO_L6P_T0_13	IO_L16P_T2_13	W15	V3 IO_18
IO_L6N_T0_VREF_13	IO_L16N_T2_13	W16	V3 IO_17
	IO_L17P_T2_13	T16	V3 IO_12
	IO_L17N_T2_13	U16	V3 IO_16

XC7A200T-2FBG484I

B13_B14

IFCLK	PA0/INT0	V3 IO_01
24MHz FPGA	PA1/INT1	V3 IO_02
RDY0/SLRD	PA2/SLOE	V3 IO_03
RDY1/SLWR	PA3/WU	V3 IO_04
U_LED1	PA4/FIFOADR0	V3 IO_05
U_LED2	PA5/FIFOADR1	V3 IO_06
U_LED3	PA6/PKTEND	V3 IO_07
U_LED4	SCL_F	V3 IO_08
CTL0/FLAGA	SDA_F	V3 IO_09
CTL1/FLAGB	PA7/FLAGD/SLCS	V3 IO_10
CTL2/FLAGC		V3 IO_11
FD0		V3 IO_12
FD1		V3 IO_13
FD2		V3 IO_14
FD3		V3 IO_15
FD4		V3 IO_16
FD5		V3 IO_17
FD6		V3 IO_18
FD7		V3 IO_19
/REPROG		V3 IO_20
		V3 IO_21
		V3 IO_22
		V3 IO_23
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		V3 IO_25
		V3 IO_26
		V3 IO_27



Title:

FPGA_B13_B14

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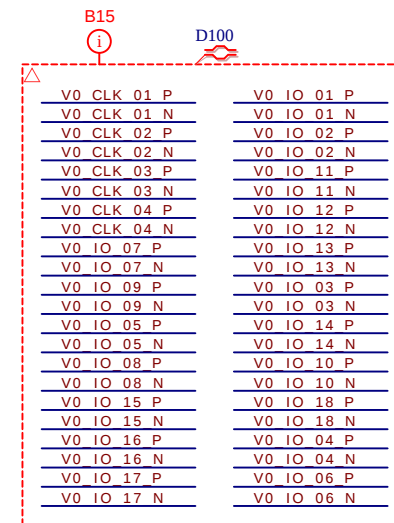
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82I51-ARev.
02

Date: 22.11.2023

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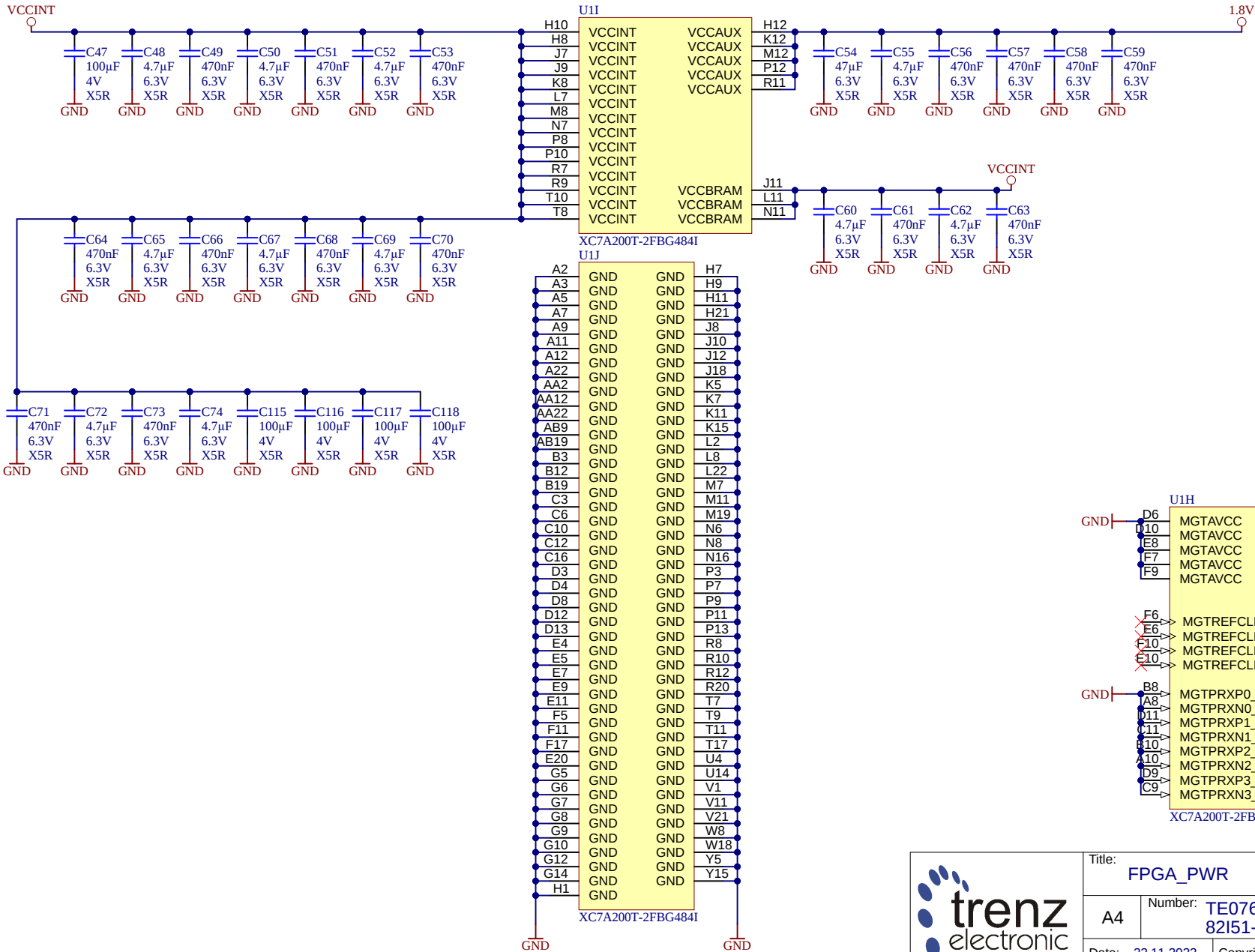
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Filename: FPGA_B13_B14.SchDoc









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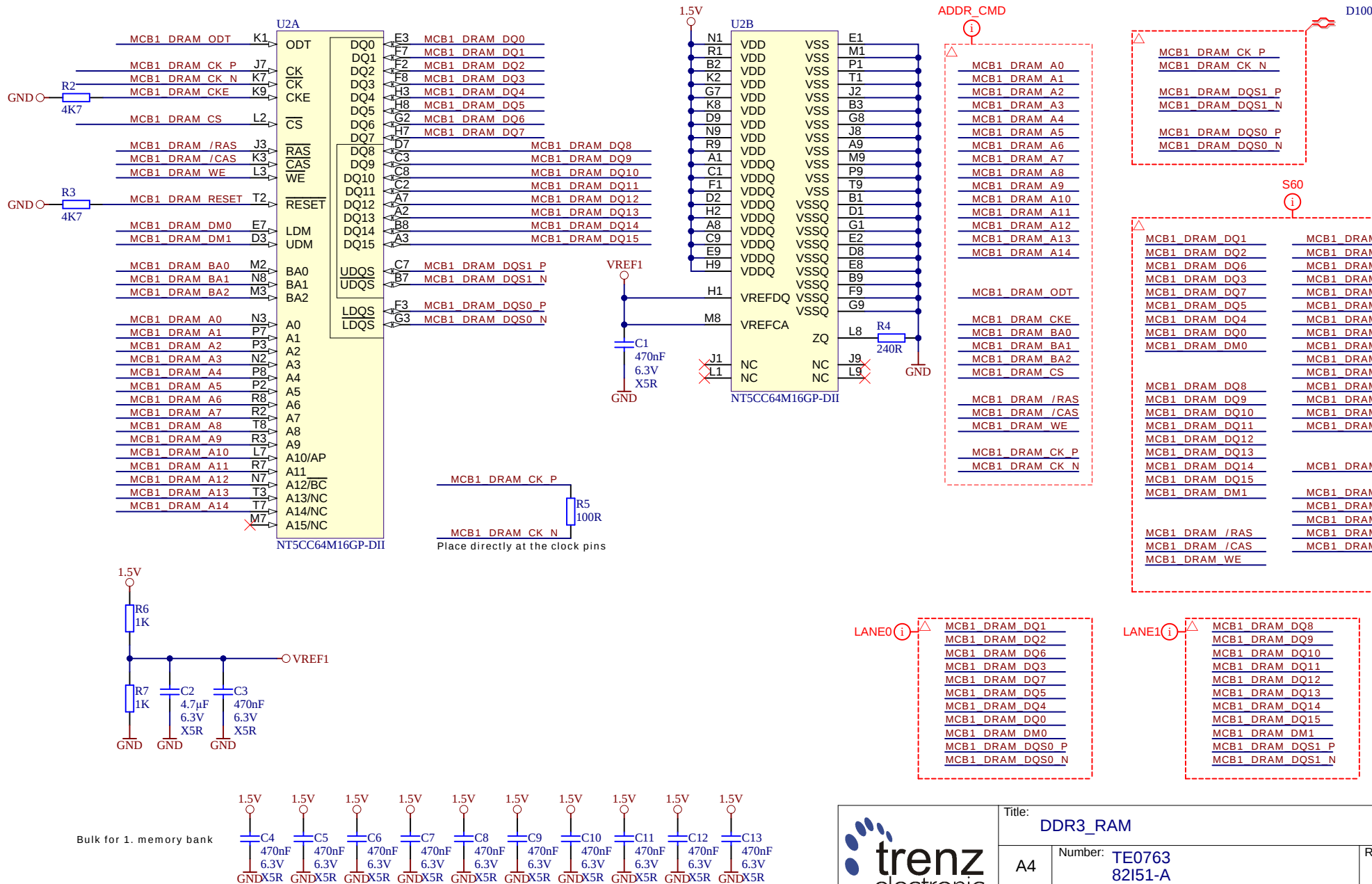
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