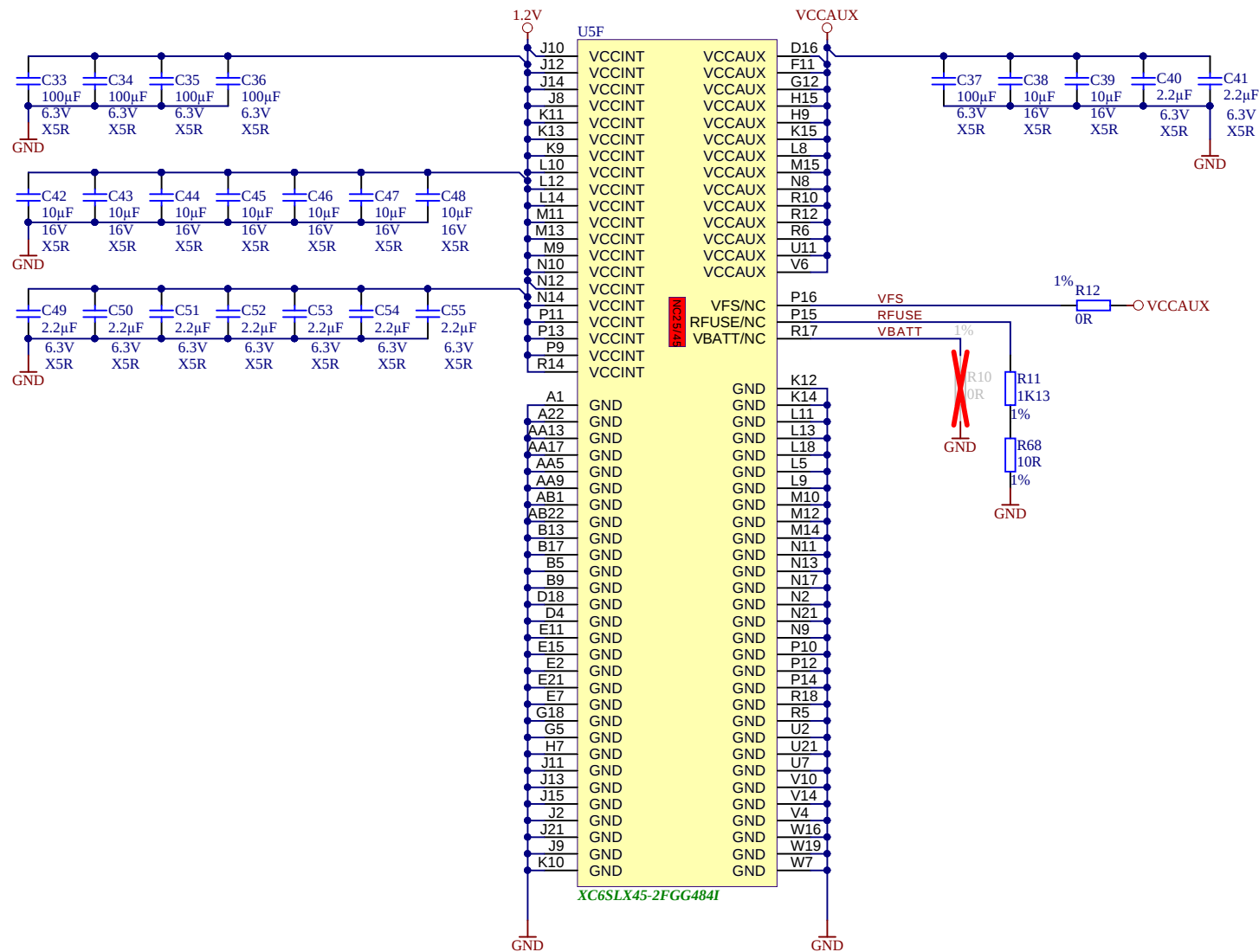


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Title: TE0600 - FPGA_PWR		
A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT	Page2 of 12
Filename: 01.SchDoc		

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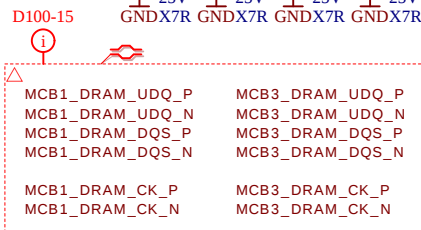
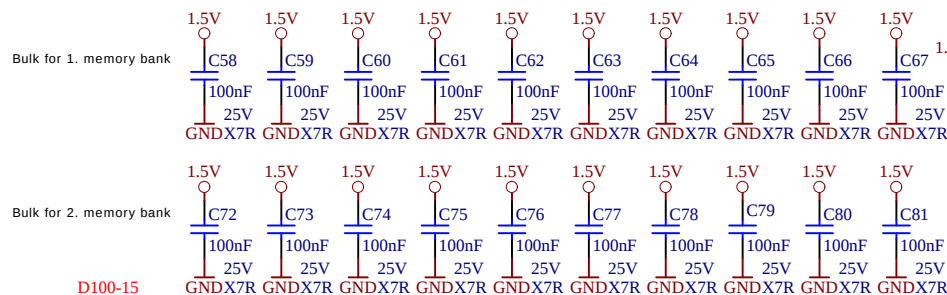
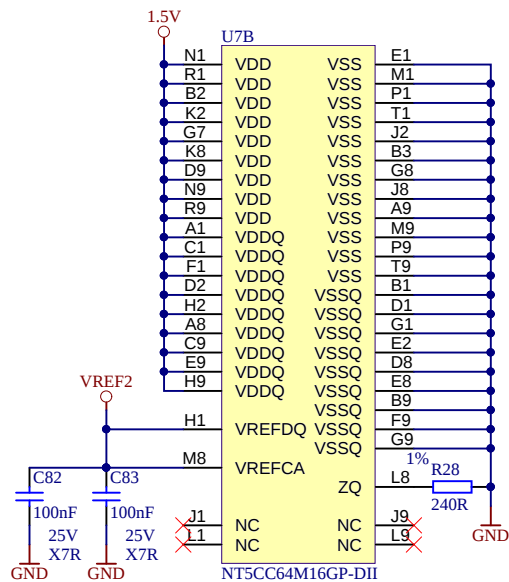
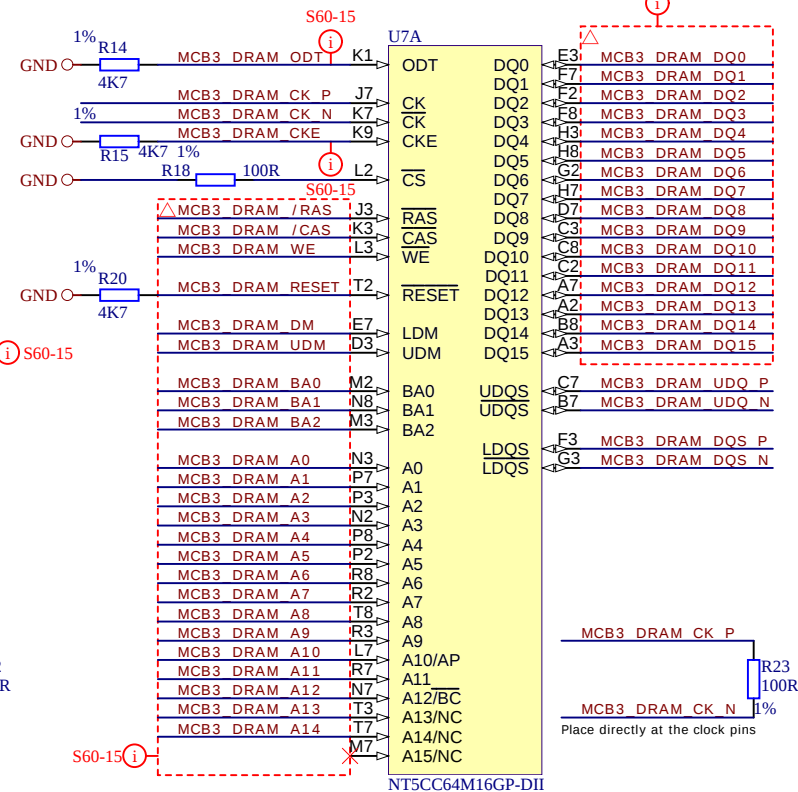
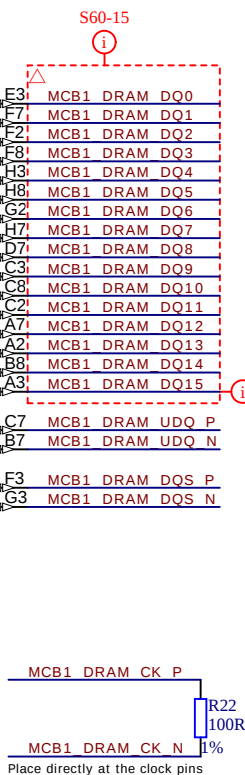
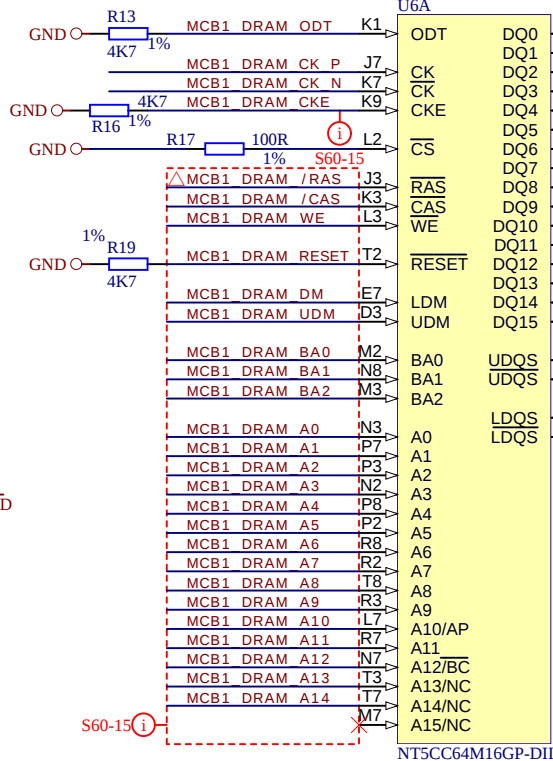
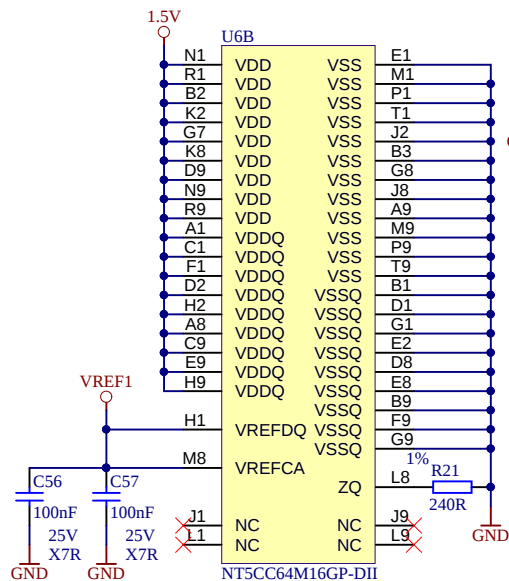
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Title: TE0600 - DDR3_RAM		
A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03
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Trace widths should be 3 to 5 mils.

- Trace spacing should be three times the trace width.
- Signals must not be routed over splits or voids.
- Routing of differential pairs adjacent to noisy signal lines or high-speed switching devices such as clock chips should be avoided.
- The spacing between differential clocks/strobes and other signals on the same PCB layer should be 20 mil. The 20 mil spacing should be maintained when using serpentine routing for length matching.

Differential clocks/strobes are to be routed as 1000 differential signals. The clock pairs must be routed on the same PCB layer with no layer changes or hops after the initial pad to via breakout.

The Data (DQ), Data Mask (DM), and Data Strobe (DQS) signals should receive the highest priority (that is, routed first), because they are the highest speed DDR signals.

- DQ, DM, and DQS signals should be routed in a data group (per byte). Each group should have similar loading and routing to maintain timing and signal integrity.
- The provided spacing should be 20 mil between a data group and any other signals.
- DQS signals should be isolated from other signals by 20 mil to avoid crosstalk.
- There should be a maximum of ±25 ps electrical delay (±150 mil) between any DQ/DM and its associated DQS strobe.
- A data group should be referenced to a GROUND plane.
- DQ bit swapping at the memory interface is permitted to facilitate layout.

Swapping should only be done within a data group.

- DQS to DQS_N trace lengths should be matched (±10 mil).
- Memory terminations (if external terminations are used) should be placed after the associated memory component in a fly-by fashion.
- For 16-bit DDR devices, the LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±25 ps of the electrical delay (±150 mil).

When the data groups have been routed, the next highest priority is the differential clock (CK / CK_N). The clock should be routed first because all address and control trace length matching must be referenced to the differential clock PCB trace length, which might need to be adjusted as the layout task proceeds.

- CK to CK_N trace lengths must be matched (±10 mil).
- CK and DQS trace lengths must be matched (±250 mil) to maximize setup and hold margins.
- There must be a maximum ±50 ps electrical delay (±300 mil) between any address/control signals and the associated CK and CK_N differential clock FPGA output.
- Address and control signals can be referenced to a POWER plane if a GROUND plane is not next to this group of signals in the PCB stack-up.

To avoid crosstalk, address and command signals should be kept on a different routing layer from DQ, DQS, and DM.

- Differential clock terminations (if external terminations are used) must be located as close as possible to the load, after the clock pads of the PCB. PCB trace lengths used in trace length matching must exclude the CLINE length of the PCB trace from memory ball to terminating resistor.

Classnames:
S60-15 uses 1.5V or GND plane as reference
D100-15 uses 1.5V or GND plane as reference

S60-25 uses 2.5V or GND plane as reference
D100-25 uses 2.5V or GND plane as reference

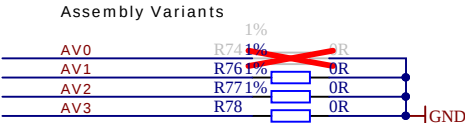
S60-I0 uses VCCI00 or GND plane as reference
D100-I0 uses VCCI00 or GND plane as reference

S60-33 uses 3.3V or GND plane as reference
D100-33 uses 3.3V or GND plane as reference

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AV0 = 0 -> commercial AV0 = 1 -> Industrial
AV1 = 0 -> speedgrade 2 AV1 = 1 -> speedgrade 3
AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte
AV3 = Open -> Customized variants

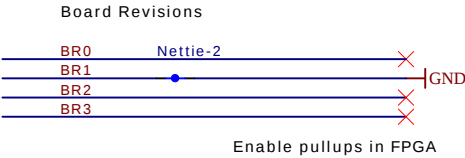


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BR3 BR2 BR1 BR0

1 1 1 1 | -01 Initial revision
1 1 1 0 | -02
1 1 0 1 | -03

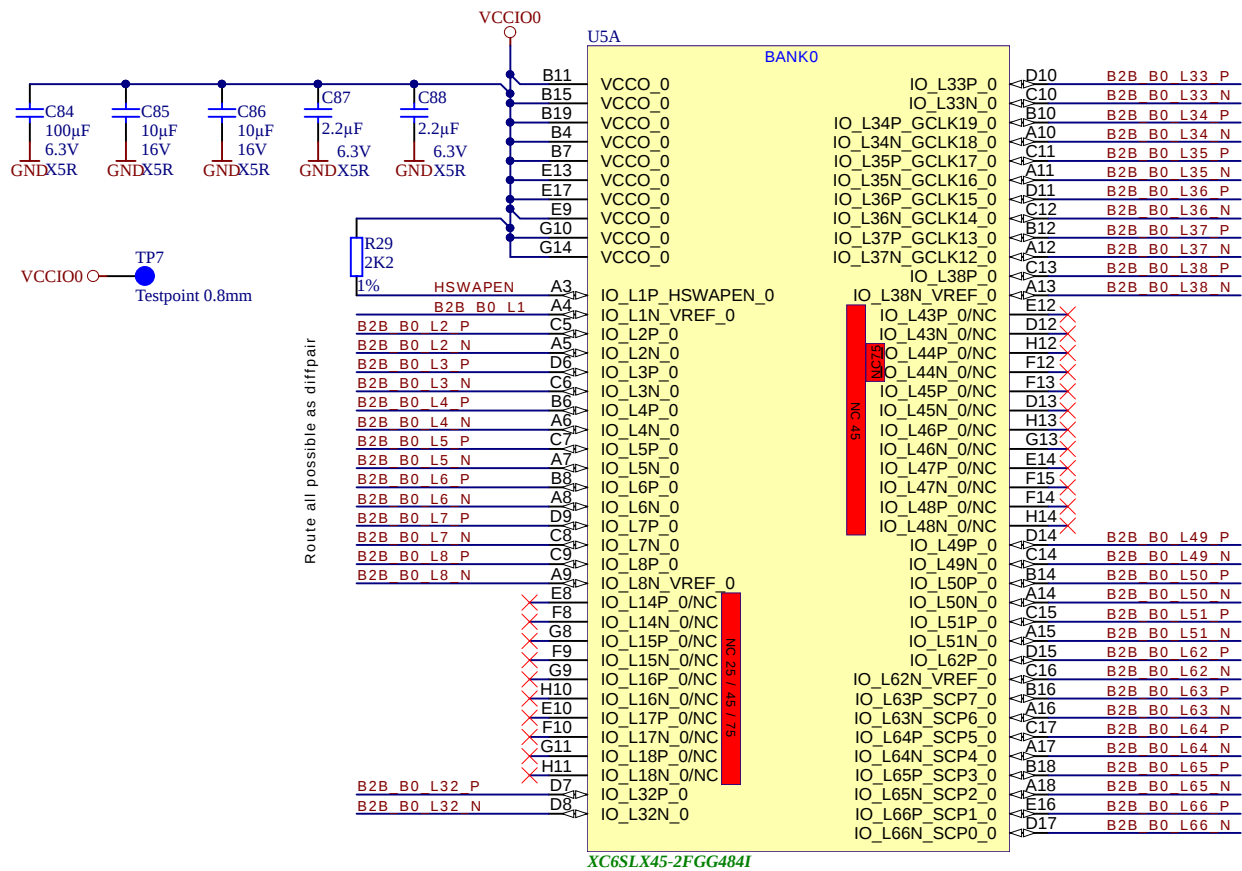


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D

	Title: TE0600 - Configuration		
	A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03
	Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT	Page4 of 12
	Filename: 03.SchDoc		

D

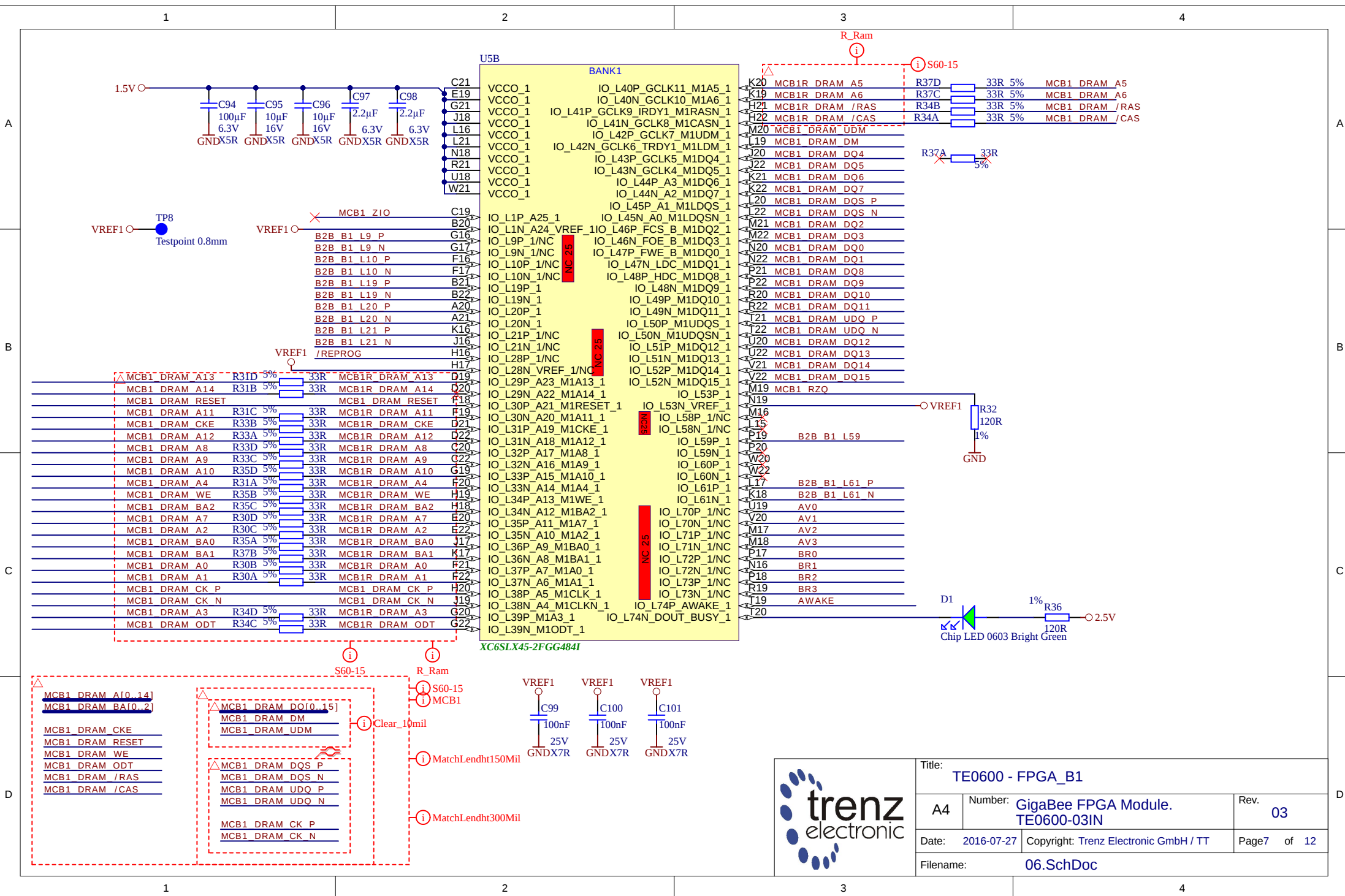


XC6SLX45-2FGG484I

wich are marked NC100



Title: TE0600 - FPGA_B2		
A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03
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Filename: 05.SchDoc		

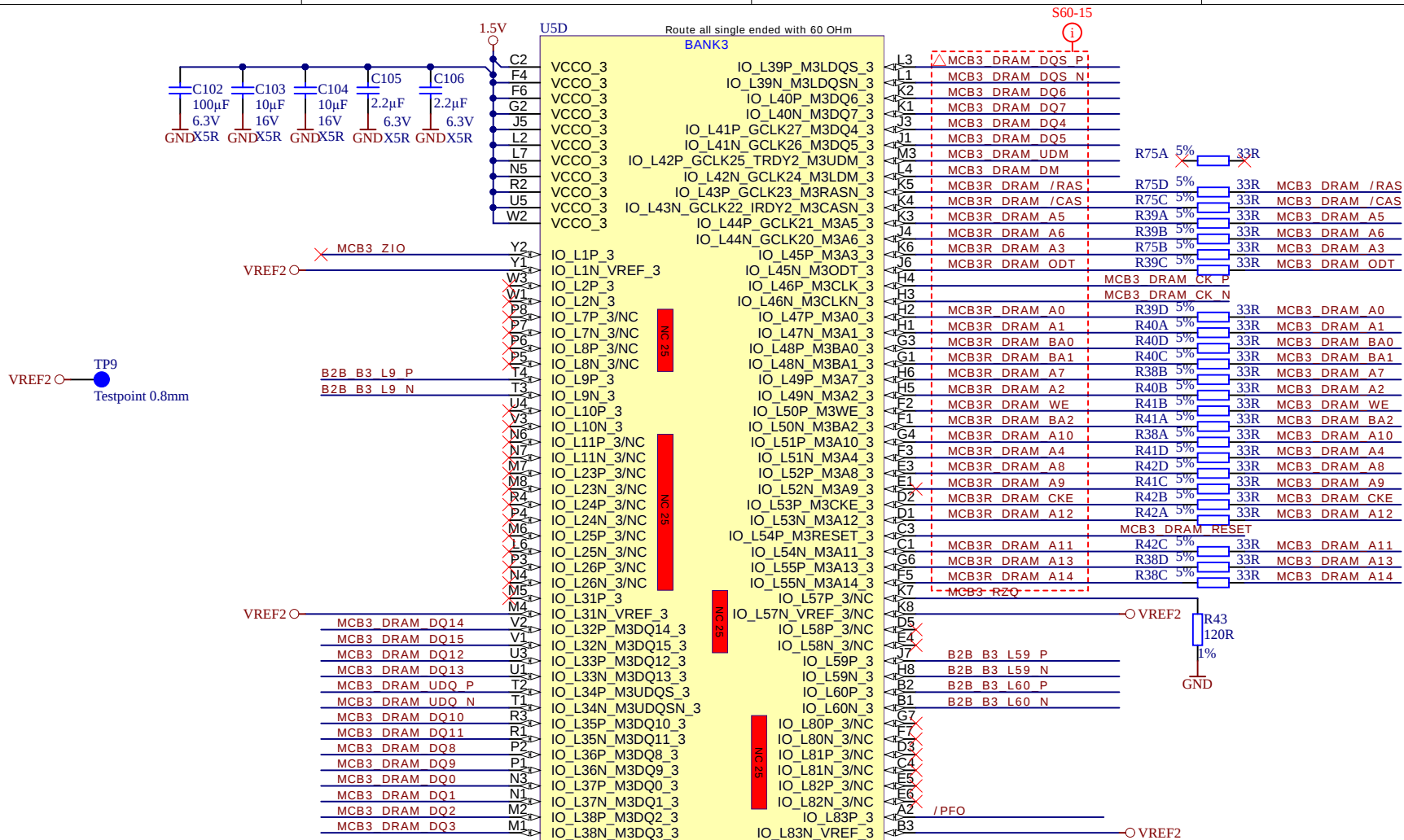


1

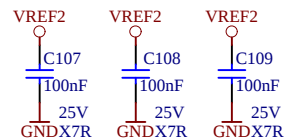
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XC6SLX45-2FGG484I



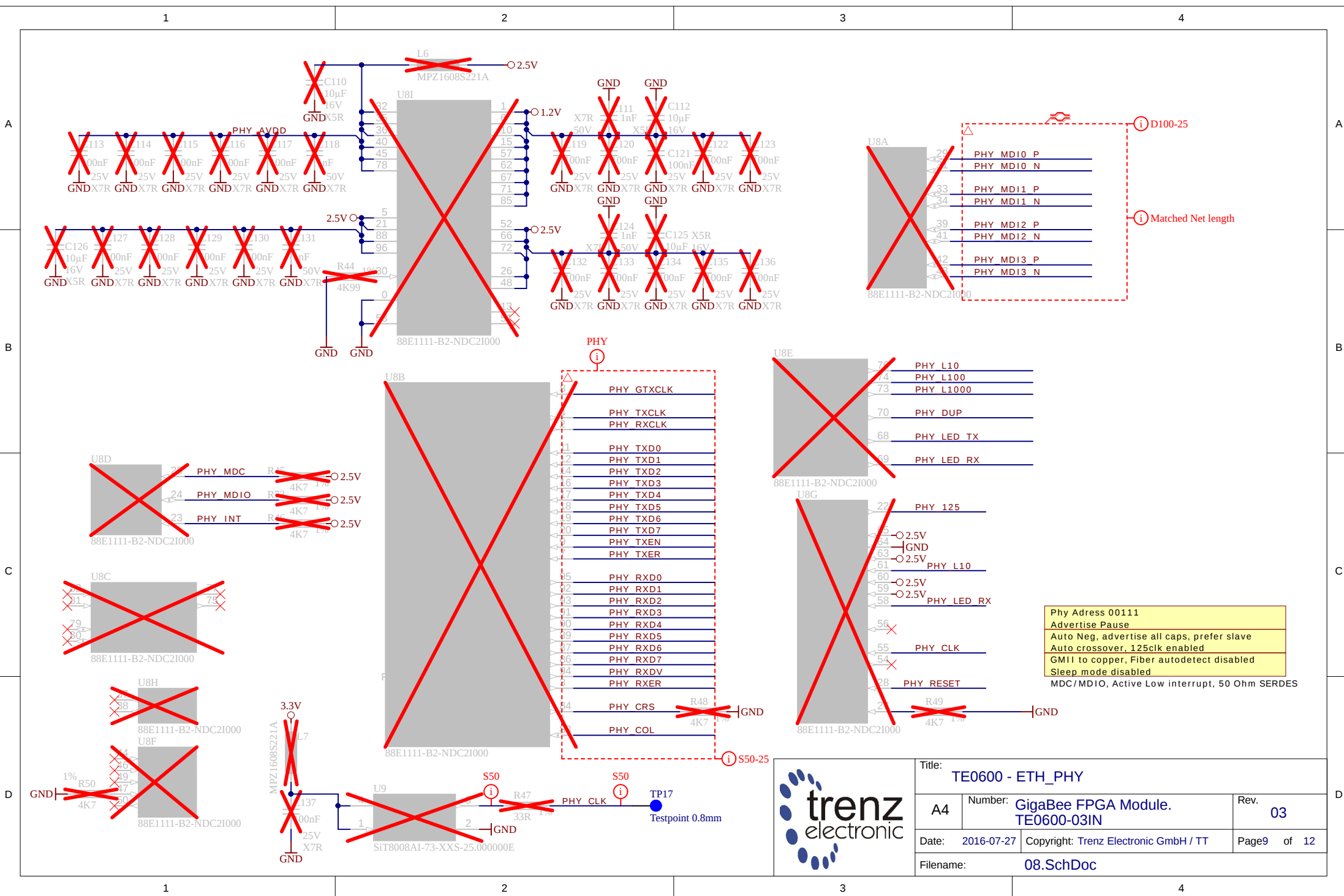
Title: TE0600 - FPGA_B3		
A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03
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Filename: 07.SchDoc		

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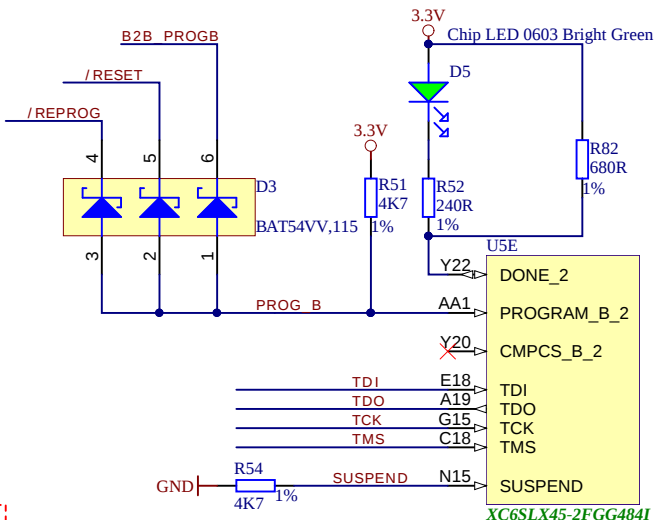


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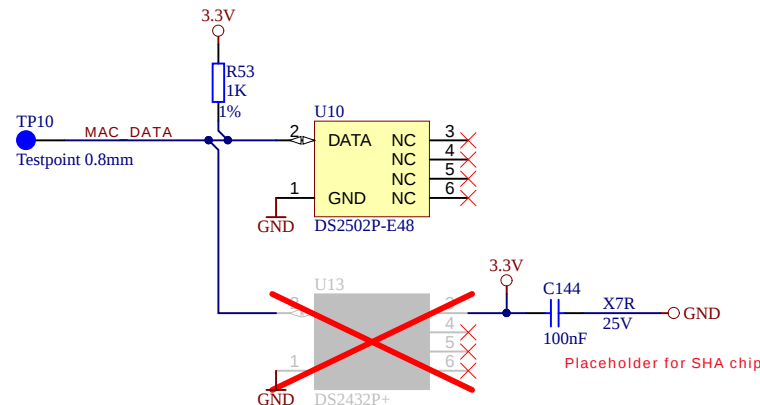
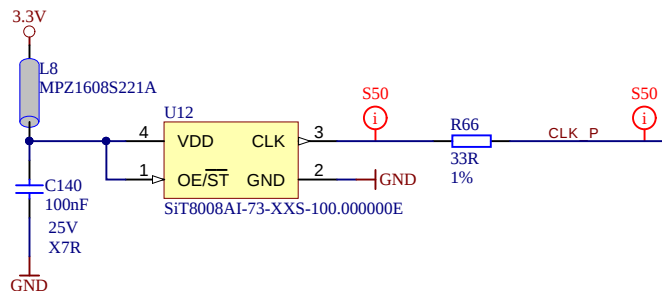
2

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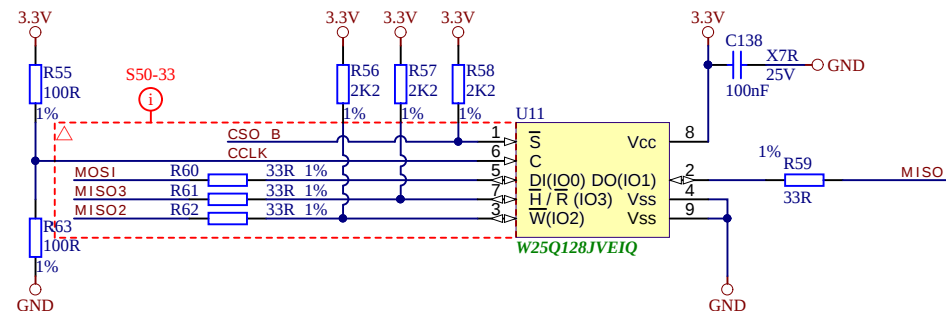
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S50-33



Placeholder for SHA chip



Put clk termination close to the input pin

Testpoint 0.8mm TP16 CLK P

Testpoint 0.8mm TP22 PROG B



Title: TE0600 - FPGA_CFG

A4 Nummer: GigaBee FPGA Module.
TE0600-03IN

Rev. 03

Datum: 2016-07-27 Zeichner: Trenz Electronic GmbH / TT

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Filename: 09.SchDoc

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- 1) added NetTie (board revision 03)
- 2) optimized placement and routing pwr DCDC
- 3) added tsports
- 4) changed OSC U9 (AN25008, SiT8008A1-73-XXS-25.000000E)
- 5) update Razorbeam Connectors, full update lib
- 6) added serial number (traceability pad)
- 7) added thermal vias to mounting holes
- 8) changed SPI flash (AN26012, W25Q128FVEIG 3V 128MBit Serial Flash)
- 9) changed DDR3 (AN27202, AN27039)
- 10) U13 (DS2432P+) is not populated

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Title: TE0600 - Changes list			
A4	Number: GigaBee FPGA Module. TE0600-03IN	Rev. 03	
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