
# TRM TE0715-03

**Authors:** Philipp Bernhardt, Antti Lukats, Thorsten Trenz, Emmanuel Vassilakis
**Revision:** V33
**Date:** 09-May-2016 08:06

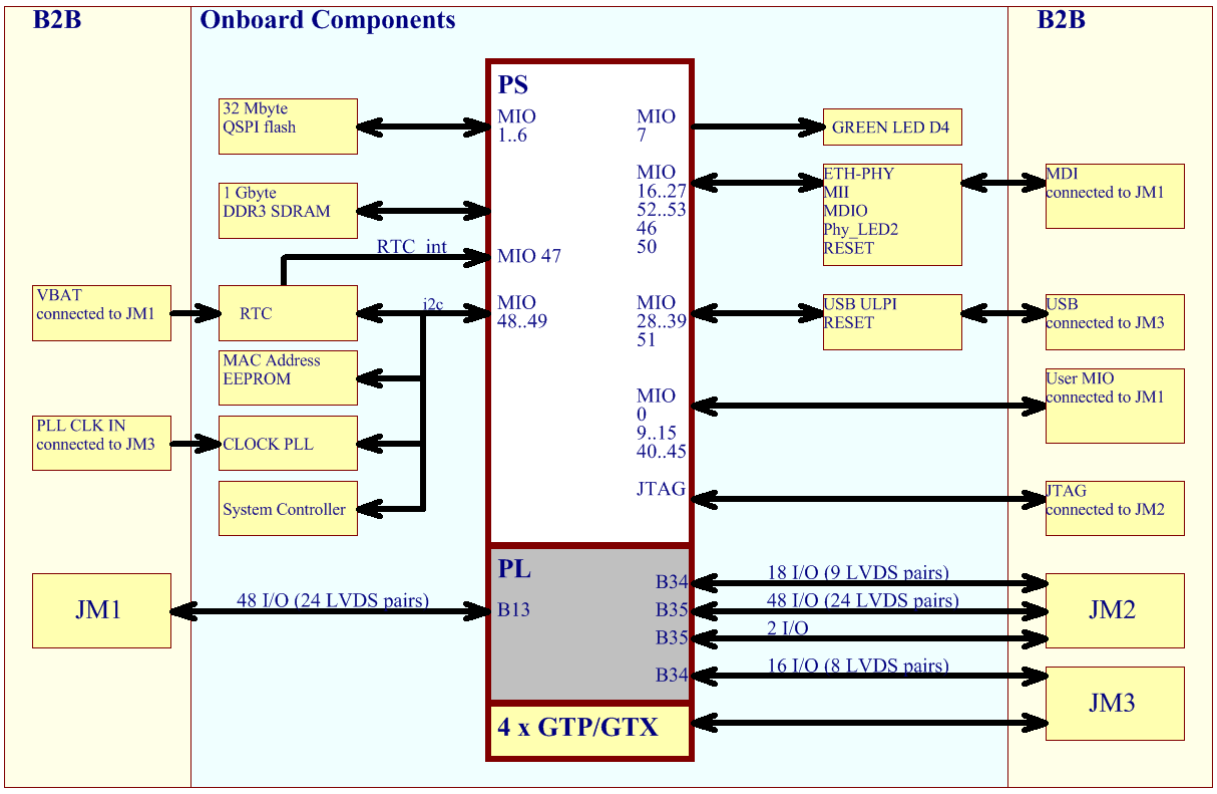
# Table of Contents

# Overview

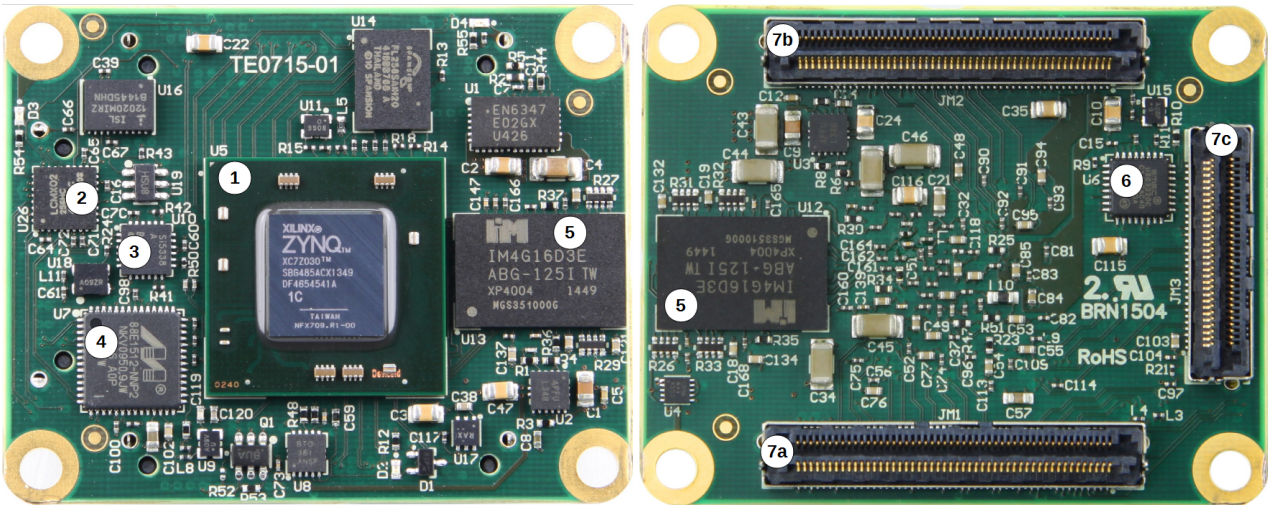
The online version of this manual and other documents can be found here: https://wiki.trenz-electronic.de/display/PD/TE0715

The Trenz Electronic TE0715 is an industrial-grade SoM (System on Module) based on Xilinx Zynq-7000 SoC (7015 or 7030), with a gigabit Ethernet PHY transceiver, 1 gigabyte DDR3 SDRAM, 32 megabyte Flash memory, a USB PHY transceiver and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips. All modules in 4 x 5 cm form factor are mechanically compatible.

## Block diagram



## Board Components




**Main Components:**

1. Zynq-7000 All Programmable SoC
2. System Controller CPLD
3. Programmable clock generator
4. 10/100/1000 Mbps Ethernet PHY
5. DDR3-SDRAM
6. Hi-Speed USB 2.0 ULPI Transceiver
7. B2B-Connector
    a. JM1
    b. JM2
    c. JM3

## Key Features

- Industrial-grade Xilinx Zynq-7000 (Z-7015, Z-7030) SoM
- Rugged for shock and high vibration
- 2 × ARM Cortex-A9
- 10/100/1000 tri-speed gigabit Ethernet transceiver PHY
- MAC Address EEPROM
- 32-Bit wide 1 GByte DDR3 SDRAM
- 32 MByte QSPI Flash memory
- Programmable Clock Generator
    - Transceiver Clock (default 125 MHz)
- Plug-on module with 2 × 100-pin and 1 × 60-pin high-speed hermaphroditic strips
- 132 FPGA I/Os (65 LVDS pairs possible) and 14 PS MIO available on board-to-board connectors
- 4 GTP/GTX (high-performance transceiver) lanes
    - GTP/GTX (high-performance transceiver) clock input
- USB 2.0 high-speed ULPI transceiver

- On-board high-efficiency DC-DC converters
  - 4.0 A x 1.0 V power rail
  - 1.5 A x 1.5 V power rail
  - 1.5 A x 1.8 V power rail
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Temperature compensated RTC (real-time clock)
- User LED
- Evenly-spread supply pins for good signal integrity

Assembly options for cost or performance optimization available upon request.

# Signals, Interfaces and Pins

## System Controller I/O Pins

Special purpose pins used by TE0720 are also available on TE0715 they are connected to smaller System Controller CPLD and have different or no function in default configuration.

| Name | Note |
|---|---|
| EN1 | No hard wired function on PCB, when forced low pulls POR_B low to emulate power on reset |
| PGOOD | Driven low by System Controller if power supply power fail detected |
| NOSEQ | No function |
| RESIN | Active low reset, gated to POR_B |
| JTAGEN | Low for normal operation |

## Boot Modes

By default the TE-0715 supports QSPI and SD boot modes.

Two boot modes are controlled by the MODE signal on the board to board (B2B) connector:

| MODE signal | Boot Mode |
|---|---|
| high or open | SD Card |
| low or ground | QSPI |

## JTAG

JTAG access to the Xilinx Zynq-7000 device is provided through connector JM2.

| Signal | B2B Pin |
|---|---|
| TCK | JM2: 99 |
| TDI | JM2: 95 |
| TDO | JM2: 97 |
| TMS | JM2: 93 |

JTAGEN pin in JM1 should be kept low or grounded for normal operation.

# Clocking

| Clock | Frequency | IC | FPGA | Notes |
|---|---|---|---|---|
| PS CLK | 33.3333 Mhz | U11 | PS_CLK | PS Subsystem main clock |
| ETH PHY reference | 25 MHz | U9 | - | |
| USB PHY reference | 52 MHz | U15 | - | |
| PLL reference | 25 MHz | U18 | - | |
| GT REFCLK0 | - | B2B | U9/V9 | Externally supplied from base |
| GT REFCLK1 | 125 Mhz | U10 Si5338 | U5/V5 | Default clock is 125 MHz |

# Processing System (PS) Peripherals

| | IC | Designator | PS7 | MIO | Notes |
|---|---|---|---|---|---|
| SPI Flash | S25FL256SAGBHI20 | U14 | QSPI0 | MIO1..MIO6 | |
| EEPROM I2C | 24AA025E48 | U19 | I2C1 | MIO48, MIO49 | EEPROM for MAC Address |
| RTC | ISL2020 | U16 | I2C1 | MIO48, MIO49 | Temperature compensated real time clock |
| RTC Interrupt | ISL2020 | U16 | GPIO | MIO47 | Real Time Clock Interrupt |
| Clock PLL | Si5338 | U10 | I2C1 | MIO48, MIO49 | Low jitter phase locked loop |
| LED | | D4 | GPIO | MIO7 | |
| USB | USB3320 | U6 | USB0 | MIO28..MIO39 | |
| USB Reset | | | GPIO | MIO51 | |
| Ethernet | 88E1512 | U7 | ETH0 | MIO16..MIO27 | |
| Ethernet Reset | | | GPIO | MIO50 | |

# Default MIO mapping:

| MIO | Configured as | B2B | Notes |
|---|---|---|---|
| 0 | GPIO | JM1-87 | B2B |
| 1 | QSPI0 | - | SPI Flash-CS |
| 2 | QSPI0 | - | SPI Flash-DQ0 |
| 3 | QSPI0 | - | SPI Flash-DQ1 |
| 4 | QSPI0 | - | SPI Flash-DQ2 |
| 5 | QSPI0 | - | SPI Flash-DQ3 |
| 6 | QSPI0 | - | SPI Flash-SCK |
| 7 | GPIO | - | Green LED D4 |
| 8 | QSPI0 | - | SPI Flash-SCKFB |
| 9 | | JM1-91 | B2B |
| 10 | | JM1-95 | B2B |
| 11 | | JM1-93 | B2B |
| 12 | | JM1-99 | B2B |
| 13 | | JM1-97 | B2B |
| 14 | UART0 | JM1-92 | B2B |
| 15 | UART0 | JM1-85 | B2B |
| 16..27 | ETH0 | | RGMII |
| 28..39 | USB0 | | ULPI |
| 40 | SDIO0 | JM1-27 | B2B |
| 41 | SDIO0 | JM1-25 | B2B |
| 42 | SDIO0 | JM1-23 | B2B |
| 43 | SDIO0 | JM1-21 | B2B |
| 44 | SDIO0 | JM1-19 | B2B |
| 45 | SDIO0 | JM1-17 | B2B |
| 46 | GPIO | - | Ethernet PHY LED2/INTn Signal |
| 47 | GPIO | - | RTC Interrupt |
| 48 | I2C1 | - | SCL on-board I2C |
| 49 | I2C1 | - | SDA on-board I2C |
| 50 | GPIO | - | ETH0 Reset |
| 51 | GPIO | - | USB Reset |

| MIO | Configured as | B2B | Notes |
|---|---|---|---|
| 52 | ETH0 | - | MDC |
| 53 | ETH0 | - | MDIO |

# I2C Interface

The on-board I2C components are connected to MIO48 and MIO49 and configured as I2C1 by default.

**I2C addresses for on-board components:**

| Device | I2C-Address | Notes |
|---|---|---|
| EEPROM | 0x50 | |
| RTC | 0x6F | |
| Battery backed RAM | 0x57 | integrated in RTC |
| PLL | 0x70 | |

# B2B I/O

**Number of I/O's connected to the SoC's I/O bank and B2B connector:**

| Bank | Type | JMx | IO Count | IO Voltage | Notes |
|---|---|---|---|---|---|
| 13 | HR | 1 | 48 | User | |
| 34 | HR/HP | 2 | 18 | User | **1.8V max with Z7030** |
| 35 | HR/HP | 2 | 50 | User | **1.8V max with Z7030** |
| 34 | HR/HP | 3 | 16 | User | **1.8V max with Z7030** |
| 500 | MIO | 1 | 8 | 3.3V | |
| 501 | MIO | 1 | 6 | 1.8V | |
| 112 | GT | 3 | 4 Lanes | n/a | |
| 112 | GT CLK | 3 | one differential input | n/a | AC coupling capacitors on base required |

For detailed information about the pin out, please refer to the Master Pinout Table.

# Peripherals

## LED's

There are 3 LED's on TE0715:

| LED | Color | Connected to | Notes |
|---|---|---|---|
| D2 | green | DONE | Inverted DONE, ON when FPGA not configured |
| D3 | red | SC | Global status LED |
| D4 | green | MIO7 | OFF when PS7 not booted and not controlling MIO7 by software, else user controlled |

LED D2 is connected to the FPGA Done pin and will go off as soon as PL is configured.

This LED will not operate if the SC can not power on the 3.3V output rail that also powers the 3.3V circuitry on the module.

## Ethernet

The TE0715 is populated with a Marvell Alaska 88E1512 Gigabit Ethernet PHY. The Ethernet PHY RGMII Interface is connected to the Zynq Ethernet0 PS GEM0. The I/O Voltage is fixed at 1.8V for HSTL signaling.

SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3.

The reference clock input of the PHY is supplied from an on board 25MHz oscillator (U9), the 125MHz output clock is connected to IN5 of the PLL chip (U10).

**PHY connection:**

| PHY PIN | ZYNQ PS | ZYNQ PL | Notes |
|---|---|---|---|
| MDC/MDIO | MIO52, MIO53 | - | - |
| LED0 | - | J3 | can be routed via PL to any free PL I/O pin in B2B connector |
| LED1 | - | K8 | can be routed via PL to any free PL I/O pin in B2B connector |
| LED2/Interrupt | MIO46 | - | - |
| CONFIG | - | - | By default the PHY Address is strapped to 0x00 alternate configuration is possible |
| RESETn | MIO50 | - | - |
| RGMII | MIO16..MIO27 | - | - |
| SGMII | - | - | on B2B |
| MDI | - | - | on B2B |

Note: LED1 is connected to PL via level-shifter implemented in system controller CPLD.

## USB

The USB PHY USB3320 from Microchip is used on the TE0715. The ULPI interface is connected to the Zynq PS USB0. The I/O Voltage is fixed at 1.8V.

The reference clock input of the PHY is supplied from an on board 52MHz oscillator (U15).

**PHY connection:**

| PHY Pin | Zynq Pin | B2B Name | Notes |
|---|---|---|---|
| ULPI | MIO28..39 | - | Zynq USB0 MIO pins are connected to the PHY |
| REFCLK | - | - | 52MHz from on board oscillator (U15) |
| REFSEL[0..2] | - | - | 000 GND, select 52MHz reference Clock |
| RESETB | MIO51 | - | Active low reset |
| CLKOUT | MIO36 | - | Connected to 1.8V selects reference clock operation mode |
| DP,DM | - | OTG_D_P, OTG_D_N | USB Data lines |
| CPEN | - | VBUS_V_EN | External USB power switch active high enable signal |
| VBUS | - | USB_VBUS | Connect to USB VBUS via a series resistor. Check reference schematic |
| ID | - | OTG_ID | For an A-Device connect to ground, for a B-Device left floating |

The schematic for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for Host or Device modes. A Mini USB connector can be used for USB Device mode. A USB Micro connector can be used for Device mode, OTG Mode or Host Mode.

## RTC

An Intersil temperature compensated real time clock IC ISL12020M is used for timekeeping (U16). Battery voltage must be supplied to the module from the main board.

Battery backed registers are accessed at I2C slave address 0x6F.

General purpose RAM is accessed at I2C slave address 0x57.

This RTC IC is supported in Linux so it can be used as hwclock device.

## PLL

A Silicon Labs I2C-programmable clock generator Si5338A (U10) is populated on the module. The Si5338 can be programmed using the I2C-bus, to change the frequency on its outputs. It is accessible on the I2C slave address 0x70.

**PLL connection:**

| Input/Output | Default Frequency | Notes |
|---|---|---|
| IN1/IN2 | Externally supplied | need decoupling on base board |
| IN3 | 25MHz | Fixed input clock |
| IN4 | - | not available and not used |
| IN5/IN6 | 125MHz | Ethernet PHY output clock |
| CLK0 | - | not used, disabled |
| CLK1 | - | not used, disabled |
| CLK2 A/B | 125MHz | MGT reference clock 1 |
| CLK3A | 125MHz | Bank 34 clock input |
| CLK3B | - | not used, disabled |

## MAC-Address EEPROM

A Microchip 24AA025E48 EEPROM (U19) is used on the TE0715. It contains a globally unique 48-bit node address, that is compatible with EUI-48(TM) and EUI-64(TM). The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible through the I2C slave address 0x50.

# Power

TE0715-xx-30 has several HP banks on B2B Connectors, those banks have maximal Voltage tolerance of 1.8V please check special instructions for the Baseboard use with TE0715-xx-30

For startup, a power supply with minimum current capability of 3A is recommended.

VIN and 3.3VIN can be connected to the same source (3.3 V).

## Power Supplies

| | | |
|---|---|---|
| Vin | 3.3 V to 5.5 V | Typical 200 mA, depending on customer design and connections |
| Vin 3.3V | 3.3 V | Typical 50 mA, depending on customer design and connections |

## Bank Voltages

| Bank | Voltage | TE0715-xx-15 | TE0715-xx-30 |
|---|---|---|---|
| 500 MIO0 | 3.3V | | |
| 501 MIO1 | 1.8V | | |
| 502 DDR | 1.5V | | |
| 0 Config | 3.3V | | |
| 13 HR | User | Max 3.3V | Max 3.3V |
| 34 HR/HP | User | Max 3.3V | **Max 1.8V** |
| 35 HR/HP | User | Max 3.3V | **Max 1.8V** |

# Initial Delivery state

| Storage device name | Content | Notes |
|---|---|---|
| 24AA025E48 EEPROM | User content not programmed | Valid MAC Address from manufacturer |
| SPI Flash OTP Area | Empty, not programmed | Except serial number programmed by flash vendor |
| SPI Flash Quad Enable bit | Programmed | |
| SPI Flash main array | demo design | |
| EFUSE USER | Not programmed | |
| EFUSE Security | Not programmed | |

# Hardware Revision History

| Revision | Changes |
|---|---|
| 01 | Current Hardware Revision, no changes |

# Technical Specification

## Absolute Maximum Ratings

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| Vin supply voltage | -0.3 | 6.0 | V | |
| Vin33 supply voltage | -0.4 | 3.6 | V | |
| VBat supply voltage | -1 | 6.0 | V | |
| PL IO Bank supply voltage for HR I/O banks (VCCO) | -0.5 | 3.6 | V | |
| PL IO Bank supply voltage for HP I/O banks (VCCO) | -0.5 | 2.0 | V | TE0715-xx-15 does not have HP banks |
| I/O input voltage for HR I/O banks | -0.4 | VCCO_X+0.55 | V | |
| I/O input voltage for HP I/O banks | -0.55 | VCCO_X+0.55 | V | TE0715-xx-15 does not have HP banks |
| GT Receiver (RXP/RXN) and Transmitter (TXP/TXN) | -0.5 | 1.26 | V | |
| Voltage on Module JTAG pins | -0.4 | VCCO_0+0.55 | V | VCCO_0 is 3.3V nominal |
| Storage Temperature | -40 | +85 | C | |
| Storage Temperature without the ISL12020MIRZ | -55 | +100 | C | |

⚠ Assembly variants for higher storage temperature range on request

⚠ Please check Xilinx Datasheet for complete list of Absolute maximum and recommended operating ratings for the Zynq device (DS181 Artix or DS182 Kintex).

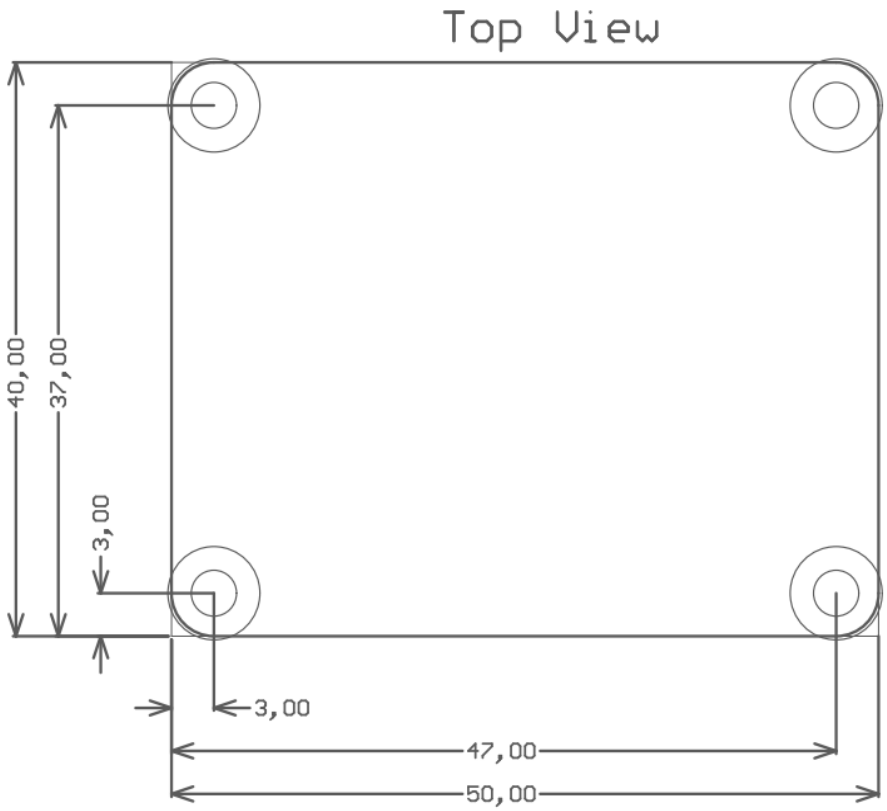
## Recommended Operating Conditions

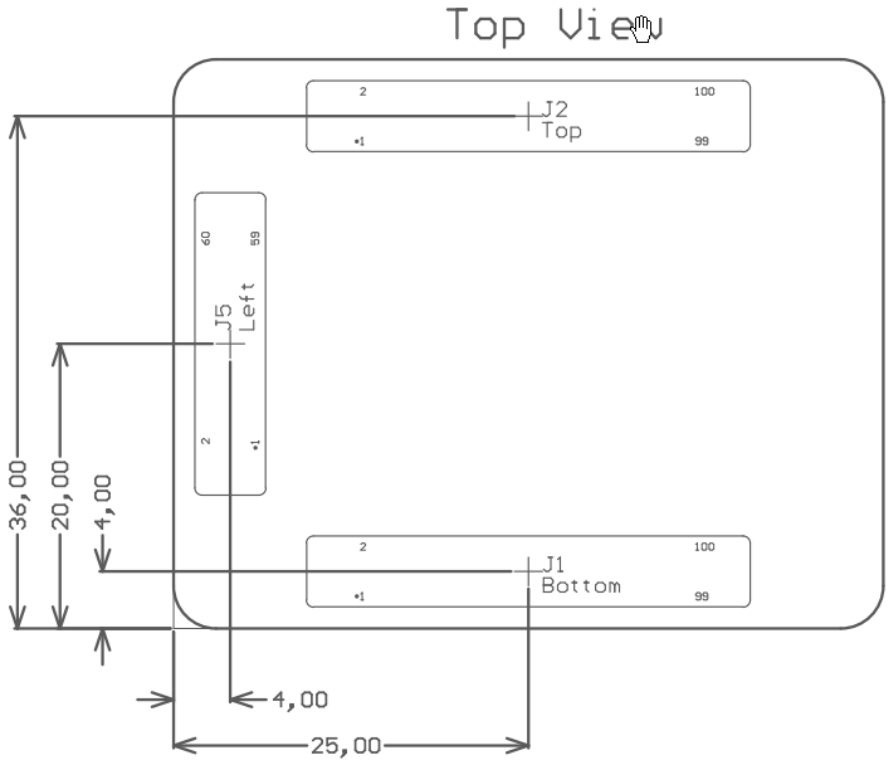
| Parameter | Min | Max | Units | Notes | Reference document |
|---|---|---|---|---|---|
| Vin supply voltage | 2.5 | 5.5 | V | | |
| Vin33 supply voltage | 3.135 | 3.465 | V | | |
| VBat supply voltage | 2.7 | 5.5 | V | | |
| PL IO Bank supply voltage for HR I/O banks (VCCO) | 1.14 | 3.465 | V | | Xilinx document DS191 |
| PL IO Bank supply voltage for HP I/O banks (VCCO) | 1.14 | 1.89 | V | TE0715-xx-15 does not have HP banks. | Xilinx document DS191 |
| I/O input voltage for HR I/O banks | (*) | (*) | V | (*) Check datasheet | Xilinx document DS191 and DS187 |
| I/O input voltage for HP I/O banks | (*) | (*) | V | TE0715-xx-15 does not have HP banks.<br>(*) Check datasheet | Xilinx document DS191 |
| Voltage on Module JTAG pins | 3.135 | 3.465 | V | VCCO_0 is 3.3 V nominal | |

## Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers.

All dimensions are shown in mm.


Top View
40,00
37,00
3,00
3,00
47,00
50,00


Top View
2
100
J2
Top
1
99
60
59
J5
Left
2
1
36,00
20,00
4,00
2
100
J1
Bottom
1
99
4,00
25,00

# Temperature Ranges

**Commercial grade modules**

All parts are at least commercial temperature range of 0°C to +70°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options.

**Industrial grade modules**

All parts are at least industrial temperature range of -40°C to +85°C. The module operating temperature range depends on customer design and cooling solution. Please contact us for options.

# Weight

| | |
|---|---|
| 26 g | Plain module |
| 8.8 g | Set of bolts and nuts |

# Document Change History

| date | revision | authors | description |
|---|---|---|---|
| 2016-04-27 | V33 | Emmanuel Vassilakis | Added the table "Recommended Operating Conditions", Storage Temperature edited |
| 2016-03-31 | v10 | Philipp Bernhardt, Antti Lukats, Thorsten Trenz, Emmanuel Vassilakis | initial version |

# Disclaimer

## Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

## Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

## Copyright Notice



## Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

# Environmental protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet.

According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products.

Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

## RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

## WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment.

Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.