U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B44
FPGA-B44.SchDoc

U_FPGA-B45
FPGA-B45.SchDoc

U_FPGA-B46
FPGA-B46.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_FPGA-B64
FPGA-B64.SchDoc

U_FPGA-B65
FPGA-B65.SchDoc

U_FPGA-B66
FPGA-B66.SchDoc

U_FPGA-B67
FPGA-B67.SchDoc

U_FPGA-B68
FPGA-B68.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_CPLD
CPLD.SchDoc

U_Clock
Clock.SchDoc

U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc

U_POWER_2
POWER_2.SchDoc

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

PM1
FIDU-DOT - mini

PM2
FIDU-DOT - mini

PM3
FIDU-DOT - mini

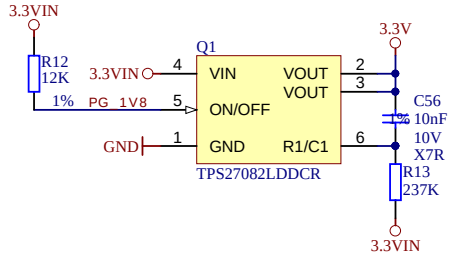
PM4
FIDU-DOT - mini

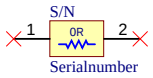
PM5
FIDU-DOT - mini

PM6
FIDU-DOT - mini

FIDU-DOT - mini

FIDU-DOT - mini

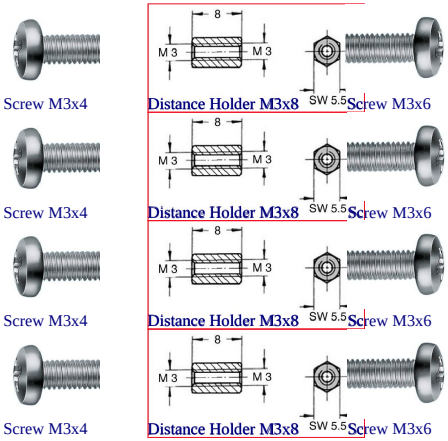




Serialnumber

Serial
Serial
Serialnumber 6,3 x 6.3mm

Top of Board



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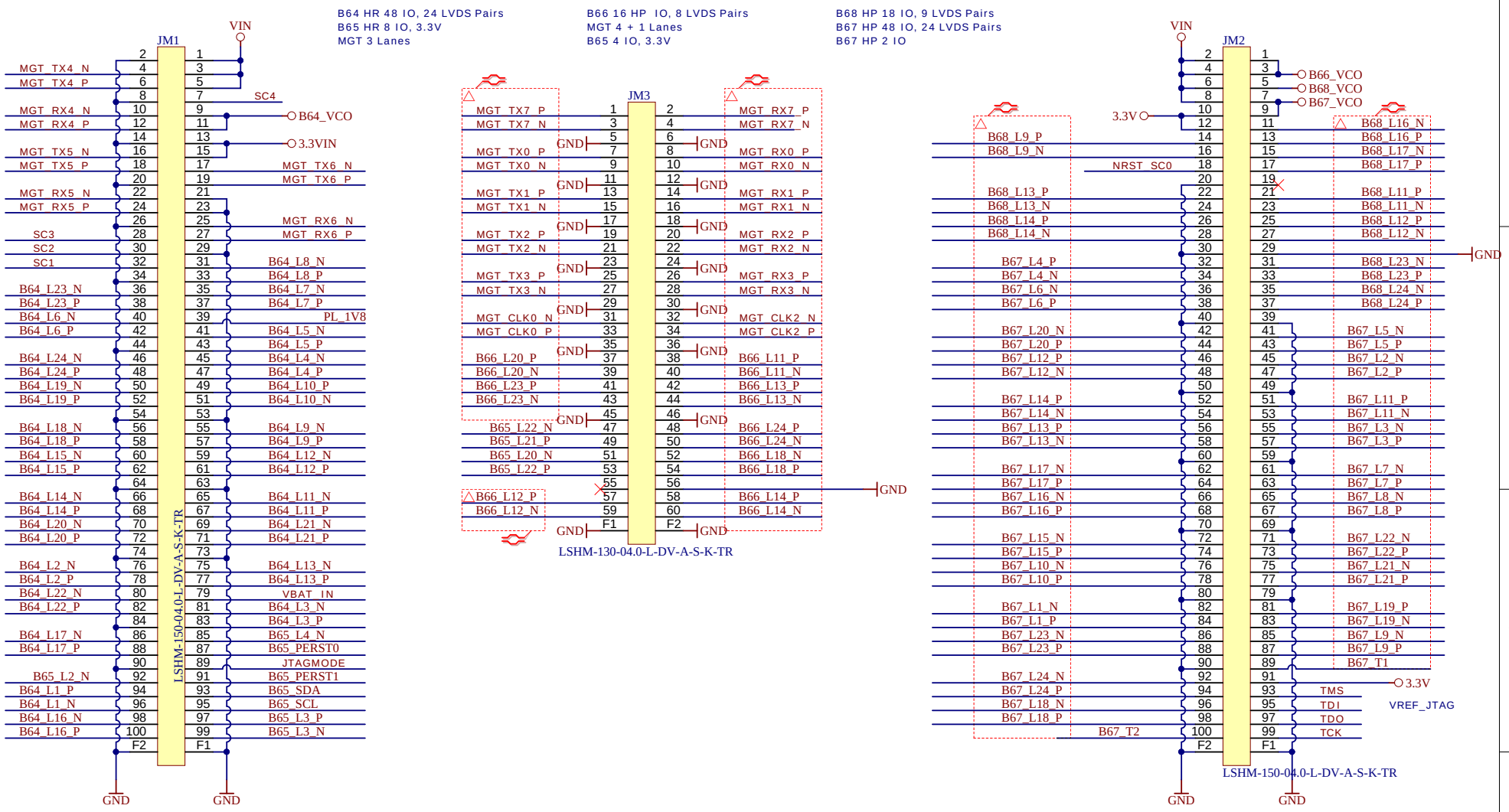
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page1 of 21
Filename: TE0841.SchDoc			


B64 HR 48 IO, 24 LVDS Pairs
B65 HR 8 IO, 3.3V
MGT 3 Lanes
B66 16 HP IO, 8 LVDS Pairs
MGT 4 + 1 Lanes
B65 4 IO, 3.3V
B68 HP 18 IO, 9 LVDS Pairs
B67 HP 48 IO, 24 LVDS Pairs
B67 HP 2 IO
JM1
LSHM-150-04.0-L-DV-A-S-K-TR
JM3
LSHM-130-04.0-L-DV-A-S-K-TR
JM2
LSHM-150-04.0-L-DV-A-S-K-TR
VIN
SC4
B64_VCO
3.3VIN
MGT_TX6_N
MGT_TX6_P
MGT_RX6_N
MGT_RX6_P
B64_L8_N
B64_L8_P
B64_L7_N
B64_L7_P
PL_1V8
B64_L5_N
B64_L5_P
B64_L4_N
B64_L4_P
B64_L10_P
B64_L10_N
B64_L9_N
B64_L9_P
B64_L12_N
B64_L12_P
B64_L11_N
B64_L11_P
B64_L21_N
B64_L21_P
B64_L13_N
B64_L13_P
VBAT_IN
B64_L3_N
B64_L3_P
B65_L4_N
B65_PERST0
JTAGMODE
B65_PERST1
B65_SDA
B65_SCL
B65_L3_P
B65_L3_N
GND
B66_VCO
B68_VCO
B67_VCO
3.3V
NRST_SC0
B67_T2
TMS
TDI
TDO
TCK
VREF_JTAG
Title: TE0841
A4
Number: TE0841 035-1C
Rev. 02
Date: 2018-03-14
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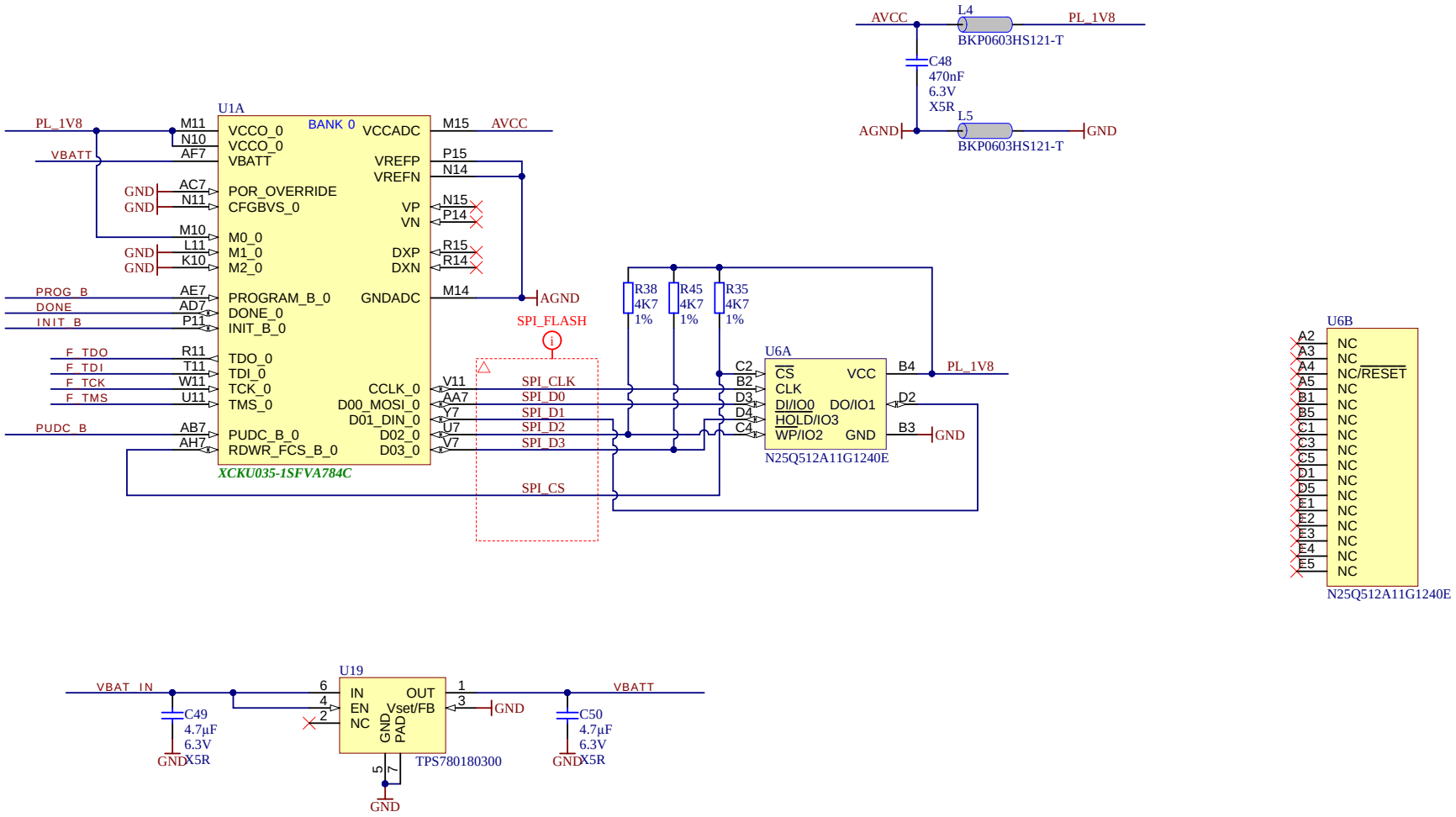
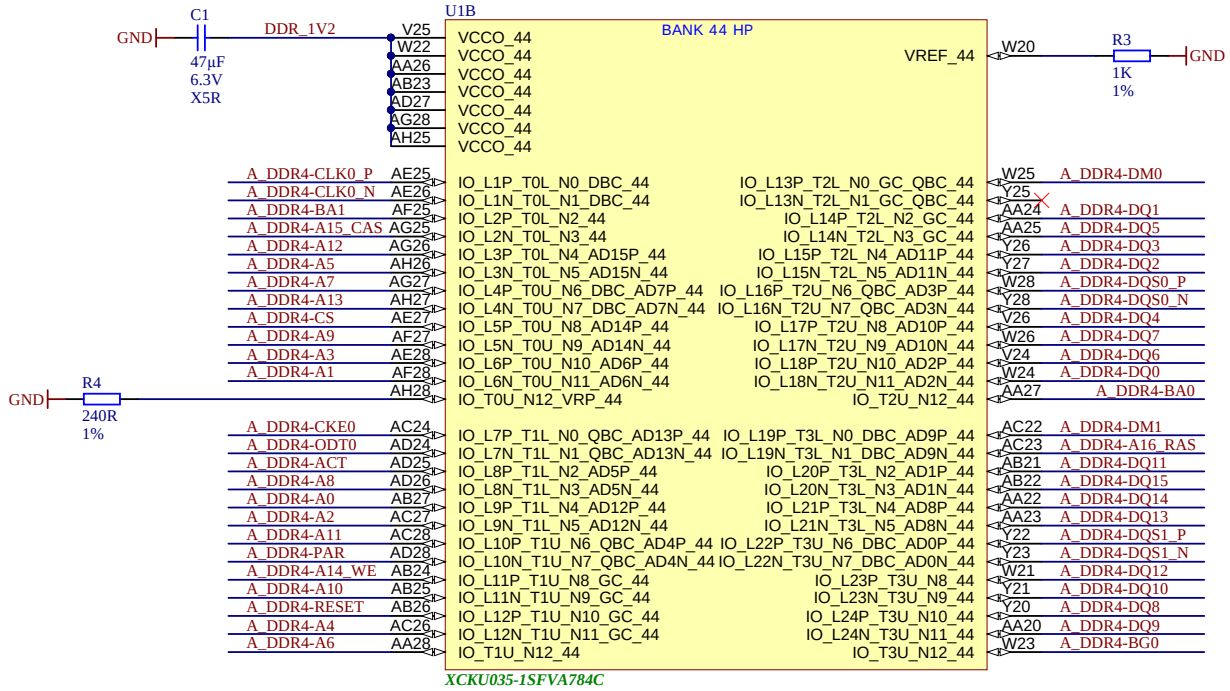
Page2 of 21
Filename: B2B-Connectors.SchDoc



trenz electronic	Title: TE0841		
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page3 of 21
Filename: FPGA-MISC.SchDoc			



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Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page4 of 21
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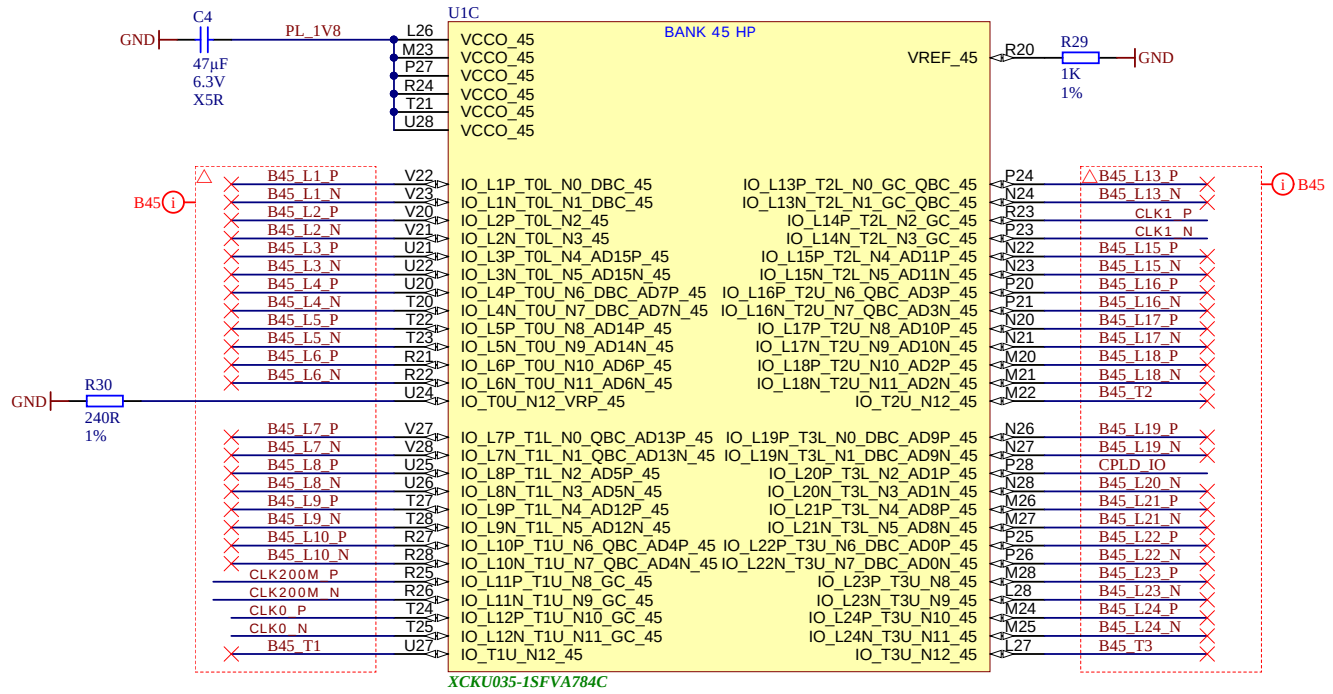

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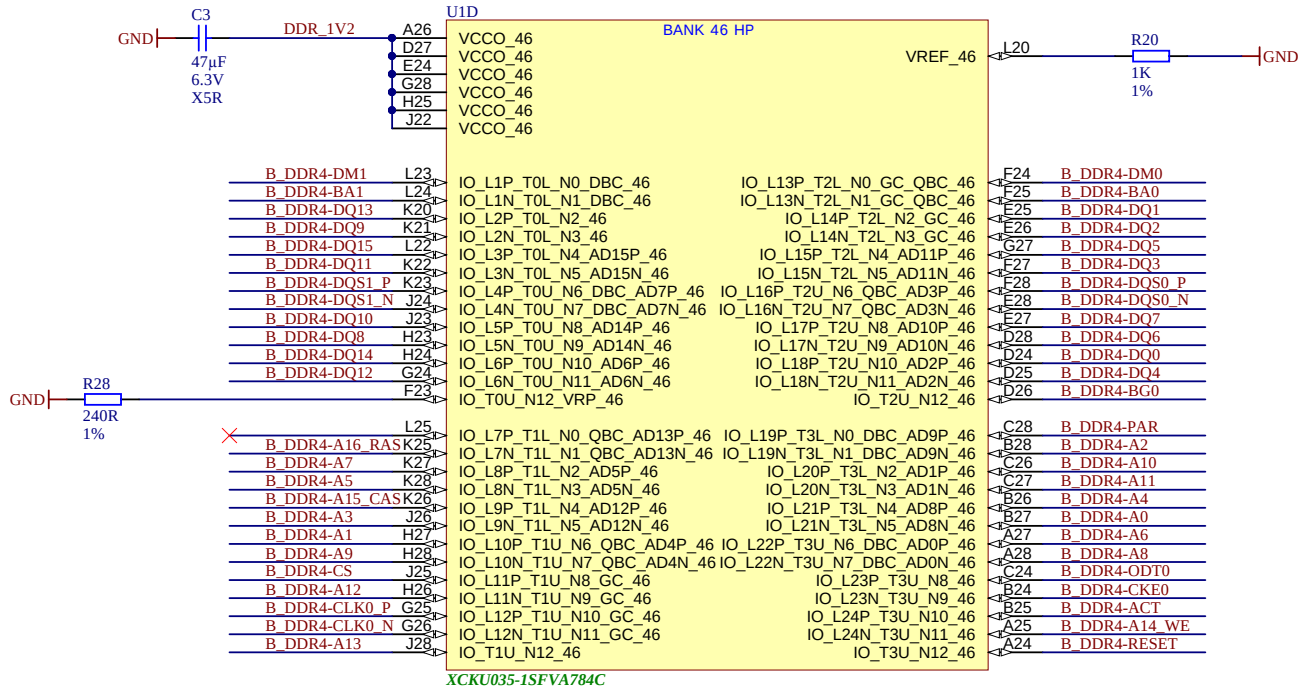
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page5 of 21
Filename: FPGA-B45.SchDoc			



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Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page6 of 21
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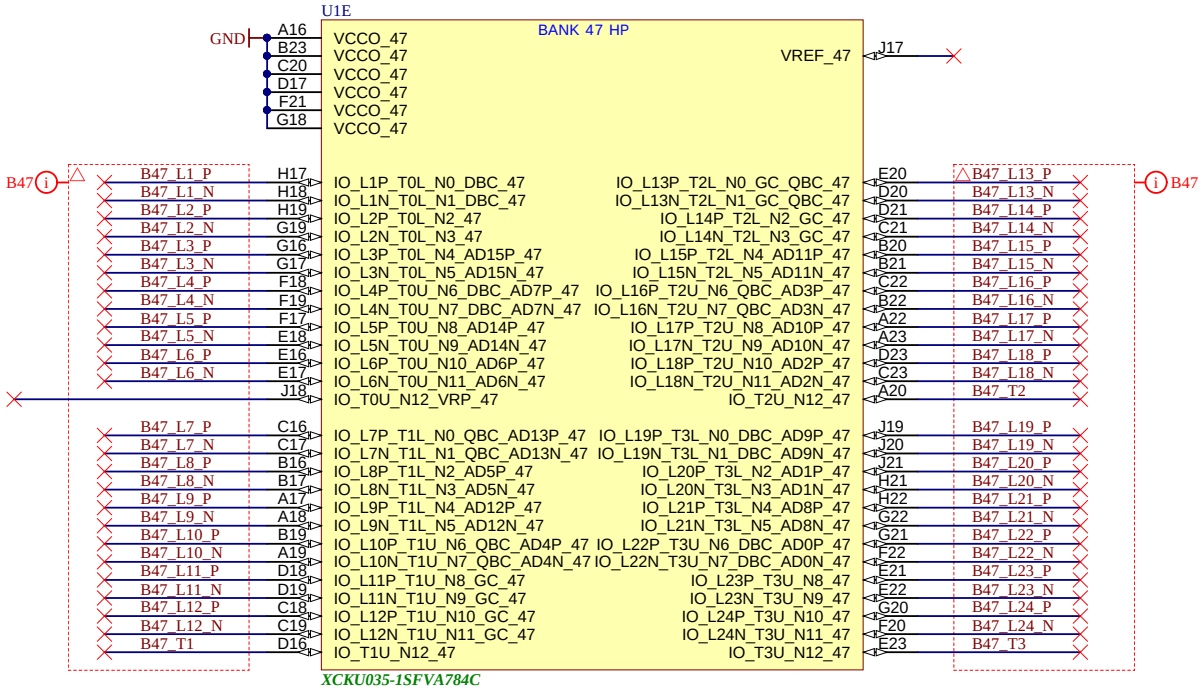

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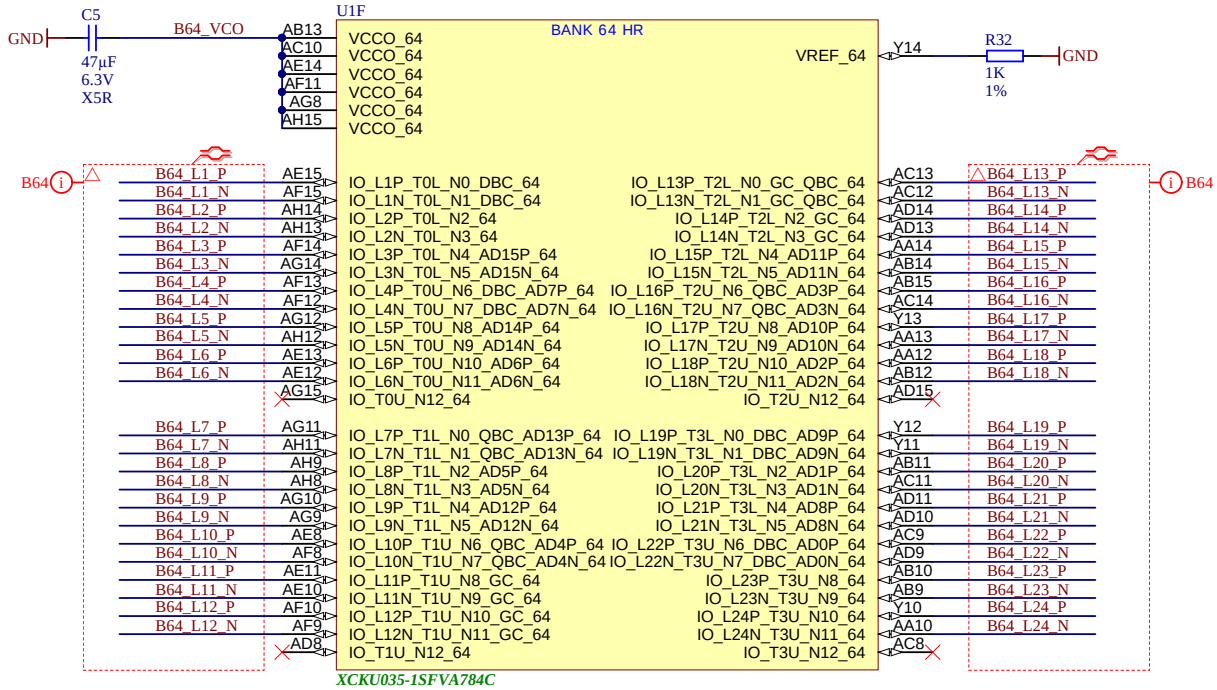
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page7 of 21
Filename: FPGA-B47.SchDoc			



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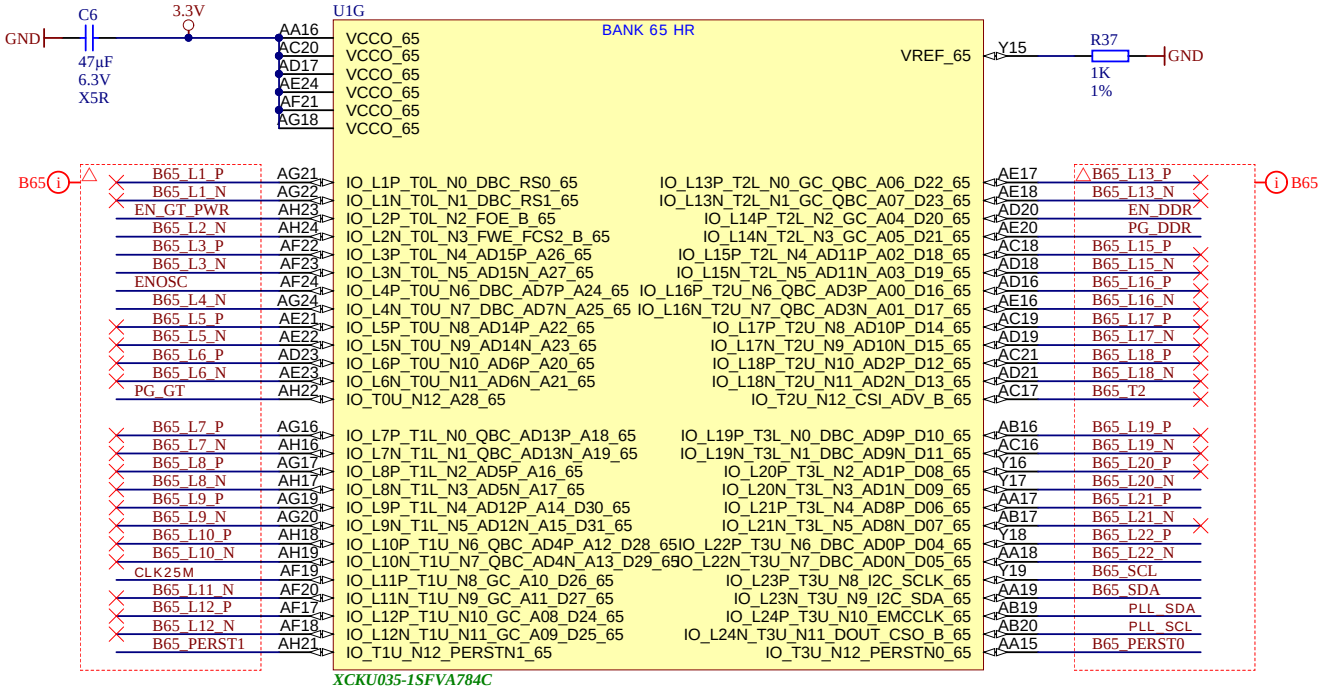
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page8 of 21
Filename: FPGA-B64.SchDoc			



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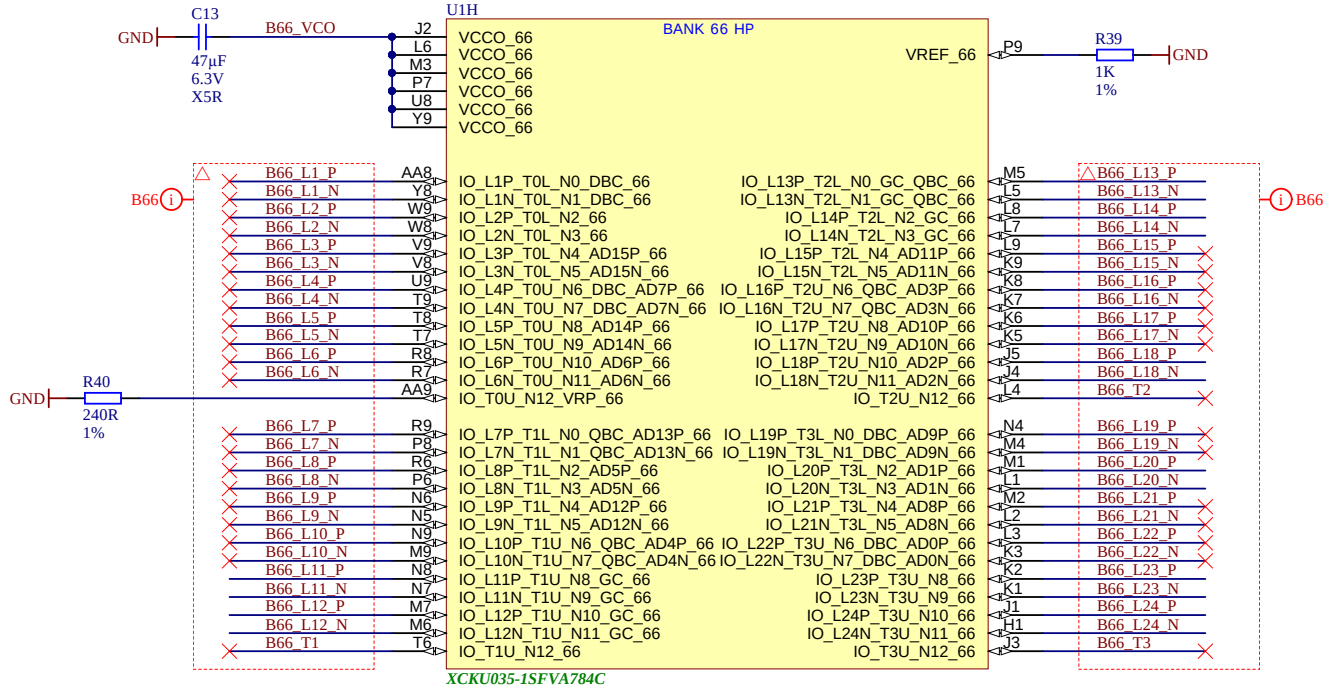
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page9 of 21
Filename: FPGA-B65.SchDoc			



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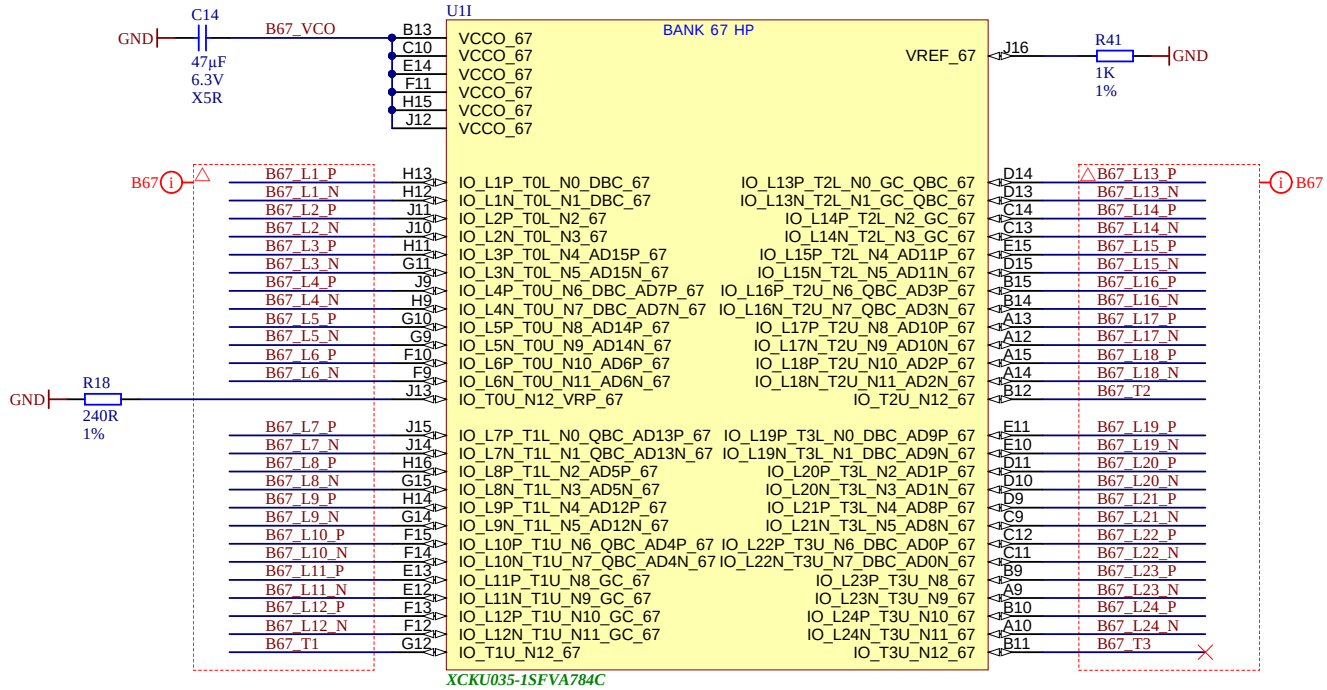
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page10 of 21
Filename: FPGA-B66.SchDoc			



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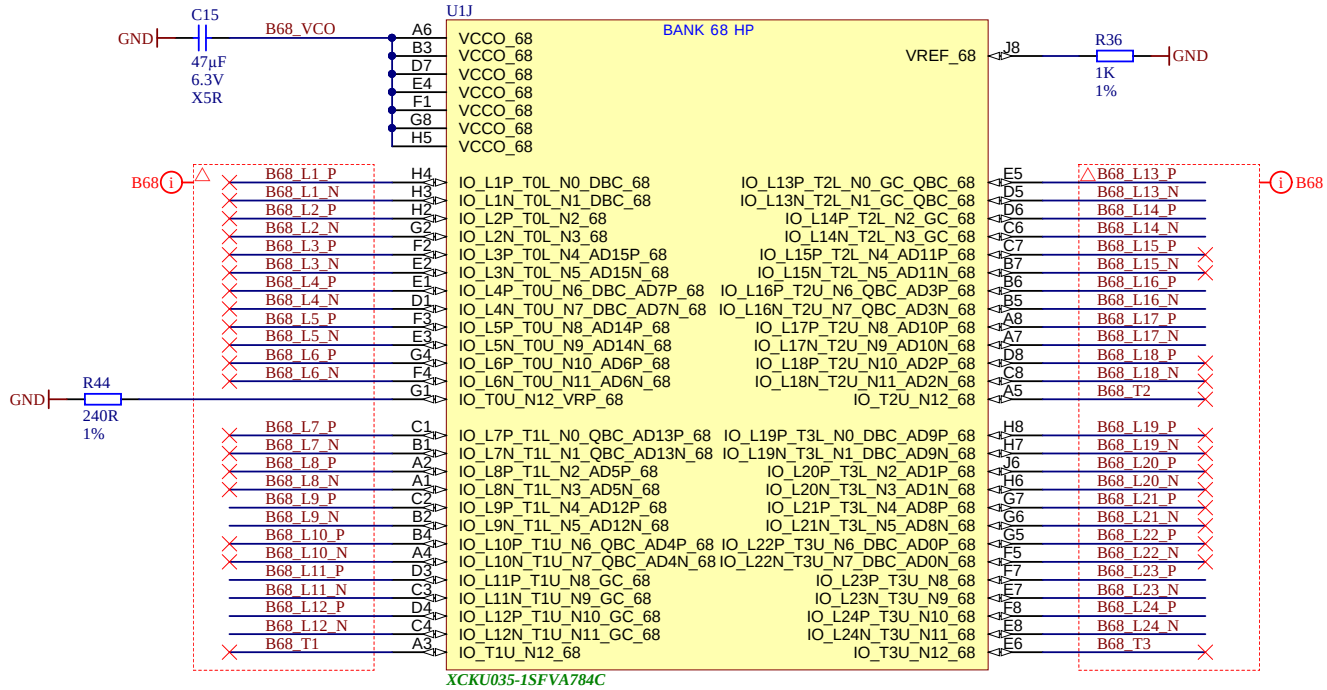
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page11 of 21
Filename: FPGA-B67.SchDoc			



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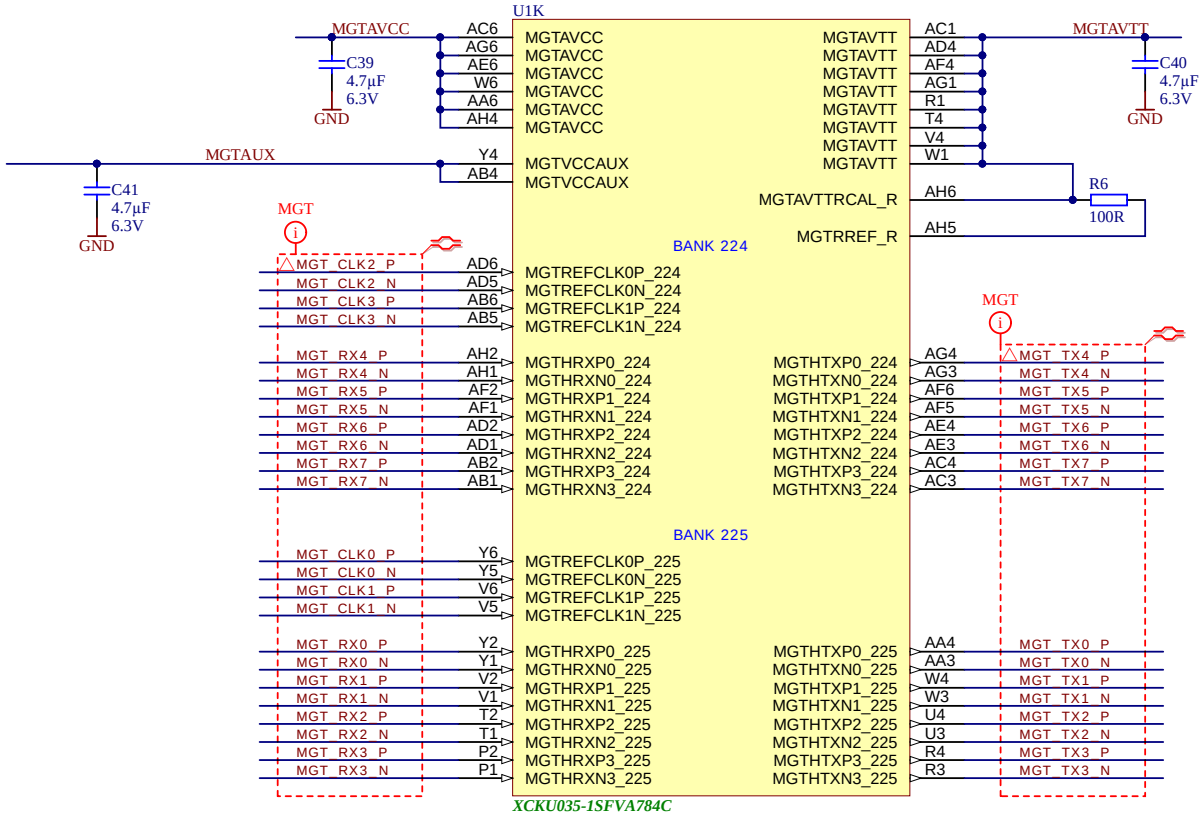
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page12 of 21
Filename: FPGA-B68.SchDoc			



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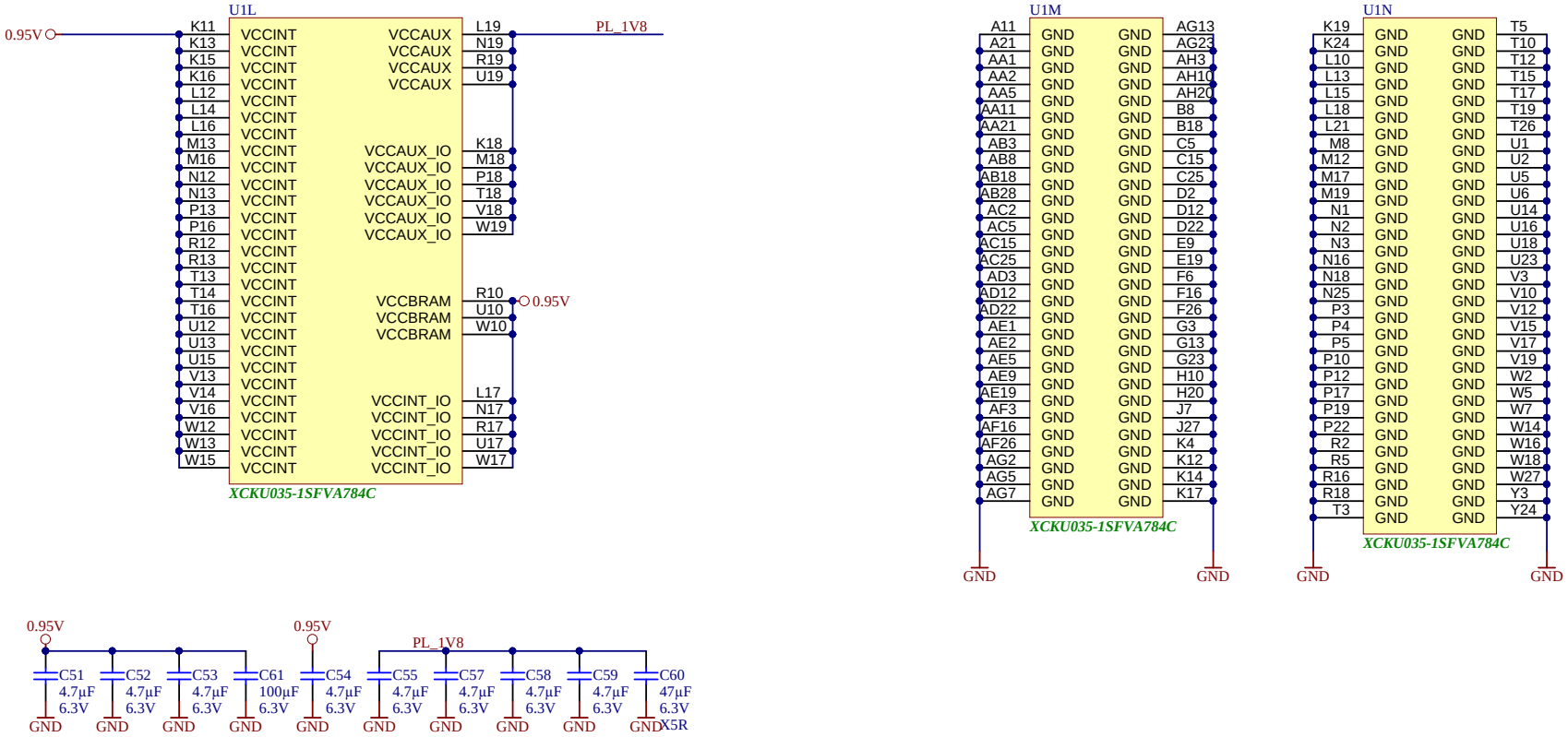
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page13 of 21
Filename: FPGA-MGT.SchDoc			



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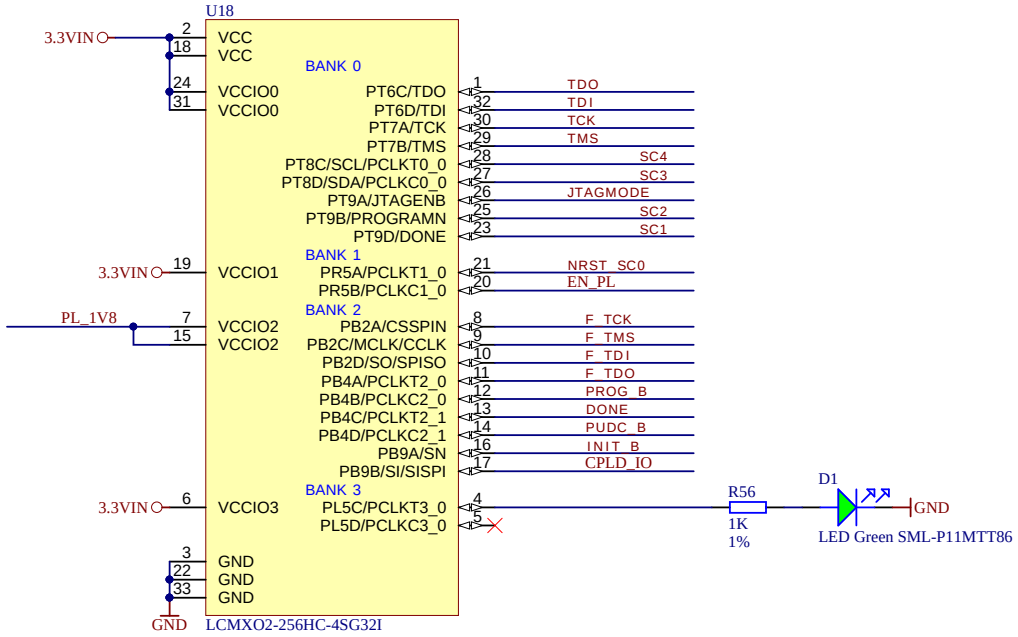
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page14 of 21
Filename: FPGA-PWR.SchDoc			



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A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page15 of 21
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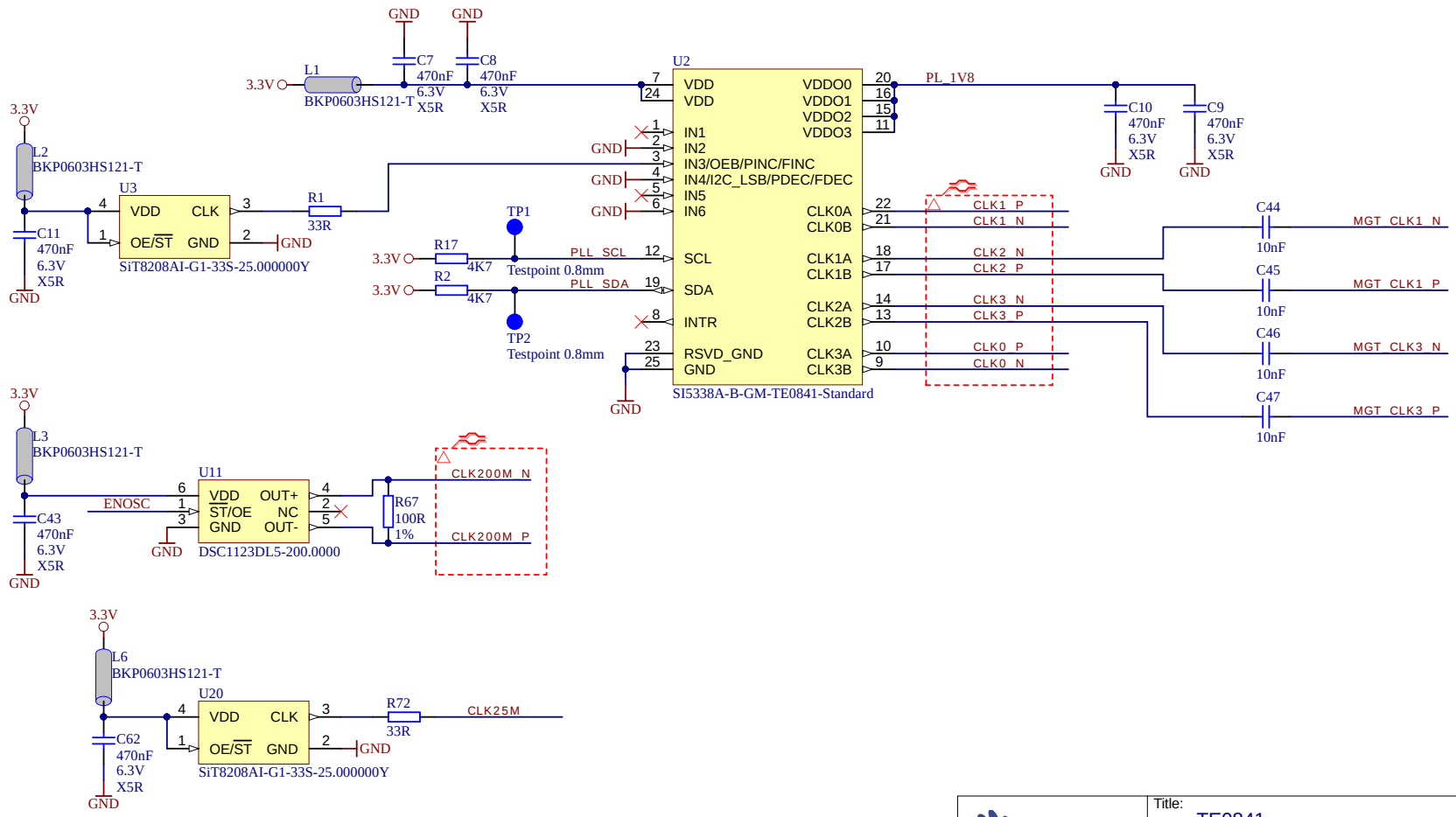

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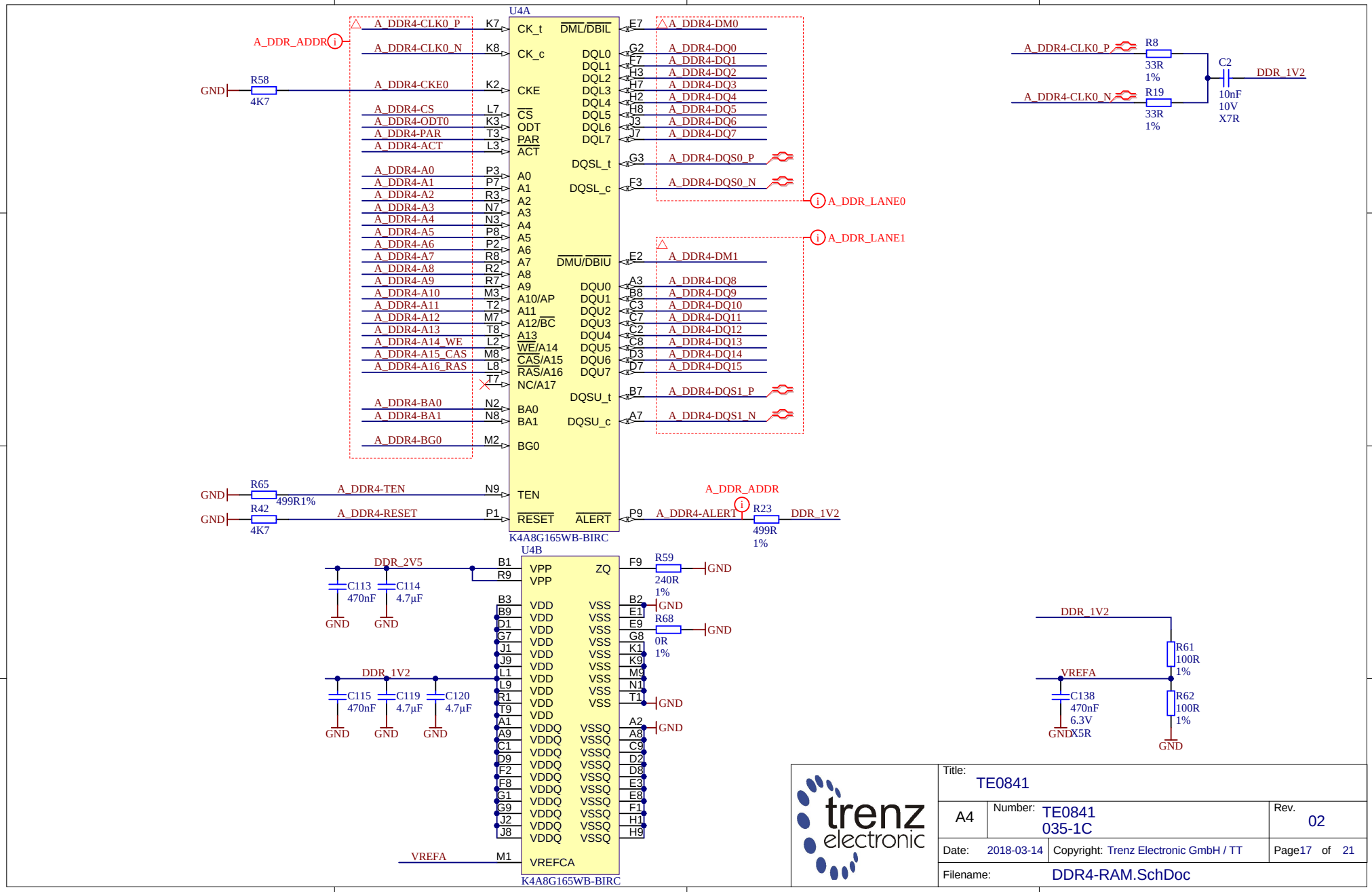
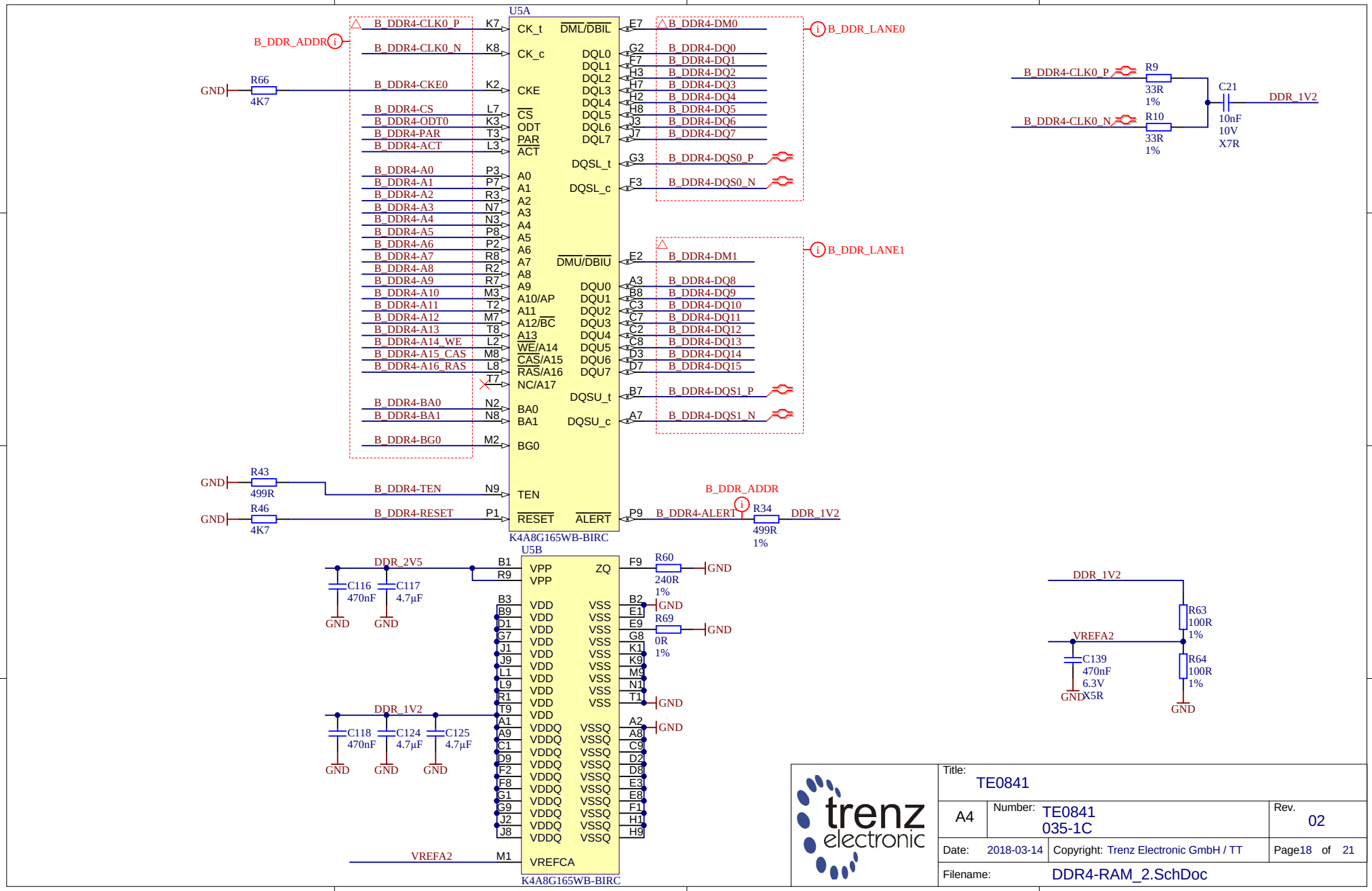
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page16 of 21
Filename: Clock.SchDoc			



trenz electronic	Title: TE0841		
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page17 of 21
Filename: DDR4-RAM.SchDoc			


U5A
K4A8G165WB-BIRC
B_DDR_ADDR
B_DDR_LANE0
B_DDR_LANE1
B_DDR4-CLK0_P K7 CK_t
B_DDR4-CLK0_N K8 CK_c
B_DDR4-CKE0 K2 CKE
B_DDR4-CS L7 CS
B_DDR4-ODT0 K3 ODT
B_DDR4-PAR T3 PAR
B_DDR4-ACT L3 ACT
B_DDR4-A0 P3 A0
B_DDR4-A1 P7 A1
B_DDR4-A2 R3 A2
B_DDR4-A3 N7 A3
B_DDR4-A4 N3 A4
B_DDR4-A5 P8 A5
B_DDR4-A6 P2 A6
B_DDR4-A7 R8 A7
B_DDR4-A8 R2 A8
B_DDR4-A9 R7 A9
B_DDR4-A10 M3 A10/AP
B_DDR4-A11 T2 A11
B_DDR4-A12 M7 A12/BC
B_DDR4-A13 T8 A13
B_DDR4-A14_WE L2 WE/A14
B_DDR4-A15_CAS M8 CAS/A15
B_DDR4-A16_RAS L8 RAS/A16
T7 NC/A17
B_DDR4-BA0 N2 BA0
B_DDR4-BA1 N8 BA1
B_DDR4-BG0 M2 BG0
B_DDR4-TEN N9 TEN
B_DDR4-RESET P1 RESET
E7 DML/DBIL B_DDR4-DM0
G2 DQL0 B_DDR4-DQ0
F7 DQL1 B_DDR4-DQ1
H3 DQL2 B_DDR4-DQ2
H7 DQL3 B_DDR4-DQ3
H2 DQL4 B_DDR4-DQ4
H8 DQL5 B_DDR4-DQ5
J3 DQL6 B_DDR4-DQ6
J7 DQL7 B_DDR4-DQ7
G3 DQSL_t B_DDR4-DQS0_P
F3 DQSL_c B_DDR4-DQS0_N
E2 DMU/DBIU B_DDR4-DM1
A3 DQU0 B_DDR4-DQ8
B8 DQU1 B_DDR4-DQ9
C3 DQU2 B_DDR4-DQ10
C7 DQU3 B_DDR4-DQ11
C2 DQU4 B_DDR4-DQ12
C8 DQU5 B_DDR4-DQ13
D3 DQU6 B_DDR4-DQ14
D7 DQU7 B_DDR4-DQ15
B7 DQSU_t B_DDR4-DQS1_P
A7 DQSU_c B_DDR4-DQS1_N
P9 ALERT B_DDR4-ALERT
GND R66 4K7
GND R43 499R
GND R46 4K7
B_DDR_ADDR R34 499R 1% DDR_1V2
U5B
K4A8G165WB-BIRC
DDR_2V5
B1 VPP
R9 VPP
C116 470nF GND
C117 4.7µF GND
B3 VDD
B9 VDD
D1 VDD
G7 VDD
J1 VDD
J9 VDD
L1 VDD
L9 VDD
R1 VDD
T9 VDD
DDR_1V2
C118 470nF GND
C124 4.7µF GND
C125 4.7µF GND
A1 VDDQ
A9 VDDQ
C1 VDDQ
D9 VDDQ
F2 VDDQ
F8 VDDQ
G1 VDDQ
G9 VDDQ
J2 VDDQ
J8 VDDQ
VREFA2 M1 VREFCA
F9 ZQ R60 240R 1% GND
B2 VSS GND
E1 VSS
E9 VSS R69 0R 1% GND
G8 VSS
K1 VSS
K9 VSS
M9 VSS
N1 VSS
T1 VSS GND
A2 VSSQ GND
A8 VSSQ
C9 VSSQ
D2 VSSQ
D8 VSSQ
E3 VSSQ
E8 VSSQ
F1 VSSQ
H1 VSSQ
H9 VSSQ
B_DDR4-CLK0_P R9 33R 1%
B_DDR4-CLK0_N R10 33R 1%
C21 10nF 10V X7R DDR_1V2
DDR_1V2
R63 100R 1%
VREFA2
C139 470nF 6.3V X5R GND
R64 100R 1% GND
trenz electronic
Title: TE0841
A4
Number: TE0841 035-1C
Rev. 02
Date: 2018-03-14
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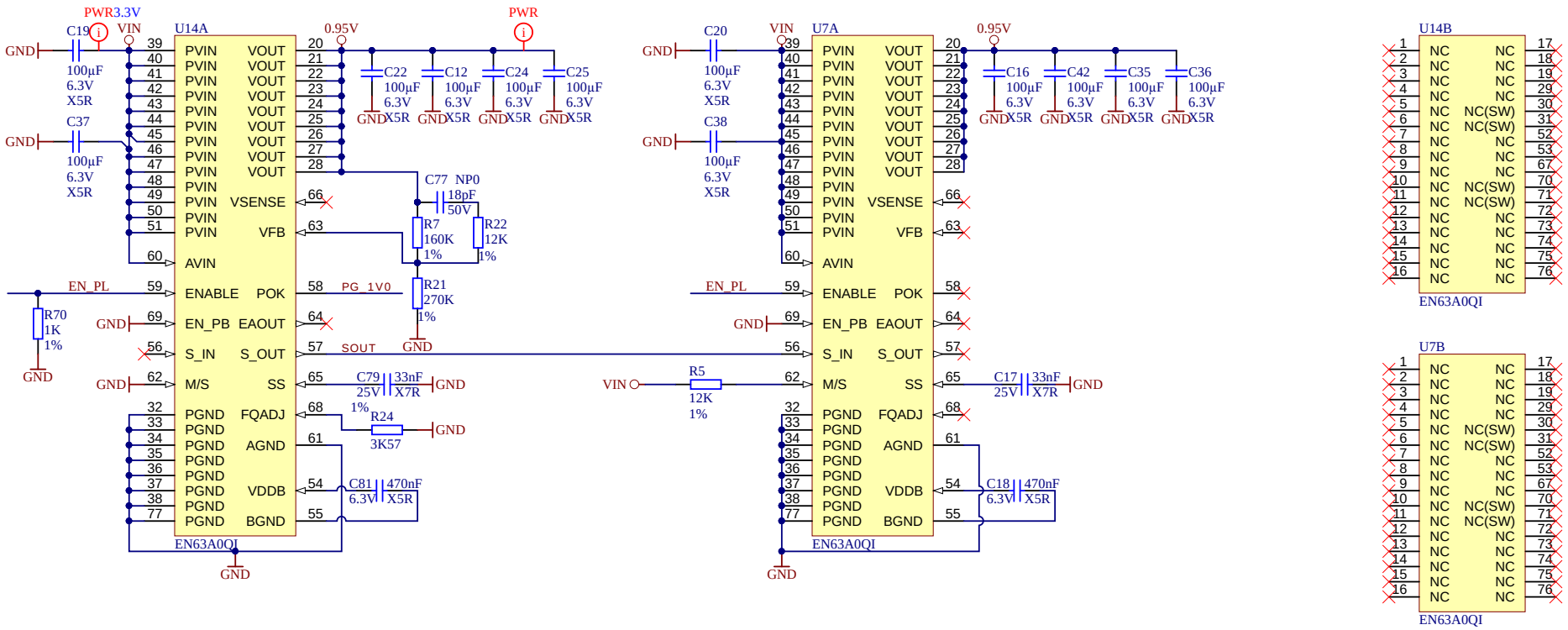
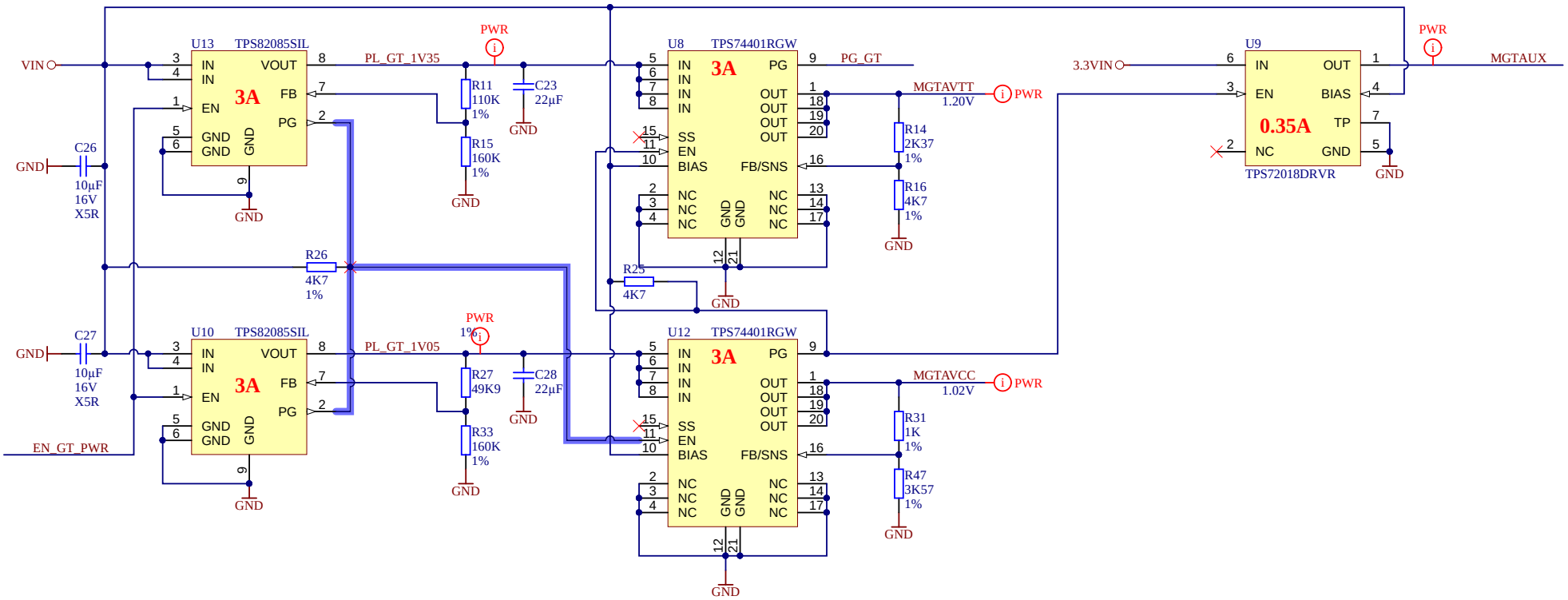
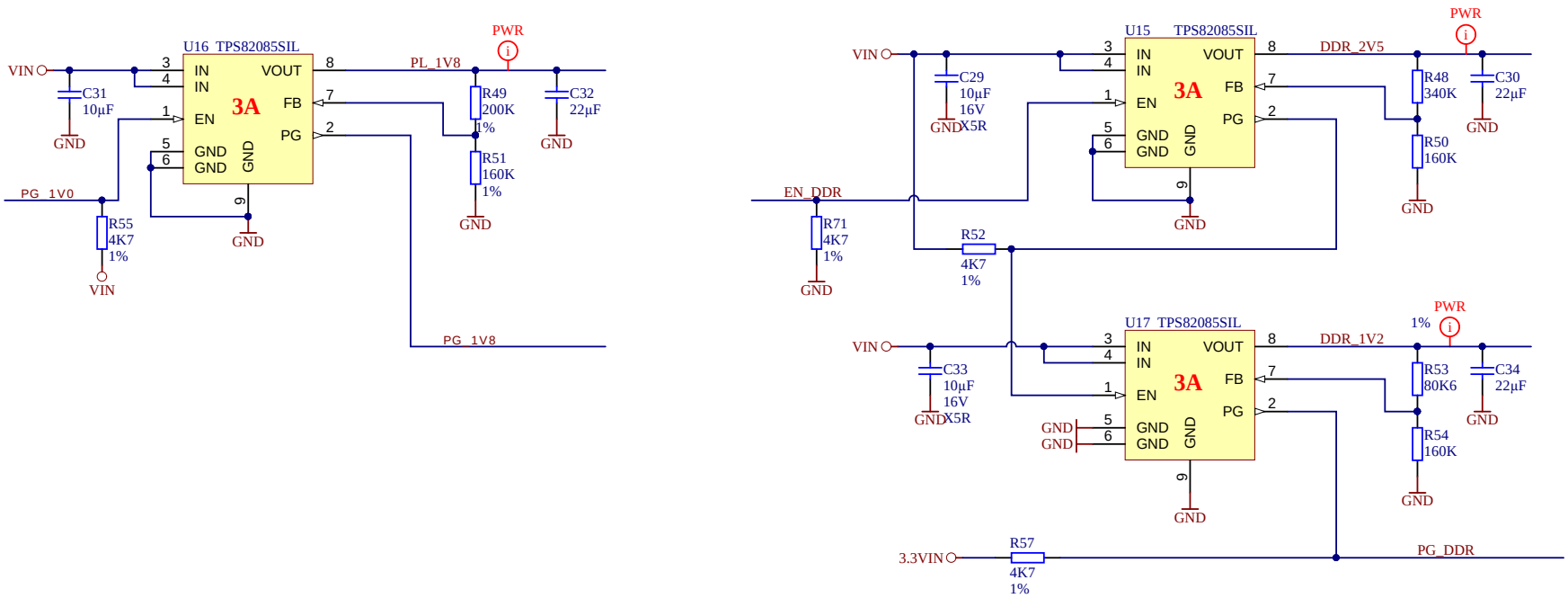
Page18 of 21
Filename: DDR4-RAM_2.SchDoc



trenz electronic	Title: TE0841		
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page19 of 21
Filename: PWR1.SchDoc			



trenz electronic	Title: TE0841		
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page20 of 21
Filename: PWR2.SchDoc			



trenz electronic	Title: TE0841		
A4	Number: TE0841 035-1C		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page21 of 21
Filename: POWER_2.SchDoc			

CHANGES REV01 TO REV01A (08.16.2017):

1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
-- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
-- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):
JM1: swapped signals B64_L6:
-- B64_L6_N - pin 40 (was pin 42)
-- B64_L6_P - pin 42 (was pin 40)
JM3: swapped signals B64_L6:
-- B66_L18_N - pin 52 (was pin 54)
-- B66_L18_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 (03.2018):

1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
2) Fixed sense connection on DCDC
3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
4) Full update LIB
5) Added additional resistors for support 16GBit DDR chips
6) Added strong pull-down to EN_PL
7) Added additional testpoints for I2C bus
8) Added additional MEMS oscillator (25MHz)
9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net
10) Added pull-down on the EN_DDR

trenz electronic	Title: TE0841 - Changes list		
	A4	Number: TE0841 035-1C	Rev. 02
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH	Page22 of 22
	Filename: Revision_Changes.SchDoc		