

TE0960 TRM

Revision v.32

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4 Overview

The TE0960 is a development board for AMD Versal AI Edge Gen 2 SoCs which supports three LPDDR5 chips, UFS storage and QSPI flash. It supports a M.2 M key device, a microSD card, two Ethernet PHYs via RJ45 connectors and offers three USB Type C for high speed data exchange, DisplayPort over USB, High Speed Debug Port and USB 2.0/OTG.
Additional IOs are accessible via SFC / FPC connectors, Pmods and pin headers. It offers a PWM Fan header for cooling and multiple DIP switches, buttons and LEDs.

Refer to https://trenz.org/te0960-info for current online available documentation.

4.1 Key Features

- **SoC**
  - AMD Versal AI Edge Gen 2 [1]: XC2VE3304 / XC2VE3358 / XC2VE3504 / XC2VE3558
  - Speedgrade [1]: -1 / -2
  - Temperature Range [1]: E / I
  - Voltage [1] : -L / -M
  - Package [1]: SSVA1440 / SFVA1440
- **RAM/Storage**
  - 3x 32 GBit LPDDR5 SDRAM [2]
  - up to 2 GBit QSPI Flash (with XiP support) [2]
  - up to 512 GByte UFS storage [2]
  - 3x EEPROM with unique EUI-48 ™ / MAC address
  - 128 Kbit EEPROM
  - EEPROM with FTDI programmer configuration
- **Interfaces**
  - **Programming / AMD HSDP**
    - 1x USB Type C
    - High-Speed Debug Port (HSDP) / 1x MGT lane
    - USB 2.0 to JTAG/UART bridge
    - EEPROM for JTAG/UART bridge with programmer configuration
    - ESD protection on USB 2.0 and USB HSDP lines
    - LED status signalling - 2x UART / 1x voltage - all green
    - Shared oscillator with CLK generator
  - **USB 3.x with DisplayPort support**
    - 1x USB Type C
    - Port controller
    - Pin Header for I2C connection to USB 3.x port controller
    - ESD protection
  - **USB 2.0/OTG**
    - 1x USB Type C
    - Oscillator
    - 1x over current LED - red
    - ESD protection
    - 2x4 pin header for USB 3.x port controller I2C configuration
  - **Ethernet Interfaces**
    - 2x 10/100/1000 BASE-T/X ETH PHYs with IEEE 802.3 and 1588v2/PTP support
    - 2x RJ45 MagJack Ethernet with 2x status LEDs - all green
    - zSFP+ connector
  - **Storage Media**
    - MicroSD socket with voltage enable, selectable voltage and card detect

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    - M.2 M key socket with PCIe x2
    - PCIe common oscillator for M.2 socket
  - **Extension interfaces**
    - CRUVI GTX - with LS and HS signals:
      - 24x SE / 12x DIFF
      - 8x SE
      - 4x control, I2C, 12 V and 3.3 V
    - CRUVI GTX - with LS / HS and GTX [3] signals:
      - 24x SE / 12x DIFF [3]
      - 4x MGT (RX/TX) and 1x CLK
      - 8x SE
      - 4x control, I2C, 12 V and 3.3 V
    - 2x / 4x [3] FFC/FPC connectors for CSI/DSI/MIPI with each:
      - 10x SE / 5x DIFF
      - 2x GPIO
      - I2C and 3.3 V
    - 2x Pmod for combined 16x SE / 8x DIFF [3] with ESD protection
    - CAN
      - 2x 2x5 box header for CAN
      - 2x CAN transceiver with fault flag and silent mode
      - ESD protection for signal lines
- **On Board**
  - Trusted platform module 2.0 with presence/detection button
  - Clocks for SoC PL, SoC PS, LPDDR5, UFS storage, ETH PHYs, M.2
  - Programmable PLL with 2x Oscillators
  - 4x pin header for PLL I2C
  - 2x17 pin header - 20x SE / 10x DIFF [3]
  - LEDs:
    - 1x status 12.0 V supply - green
    - 3x status SoC
      - POR_B - LED - green
      - DONE - LED - green
      - ERROR_OUT - LED - red
    - 1x status M.2 activity - green
    - 4x User LED - green
  - Button:
    - 1x Reset
    - 2x User
  - DIP Switch:
    - 2x User
    - 1x Power Off
    - 4x Boot Mode Setup
  - Jumper for:
    - USB 3.x port controller I2C voltage setup
    - SoC Fuse Programming
    - CAN termination
- **Cooling**
  - Programmable fan controller with ambient temperature sensor
  - 4x pin header for 12 V PWM fan
- **Power**
  - Single Rail 12.0 V power supply - Molex Mini-Fit 6 pins [4]
  - Supply protection - Over- & Under- voltage, Reverse polarity and fuse
  - I2C interface for most DCDCs
  - Monitoring for most voltage rails
  - Current and voltage monitoring for LPDDR5 voltages

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    - Backup battery holder - CR1220 / 3.0 V lithium
- **Dimension**
    - 150.00 mm x 200.00 mm
    - Enclosure ready
- **Notes**

[1] Available as assembly variant or upon request.

[2] Other pin/package-compatible sizes/devices upon request.

[3] Only for variants with XC2VE35xx.

[4] Consider to use proper pinout.

4.2 Block Diagram

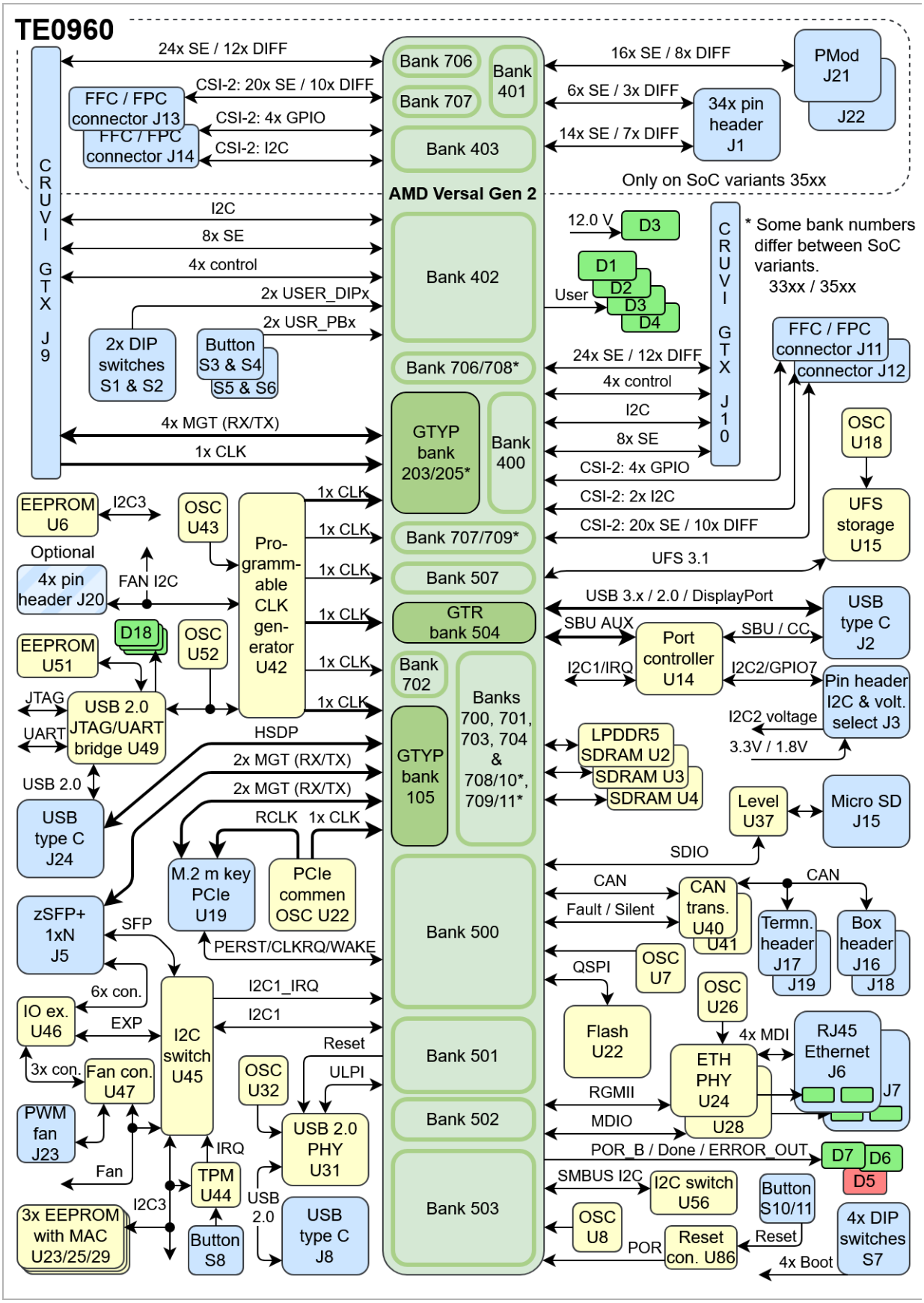
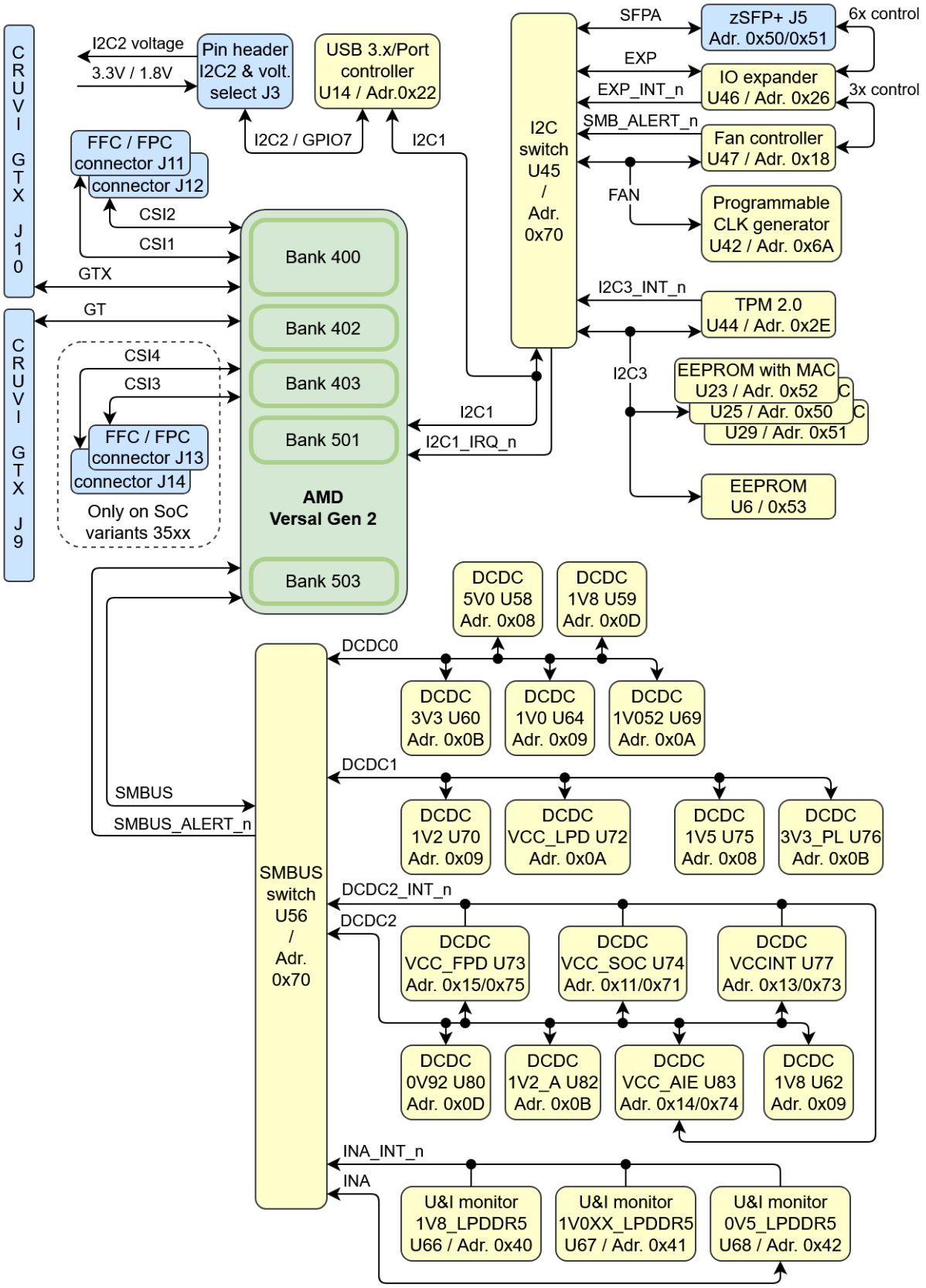


Figure 1: TE0960 block diagram

TE0960 - I2C / SMBUS



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4.3 Main Components

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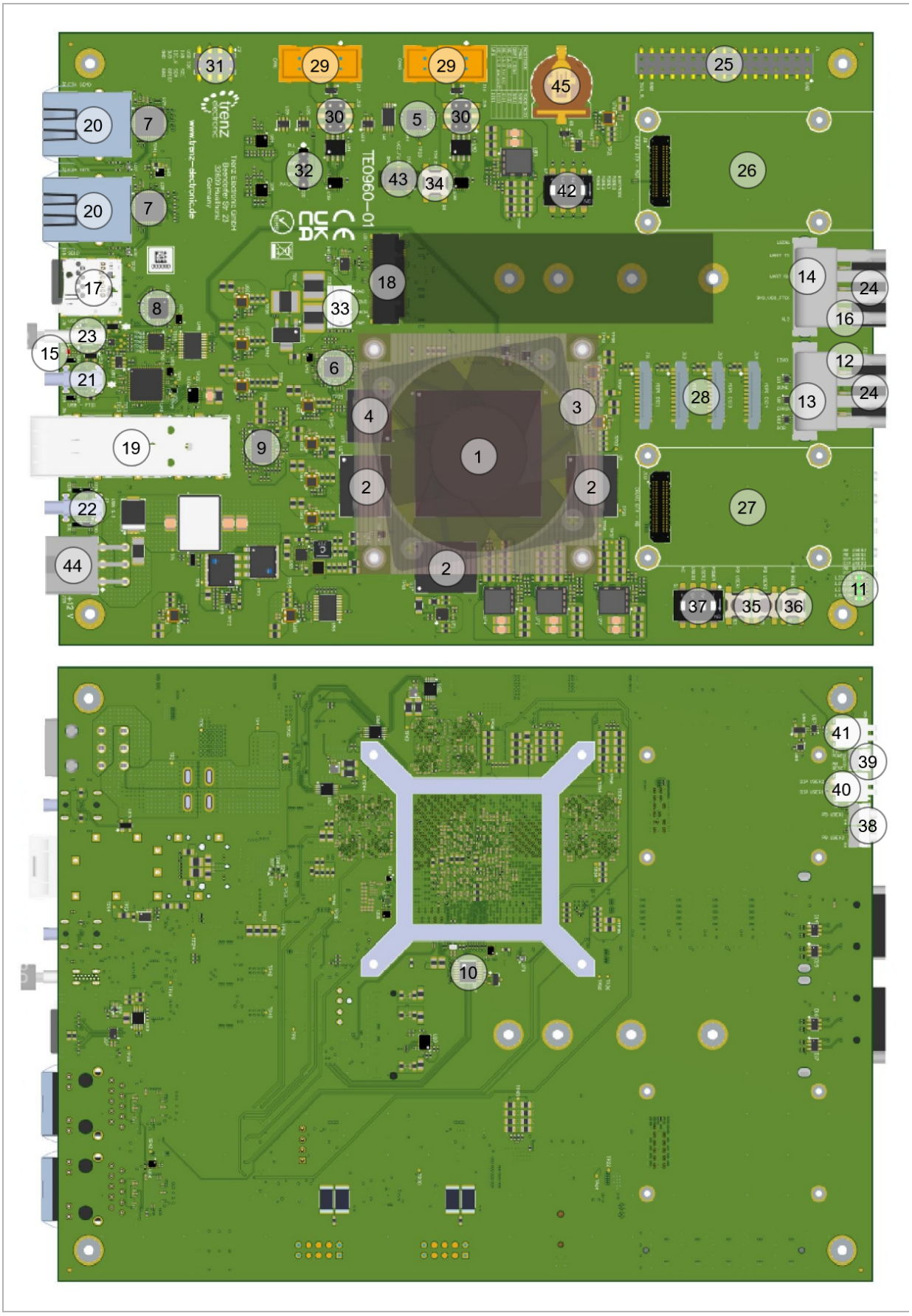


Figure 2: TE0960 main components

1. AMD Versal AI Edge Gen 2 SoC, U1
2. LPDDR5 SDRAM, U2, U3, U4
3. NOR flash, U5
4. UFS storage, U15
5. TPM 2.0, U44
6. Programmable PLL, U42
7. Ethernet PHYs, U24, U28
8. USB 2.0/OTG PHY, U31
9. USB 3.x channel control logic, U14
10. Fan controller, U47
11. 4x user LEDs - green, D1, D2, D3, D4
12. 1x status LED 12.0 V supply - green, D22
13. 3x status LEDs SoC - POR_B, DONE and ERROR_OUT - 2x green and red, D7, D6, D5
14. 3x status LEDs programmer: 2x UART - green / 1x voltage - green, D18, D19, D20
15. 1x status LED USB 3.x over current - red, D9
16. 1x status LED M.2 activity - green, D8
17. MicroSD socket, J15
18. M.2 M key socket with PCIe x2, U19
19. zSFP+ 1xN connector, J5
20. 2x RJ45 mag-jack ethernet with 2x status LEDs, J6, J7
21. 1x USB type C for programming and debugging, J24
22. 1x USB type C for data transfers and DisplayPort, J2
23. 1x USB type C for data transfers / USB 2.0/OTG, J8
24. 2x Pmod for combined 16x SE / 8x DIFF [1)], J21, J22
25. 2x17 pin header - 20x SE / 10x DIFF [1)], J1
26. CRUVI GTX - with LS / HS and GTX [1)] signals, J9
27. CRUVI GTX - with LS and HS signals, J10
28. 2x / 4x [1)] FFC/FPC connectors for CSI/DSI/MIPI, J11, J12, J13 [1)], J14 [1)]
29. 2x5 box header for CAN, J16, J18
30. 2x3 pin header for CAN termination, J17, J19
31. 2x4 pin header for USB 3.x port controller I2C, J3
32. 4x pin header for PLL I2C, J20
33. 4x pin header for 12 V PWM fan, J23
34. Button TPM presence detection, S8
35. Buttons: 2x user definable, S3, S5
36. Buttons: reset, S11
37. DIP switches - 2x user definable, 1x module power, 1x not connected, S1
38. Buttons for enclosure: 2x user definable, S4, S6
39. Buttons for enclosure: reset, S10
40. DIP switches for enclosure: 2x user definable, S2
41. DIP switches for enclosure: 1x module power, 1x not connected, S9
42. DIP switches - 4x boot mode, S7
43. Jumper SoC OTP storage VCC_FUSE voltage, J4
44. Molex Mini-Fit 6 pin socket - 12.0 V power supply, J25
45. Backup battery holder, B1

Notes

[1)] Only on SoC 35xx variants

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4.4 Initial Delivery State

Storage device name	Designator	Content	Notes
SoC	U1	Not programmed	
UFS	U15	Not programmed	
QSPI Flash	U22	Not programmed	
TPM 2.0	U44	Firmware by the manufacturer.	
Programmable PLL	U42	Programmed - I2C overwriting possible	OUT0 : 156¼ MHz OUT1 : 26 MHz OUT2 : 24 MHz OUT3: 156¼ MHz OUT4 : 156¼ MHz OUT5 : 156¼ MHz
EEPROM with MAC	U23 / U25 / U29	MAC is burned-in by the manufacturer.	
EEPROM	U6	Not programmed	
EEPROM	U51	Programmer configuration.	**Do not overwrite!**

Table 1: Initial delivery state of programmable devices

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5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO count	Notes
2x17 pin header	J1	HDIO	6x SE / 3x DIFF	Only on 35xx SoC variants. 3.3 V - Bank 401.
2x17 pin header	J1	HDIO	14x SE / 7x DIFF	Only on 35xx SoC variants. 3.3 V - Bank 403
CRUVI GTX	J9	HS / X5IO	24x SE / 12x DIFF	Only on 35xx SoC variants. 1.2 V - Bank 706
FFC / FPC	J13	X5IO	10x SE / 5x DIFF / 5x MIPI lanes	Only on 35xx SoC variants. 1.2 V - Bank 707
FFC / FPC	J13	HDIO	2x SE	Only on 35xx SoC variants. 3.3 V - Bank 403
FFC / FPC	J13	I2C / HDIO	2x SE	Only on 35xx SoC variants. 3.3 V - Bank 403
FFC / FPC	J14	X5IO	10x SE / 5x DIFF / 5x MIPI lanes	Only on 35xx SoC variants. 1.2 V - Bank 707
FFC / FPC	J14	HDIO	2x SE	Only on 35xx SoC variants. 3.3 V - Bank 403

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Connector Type	Designator	Interface	IO count	Notes
FFC / FPC	J14	I2C / HDIO	2x SE	Only on 35xx SoC variants. 3.3 V - Bank 403
Pmod	J21	HDIO	8x SE / 4x DIFF	Only on 35xx SoC variants. 3.3 V - Bank 401
Pmod	J22	HDIO	8x SE / 4x DIFF	Only on 35xx SoC variants. 3.3 V - Bank 401
USB type C	J2	USB 3.x / MGT	4x GTR (RX/TX)	Bank 504
USB type C	J2	USB 2.0	1x DIFF	Bank 504
USB type C	J2	USB SBU	2x SE	Bank 504
USB type C	J2	USB CC	2x SE	Bank 504
3x pin header	J4	FUSE programming	1x SE	
zSFP+	J5	MGT	1x GTYP (RX/TX)	Bank 105
zSFP+	J5	I2C	2x SE	
RJ45	J6	Ethernet	4x DIFF	
RJ45	J7	Ethernet	4x DIFF	
USB type C	J8	USB 2.0/MIO	1x DIFF	
CRUVI GTX	J9	LS / HDIO	8x SE	3.3 V - Bank 401/402 [1)]

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Connector Type	Designator	Interface	IO count	Notes
CRUVI GTX	J9	MGT	4x GTYP (RX/TX)	Bank 203/205
CRUVI GTX	J9	MGT CLK	1x DIFF	Bank 203/205
CRUVI GTX	J9	I2C / HDIO	2x SE	3.3 V - Bank 401/402 [1)]
CRUVI GTX	J10	HS/X5IO	24x SE / 12x DIFF	1.2 V - Bank 706/708 [1)]
CRUVI GTX	J10	LS / HDIO	8x SE	3.3 V - Bank 400
CRUVI GTX	J10	I2C / HDIO	2x SE	3.3 V - Bank 400
FFC / FPC	J11	X5IO	10x SE / 5x DIFF / 5x MIPI lanes	1.2 V - Bank 707/709 [1)]
FFC / FPC	J11	HDIO	2x SE	3.3 V - Bank 400
FFC / FPC	J11	I2C / HDIO	2x SE	3.3 V - Bank 400
FFC / FPC	J12	X5IO	10x SE / 5x DIFF / 5x MIPI lanes	1.2 V - Bank 707/709 [1)]
FFC / FPC	J12	HDIO	2x SE	Bank 400
FFC / FPC	J12	I2C / HDIO	2x SE	Bank 400
µSD socket	J15	SDIO	6x SE	Bank 500
2x5 box header	J16	CAN	1x DIFF	Bank 501
2x5 box header	J17	CAN	1x DIFF	Bank 501
M.2 M key	U19	PCIe	2x GTYP (RX/TX)	Bank 105

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Connector Type	Designator	Interface	IO count	Notes
4x pin header	J23	PWM fan	GND / 12 V / Speed / PWM	
USB type C	J24	HSDP / MGT	1x GTYP (RX/TX)	Bank 105
USB type C	J24	JTAG	USB 2.0	Bank 503
USB type C	J24	UART	USB 2.0	Bank 501

Table 2: Board connectors

Notes

[1)] Bank number depends on SoC assembly variant.

5.2 Test Points

Test Point	REV01			
	Top	Bottom	Signal	Notes
TP1	x		12V0_IN	
TP2		x	12V0_IN	
TP3	x		12V_IN_FUSED	
TP4		x	12V_IN_FUSED	
TP5	x		12V0	
TP6		x	12V0	
TP7	x		12V0_FAN	
TP8		x	12V0_FAN	

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Test Point	REV01			
	Top	Bottom	Signal	Notes
TP9	x		5V0	
TP10		x	5V0	
TP11	x		5V0_VIN_FTDI	
TP12		x	5V0_VIN_FTDI	
TP13	x		5V0_VBUS_FTDI	
TP14		x	5V0_VBUS_FTDI	
TP15	x		5V0_USB	
TP16		x	5V0_USB	
TP17	x		USB2_5V0	
TP18		x	USB2_5V0	
TP19	x		3V3_PS	
TP20		x	3V3_PS	
TP21	x		3V3_PL	
TP22		x	3V3_PL	
TP23	x		3V3_VDD_FTDI	

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Test Point	REV01			
	Top	Bottom	Signal	Notes
TP24		x	3V3_VDD_FTDI	
TP25	x		2V5	
TP26		x	2V5	
TP27	x		V_SD_IO	
TP28		x	V_SD_IO	
TP29	x		1V8	
TP30		x	1V8	
TP31	x		1V8_LPDDR5	
TP32		x	1V8_LPDDR5	
TP33	x		1V5	
TP34		x	1V5	
TP35	x		1V5_A	
TP36		x	1V5_A	
TP37	x		1V2	
TP38		x	1V2	
TP39	x		1V2_A	
TP40		x	1V2_A	

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Test Point	REV01			
	Top	Bottom	Signal	Notes
TP41	x		1V1	
TP42		x	1V1	
TP43	x		1V0XX_LPDDR5	
TP44		x	1V0XX_LPDDR5	
TP45	x		1V0	
TP46		x	1V0	
TP47	x		0V92	
TP48		x	0V92	
TP49	x		0V8_VCCRAM	
TP50		x	0V8_VCCRAM	
TP51	x		VCC_LPD	
TP52		x	VCC_LPD	
TP53	x		VCC_FPD	
TP54		x	VCC_FPD	
TP55	x		VCC_SOC	
TP56		x	VCC_SOC	
TP57	x		VCCINT	

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Test Point	REV01			
	Top	Bottom	Signal	Notes
TP58		x	VCCINT	
TP59	x		VCC_AIE	
TP60		x	VCC_AIE	
TP61	x		0V5_LPDDR5	
TP62		x	0V5_LPDDR5	
TP63	x		VCC_BATT	
TP64		x	VCC_BATT	
TP65	x		O2	
TP66	x		O1	
TP67	x		O3	
TP68	x		SEL	
TP69	x		CON_DET	
TP70	x		F_UART_TX	
TP71	x		F_UART_RX	
TP72	x		FAULT_n	

Table 3: Test points information

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6 On-board Peripherals

Chip / Interface	Designator	Connected to	Notes
SoC	U1	• QSPI Flash U5 • LPDDR5 U2, U3, U4 • UFS storage U15 • MicroSD socket J15 • M.2 M key PCIe x2 socket U19 • Ethernet PHYs U24, U28 • zSFP+ slot J5 • USB 3.x port controller U14 • USB 2.0/OTG PHY U31 • USB 2.0 to JTAG/UART bridge U49 • USB type C for data and DisplayPort J2 • PCIe common OSC U22 • Programmable PLL U42 • I2C switch U45 • I2C / SMBUS switch U56 • CAN transceivers U40, U41 • Oscillators U7, U8 • 4x user definable LEDs D1, D2, D3, D4 • CRUVI GTX - with LS / HS and GTX [1)] signals J9 • CRUVI GTX - with LS and HS signals J10 • 2x / 4x [1)] FFC/FPC connectors for CSI/DSI/ MIPI J11, J12, J13 [1)], J14 [1)] • Pmods [1)] J21, J22 • User buttons S3, S5 and S4, S5 • 2x DIP switches user definable S1 • 4x DIP switches boot mode S7 • Jumper SoC FUSE Programming voltage J4	
QSPI Flash	U5	• SoC U1	

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Chip / Interface	Designator	Connected to	Notes
LPDDR5	U2, U3, U4	• SoC U1	
UFS storage	U15	• SoC U1 • Clock Buffer U17 / Oscillator U18	
µSD socket	J15	• SoC U1 • Power regulator U36 • SDIO level shifter U37	
USB 3.x port controller	U14	• SoC U1 bank GTR 504 • 2x4 pin header - I2C signals and voltage select J3 • USB Type C J2	
Ethernet PHYs	U24 / U28	• SoC U1 • Oscillator U26 • RJ45 magnetic jack J6, J7	
USB 2.0/OTG PHY	U31	• SoC U1 • Oscillator U32 • VBUS current limiting switch U33 • USB Type C J8	
USB 2.0 to JTAG/UART bridge	U49	• EEPROM U51 • Oscillator U52 • Level shifter U10 / SoC U1 bank 503 (JTAG) • Level shifter U50 / SoC U1 bank 501 (UART) • LEDs UART activity D18, D19 • LED 3V3_VDD_FTDI D20 • USB 3.x Type C J24	
EEPROM	U6	• I2C	

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Chip / Interface	Designator	Connected to	Notes
EEPROM with MAC	U23 / U25 / U29	• I2C	
EEPROM for programmer	U51	• USB 2.0 to JTAG/UART bridge U49	

Programmable PLL	U42	• SoC U1:
		  • Bank X5IO 702
		  • Bank 507
		  • Bank GTR 504
		  • Bank GTYP 105
		  • Bank GTYP 203/205 [2)]
		  • Bank X5IO 707/709 [2)]
			156¼ MHz
			26 MHz
			24 MHz
			156¼ MHz
			156¼ MHz
			156¼ MHz

PCIe common OSC	U22	• SoC U1 GTYP bank 105 • M.2 m key socket U19	Both 100 MHz
Oscillator	U52	• Programmable PLL U42 • USB 2.0 to JTAG/UART bridge U49	12 MHz
Oscillator	U43	• Programmable PLL U42	24 MHz
Oscillator	U18	• Clock Buffer U17 / UFS storage U15	26 MHz
Oscillator	U7	• SoC bank 500	26 MHz
Oscillator	U8	• SoC U1 bank 503	33⅓ MHz
Oscillator	U32	• USB 2.0 PHY U31	52 MHz
Oscillator	U26	• ETH PHYs U24/U28	25 MHz

Table 4: On-board peripherals

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Notes

[1] Only on SoC 35xx variants

[2] Bank number SoC variant dependent. 33xx / 35xx

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7 Configuration and System Control Signals

Control signals represent hardware defined logic states, for final state consider the firmware and reference designs.

7.1 Control Signals and Buses

Signal Name	Connector.Pin	Direction [1)]	Description
GTX_EN_EXT_PWR	J9.D14	OUT	External IO device power enable signal.
GTX_PG_EXT_PWR	J9.D15	IN	External IO device power good signal.
GTX_RFU1 / GTX_RFU2	J9.D16 / J9.C18	-	Reserved for future use. - Can be used as IO.
GTX_EN_EXT_PWR	J10.D14	OUT	External IO device power enable signal.
GTX_PG_EXT_PWR	J10.D15	IN	External IO device power good signal.
GTX_RFU1 / GTX_RFU2	J10.D16 / J10.C18	-	Reserved for future use. - Can be used as IO.
CAN (CAN0_N / CAN0_P)	J16.3 / J16.4	INOUT	
CAN (CAN1_N / CAN1_P)	J17.3 / J17.4	INOUT	
I2C (PLL_I2C_SDA/ I2C3_SDA / PLL_I2C_SCL/ I2C3_SCL)	J20.3 / J20.1	Signal dependent	Pay attention to REV01 patch.
I2C (I2C2_SDA / I2C2_SCL)	J3.4 / J3.2	Signal dependent	

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Signal Name	Connector.Pin	Direction [1)]	Description
I2C (GTX_SDA_LS / GTX_SCL_LS)	J9.C20 / J9.C19	Signal dependent	
I2C (CSI1_SDA / CSI1_SCL)	J11.2 / J11.3	Signal dependent	
I2C (CSI2_SDA / CSI2_SCL)	J12.2 / J12.3	Signal dependent	
I2C (CSI3_SDA / CSI3_SCL)	J13.2 / J13.3	Signal dependent	
I2C (CSI4_SDA / CSI4_SCL)	J14.2 / J14.3	Signal dependent	
LEDs (USER_LED1 / USER_LED2 / USER_LED3 / USER_LED4) / D1, D2, D3, D4	-	OUT	User definable, green
LED (USB1_OC_n) / D9	-	OUT	USB J8 bus over current signal, red.
LED (3V3_VDD_FTDI) / D20	-	OUT	Power indication LED, green.
LEDs (F_UART_RX_LED / F_UART_TX_LED) / D18, D19	-	OUT	Receive / Transmit indication LEDs, green
LED (12V0) / D22	-	OUT	Board Main Power Indication LED, green.
LED (ERROR_OUT) / D5	-	OUT	SoC Error State Indication LED, red.
LED (DONE) / D6	-	OUT	SoC Boot Indication LED, green.

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Signal Name	Connector.Pin	Direction [1)]	Description
LED (POR_B_n) / D7	-	OUT	Power-On Reset Indication LED, green.
LED (M2_LED) / D8	-	OUT	M.2 Activity Indication LED, green.

Table 5: Control signals and buses

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.
- INOUT: Bidirectional signal.
- Signal dependent: The signal direction depends on the function within the bus.

7.2 Jumpers

Jumper header	Net name / Connector.pin		
	Output	Input	Notes
J3	I2C_V / J3.3		Set I2C bus I2C2 voltage.
		1V8 / J3.1	Set I2C2 bus voltage to 1.8 V.
		3V3_PS / J3.5	Set I2C2 bus voltage to 3.3 V.
J4	VCC_FUSE / J4.2		Set the SoC voltage for eFUSE programming.
		1V8 / J4.1	Enable eFUSE programming.
		GND / J4.3	Disable eFUSE programming.
J18	CAN0_N / J18.3		Set CAN termination for signal CAN0_N.
		No net name / J18.1	Connect to termination.

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Jumper header	Net name / Connector.pin		
	Output	Input	Notes
	CAN0_P / J18.4		Set CAN termination fro signal CAN0_P.
		No net name / J18.2	Connect to termination.
J19	CAN1_N / J19.3		Set CAN termination for signal CAN1_N.
		No net name / J19.1	Connect to termination.
	CAN1_P / J19.4		Set CAN termination for signal CAN1_P.
		No net name / J19.2	Connect to termination.

Table 6: Jumpers

7.3 Buttons

		Voltage level		
Button	**Signal**	**Low**	**high**	**Function**
S3/S4	USER_PB1	pressed	unpressed	User definable.
S5/S6	USER_PB2	pressed	unpressed	User definable.

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		Voltage level		
Button	**Signal**	**Low**	**high**	**Function**
S8	TPM_PP	unpressed	pressed	Trusted platform module 2.0 presence detection.
S10/S11	MR_RC_n	pressed	unpressed	Manuel board reset.

Table 7: Buttons

7.4 DIP Switches

DIP switch group	DIP switch	Signal name / Connector.pin	Description
S1	S1A	PWR_OFF / S1.8	Disable module / assert U55 (Input protection) state.
	S1B	USER_DIP2 / S1.7	S1B is parallel to S2B. S1C is parallel to S2A. User definable.
	S1C	USER_DIP1 / S1.6	
	S1D	No net name / S1.5	Not connected / No function.
S2	S2A	USER_DIP1 / S2.4	S1B is parallel to S2B. S1C is parallel to S2A. User definable. S2 intended for enclosure usage.
	S2B	USER_DIP2 / S2.3	
S7	S7A	BOOT_SEL0# / S7.1	Select SoC boot mode.
	S7B	BOOT_SEL1# / S7.2	
	S7C	BOOT_SEL2# / S7.3	

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DIP switch group	DIP switch	Signal name / Connector.pin	Description
	S7D	BOOT_SEL3# / S7.4	
S9	S9A	PWR_OFF / S9.4	Disable module / assert U55 (Input protection) state. S1A is parallel to S9A. S9A intended for enclosure usage.
	S9B	No net name / S9.3	Not connected / No function.

Table 8: DIP switches

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8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name / Schematic Name	Description	Connector.Pin	Direction 1)	Notes
12V0_in / 12V_IN_FUSED	Board Power Supply	J25.1 / J25.2 / J25.3	IN	Pay attention to connector pinout!
VBATT	Backup supply (CR1220 / 3.0 Lithium) for SoC RTC	B1	IN	
12V0_FAN	Supply for 12 V PWM fan.	J23.2	OUT	
3V3_PL	3.3 V for external IO devices/reference voltage.	J1.33 / J1.34 2) J11.1 / J12.1 J13.1 / J14.1 2) J21.6 / J21.12 / J22.6 / J22.12 2)	OUT	
3V3_PS	3.3 V for external IO devices/reference voltage.	J3.5 / J20.4	OUT	Dependent on resistor R259 assembly.

Table 9: Power rails

Notes

1) Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

2) Only on SoC 35xx variants.

8.2 Recommended Power up Sequencing

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Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals.
1	12V0_IN	12.0 V (± 5 %)	-	Power supply.	Carrier power supply.
2	PWR_OFF	-	-	Release signal Power_OFF via DIP switch S1A or S9A.	

Table 10: Power sequencing

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9 Board to Board Connectors

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10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Warning!
The listed values ONLY reflect this board. Connected Carriers / SoMs / Boards are not considered.

Power Rail Name / Schematic Name	Description	Min	Max	Unit	Notes
12V0_IN / 12V_IN_FUSED	Board Power Supply.	-0.3	50	V	
VBATT	Backup supply for SoC RTC.	–0.3	6.3	V	

Table 11: Absolute maximum ratings

*) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Condition". Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

10.2.1 Temperature range

Trenz Electronic classifies modules into temperature range categories by subsumption of its component data (PCB, ICs, connectors, passive components). The temperature ranges are values for ambient air temperature and do not reflect the junction temperature of individual components.

The categories are:

- Modules with commercial (C) temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 70 °C.
- Modules with extended (E) temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 85 °C.
- Modules with industrial (I) temperature grade are equipped with components that cover at least the ambient temperature range of -40 °C to 85 °C.

These categories do not take into account the entire custom system consisting of:

- Customer SoC design. The allowed main SoC temperature range is specified from the vendor by junction temperature using corresponding classes (C, E, I). See vendor documentation.
- Cooling solution, active and or passive cooling.
- Climate or environmental conditions besides ambient temperature range.
- Module orientation, neighbouring assemblies, neither other heat sources nor the SoC as heat source to other components.

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Classification of the module can be looked up here: Article Number Information i.e.: TExxxx-xx-xx'I'xx, the 'I' indicates that all components are at least in Industrial temperature class.

The temperature of individual components should not exceed the specified range due to self-heating or heating by adjacent components. The actual operating temperature range will depend on the customer design, usage, environment and cooling solution. Consult Cooling Solutions for more information.

10.2.2 Voltage rails

The following table aims to be generic for all variants. The voltage ranges are consistent across assembly variants, but exceptions are possible (custom request).

Power Rail Name / Schematic Name	Min	Max	Units	Notes
12V0_IN / 12V_IN_FUSED	11.4	12.6	V	
VBATT	-	3.0	V	

Table 12: Recommended operating conditions

10.3 Physical Dimensions

- Module size: 150.0 mm x 200.0 mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 2.1 mm ±10 %.

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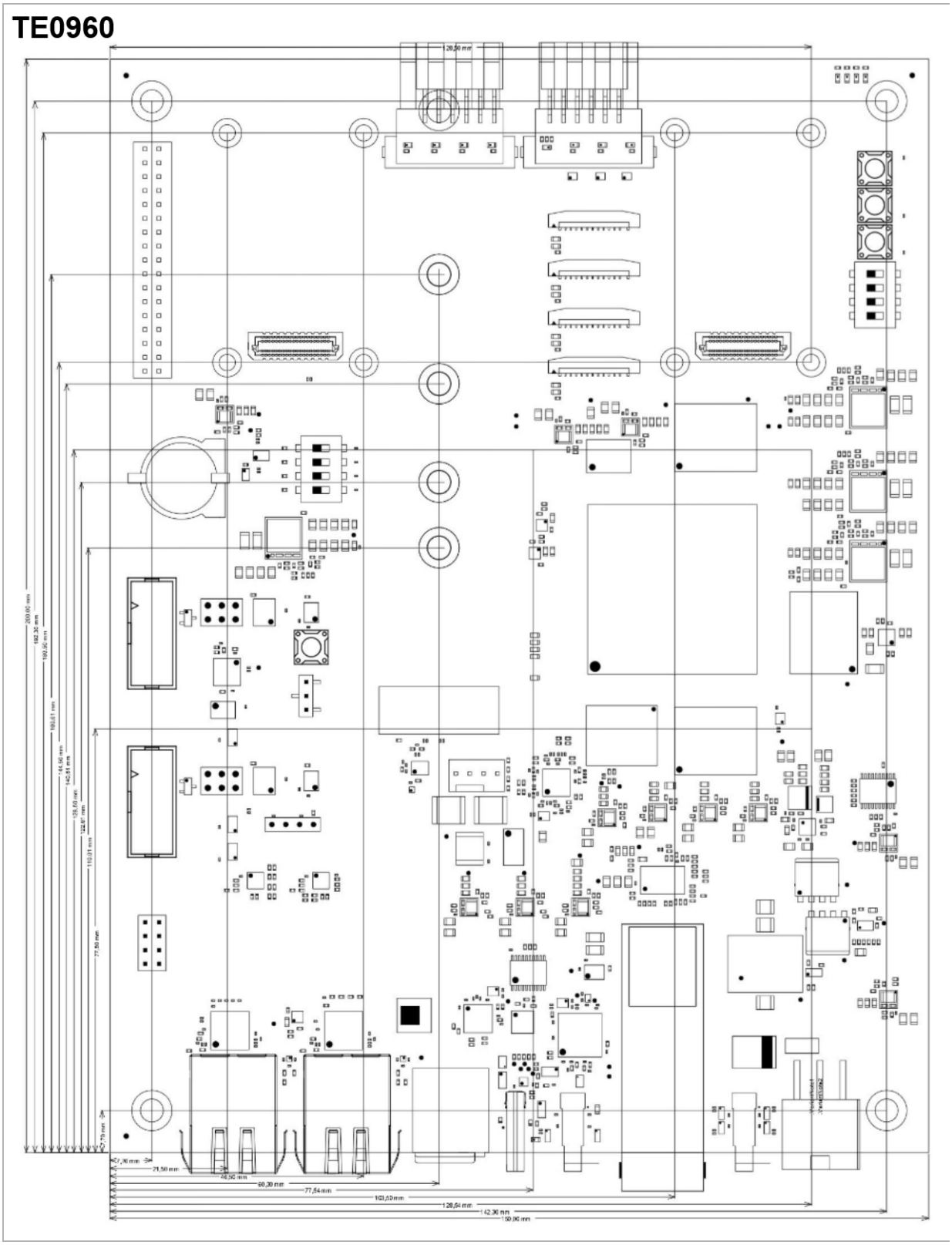


Figure 3: Physical dimension

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11 Currently Offered Variants

Trenz shop TE0960 overview page *	
English page	German page

Table 13: Trenz Electronic shop overview
*) Module article name encoding table: AMD Versal based modules

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12 Revision History

12.1 Hardware Revision History

The hardware revision number can be found on the PCB board together with the module's model number, separated by a dash.

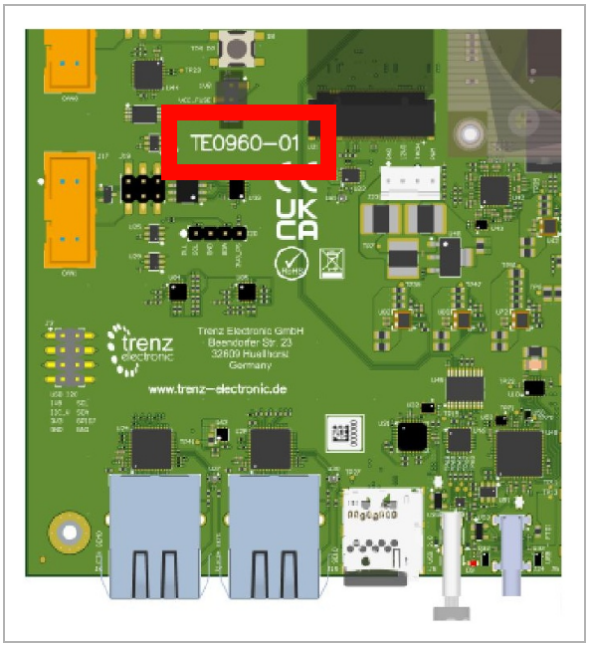


Figure 4: Board hardware revision number

Date	Revision	Changes	Documentation Link
2026-09	01	Initial Release	REV01

Table 14: Hardware revision history

12.2 Document Change History

Date	Revision	Contributor	Description
2026-11-13	v.32	Kilian Jahn	• Initial Release
--	all	ED , Kilian Jahn	• --

Table 15: Document change history

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2025-08-01

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