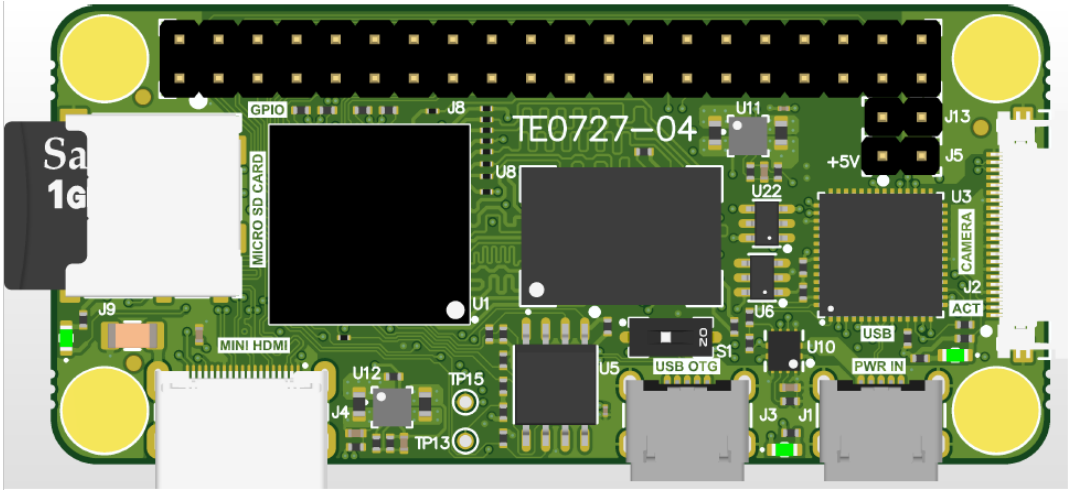

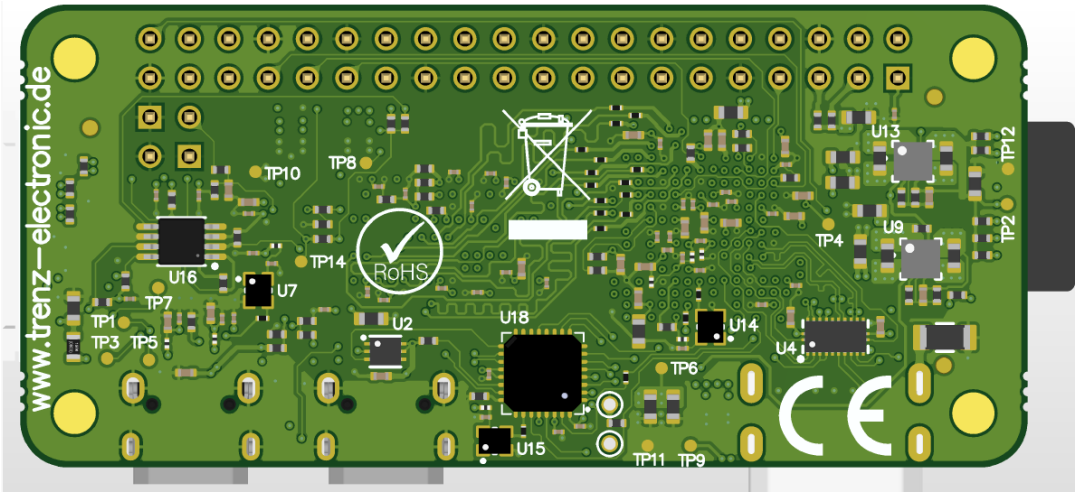

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0727 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices		
	A4	Number: TE0727 41C38	Rev. 04
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REV	Description	
-01	Initial revision	
-02	1) Fixed I2C connection, added I2C MUX (U16) 2) Added optional pin-header connector for select JTAG boot mode 3) Added 2x user LEDs 4) Changed obsolete DDR3 chip 5) Fixed wrong type connector for CSI 6) full update lib	
-03	1. EOL components U11 , U12 (EP53A7LQI), U9 , U13 (EP53A7HQI) were replaced by MPM3834CGPA; 2. EOL component U16 (PCA9540BGD,125) was replaced by PCA9540BDP,118; 3. EOL components L1 - L7, L10 BKP0603HS121-T replaced by MPZ0603S121HT000. 4. Added S1 switch and R53 for "JTAG only mode" enable; 5. The signals were renamed: - SPI-DQ0/M0 ---> SPI-DQ0/M3, - SPI-DQ3/M3 ---> SPI-DQ3/M0 according to AMD Table 6-4; 6. Power supply rail of Bank 35 was changed from 1.8V to 3.3V; 7. Added decoupling capacitors C52, C53, C73, C85 according to AMD specification (UG 933); 8. The capacitors were replaced: - C7, C16, C54, C71, C93: 47µF (0805) ---> 47µF (0603), - C1, C4, C12, C15, C18, C19, C24, C35, C57, C63, C65, C79, C81, C87, C89 4.7µF (0402)---> 10µF (0402), - C29, C32, C33, C41, C42, C43, C44, C47: 10µF (0402) ---> 22µF (0603); 9. Capasitor C86 replaced by 47µF (was 10µF); 10. Added power diagram; 11. Added Block diagramm; 12. Added TestPoints TP16, TP17, TP18; 13. J5 and J13 connectors are polarity changed.	VG (23.05.2023)
-04	1. J5 and J13 connectors changed back; 2. Power Supply Sequencing was changed according to DS187; 3. Test points TP16, TP17, TP18 removed; 4. U10 Current limit changed 1.24A → 2.037A, R28 replaced by 56K (was 100K); 5. U7(SiT8008AI-73-XXS-12.000000E) replaced by SiT8008BI-73-XXS-12.000000E; 6. U14(SiT8008AI-73-XXS-33.333333E) replaced by SiT8008BI-73-XXS-33.333333E; 7. U15 (SiT8008AI-73-XXS-52.000000E) replaced by SiT8008BI-73-XXS-52.000000E; 8. Green LEDs D1, D2, D3 replaced by 19-213/G6C-BM1N2/DT; 9. The capacitors were replaced: - C51: 470nF ---> 10µF; - C55, C56: 470nF ---> 47µF; 10. The capacitors C13, C25 (0805) replaced by (0402) (BOM optimisation); 11. Added resistor R140 according to UG933.	VG (30.04.2024)
	12. U5 is EOL and replaced by S25FL128LAGMFI013 (created new assembly variant).	VG (22.07.2024)
	13. Digilent License has been removed. 14. J2 ZIF FPC 54548-2271 is EOL and replaced with 687122183722 in assembly variant.	VG (04.03.2026)

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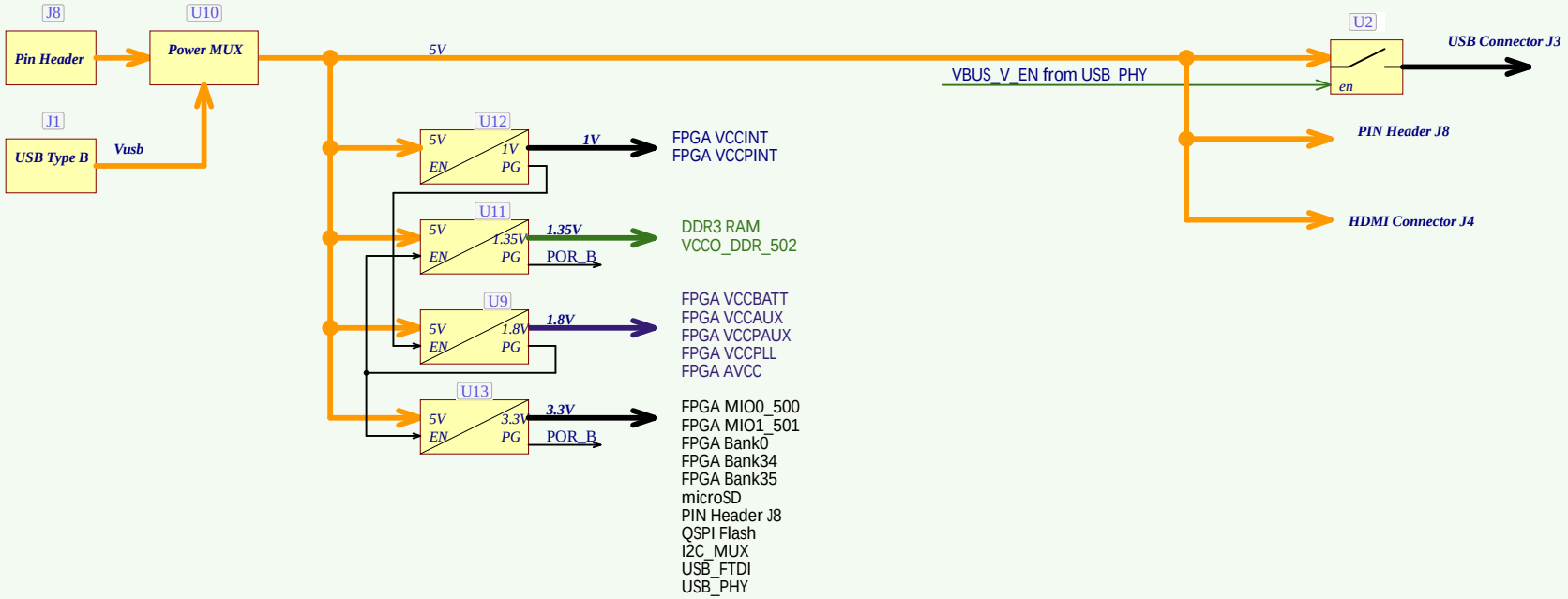
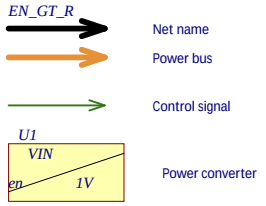
Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V	OUT	5V	+/-5%	Micromodule Power	-
USB_B_Vbus	IN	5V	+/-5%	Micromodule Power	-
USB_Vbus	IN	5V	+/-5%	Internal Power	-
3.3V	OUT	3.3V	+/-3%	Internal Power	-



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Title: Power_Diagram			
A4	Number: TE0727 41C38		Rev. 04
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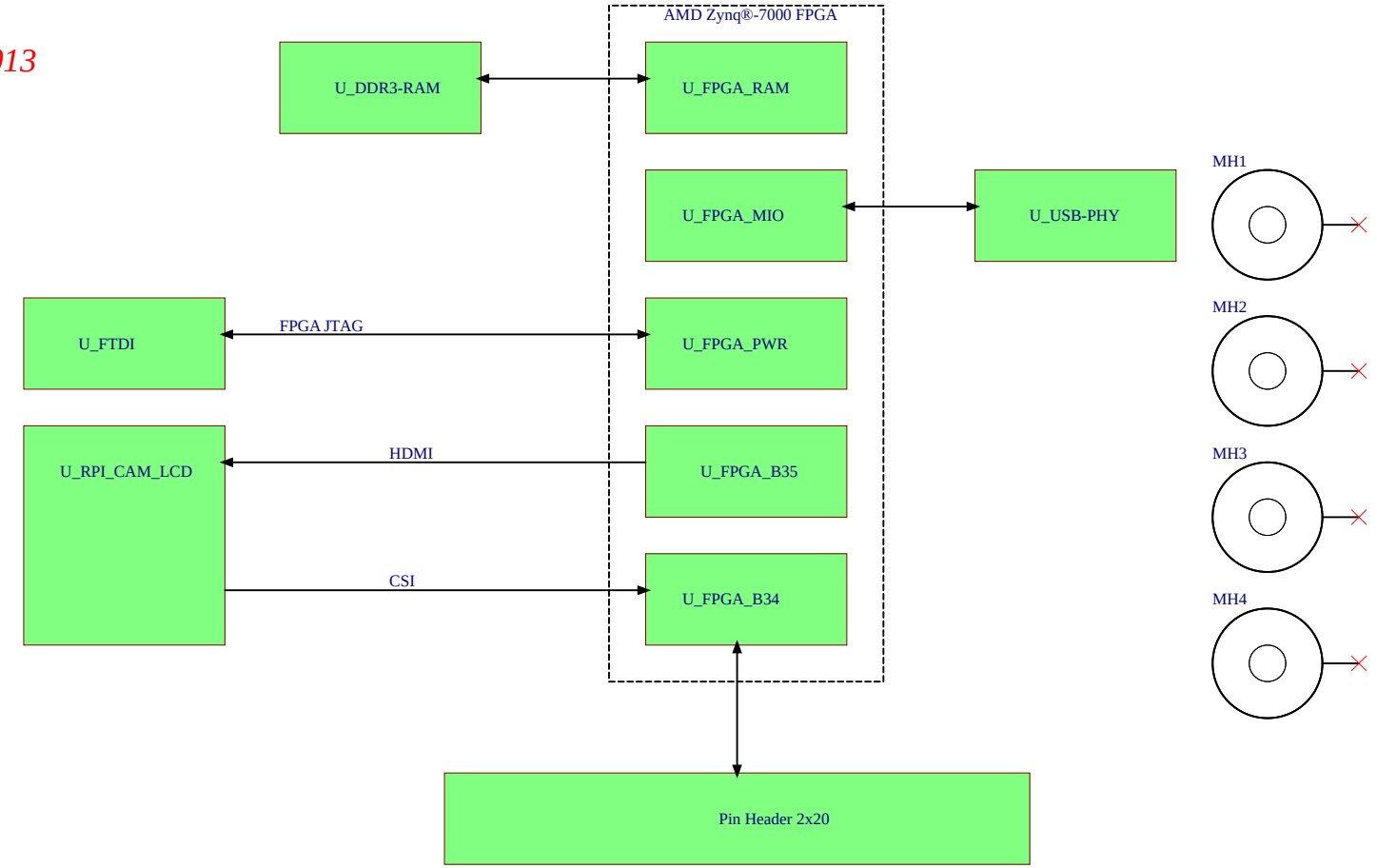
Special notes:

U5 replaced with S25FL128LAGMFI013



PM1 PM2 PM3

PM4 PM5 PM6

Serial
Serial
Serialnumber 6,3 x 6.3mm

U_PowerSupply

Drawn by	VG
Checked by	IG
Assembly variant	41C38
Created by	VG
Modified by	
Modified at	

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Title: Overview		
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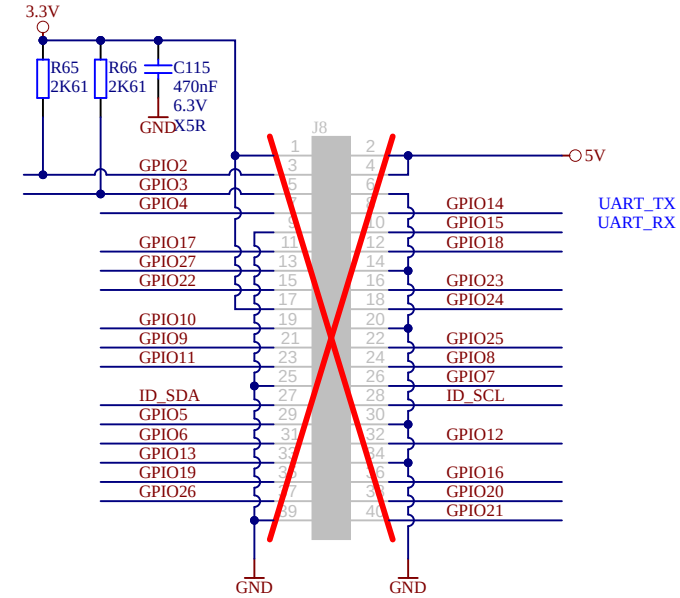

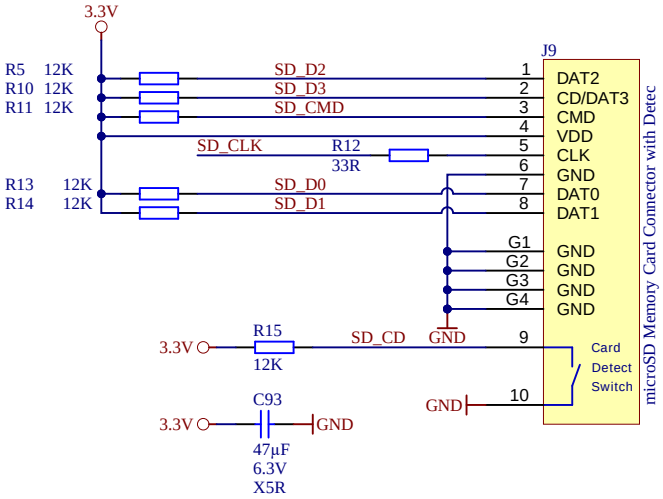

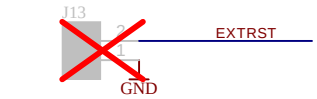

trenz electronic	Title: Connectors		
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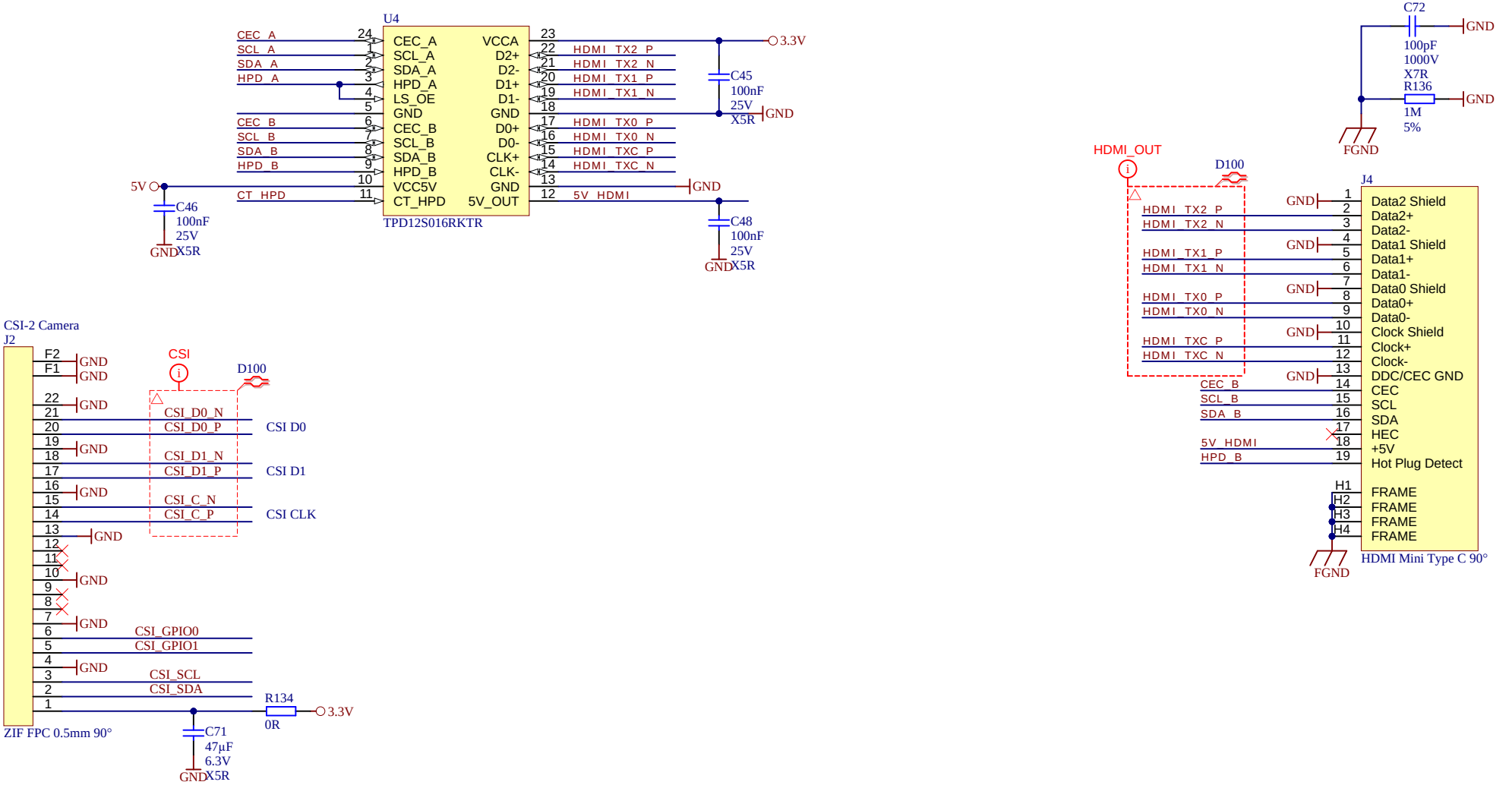
Filename: RPi-Headers.SchDoc			



trenz electronic	Title: Connectors		
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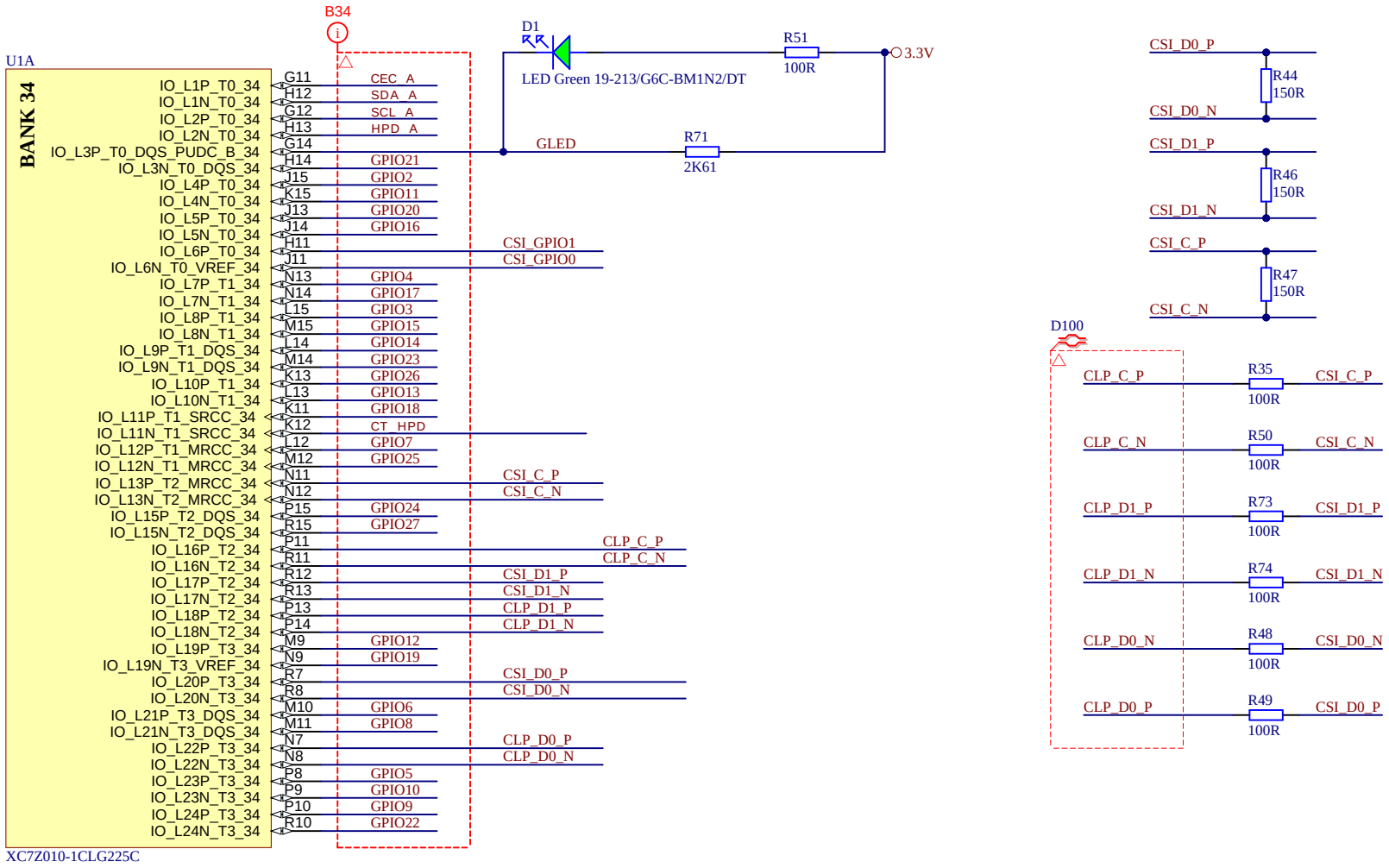
	Filename: RPi-CAM-LCD.SchDoc		



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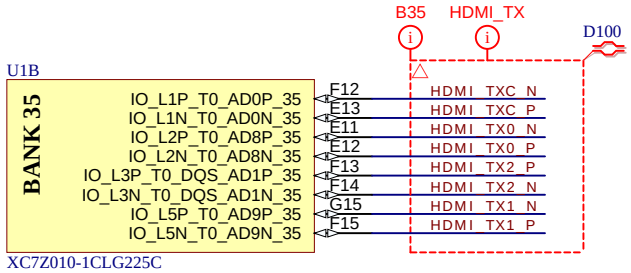
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page7 of 15
Filename: FPGA_B34.SchDoc			



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Title: FPGA B35			
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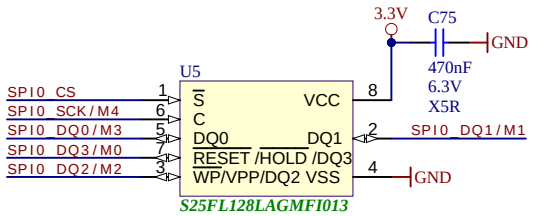
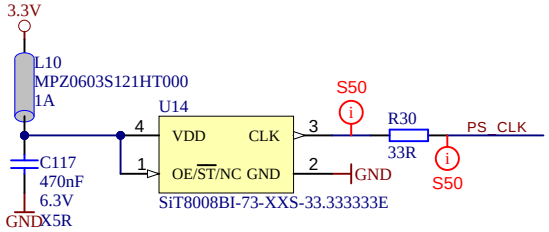
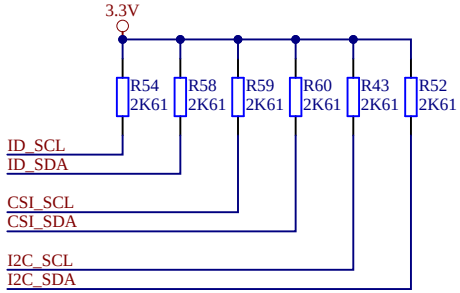
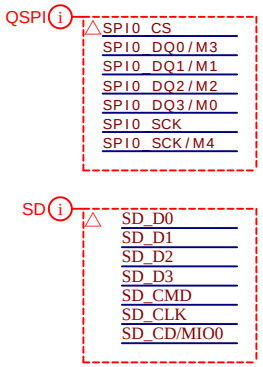
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page 8 of 15
Filename: FPGA_B35.SchDoc			









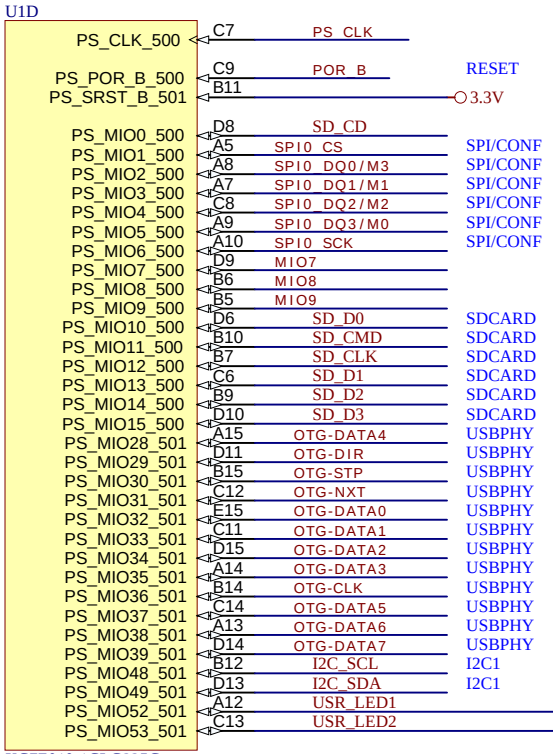
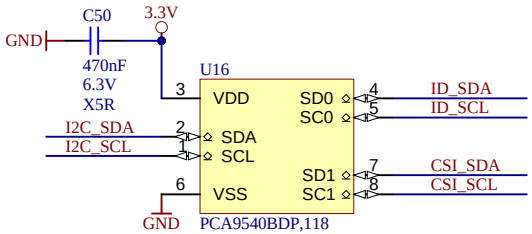
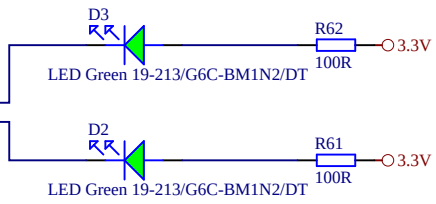
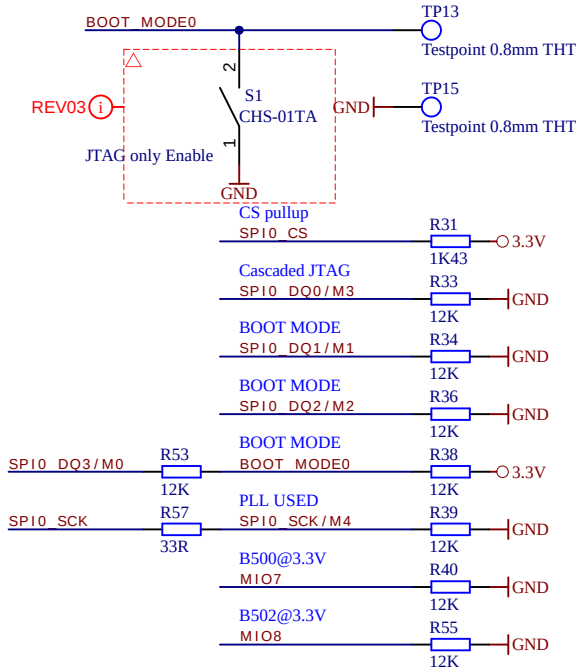


Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8] VMODE[1]	MIO[7] VMODE[0]	MIO[6] BOOT_MODE[4]	MIO[5] BOOT_MODE[0]	MIO[4] BOOT_MODE[2]	MIO[3] BOOT_MODE[1]	MIO[2] BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common[1]			0	0	0		
NOR Boot[3]			0	0	1		**JTAG Chain Routing**[2]
NAND			0	1	0		0: Cascade mode
Quad-SPI[3]			1	0	0		1: Independent mode
SD Card			1	1	0		







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Title: FPGA MIO			
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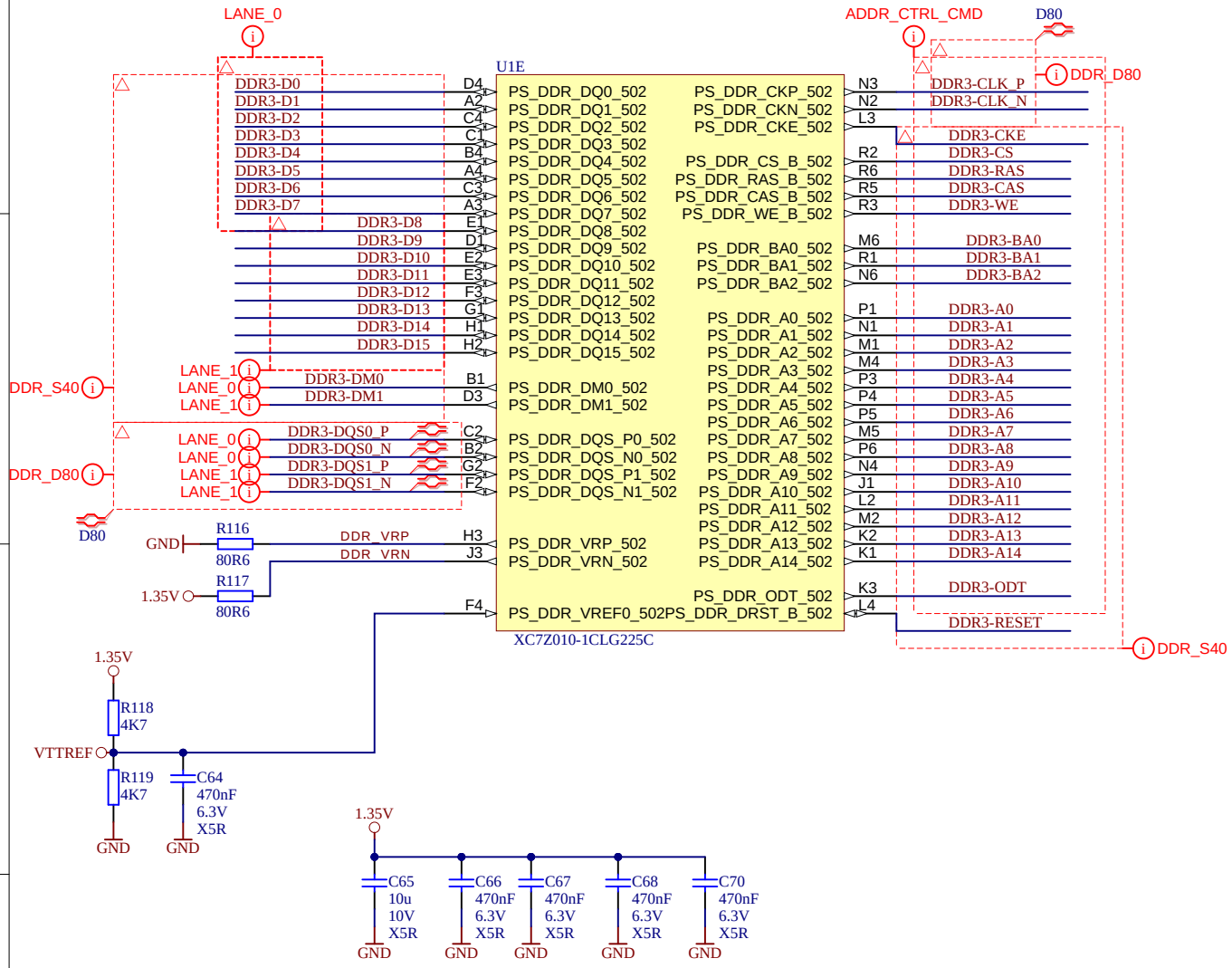
Filename: FPGA_MIO.SchDoc			



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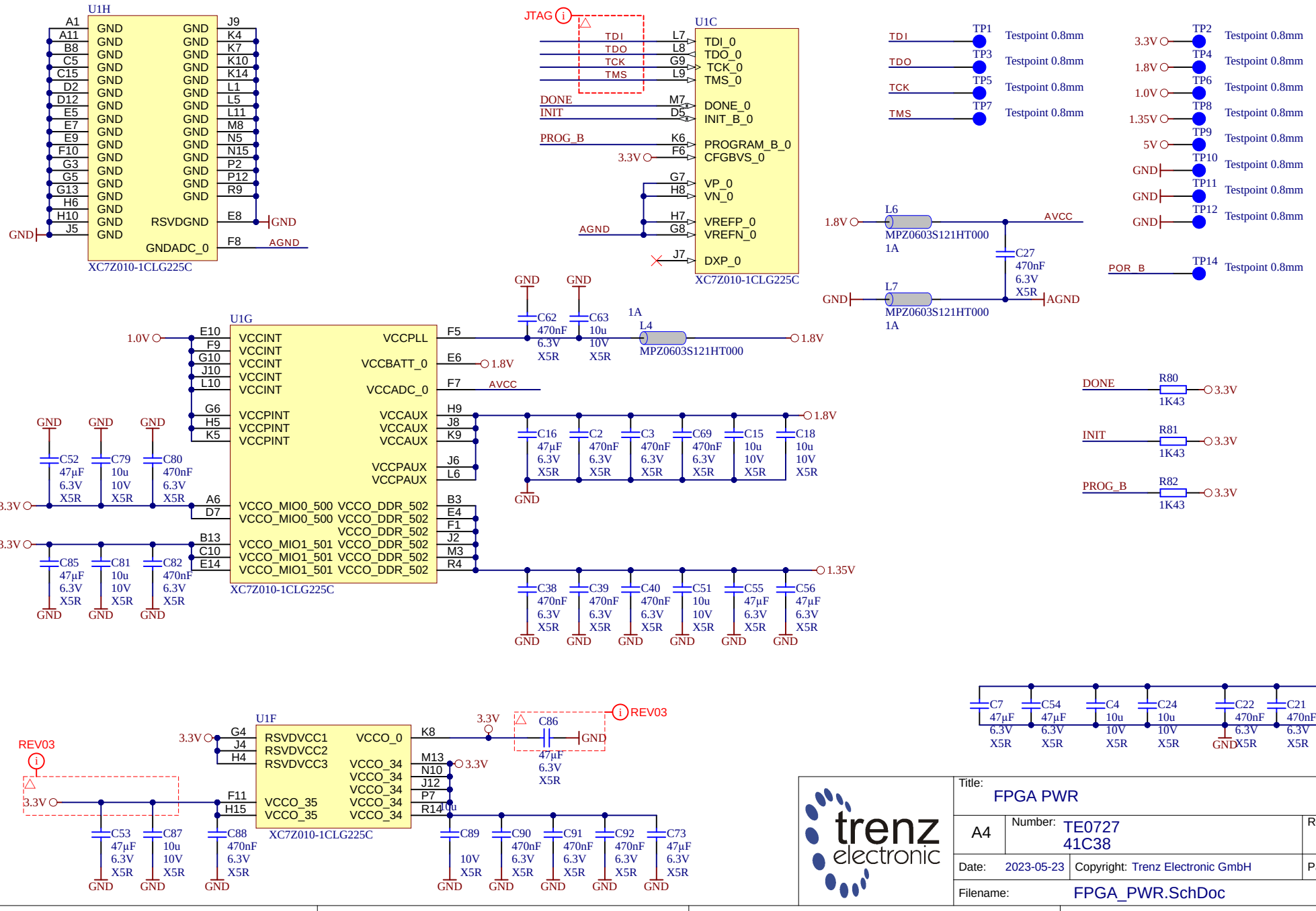
	Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page10 of 15
	Filename: FPGA_RAM.SchDoc		


U1H
XC7Z010-1CLG225C
U1C
XC7Z010-1CLG225C
JTAG
TDI
TDO
TCK
TMS
DONE
INIT
PROG_B
U1G
XC7Z010-1CLG225C
U1F
XC7Z010-1CLG225C
REV03
TP1 Testpoint 0.8mm
TP2 Testpoint 0.8mm
TP3 Testpoint 0.8mm
TP4 Testpoint 0.8mm
TP5 Testpoint 0.8mm
TP6 Testpoint 0.8mm
TP7 Testpoint 0.8mm
TP8 Testpoint 0.8mm
TP9 Testpoint 0.8mm
TP10 Testpoint 0.8mm
TP11 Testpoint 0.8mm
TP12 Testpoint 0.8mm
TP14 Testpoint 0.8mm
L6 MPZ0603S121HT000 1A
L7 MPZ0603S121HT000 1A
L4 MPZ0603S121HT000 1A
C27 470nF 6.3V X5R
R80 1K43
R81 1K43
R82 1K43
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Title: FPGA PWR
A4
Number: TE0727 41C38
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Date: 2023-05-23
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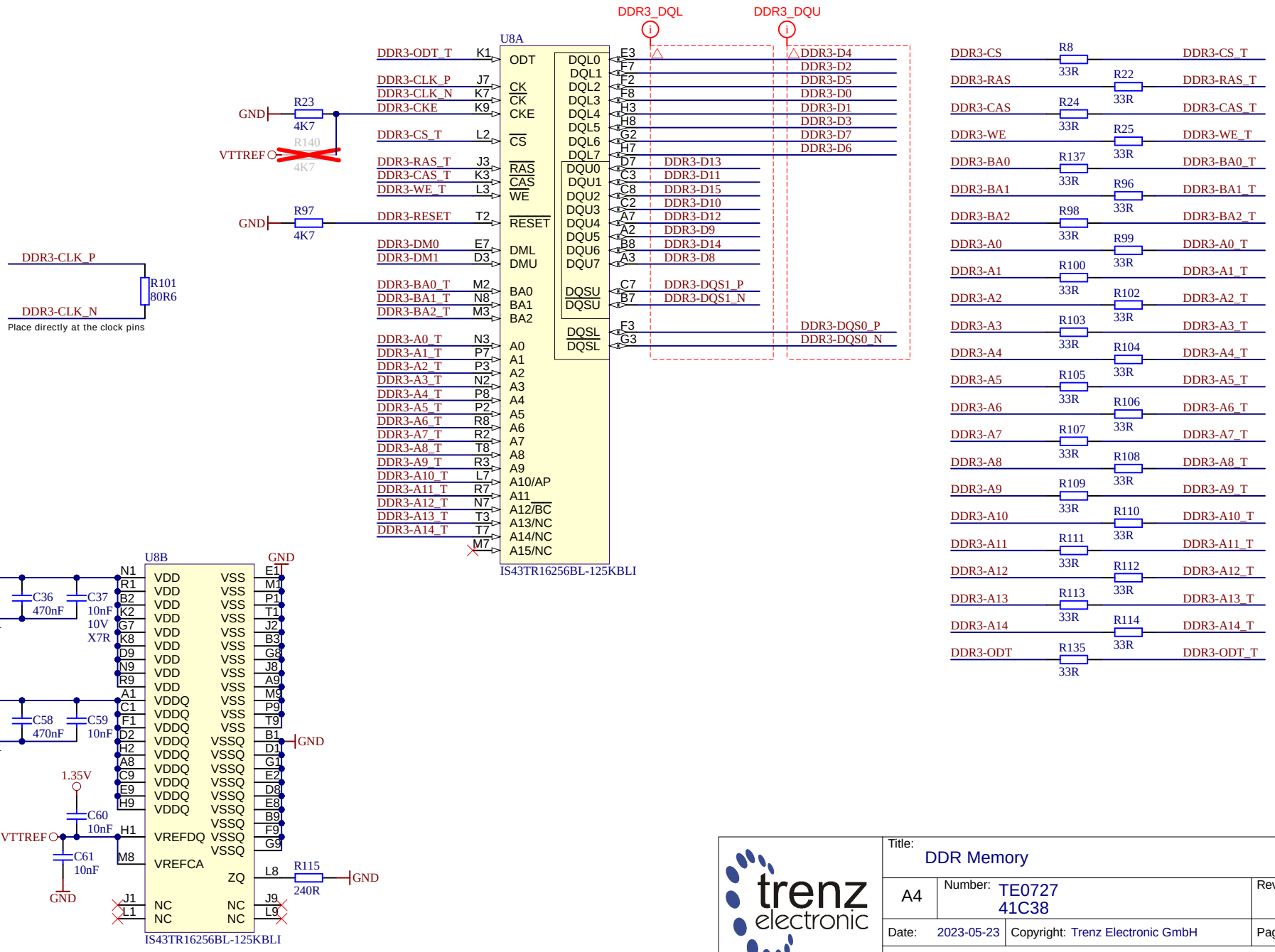
Filename: FPGA_PWR.SchDoc



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Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page12 of 15
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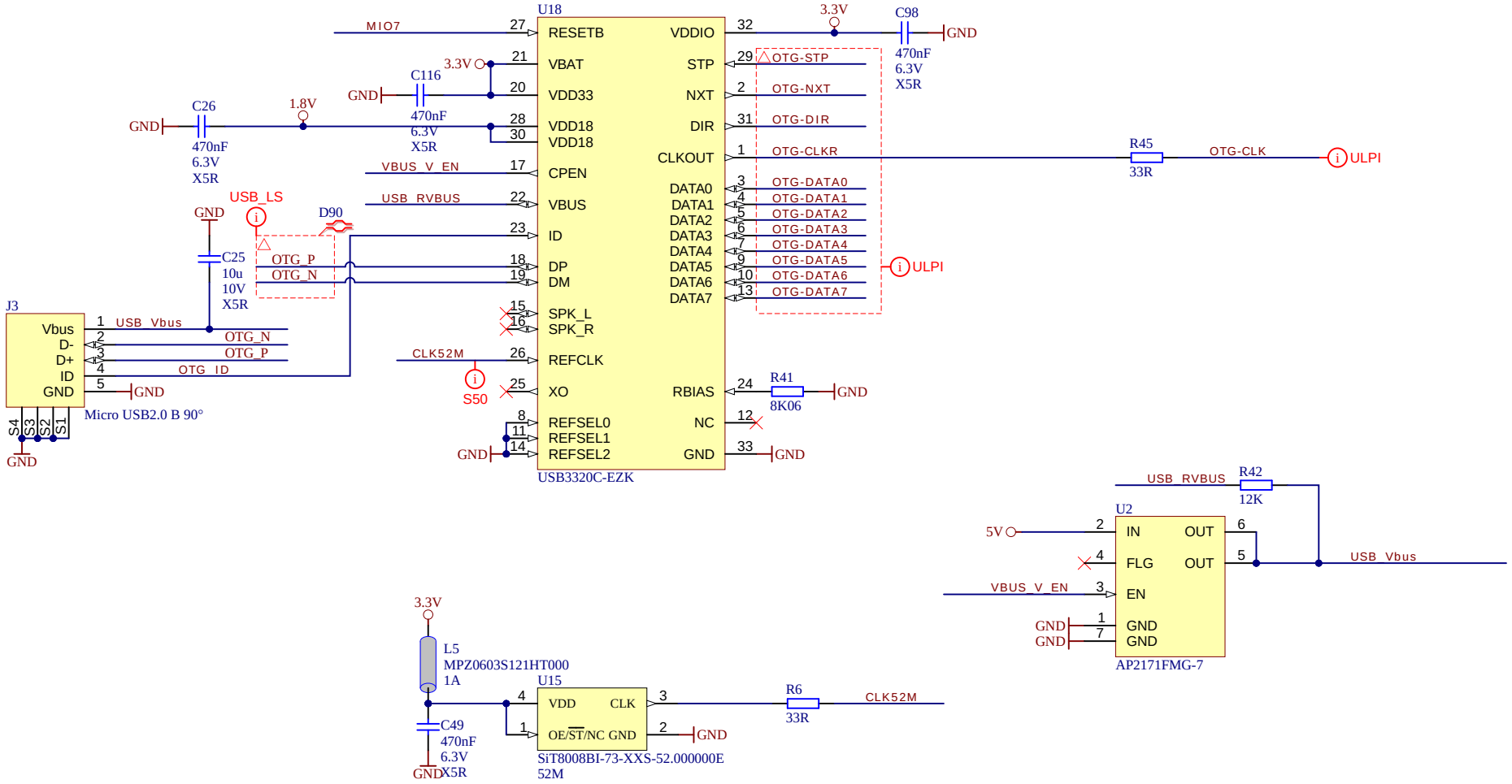

trenz electronic	Title: USB		
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	Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page13 of 15
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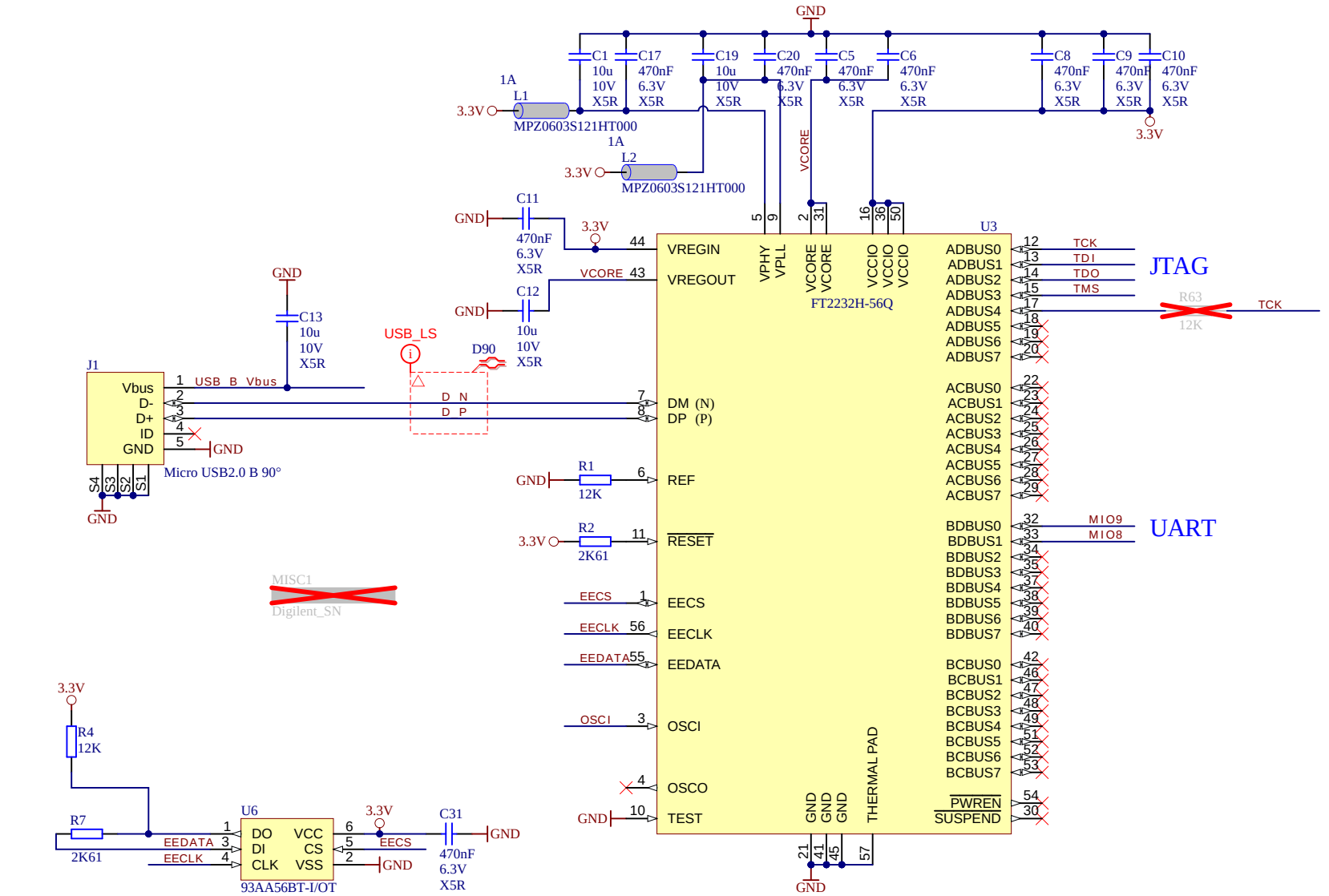

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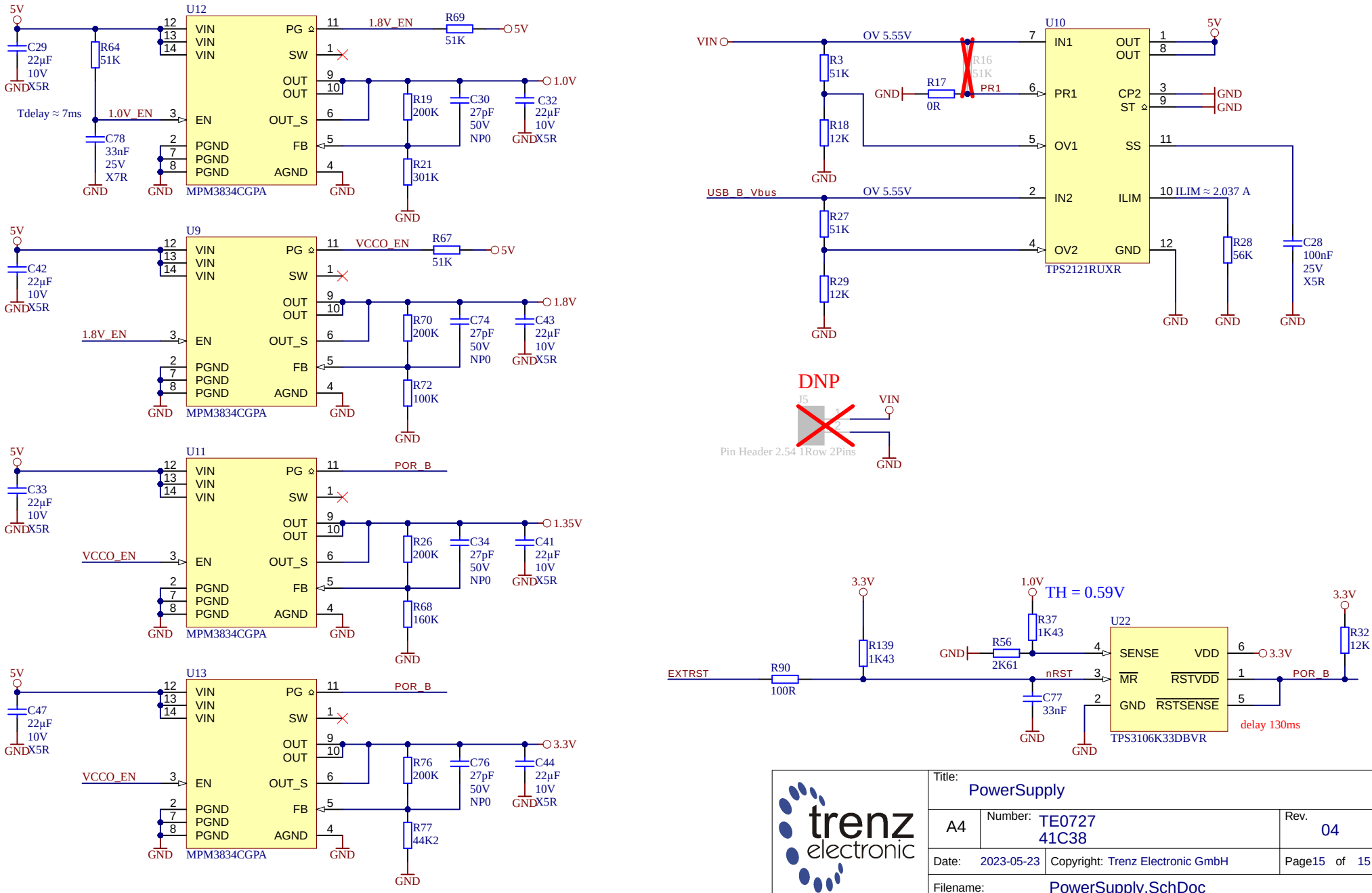
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page14 of 15
Filename: FTDI.SchDoc			



Title: PowerSupply			
A4	Number: TE0727 41C38		Rev. 04
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Filename: PowerSupply.SchDoc			