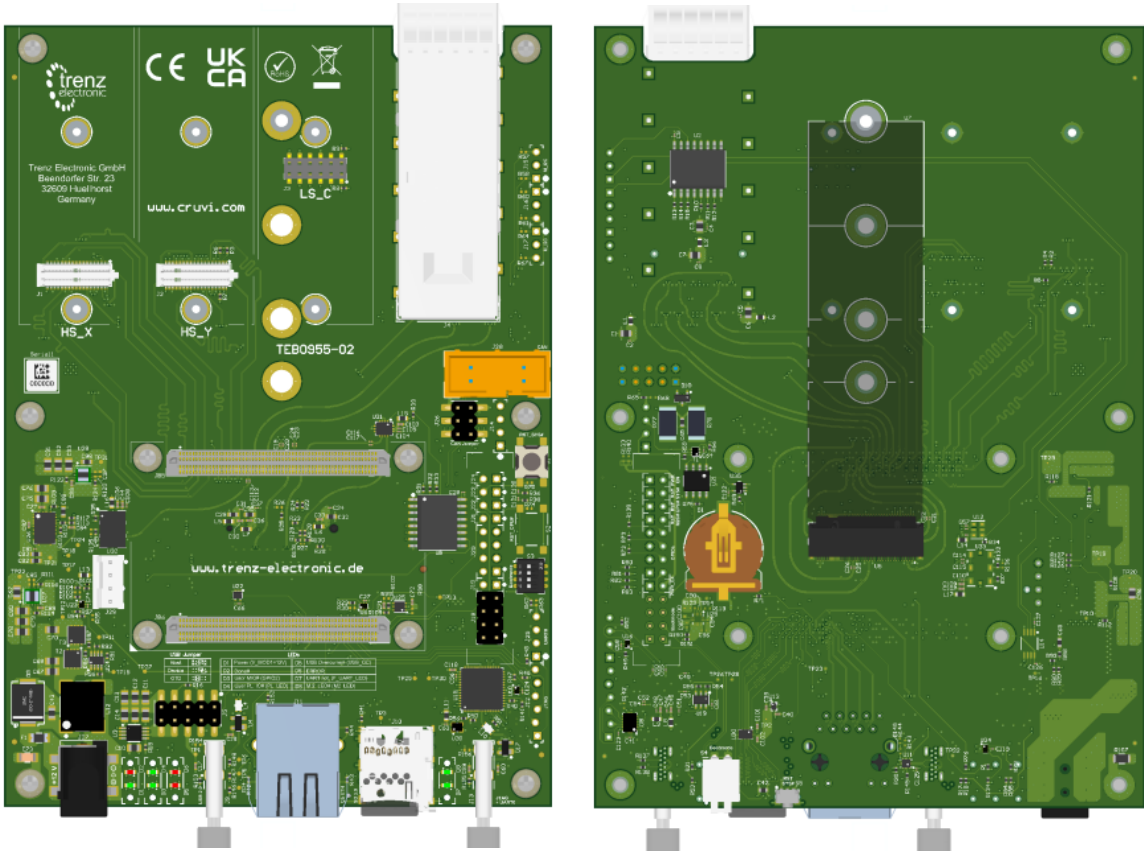




Pictures shows REV02 Variant A (default), other assembly variants may differ.

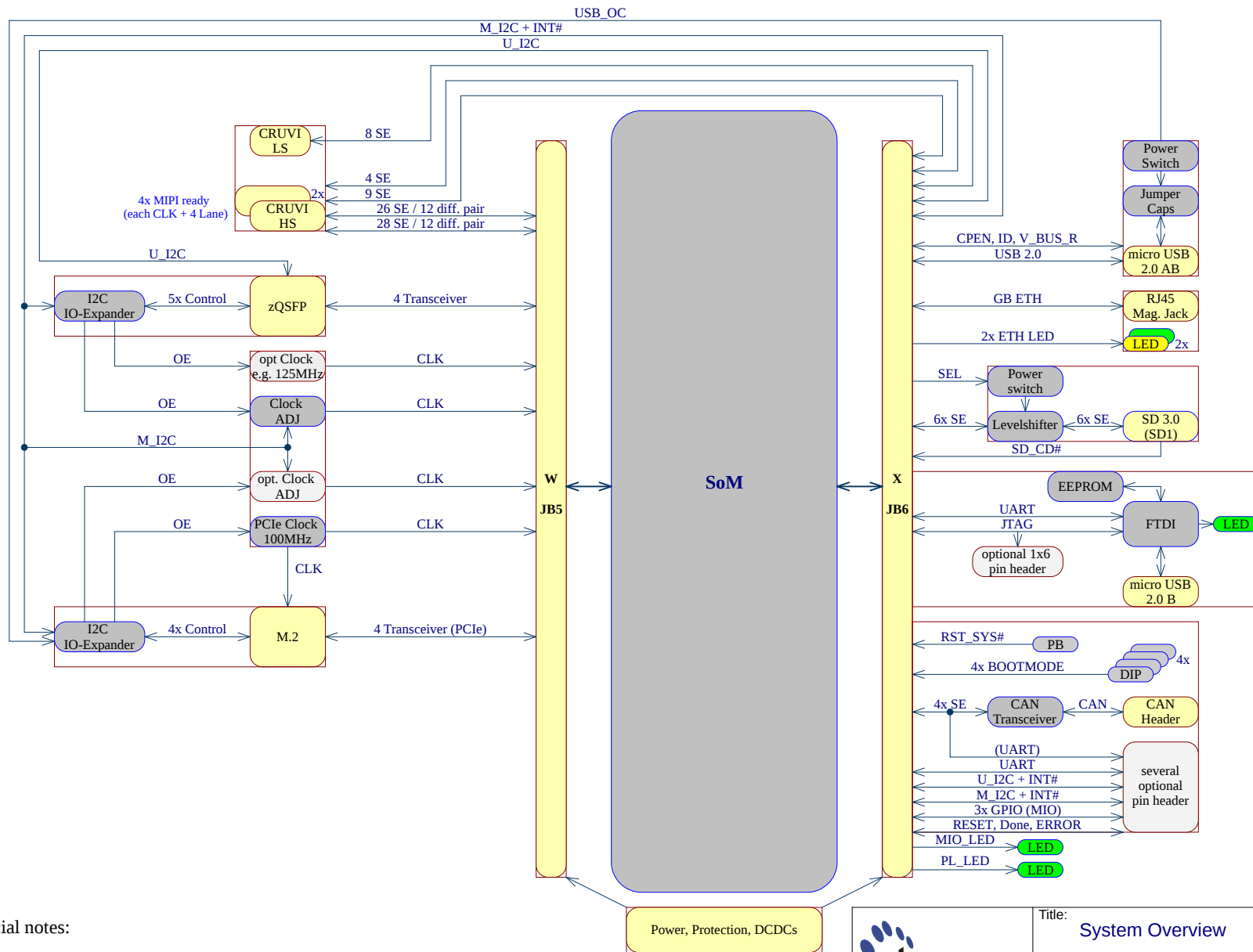
Regarding the usage of our schematics and alike documentation for Trenz baseboard TEB0955.

Baseboard is Open Source Hardware and therefore free to use, adapt and can be modified to suit your needs as described in the "The MIT License".

Permission is hereby granted, free of charge, to any person obtaining a copy of this hardware and associated documentation files (the "Product"), to deal in the Product without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Product, and to permit persons to whom the Product is furnished to do so.

Drawn by MR			Title: Legal Notices		
Checked by			A4	Number: TEB0955 A	Rev. 02
Assembly variant A			Date: 04.03.2026		
Created by MR			Copyright: Trenz Electronic GmbH		
Modified by MR			Page 1 of 18		
Modified at 2025-03-03			Filename: Legal Notices TEB0955.SchDoc		

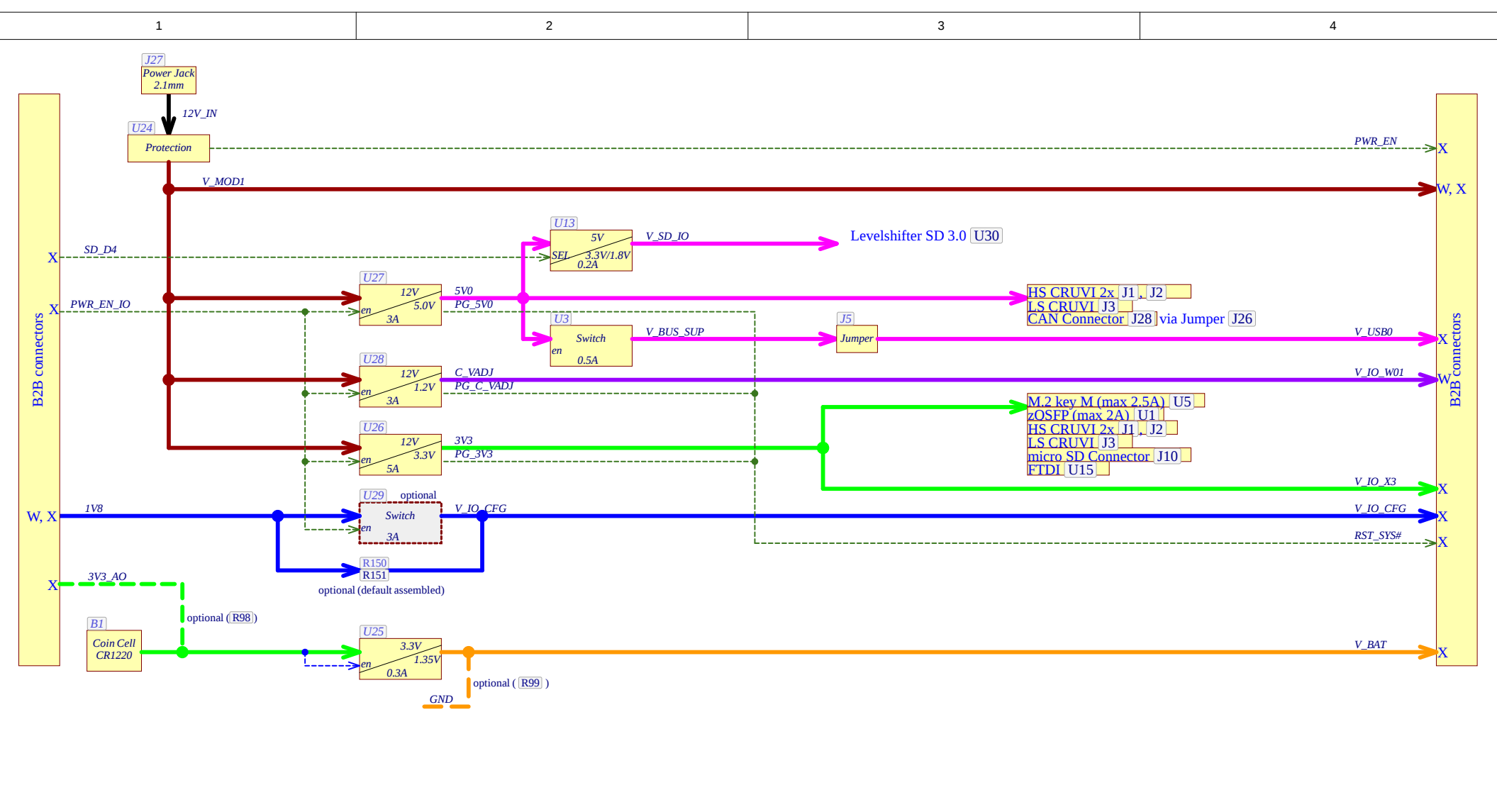
1		2		3		4																
A	<table><tr><td>REV</td><td>Description</td><td></td></tr><tr><td>-01</td><td>Initial revision</td><td>MR</td></tr><tr><td>-02</td><td>1. Corrected DIR pin connection of Levelshifter U9 and removed patch label. 2. Removed UART and JTAG test points. 3. Changed J9 and J13 from micro USB to USB-C. Therefore also added U11, optional I2C Levelshifter U14 and corresponding circuits. 4. Changed J5 from 8 pin to 10 pin header, to set PORT connection of U11 via jumper. 5. Changed MP1.. MP6 to 10mm version and removed from schematic, will be added manually to BOM when nedded. 6. Added zero Ohms R150, R151 and set power switch U29 to default not fitted. 7. Changed default assembly option for PCIe Reset: R29 fitted, R30 not fitted. 8. Changed J11 to 74991114411, replaced C43 by 0R R152. 9. Added C43. 10. Changed SD 3.0 level shifter pin compatible from NXS0506GUX to NVT4858HKZ.</td><td>MR</td></tr></table>						REV	Description		-01	Initial revision	MR	-02	1. Corrected DIR pin connection of Levelshifter U9 and removed patch label. 2. Removed UART and JTAG test points. 3. Changed J9 and J13 from micro USB to USB-C. Therefore also added U11, optional I2C Levelshifter U14 and corresponding circuits. 4. Changed J5 from 8 pin to 10 pin header, to set PORT connection of U11 via jumper. 5. Changed MP1.. MP6 to 10mm version and removed from schematic, will be added manually to BOM when nedded. 6. Added zero Ohms R150, R151 and set power switch U29 to default not fitted. 7. Changed default assembly option for PCIe Reset: R29 fitted, R30 not fitted. 8. Changed J11 to 74991114411, replaced C43 by 0R R152. 9. Added C43. 10. Changed SD 3.0 level shifter pin compatible from NXS0506GUX to NVT4858HKZ.	MR	A						
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B							B															
C							C															
D	 <table><tr><td colspan="3">Title: Revision History</td></tr><tr><td>A4</td><td>Number: TEB0955 A</td><td>Rev. 02</td></tr><tr><td>Date: 04.03.2026</td><td colspan="2">Copyright: Trenz Electronic GmbH</td></tr><tr><td colspan="3">Page 2 of 18</td></tr><tr><td colspan="3">Filename: Revision Changes.SchDoc</td></tr></table>						Title: Revision History			A4	Number: TEB0955 A	Rev. 02	Date: 04.03.2026	Copyright: Trenz Electronic GmbH		Page 2 of 18			Filename: Revision Changes.SchDoc			D
Title: Revision History																						
A4	Number: TEB0955 A	Rev. 02																				
Date: 04.03.2026	Copyright: Trenz Electronic GmbH																					
Page 2 of 18																						
Filename: Revision Changes.SchDoc																						
1		2		3		4																



Special notes:



Title: System Overview		
A4	Number: TEB0955 A	Rev. 02
Date: 13.04.2026	Copyright: Trenz Electronic GmbH	Page 3 of 18
Filename: Overview.SchDoc		



ABC_DEF

Net name
Power bus
Control signal

PL_DCIN

X.XV

Power converter

Port / Component

Power_0.SchDoc

Power_1.SchDoc



Title: Power Diagram		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 4 of 18
Filename: Power_Diagram.SchDoc		

I2C Addresses:

Device	Bus	Address	Note
-	U_I2C	-	Depends on modul
zQSFP	U_I2C	-	Depends on QSFP modul

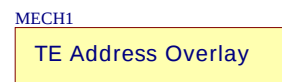
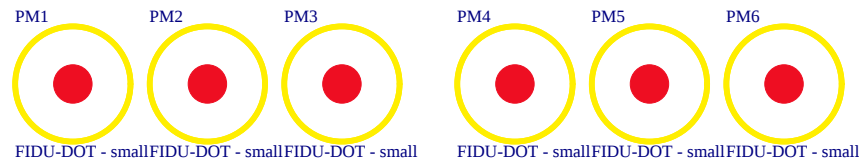
-	M_I2C	-	Depends on modul
PCF8574DWR	M_I2C	010011026H	I2C IO expander for QSFP control signals
PCF8574DWR	M_I2C	010010125H	I2C IO expander for M.2 control signals
LMK61E2BAA	M_I2C	101100058H	Programmable Clock MGT103 (QSFP)
PTN5150A	M_I2C	01111013DH	USB-C Logic Chip, connection optional via Levelshifter U14 (default not fitted)
LMK61E2BAA	M_I2C	10110105AH	Optional Programmable Clock MGT104 (M.2)

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
12V_IN	IN	12V	+/-5%	Board Power	-
V_MOD1	OUT	5V .. 12V	+/-5%	Module main power supply	-
3V3_AO	IN	3.3V	+/-3%	Always On rail from Module	Max additional (low ESR) capacitance: 18µF
1V8	IN	1.8V	+/-3%	Periphery supply from Module	Max additional (low ESR) capacitance: 30µF
V_IO_W01	OUT	1.0V .. 1.5V	+/-5%	IO supply to Module	Depends on Module: TE0955: XPIO Bank
V_IO_X3	OUT	1.8V .. 3.3V	+/-3%	IO supply to Module	Depends on Module: TE0955: HD Bank
V_IO_CFG	OUT	1.8V	+/-5%	IO CFG supply to Module	-
V_BAT	OUT	1.35V	+/-10%	Supply for BB RAM and RTC	If not used connect to GND



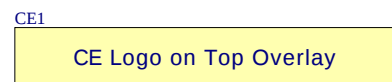
Title: TEB0955		
A4	Number: TEB0955 A	Rev. 02
Date: 24.06.2026	Copyright: Trenz Electronic GmbH	Page 5 of 18
Filename: TEB0955.SchDoc		



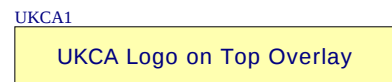
LOGO ADDRESS



LOGO PRINT



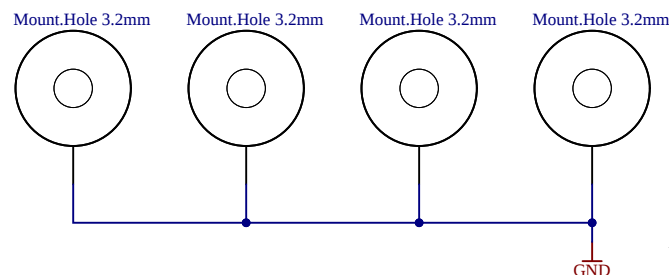
CE-TOPOVERLAY



UKCA-TOPOVERLAY

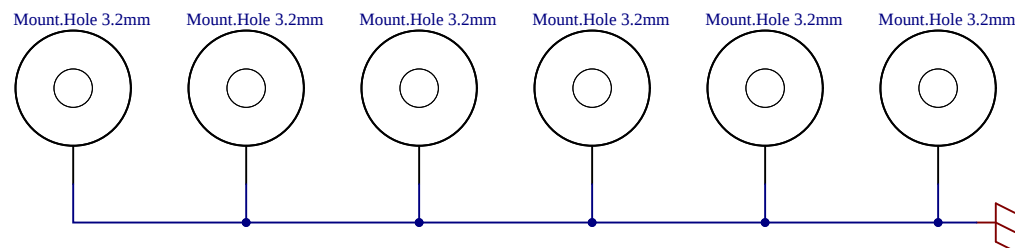
Serial1
Serial
Serialnumber 6,3 x 6.3mm

Module Mounting Holes



When using full size CRUVI extension on HS_X port, mountinghole in upper left corner of the board can not be used with distance bolt in top direction.

Carrier Mounting Holes



1

2

3

4

A

B

C

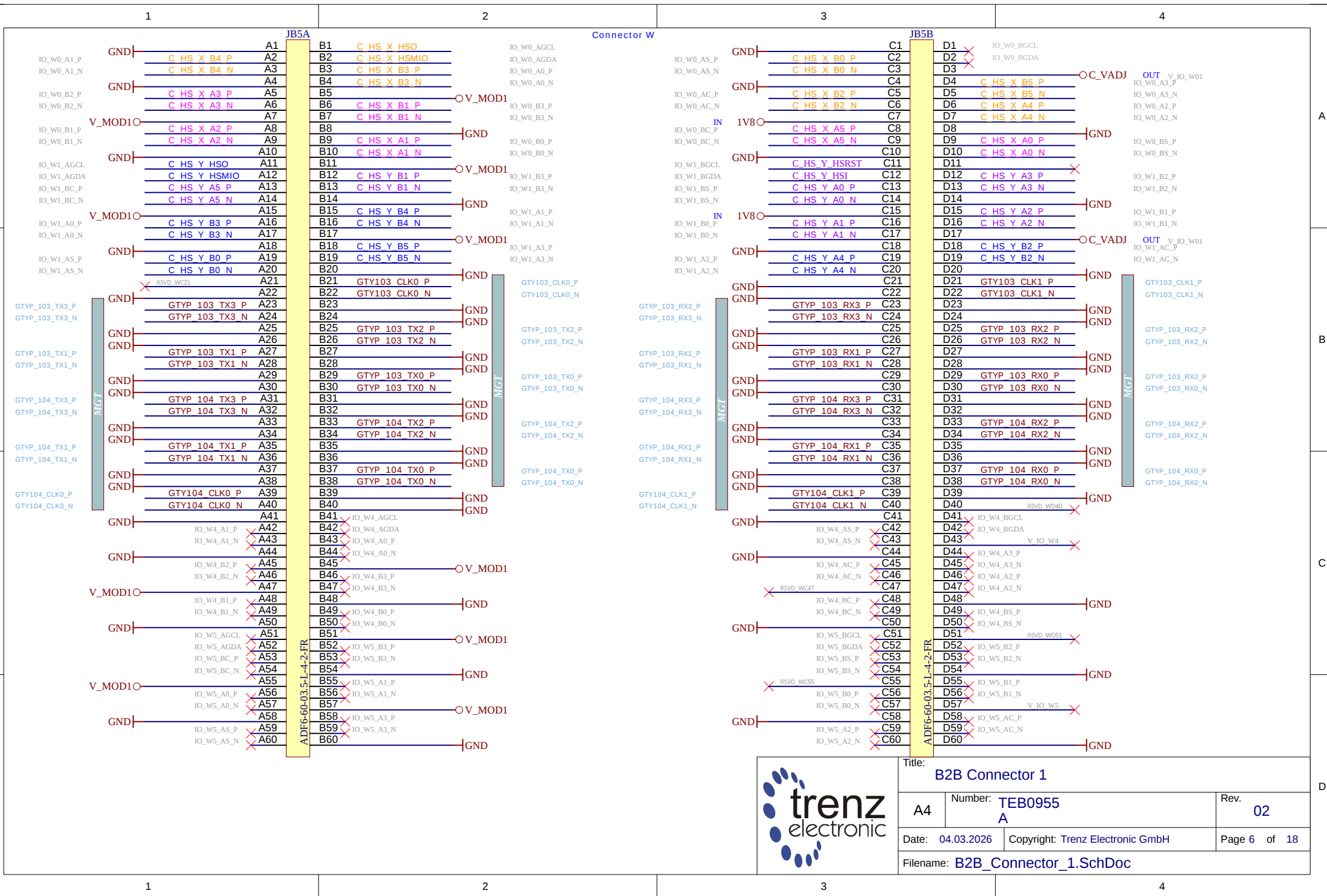
D

A

B

C

D



1

2

3

4

A

A

B

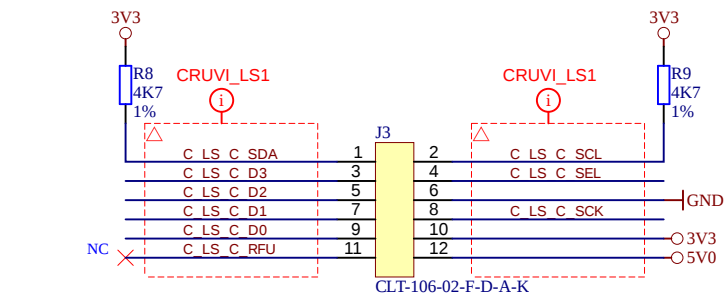
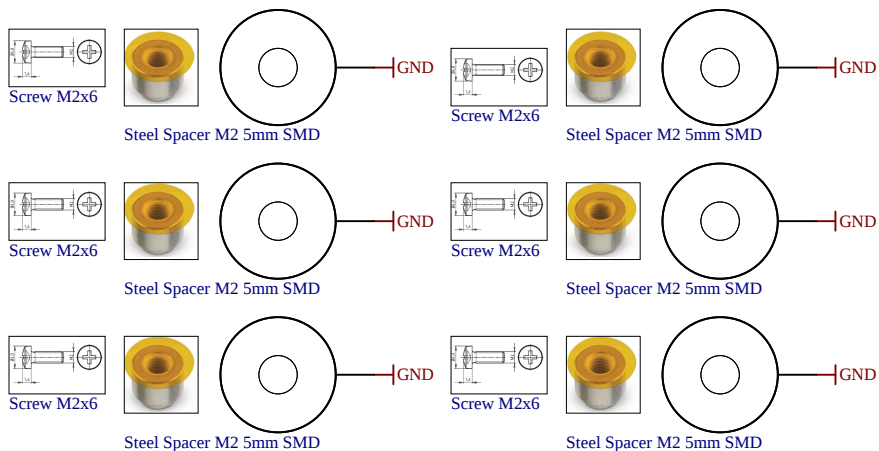
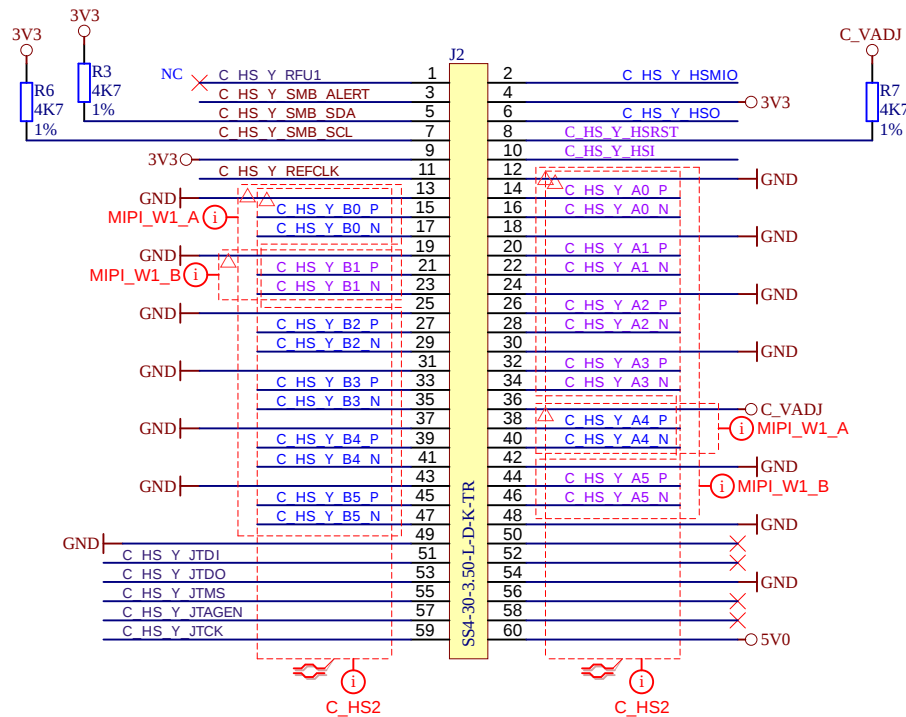
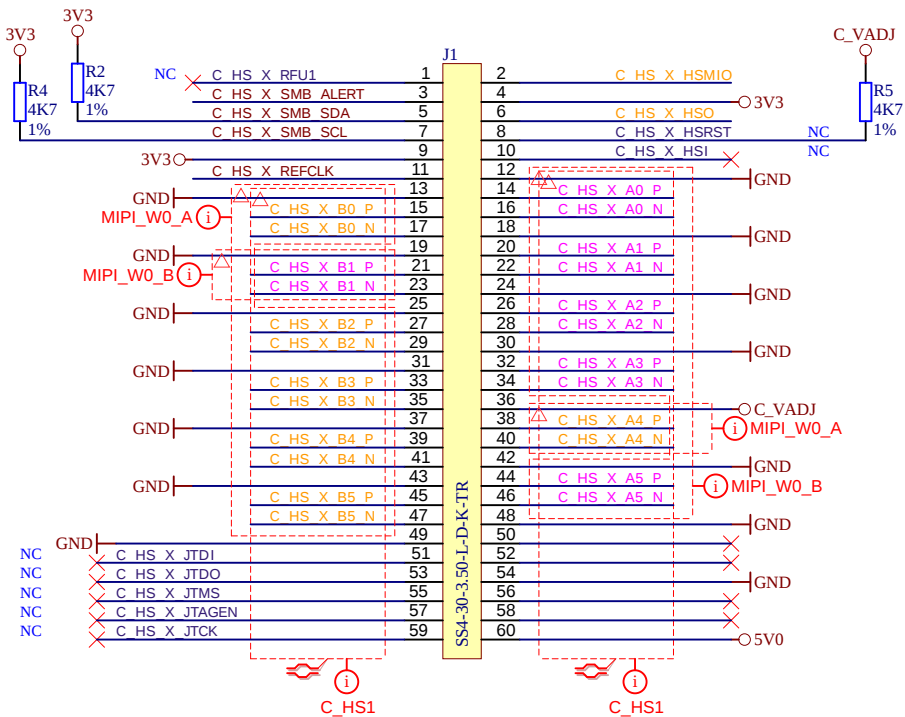
B

C

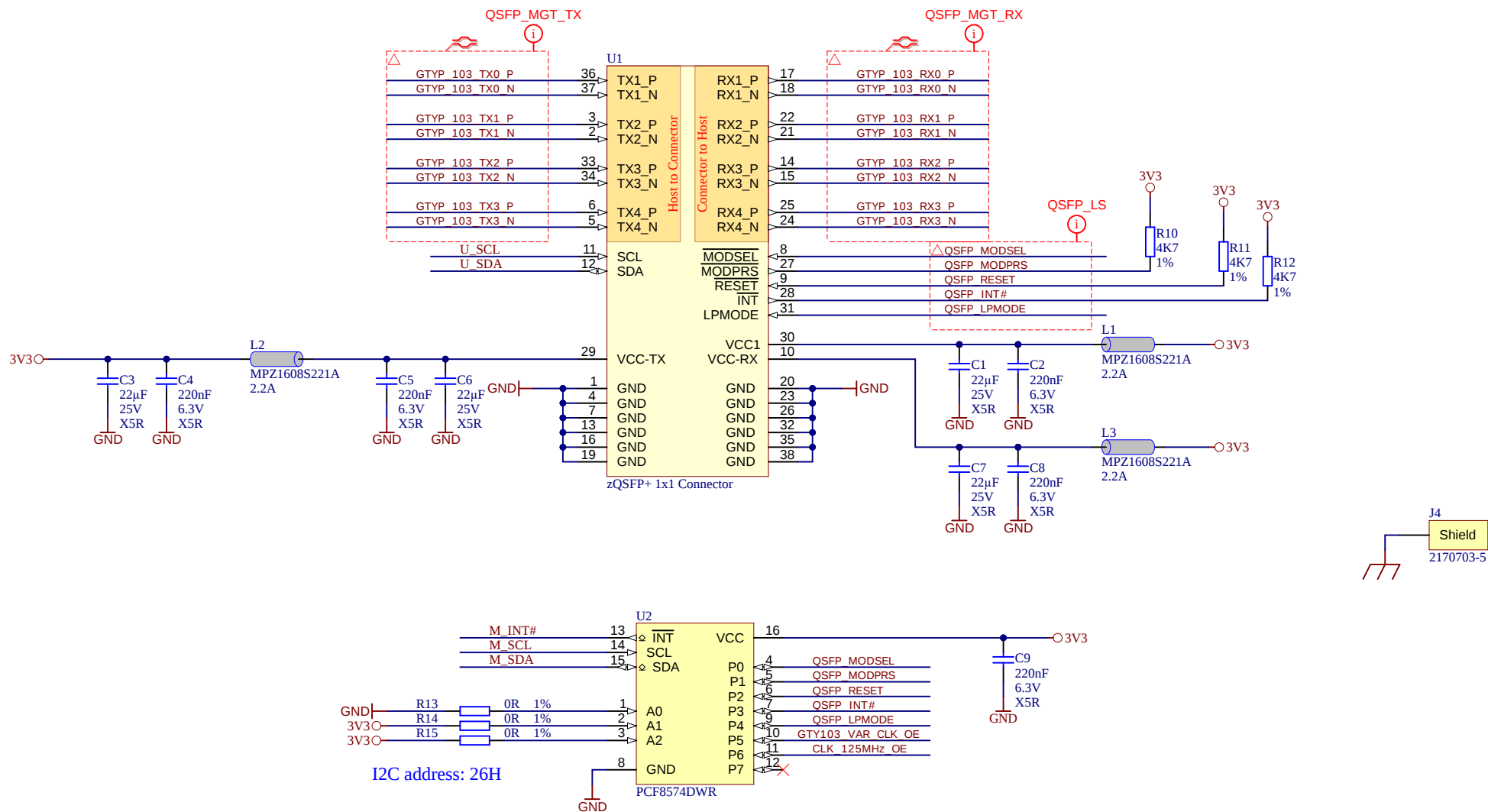
C

D

D



Title: CRUVI		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 8 of 18
Filename: CRUVI.SchDoc		



Title: QSFP		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 9 of 18
Filename: QSFP.SchDoc		

1

2

3

4

A

A

B

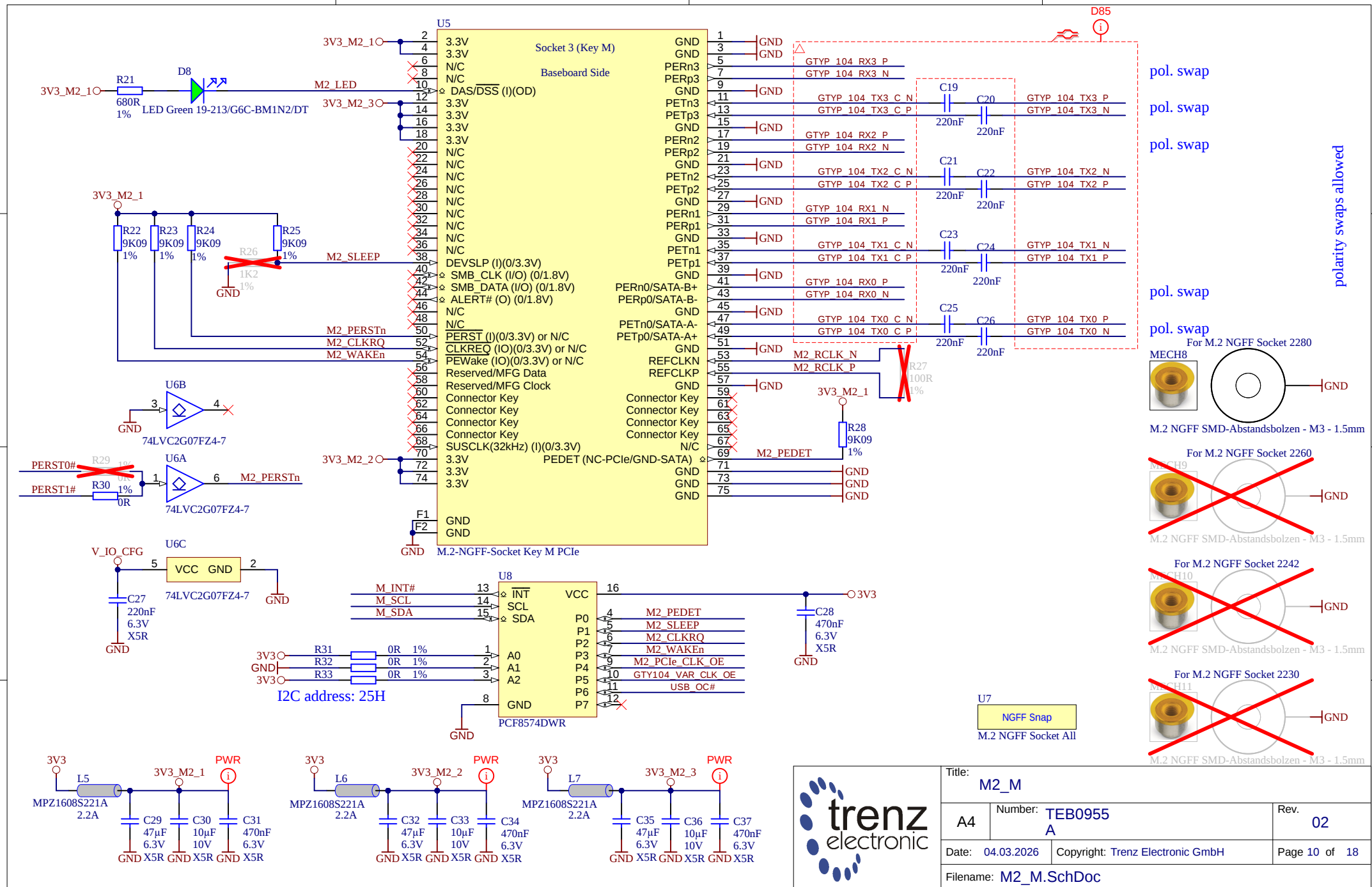
B

C

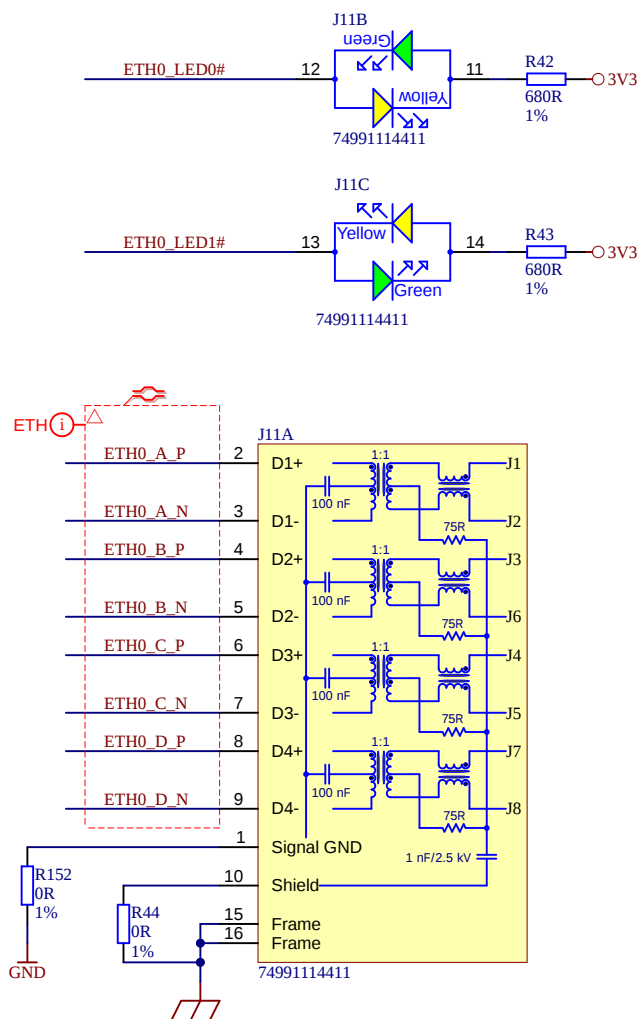
C

D

D



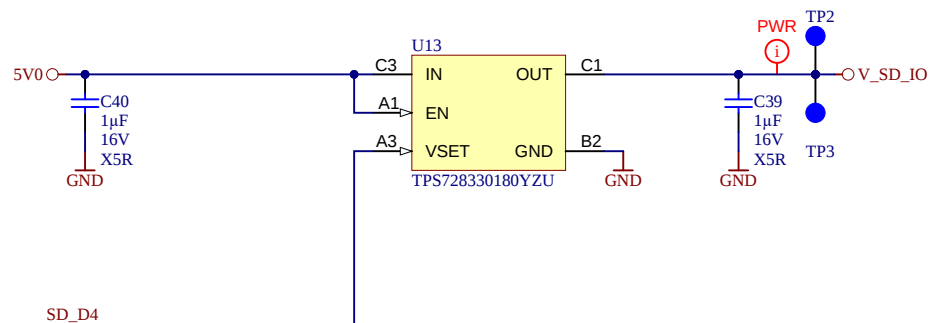
Title: M2_M		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	
Filename: M2_M.SchDoc		Page 10 of 18



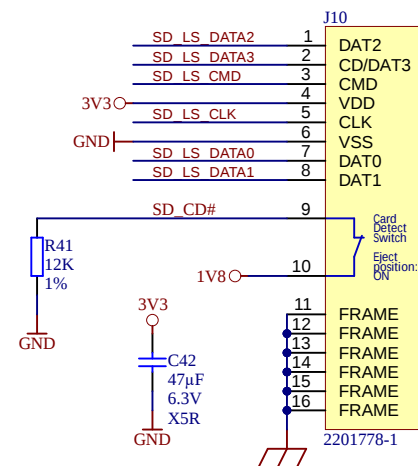
		Title: GB_ETH	
		A4	Number: TEB0955 A
Date: 04.03.2026		Copyright: Trenz Electronic GmbH	
Filename: GB_ETH.SchDoc		Page 11 of 18	

SD IO Power

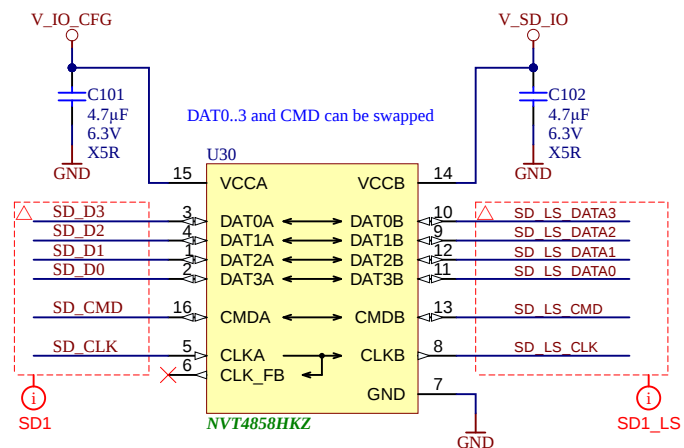
SD_D4 is SEL
SEL 'low'=3.3V, SEL 'high' =1.8V



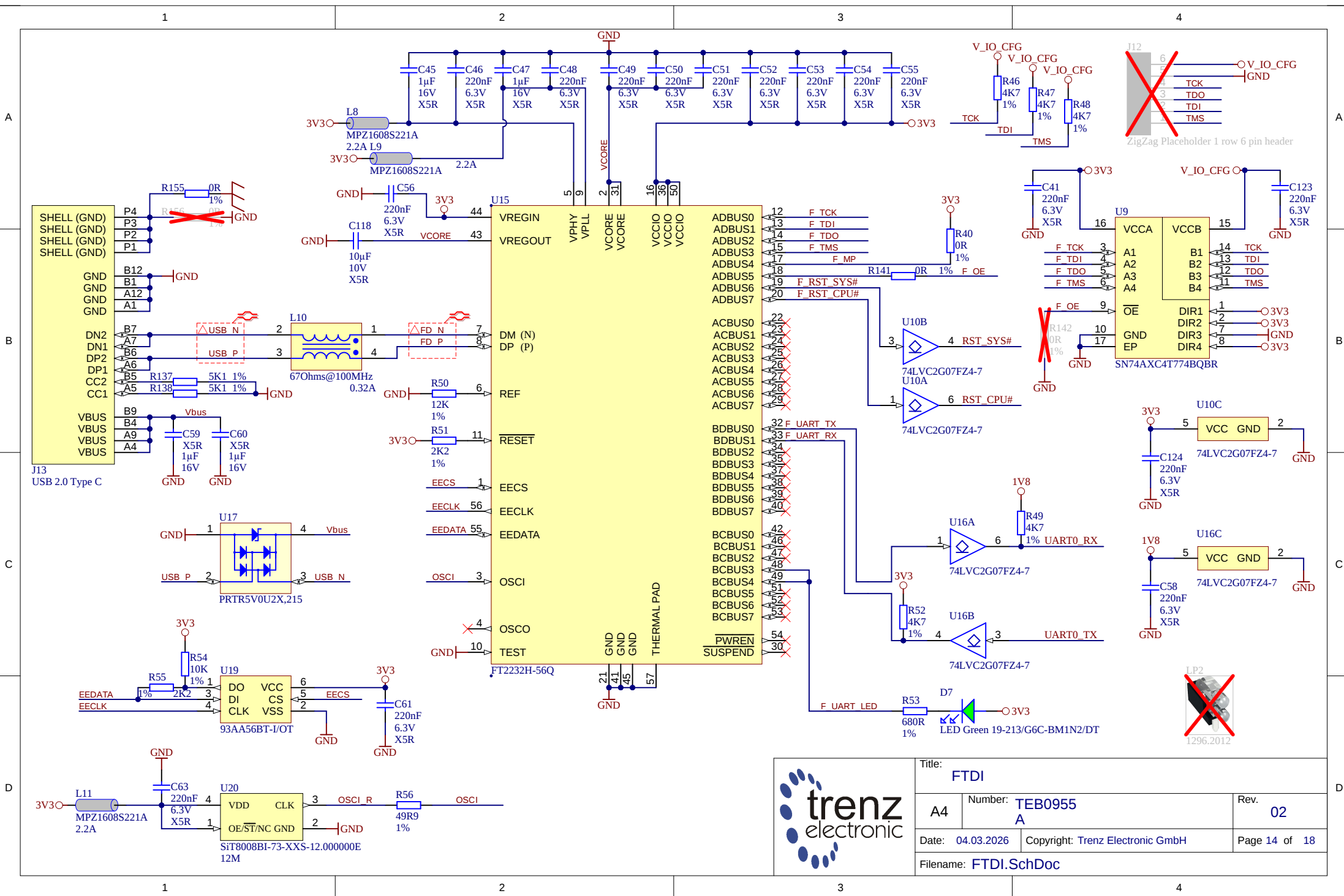
SD Connector



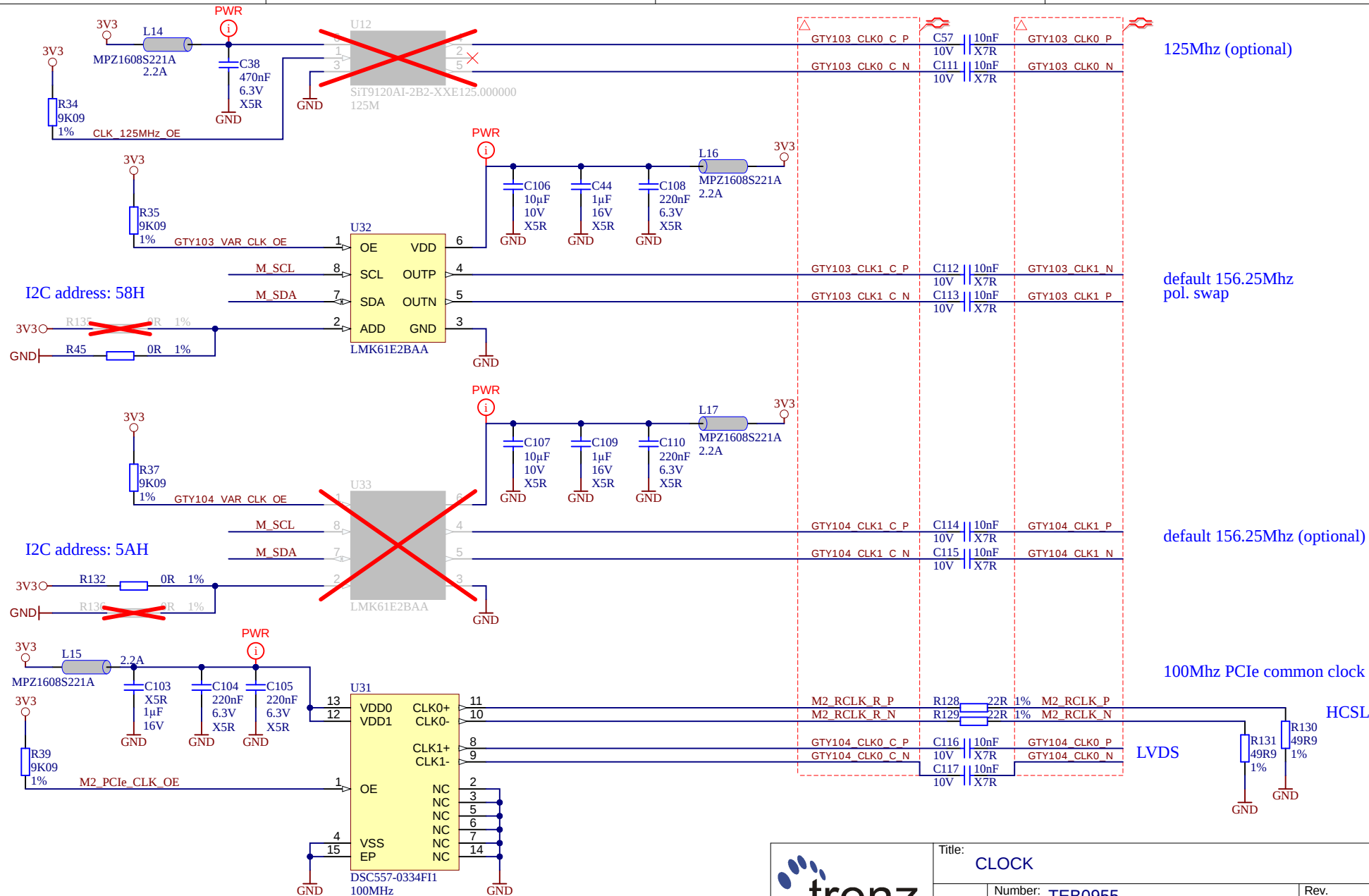
SD Levelshift



Title: SD		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 13 of 18
Filename: SD.SchDoc		



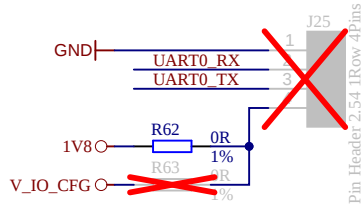
Footprint compatible with SI544BAxxxxxACC



		Title: CLOCK	
		A4	Rev. 02
Number: TEB0955 A		Page 15 of 18	
Date: 04.03.2026		Copyright: Trenz Electronic GmbH	
Filename: Clock.SchDoc			

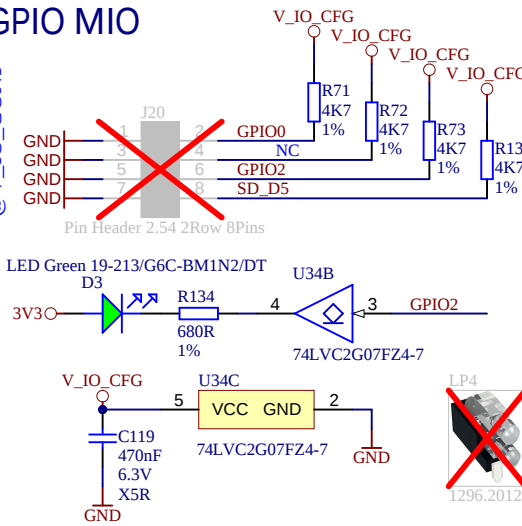
UART

2.54 mm pitch pin headers J12 and J25 can be combined into one 1x10 pin header.



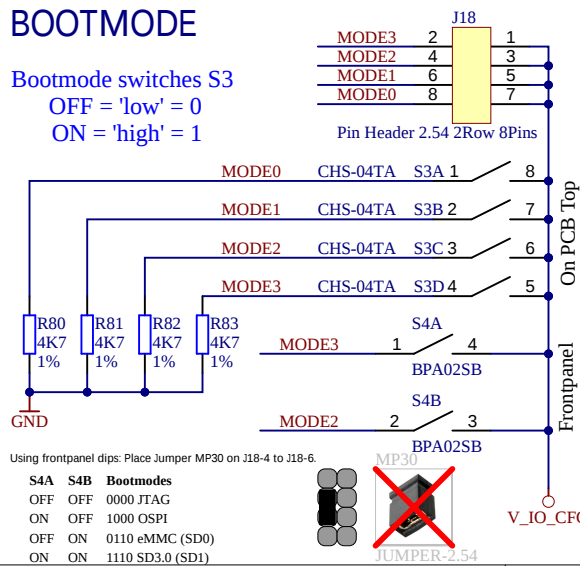
GPIO MIO

@V_IO_CFG



BOOTMODE

Bootmode switches S3
OFF = 'low' = 0
ON = 'high' = 1

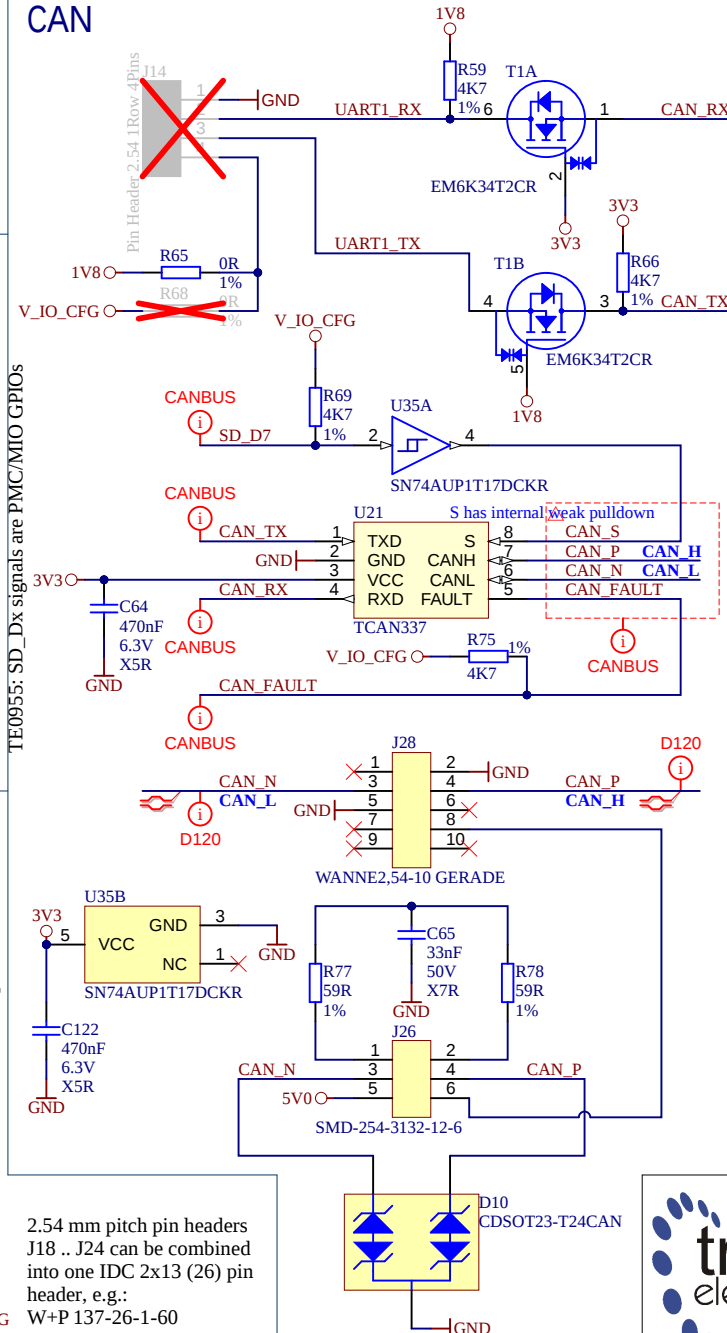


Using frontpanel dips: Place Jumper MP30 on J18-4 to J18-6.

S4A	S4B	Bootmodes
OFF	OFF	0000 JTAG
ON	OFF	1000 OSPI
OFF	ON	0110 eMMC (SD0)
ON	ON	1110 SD3.0 (SD1)

CAN

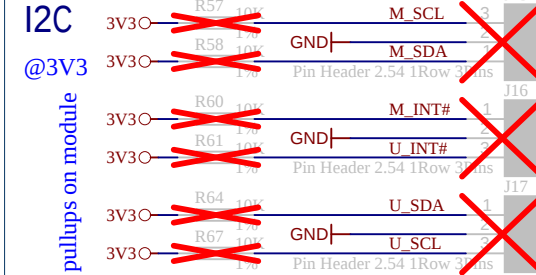
TE0955: SD_Dx signals are PMC/MIO GPIOs



2.54 mm pitch pin headers J18 .. J24 can be combined into one IDC 2x13 (26) pin header, e.g.: W+P 137-26-1-60

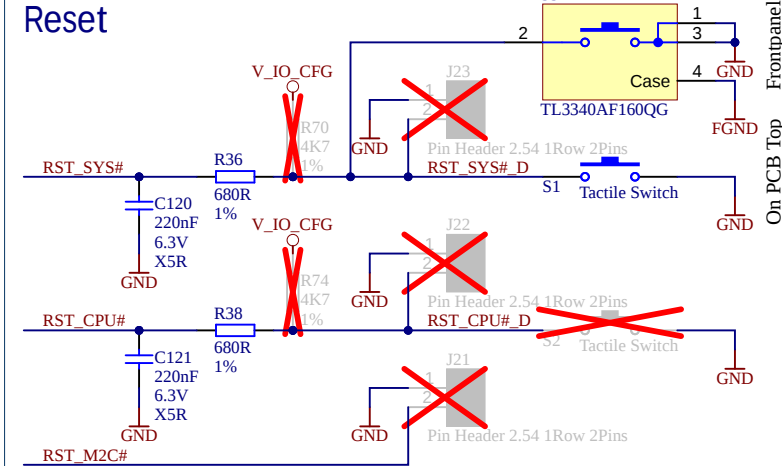
I2C

@3V3
pullups on module

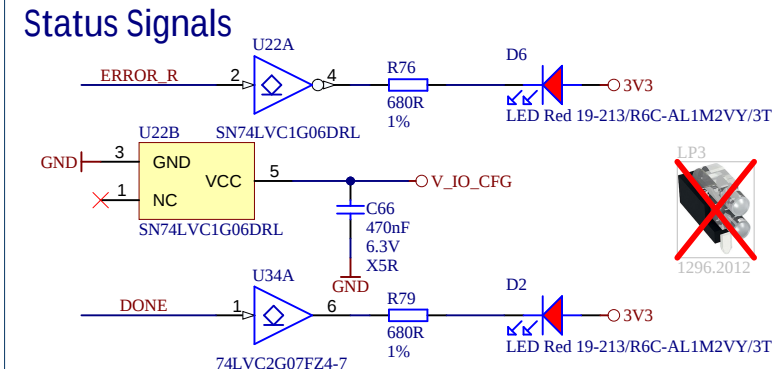


2.54 mm pitch pin headers J15, J16 and J17 can be combined depending on needs. E.g.: 1x4 pinheader for U_I2C + U_INT#.

Reset

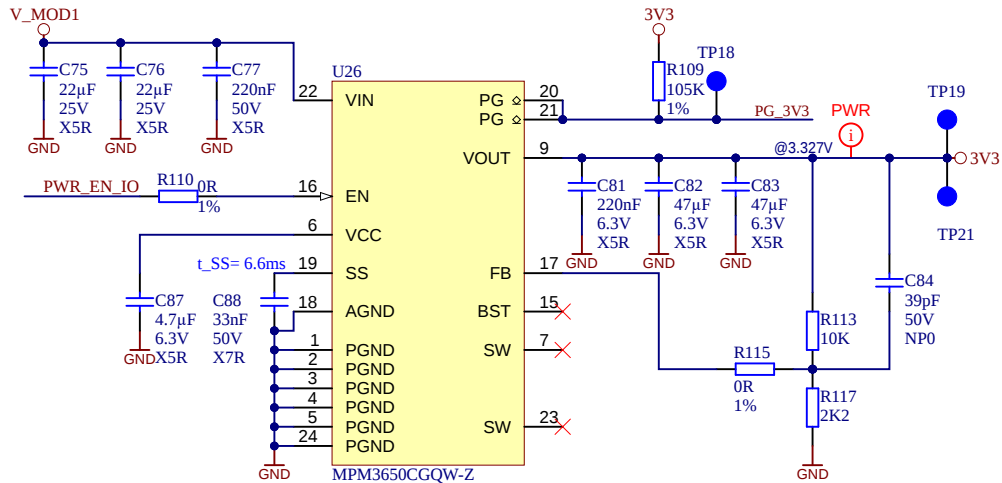


Status Signals

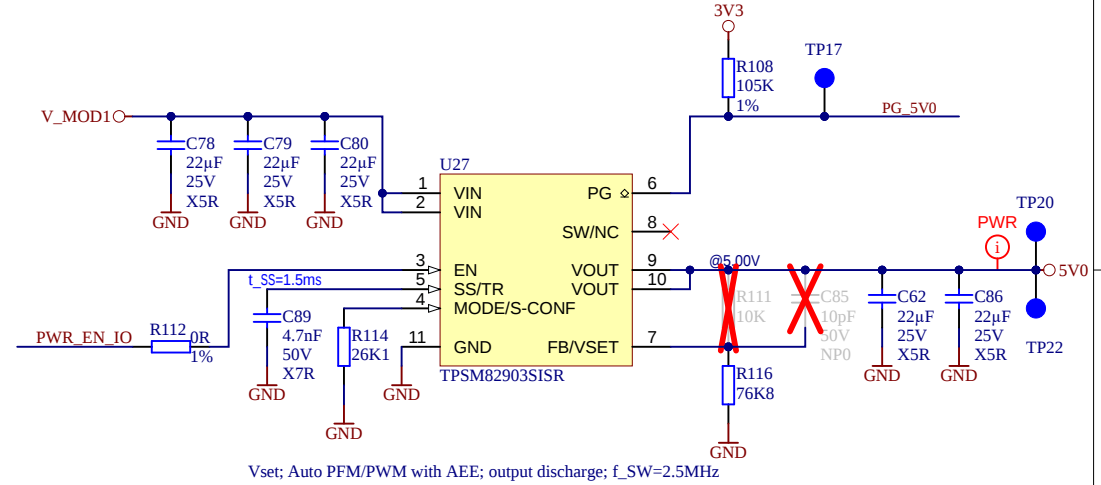


Title: MISC		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 16 of 18
Filename: MISC.SchDoc		

3V3 Supply

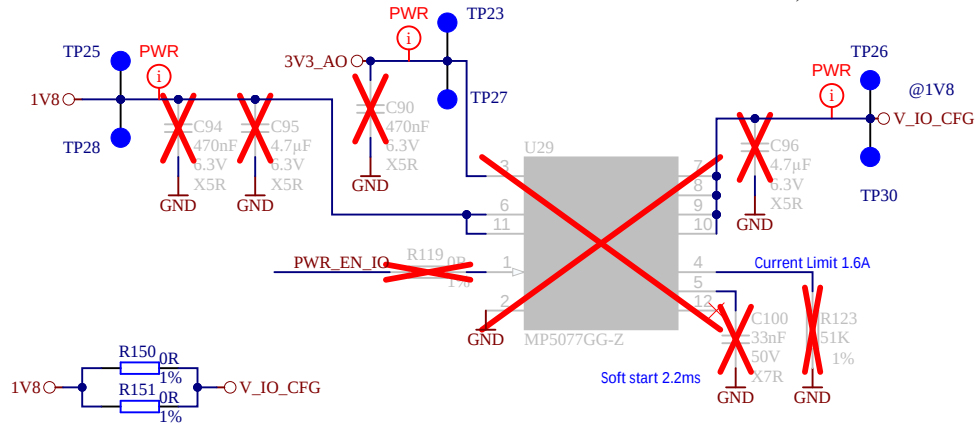


5V Supply

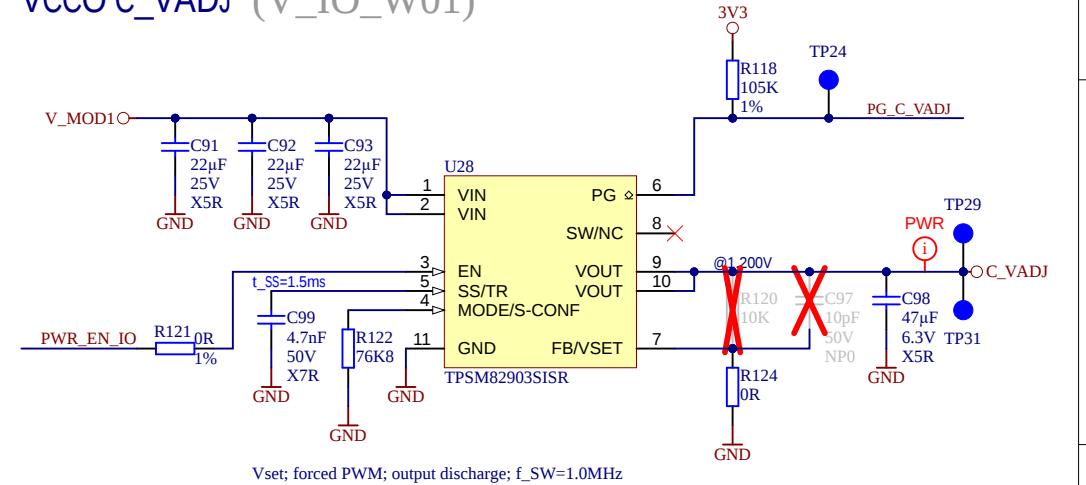


VCCO V_IO_CFG

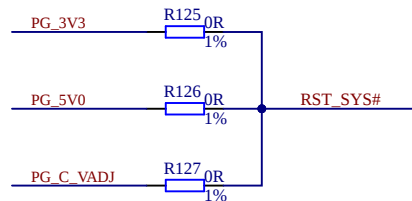
If 1V8 from module is within VCCO power sequencing group, power switch not needed. Use zero Ohms R150, R151.



VCCO C_VADJ (V_IO_W01)



PG -> Reset



Title: Power_1		
A4	Number: TEB0955 A	Rev. 02
Date: 04.03.2026	Copyright: Trenz Electronic GmbH	Page 18 of 18
Filename: Power_1.SchDoc		