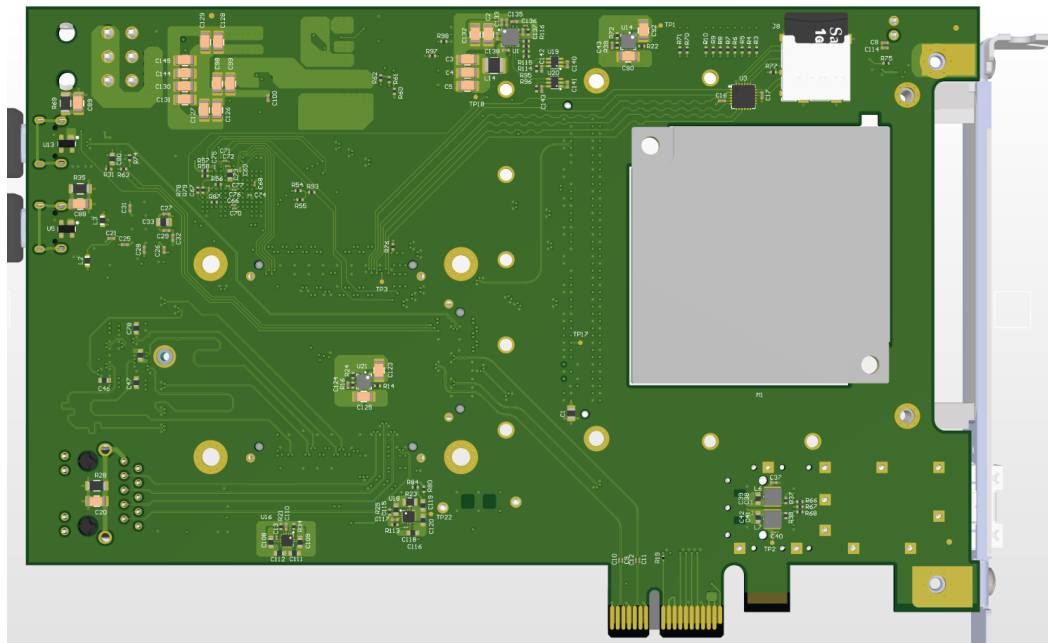
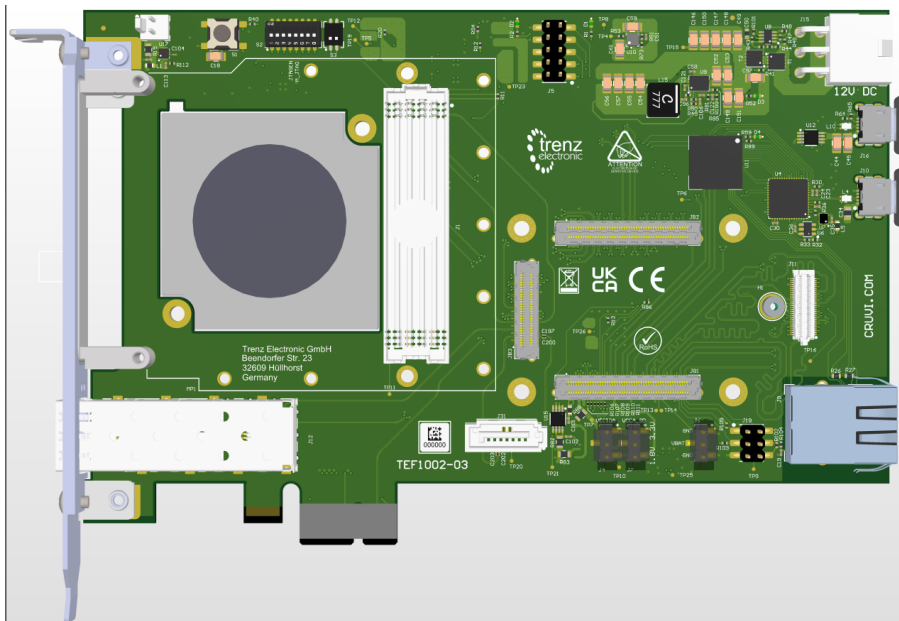




Regarding the usage of our schematics and alike documentation for Trenz baseboard TEF1002.

Baseboard is Open Source Hardware and therefore free to use, adapt and can be modified to suit your needs as described in the "The MIT License".

Permission is hereby granted, free of charge, to any person obtaining a copy of this hardware and associated documentation files (the "Product"), to deal in the Product without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Product, and to permit persons to whom the Product is furnished to do so.

Drawn by	MT
Checked by	MR
Assembly variant	A
Created by	MT
Modified by	OT
Modified at	13-06-2026



Title: TEF1002- Legal Notices			
A4	Number: TEF0002 A		Rev. 03
Date: 09.06.2026		Copyright: Trenz Electronic GmbH	Page 1 of 19
Filename: Legal Notices.SchDoc			

<

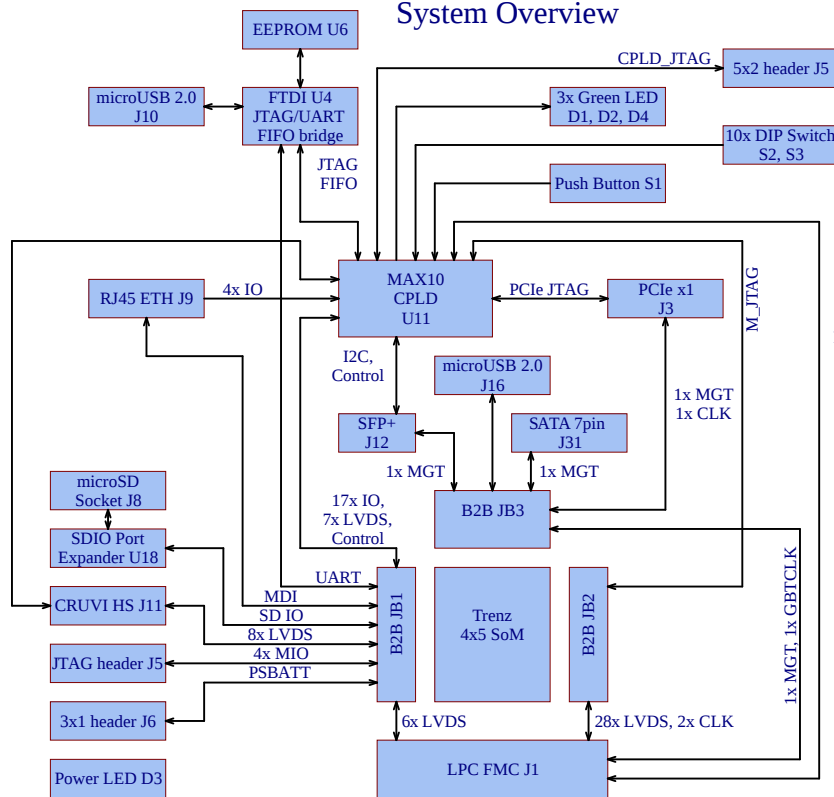
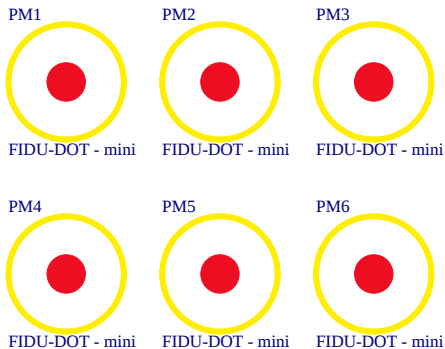
1

2

3

4

System Overview

I2C,
FMC JTAG,
ControlPWR1
PWR1.SchDocFMC_PWR
FMC_PWR.SchDoc

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

LOGO

TE Logo PRINT Layer

LOGO PRINT

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

Serial

Serial

Serialnumber 6,3 x 6.3mm

ESD

ESD Logo on Top Overlay

ESD-TOPOVERLAY



Title:

TEF1002

A4

Number:

TEF1002
A

Rev.

03

Date: 09.06.2026

Copyright: Trenz Electronic GmbH

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Filename: TEF1002.SchDoc

Assembly variant

A

Created by

MT

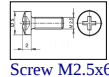
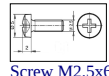
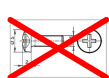
Modified by

OT

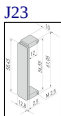
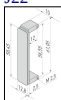
Modified at

13-06-2026

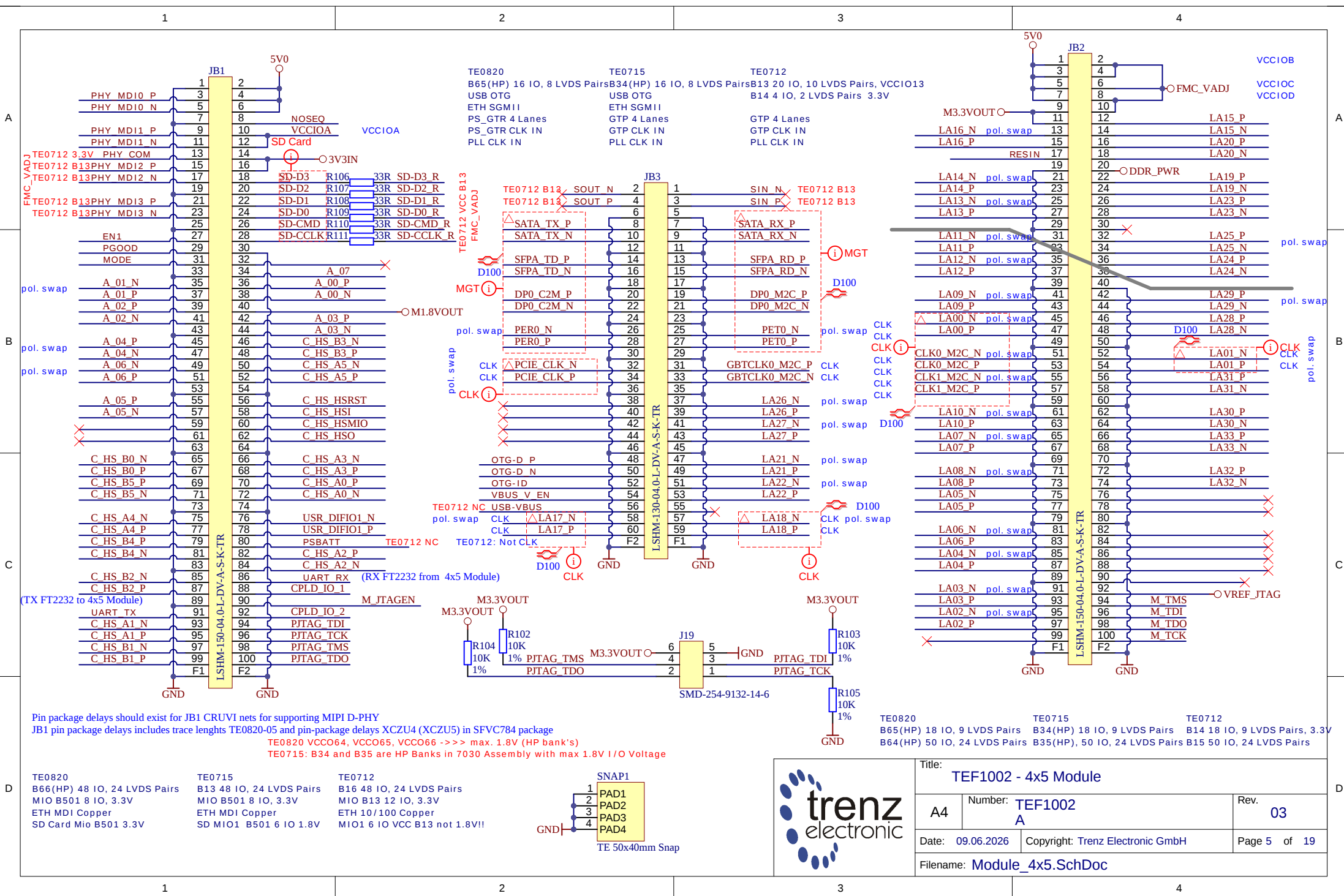
SVN Revision

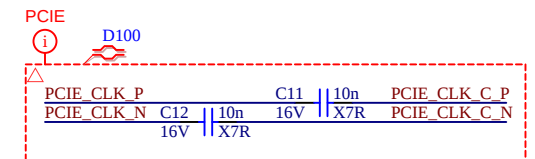
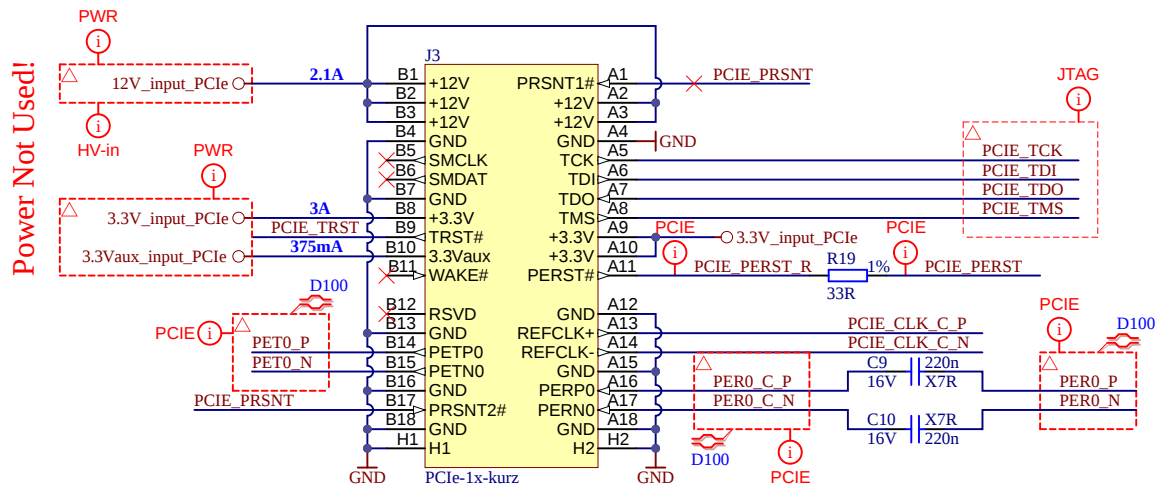


3200-479

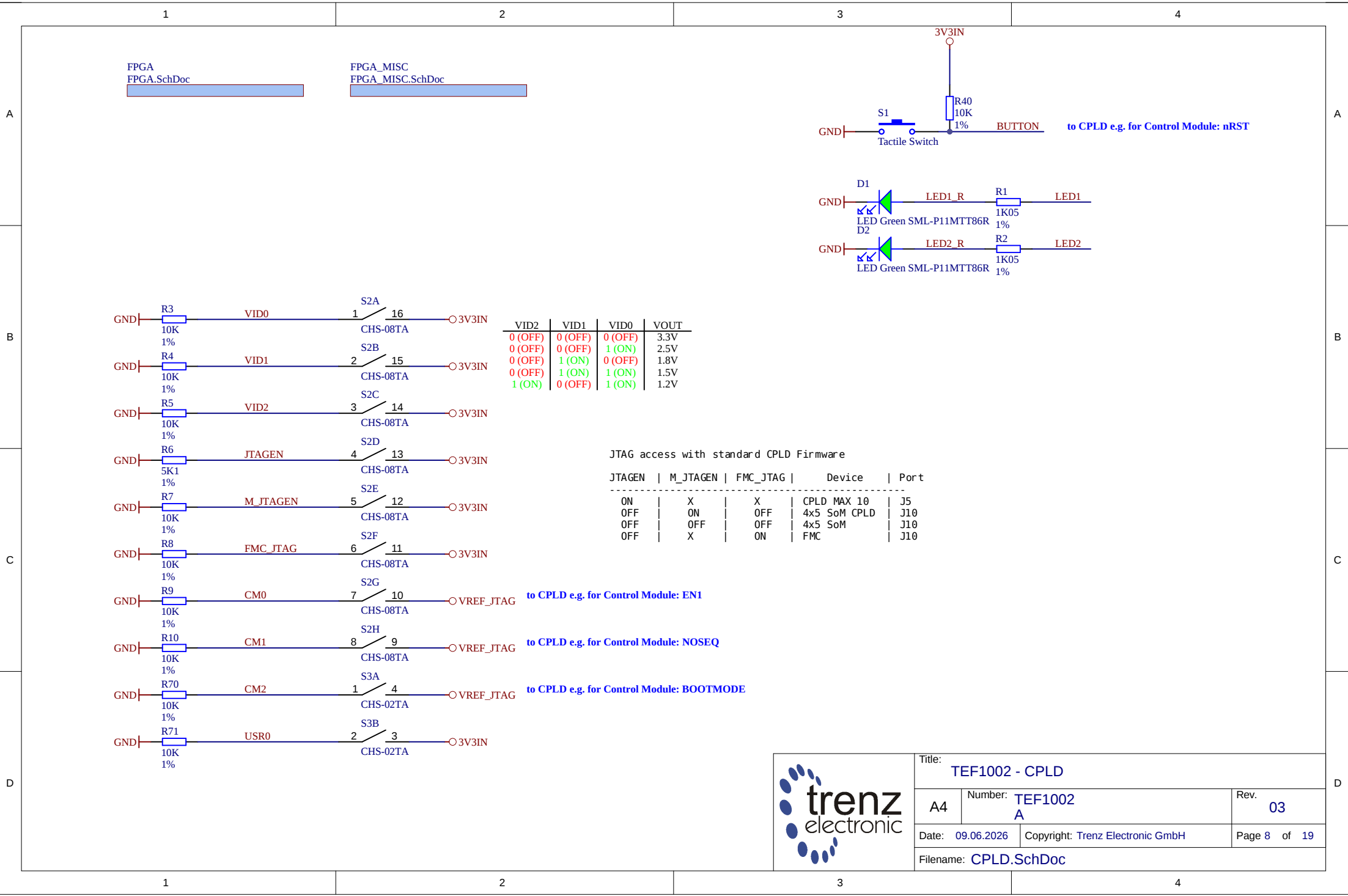
FMC gasket
J22

FMC-Bezel





		Title: TEF1002 - PCIE CONNECTOR		
		A4	Number: TEF1002 A	Rev. 03
		Date: 09.06.2026	Copyright: Trenz Electronic GmbH	Page 7 of 19
		Filename: PCIE_CONN.SchDoc		

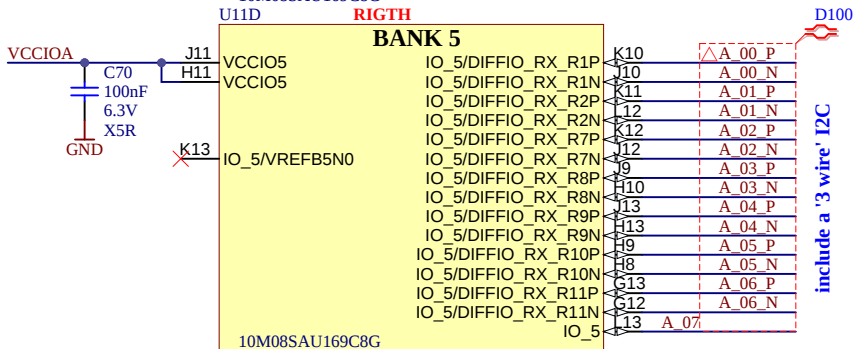
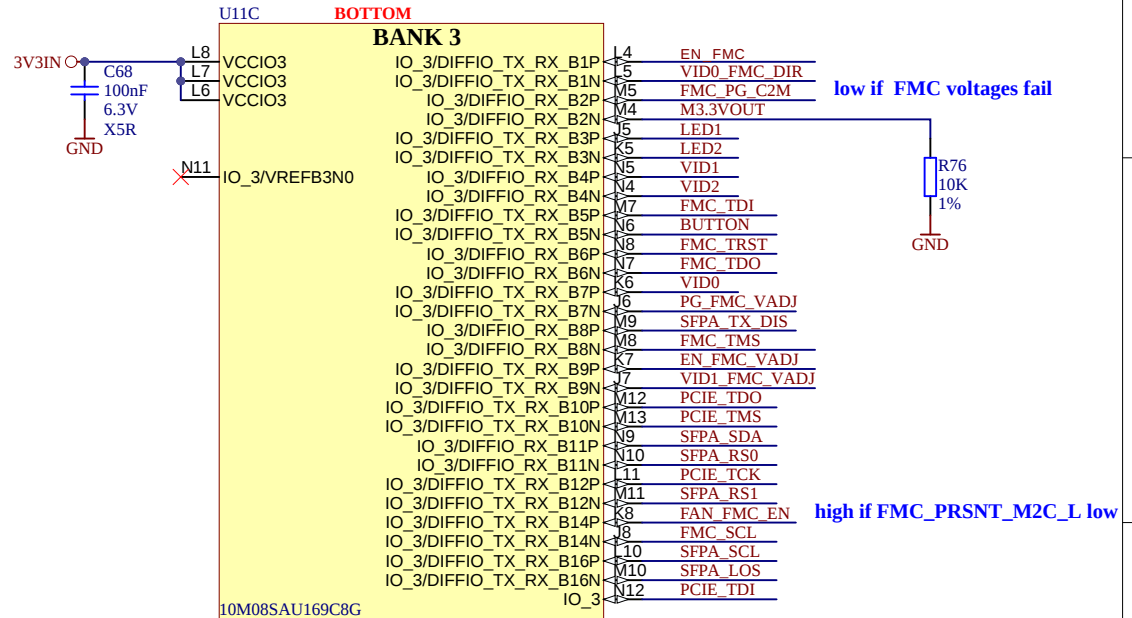
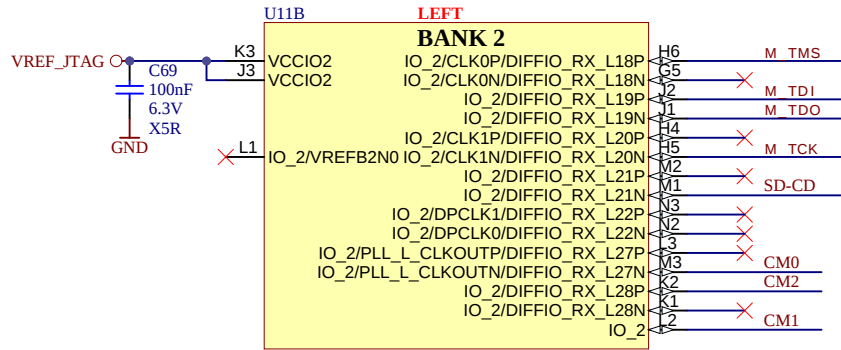
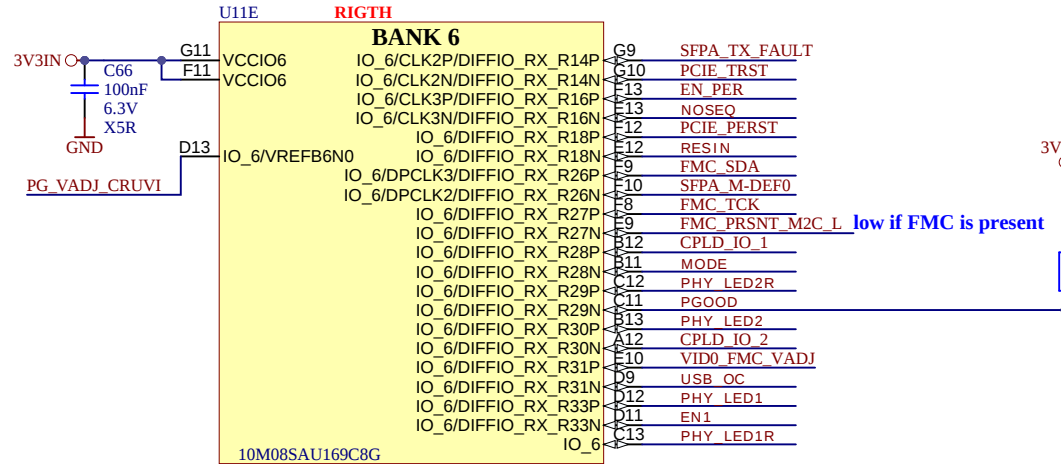
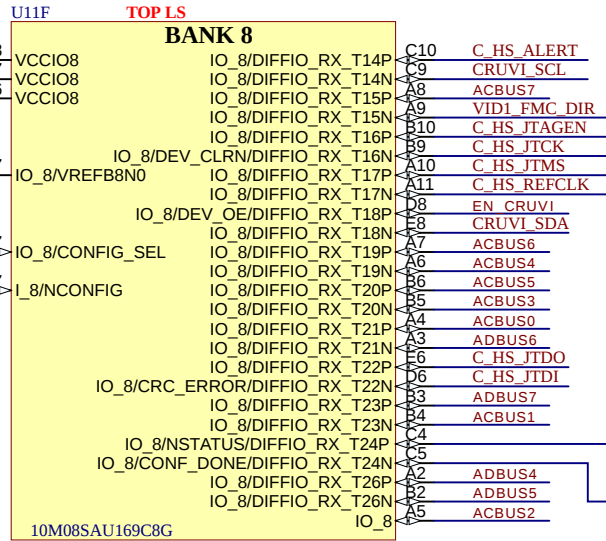


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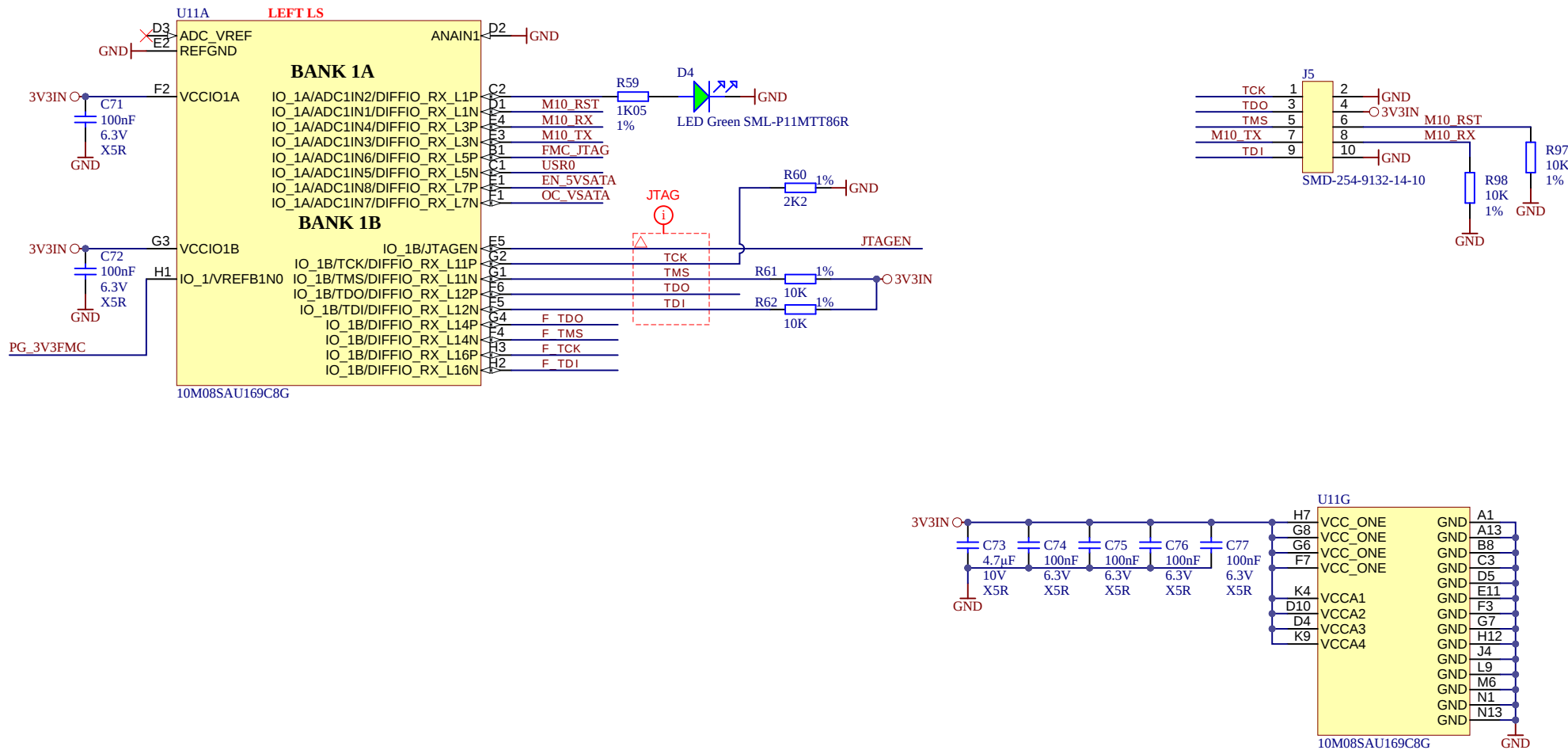
Title: TEF1002 - FPGA			
A4	Number: TEF1002 A		Rev. 03
Date: 09.06.2026		Copyright: Trenz Electronic GmbH	Page 9 of 19
Filename: FPGA.SchDoc			

1

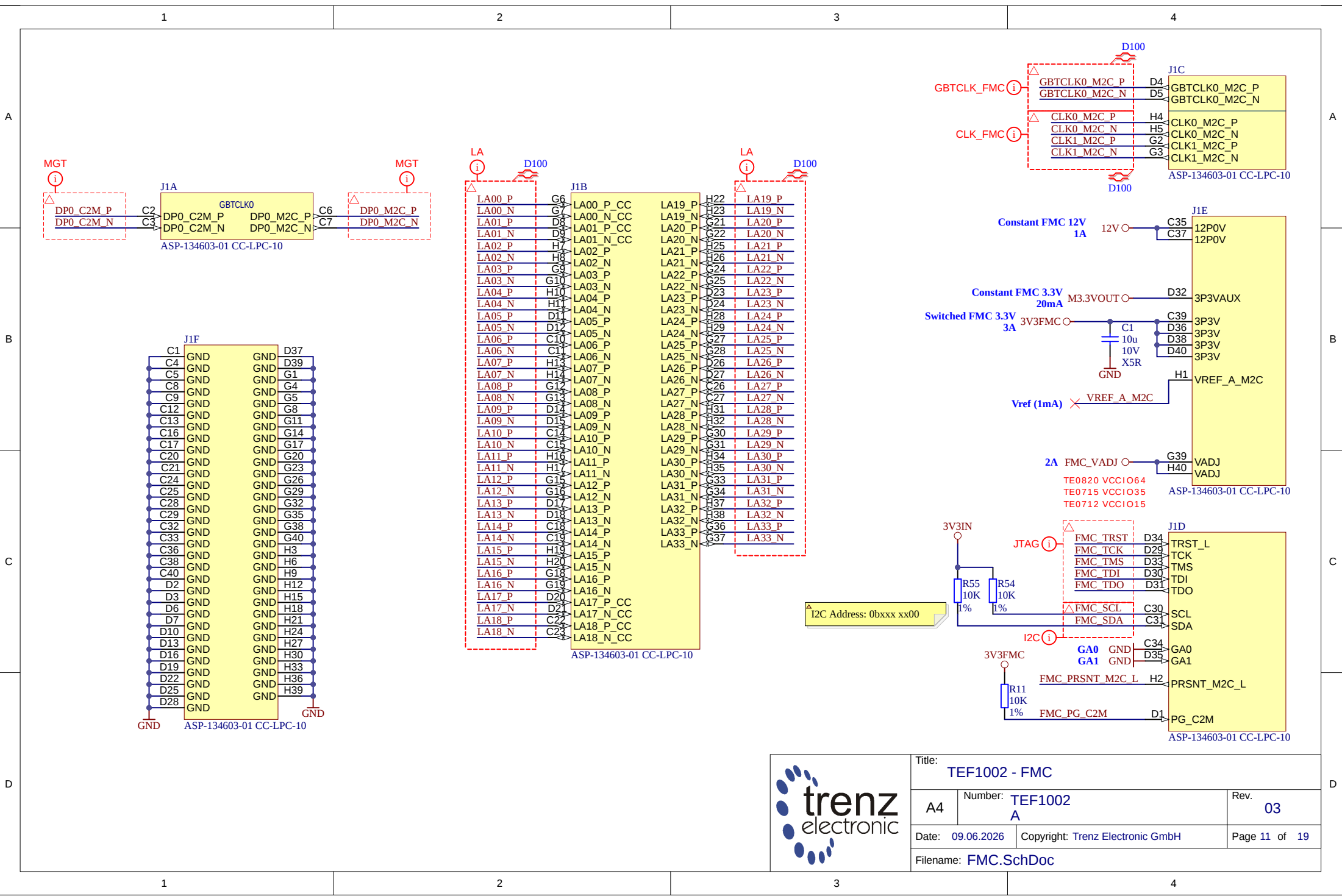
2

3

4



		Title: TEF1002 - FPGA MISC	
		A4 Number: TEF1002 A	Rev. 03
Date: 09.06.2026		Copyright: Trenz Electronic GmbH	
Filename: FPGA_MISC.SchDoc		Page 10 of 19	



1

2

3

4

A

A

B

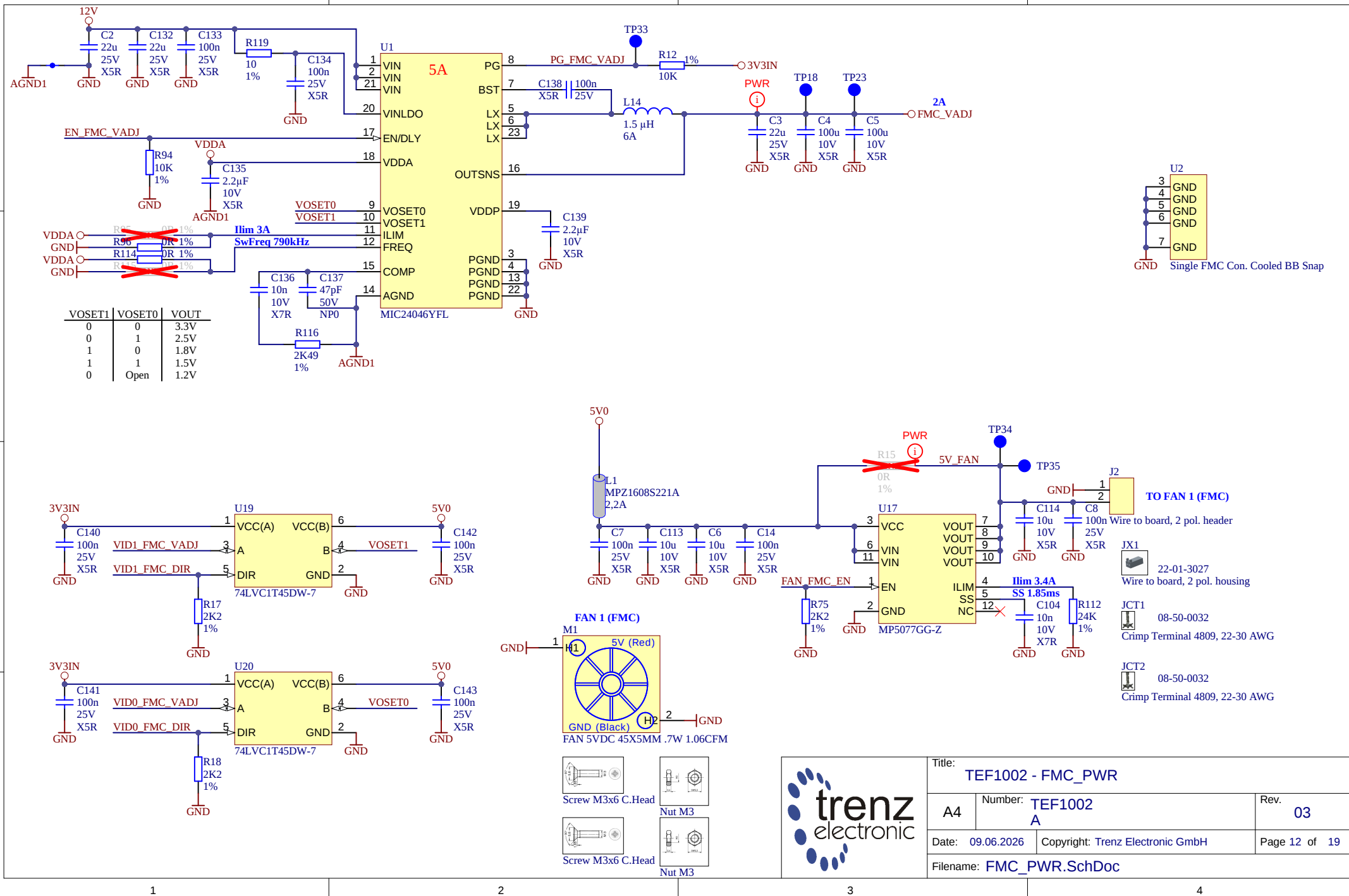
B

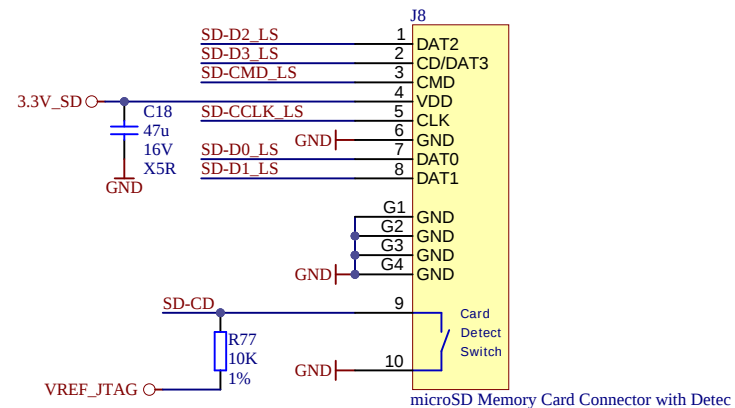
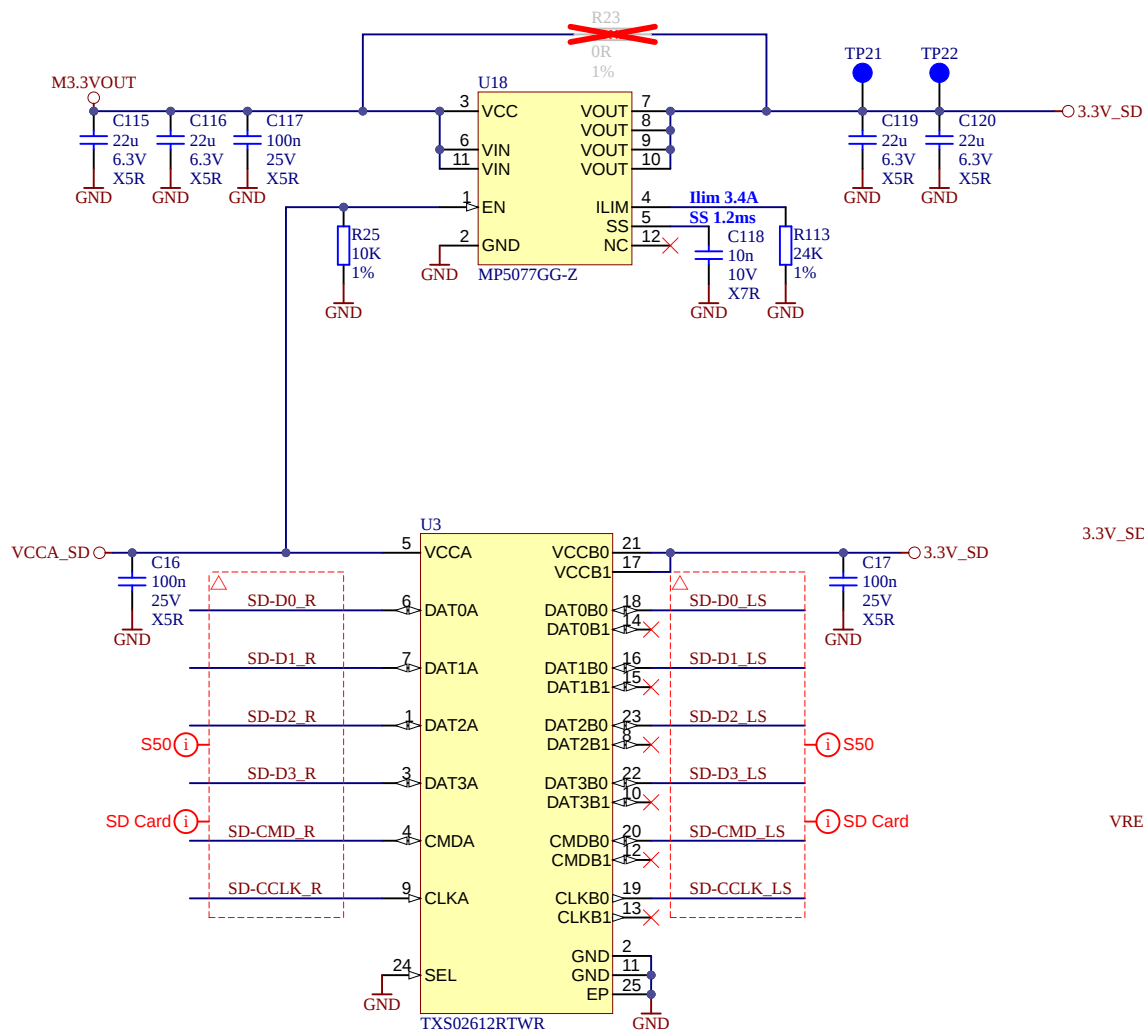
C

C

D

D





	Title: TEF1002 - SD		
	A4	Number: TEF1002 A	Rev. 03
	Date: 09.06.2026	Copyright: Trenz Electronic GmbH	Page 14 of 19
	Filename: SD.SchDoc		

1

2

3

4

A

B

C

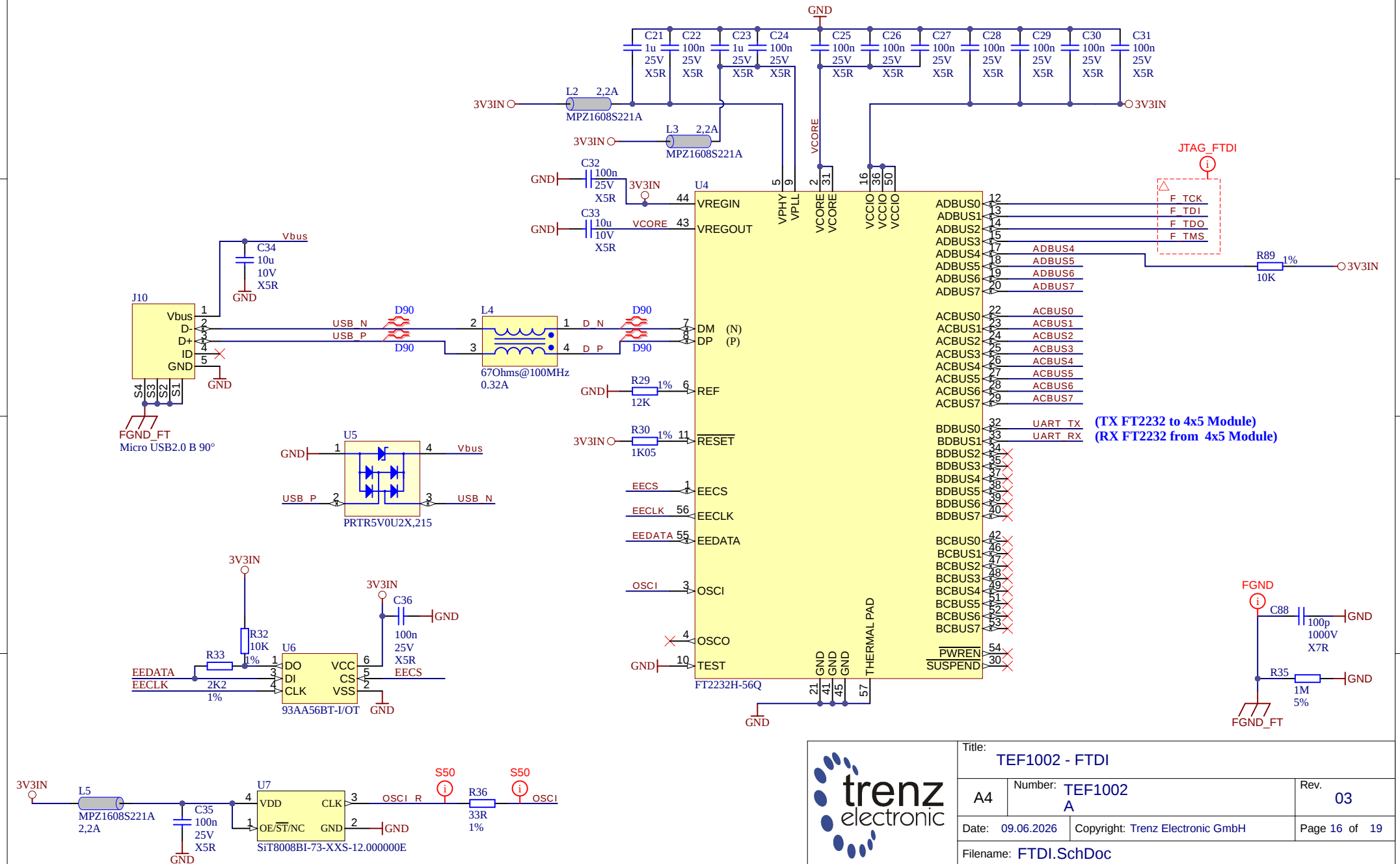
D

A

B

C

D



Title: TEF1002 - FTDI			
A4	Number: TEF1002 A		Rev. 03
Date: 09.06.2026	Copyright: Trenz Electronic GmbH		Page 16 of 19
Filename: FTDI.SchDoc			

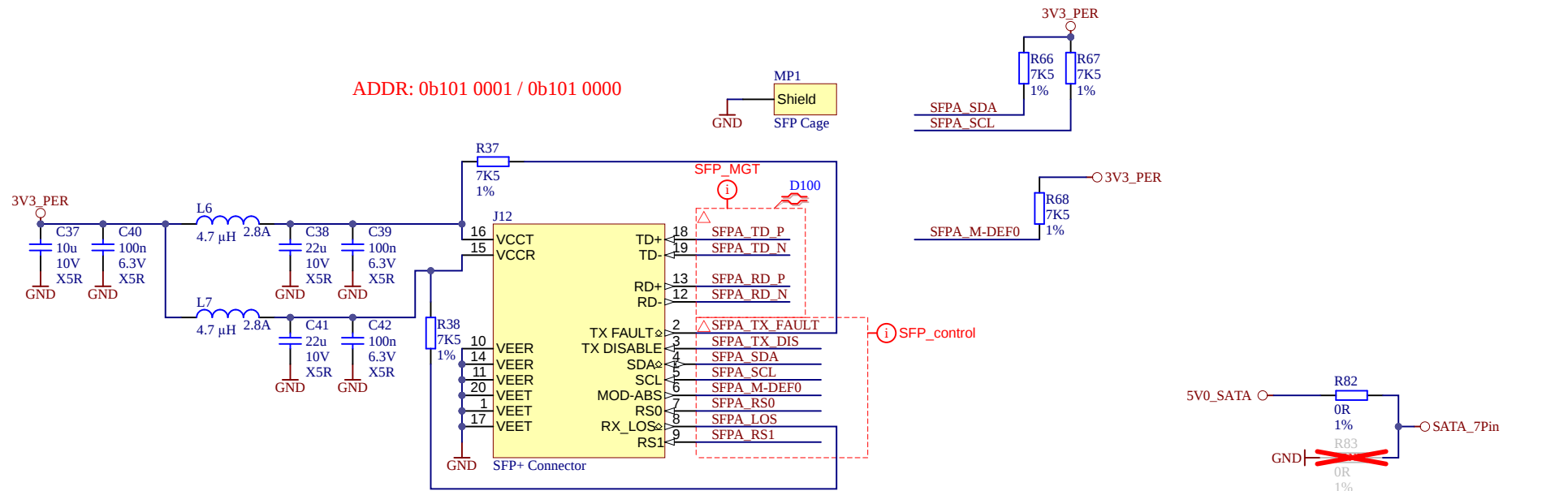
1

2

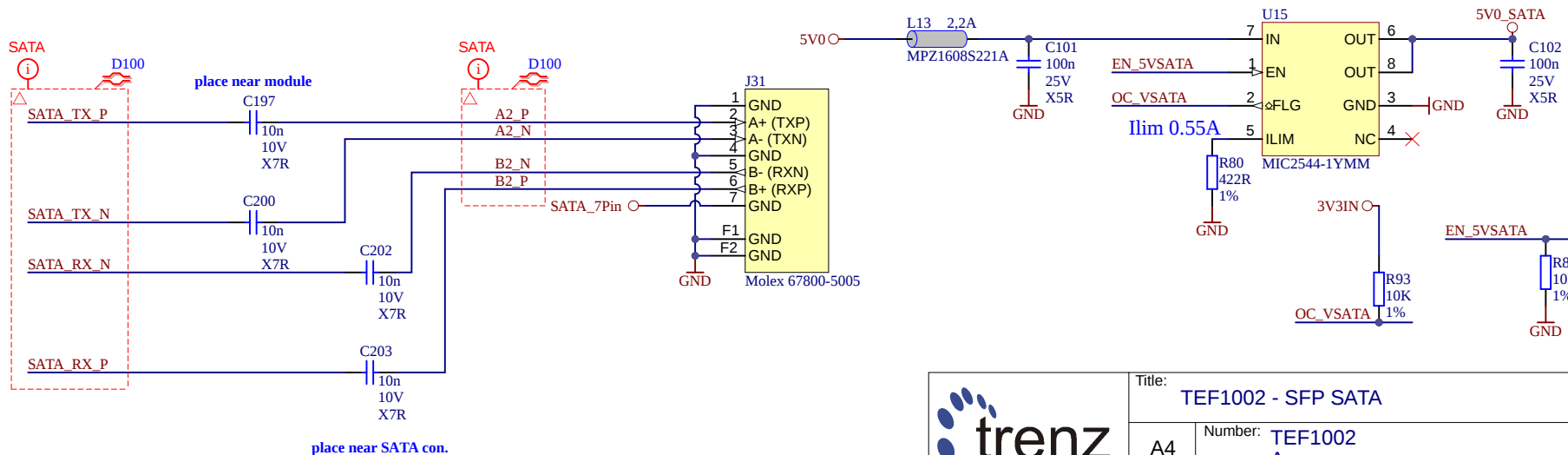
3

4

ADDR: 0b101 0001 / 0b101 0000



if OC_VSATA "LOW" -> disable by CPLD until board reset



Title: TEF1002 - SFP SATA			
A4	Number: TEF1002 A		Rev. 03
Date: 09.06.2026		Copyright: Trenz Electronic GmbH	Page 17 of 19
Filename: SFP SATA.SchDoc			

1

2

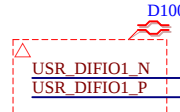
3

4

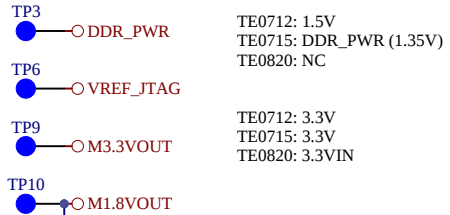
Power from PCIe

~~3.3Vaux_input_PcIe~~
~~2.1A~~
~~12V_input_PcIe~~
~~3A~~
~~3.3V_input_PcIe~~

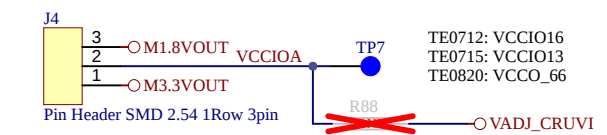
Not Used!



Power from 4x5 module

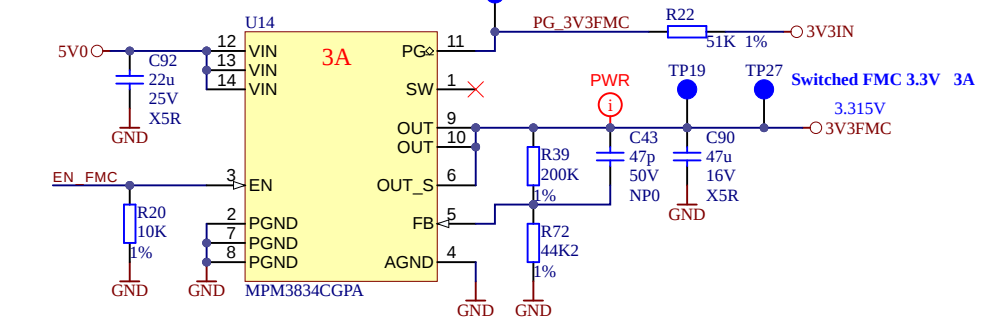
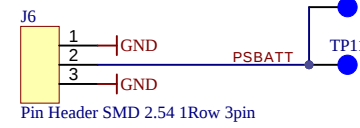
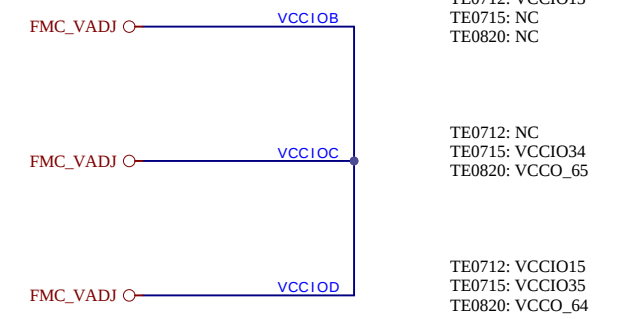
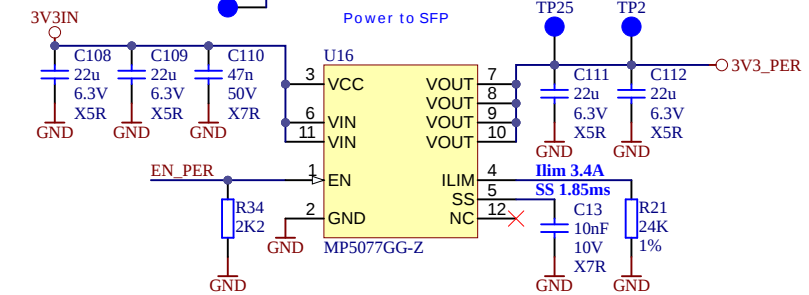


Power to 4x5 module

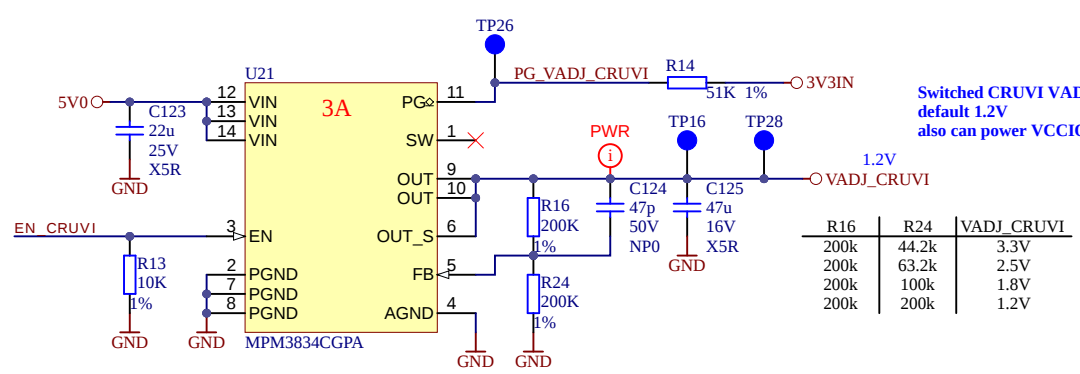


Constant FMC 3.3V 20mA

M3.3VOUT ○ TP17



Switched CRUVI VADJ 3A
default 1.2V
also can power VCCIOA through R88



Title: TEF1002 - PWR1		
A4	Number: TEF1002 A	Rev. 03
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Filename: PWR1.SchDoc		