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Schematics and other handouts serve for informational purposes only!

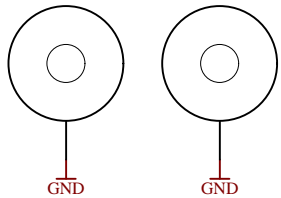


Title: TE0600 - Legal Notices		
A4	Number: TE0600 5211-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH	Page 1 of 13
Filename: Legal_Notices.SchDoc		

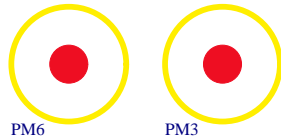
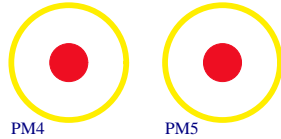
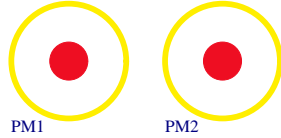
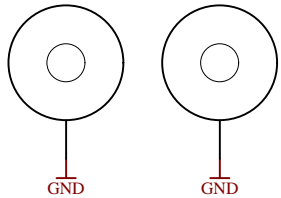
REV	Description	
-01	Initial revision	
-03	<ul style="list-style-type: none"> 1) added NetTie (board revision 03) 2) optimized placement and routing pwr DCDC 3) added tespoints 4) changed OSC U9 (AN25008, SiT8008AI-73-XXS-25.000000E) 5) update Razorbeam Connectors, full update lib 6) added serial number (traceability pad) 7) added thermal vias to mounting holes 8) changed SPI flash (AN26012,W25Q128FVEIG 3V 128MBit Serial Flash) 9) changed DDR3 (AN27202, AN27039) 10) U13 (DS2432P+) is not populated 	
-04	<ul style="list-style-type: none"> 1) Leds @ {"Id": "DPKOIGIM\SYAXGYNW"} , @ {"Id": "NFAQWINK\BHTRJHLT"} were changed to SML-P11MTT86 2) @ {"Id": "RXCWTMNI\KSNDNHO"} was added. @ {"Id": "RXCWTMNI\BJDDGYEG"} was changed from 2.2k to 100 3) @ {"Id": "NFAQWINK\WAVCSPUH"} was changed from single BAT54VV,115 to pair BAT54A,215 4) @ {"Id": "BSVLPKXO\WVYNQEAZ"} was changed from EN6347QI to MPM3860GQW-Z 5) @ {"Id": "BSVLPKXO\BKMDLTRS"} was changed from EP53F8QI to MPM3834CGPA 6) Stacked vias were removed 7) Net BR0 was connected to GND 8) B2B signal groups information was added 9) Field filename was renamed for all schematic pages 10) Legal Notices page was added 11) System overview and power-on sequencing were added for TE0600.SchDoc page 12) Testpoints @ {"Id": "GTKBAXHQ\YOBNRKRX"} - @ {"Id": "GTKBAXHQ\VIYNLZMN"} , @ {"Id": "GTKBAXHQ\ODTFUWM"} - @ {"Id": "GTKBAXHQ\PNEPKLPC"} were added 	MT

	Title: TE0600 - Changes list		
	A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
	Date: 12/2/2024	Copyright: Trenz Electronic GmbH	Page 2 of 13
	Filename: Revision_Changes.SchDoc		

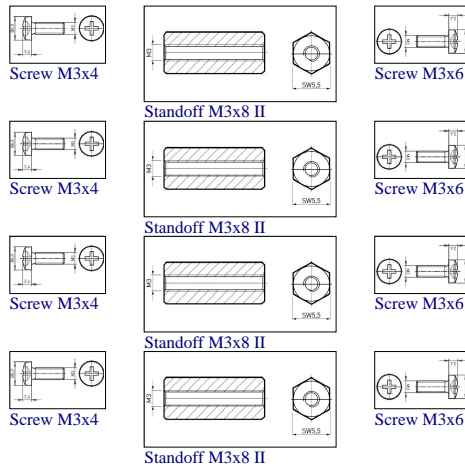
Mount.Hole 3.2mm Mount.Hole 3.2mm



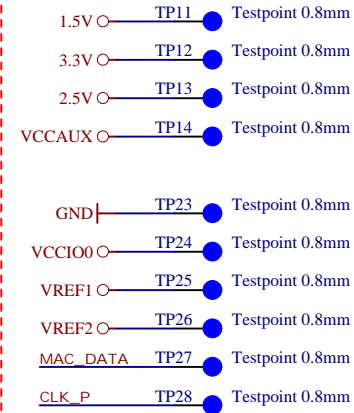
GND Mount.Hole 3.2mm Mount.Hole 3.2mm



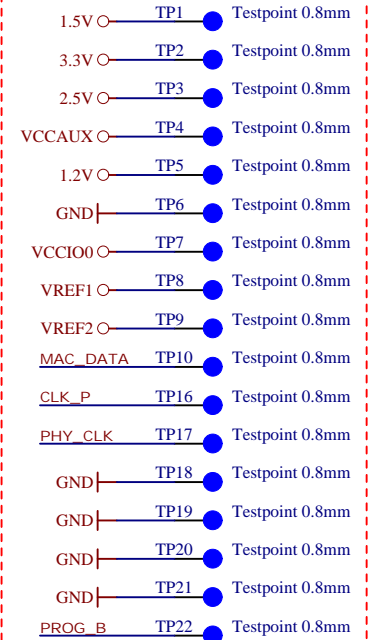
Top of Board



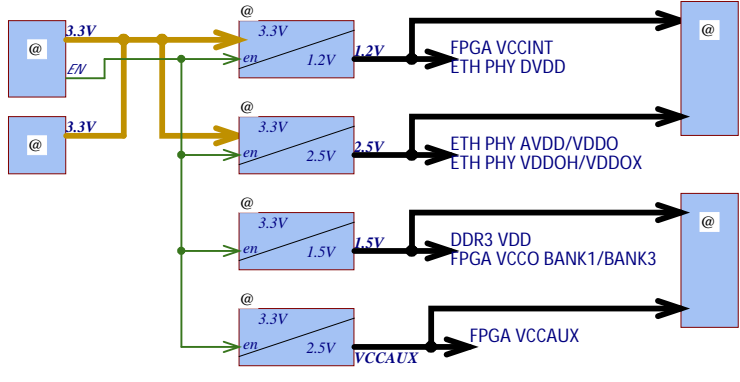
Top side testpoints:



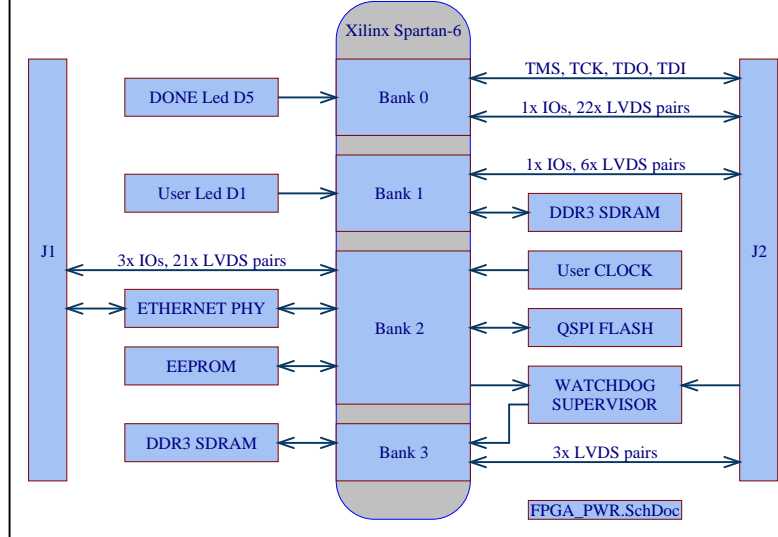
Bottom side testpoints:



Power-on sequencing



System Overview



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO0	IN	1.1 - 3.45V	+/-5%	IO Bank0	-
1.2V	OUT	1.2V	+/-3%	Power for Carrier	-
1.5V	OUT	1.5V	+/-3%	Power for Carrier	-
2.5V	OUT	2.5V	+/-3%	Power for Carrier	-
VCCAUX	OUT	2.5V	+/-3%	Power for Carrier	-

Special notes:

VariantNote1
VariantNote2

CE
CE-TOPOVERLAY
RoHS
RoHS-TOPOVERLAY
WEEE
WEEE-TOPOVERLAY
Serial
Serialnumber 6,3 x 6.3mm



Title: TE0600		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 3 of 13
Filename: TE0600.SchDoc		

B2: 45 Pins: 21 Differential; 3.3V Fixed VCCIO
 ETHERNET PHY 10/100/1G

B0: 45 Pins: 22 Differential; variable VCCIO
 B1: 13 Pins: 6 Differential; 1.5V Fixed
 B3: 6 Pins: 3 Differential; 1.5V Fixed
 JTAG: 3.3V Level

A

A

B

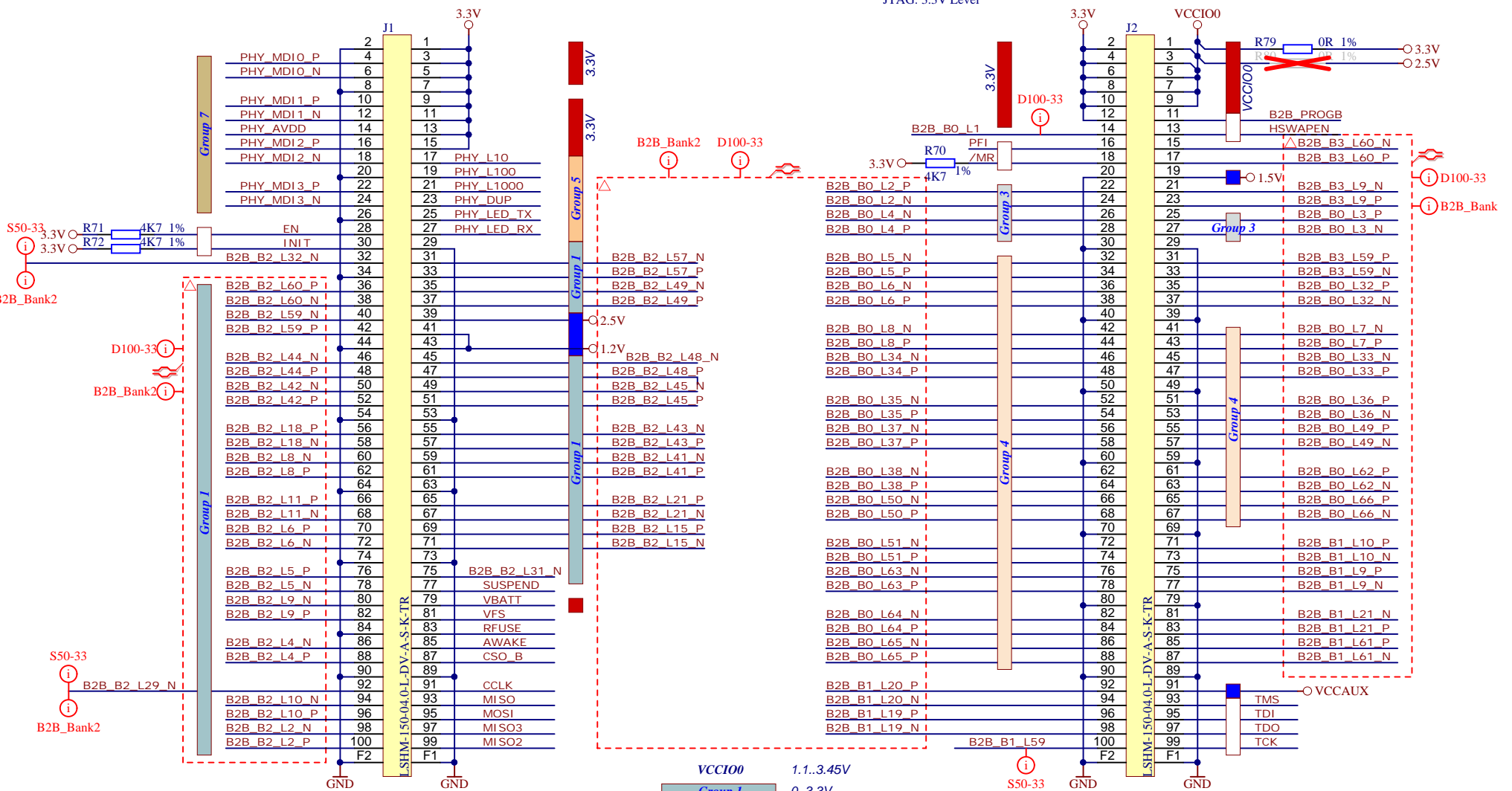
B

C

C

D

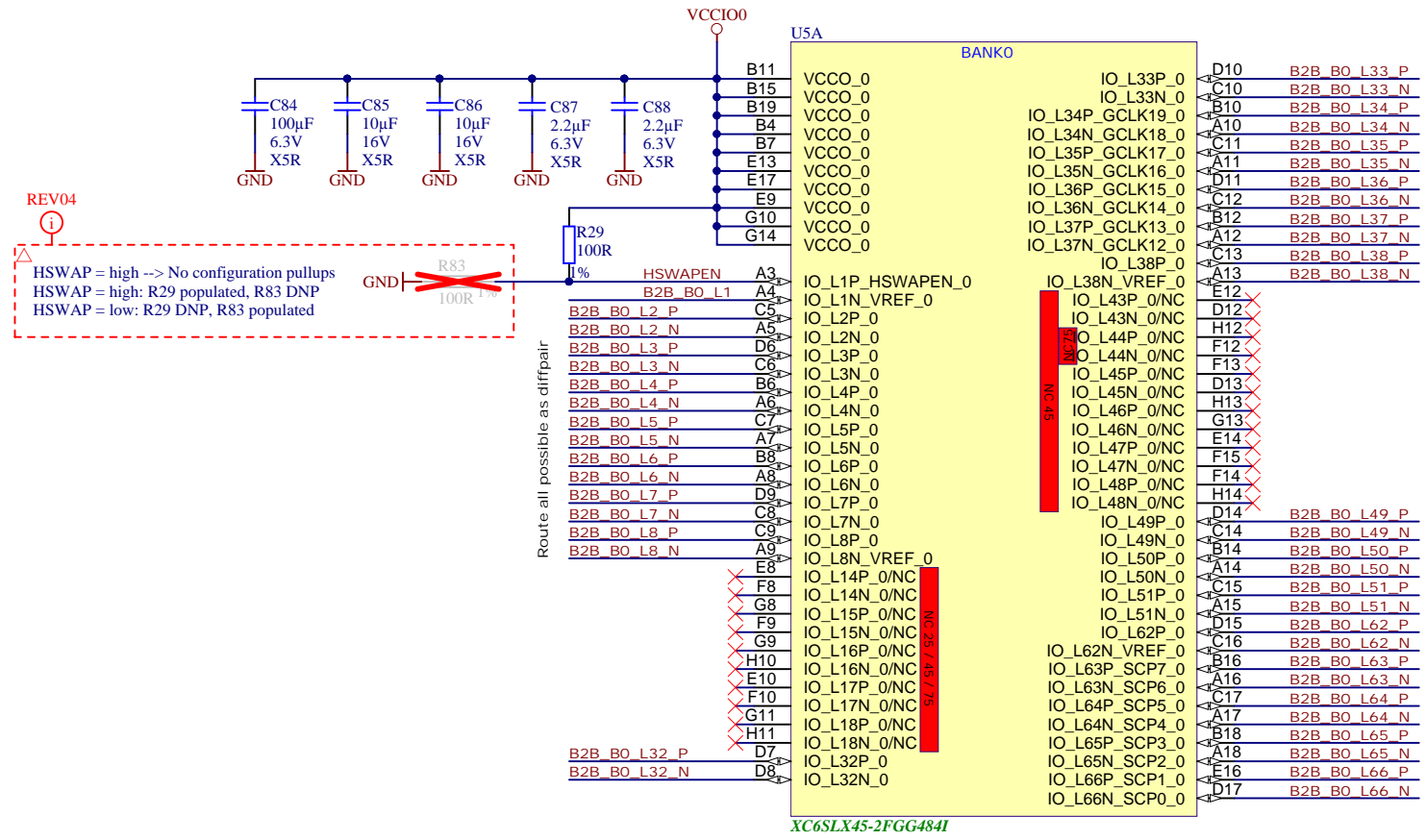
D



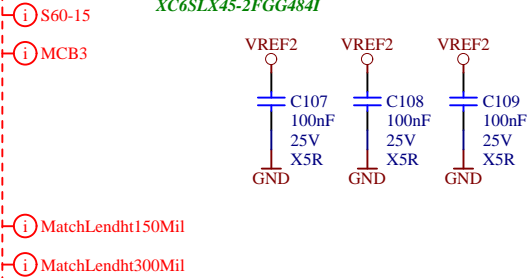
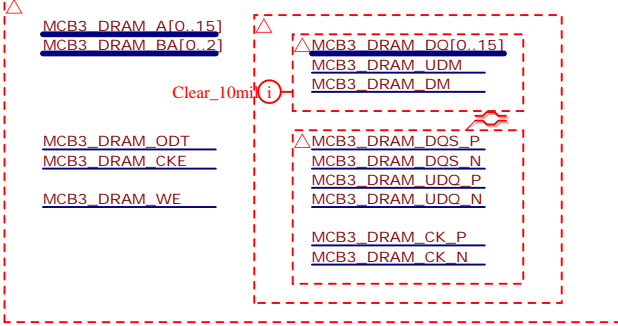
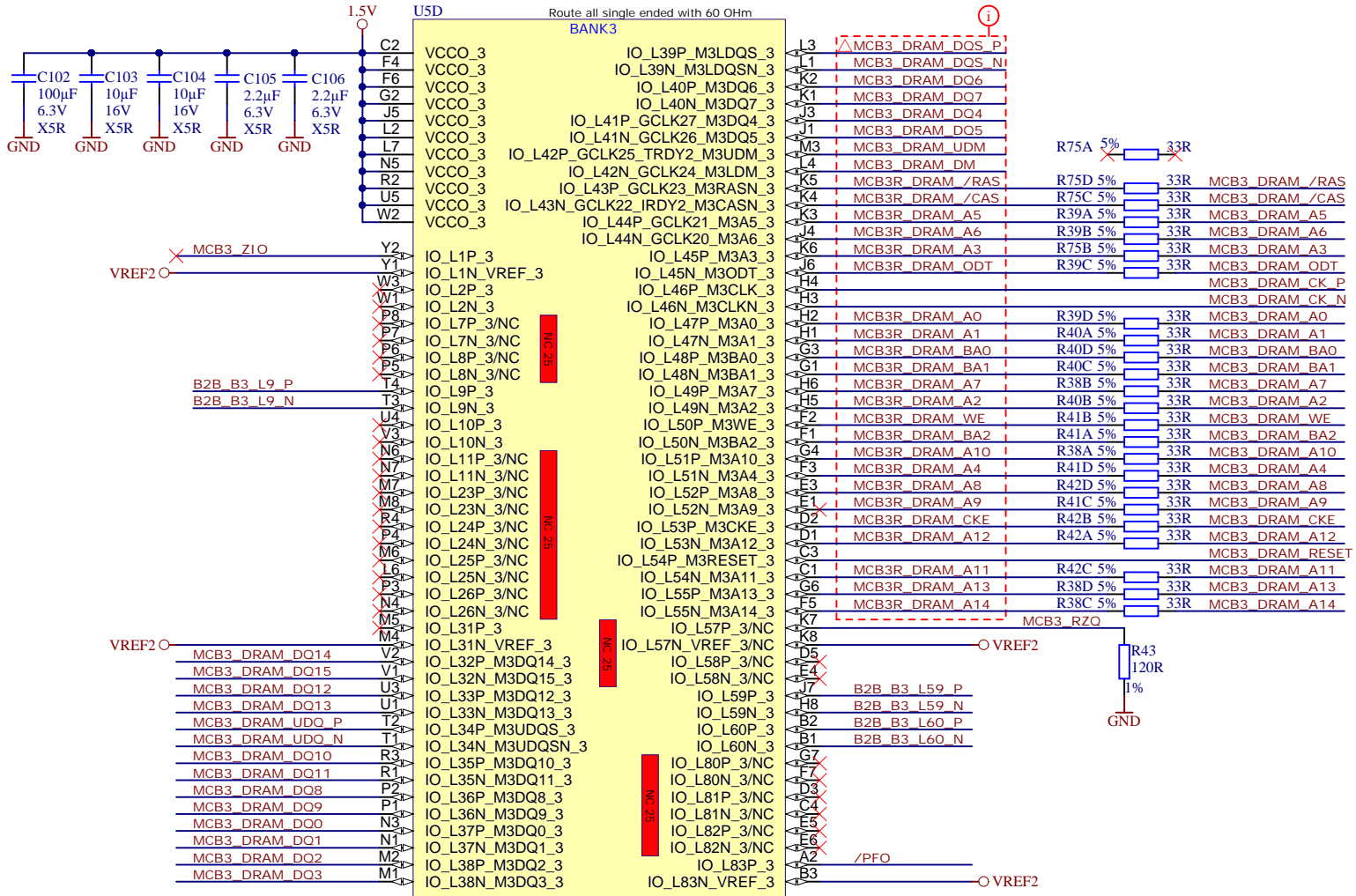
VCCIO0	1.1...3.45V
Group 1	0..3.3V
Group 3	0..VCCIO0
Group 4	0..VCCIO0
Group 5	0..VCCIO0
Group 7	ETHERNET
Special	
	PWR_in
	PWR_out



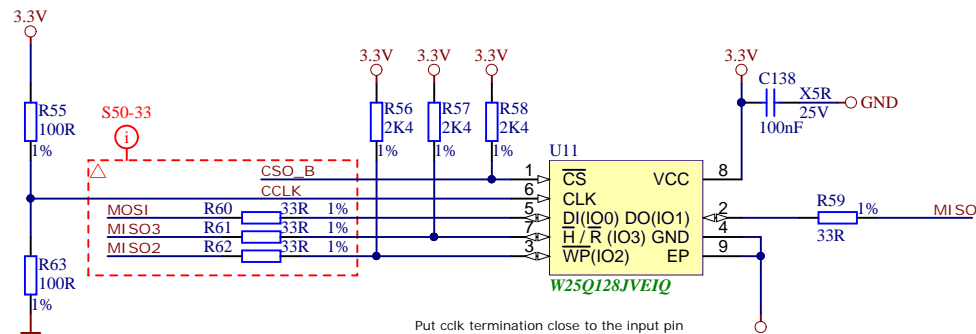
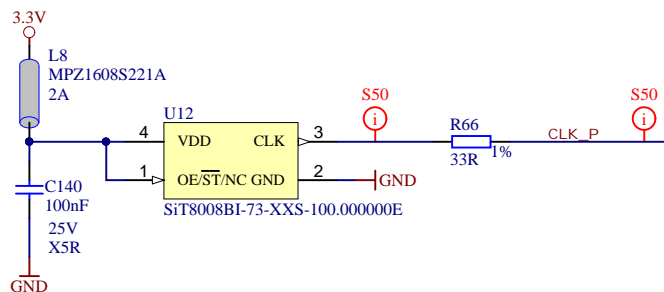
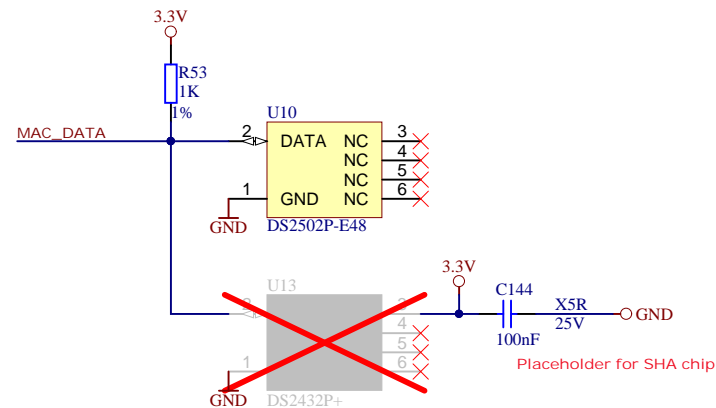
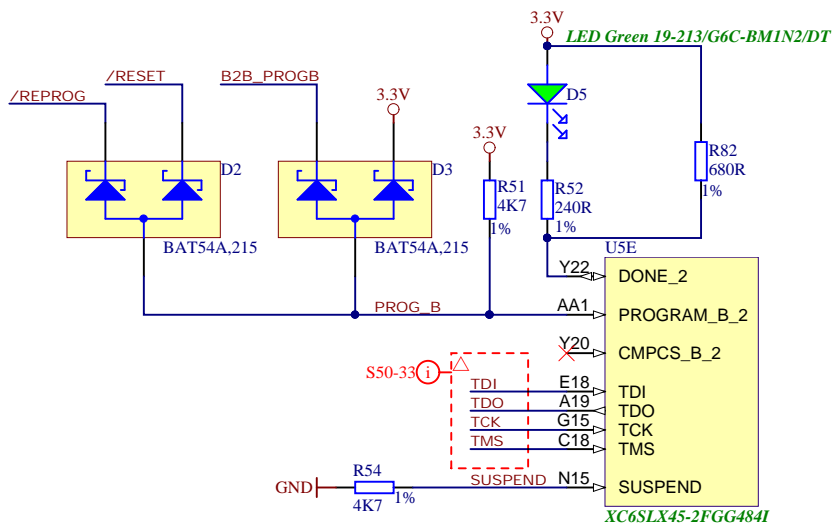
Title: TE0600 - B2B Connectors		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 4 of 13
Filename: B2B.SchDoc		



Title: TE0600 - FPGA BANK0			
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04	
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 5 of 13	
Filename: BANK0.SchDoc			



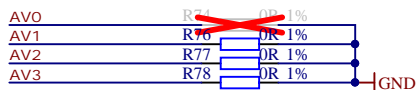
Title: TE0600 - FPGA BANK3 DDR		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 8 of 13
Filename: BANK3_DDR.SchDoc		



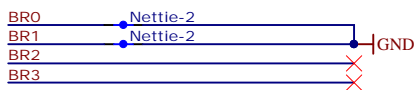
AV0 = 0 -> commercial AV0 = 1 -> Industrial
 AV1 = 0 -> speedgrade 2 AV1 = 1 -> speedgrade 3
 AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte
 AV3 = Open -> Customized variants

BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02
1	1	0	1	-03
1	1	0	0	-04

Assembly Variants

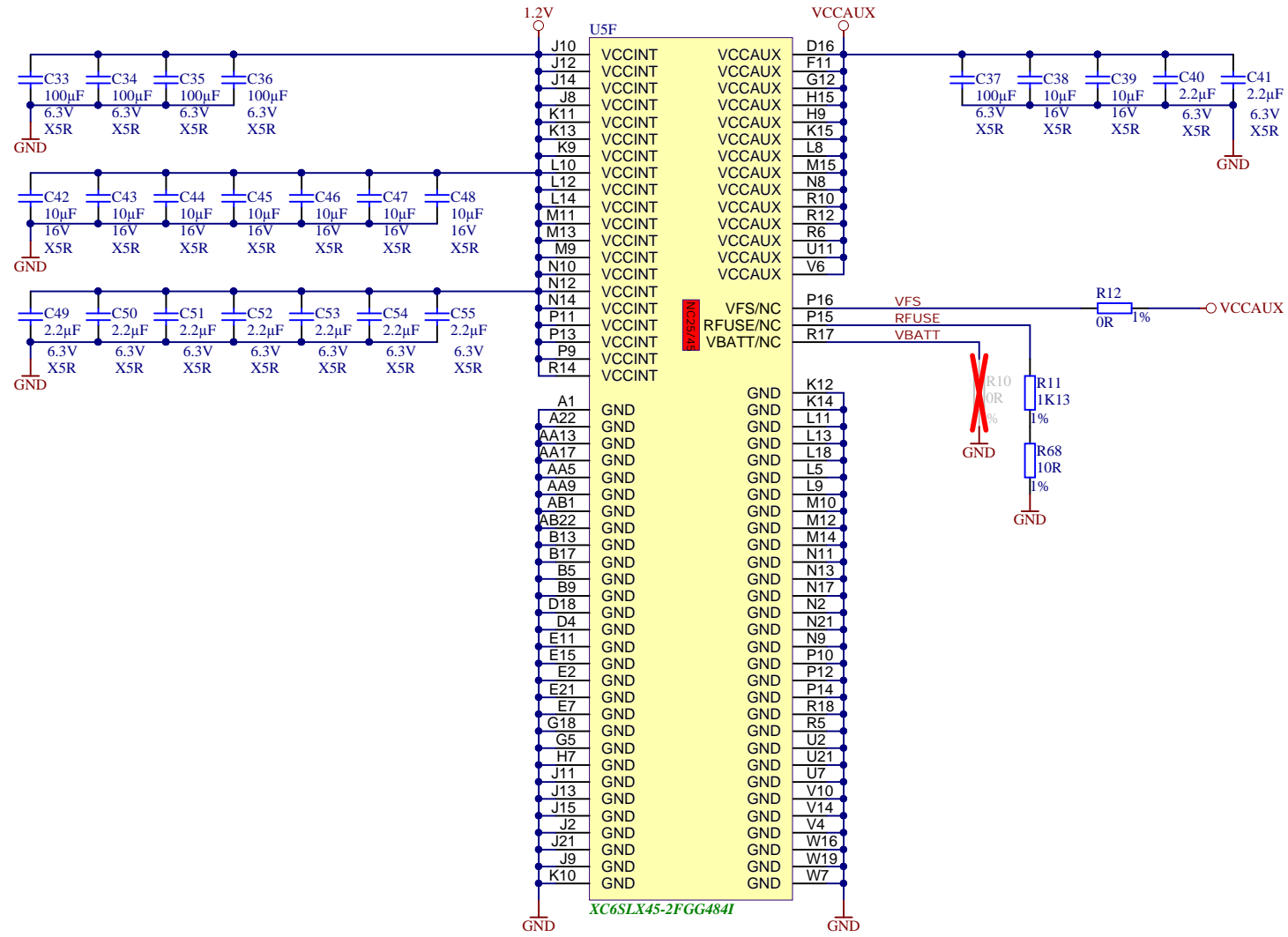



Board Revisions



Enable pullups in FPGA

Title: TE0600 - FPGA CFG		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 9 of 13
Filename: FPGA_CFG.SchDoc		



			Title: TE0600 - FPGA_PWR	
			A4	Number: GigaBee FPGA Module 52111-A
Date: 12/2/2024		Copyright: Trenz Electronic GmbH / TT		Page 10 of 13
Filename: FPGA_PWR.SchDoc				

A

B

C

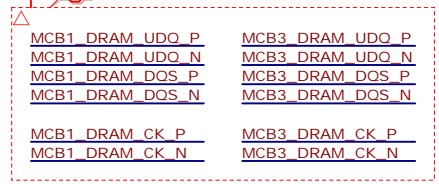
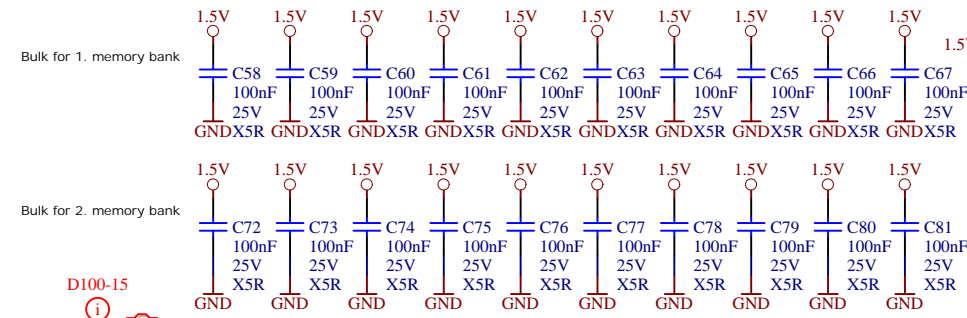
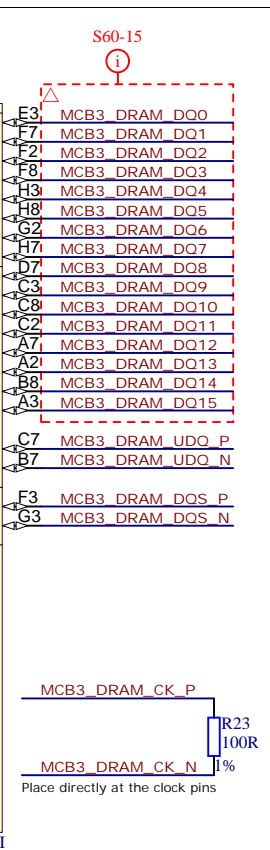
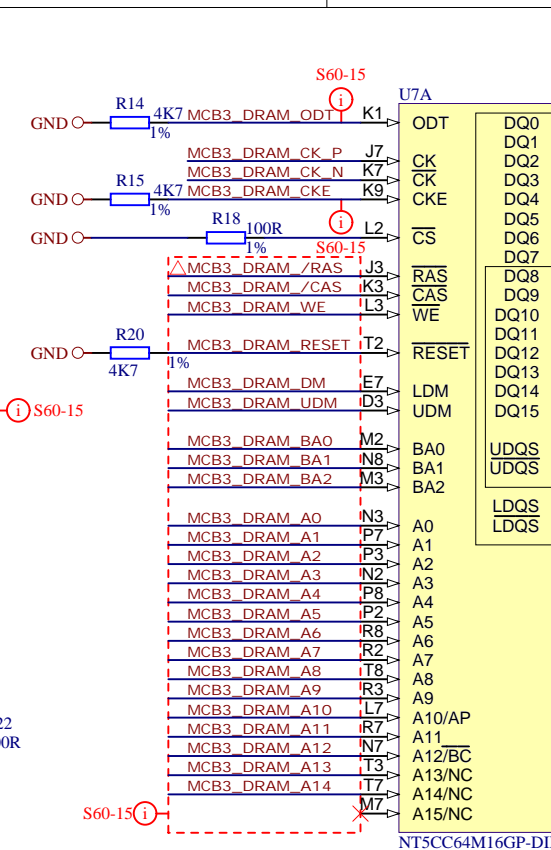
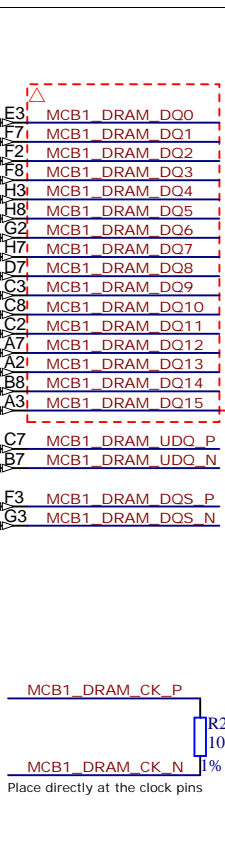
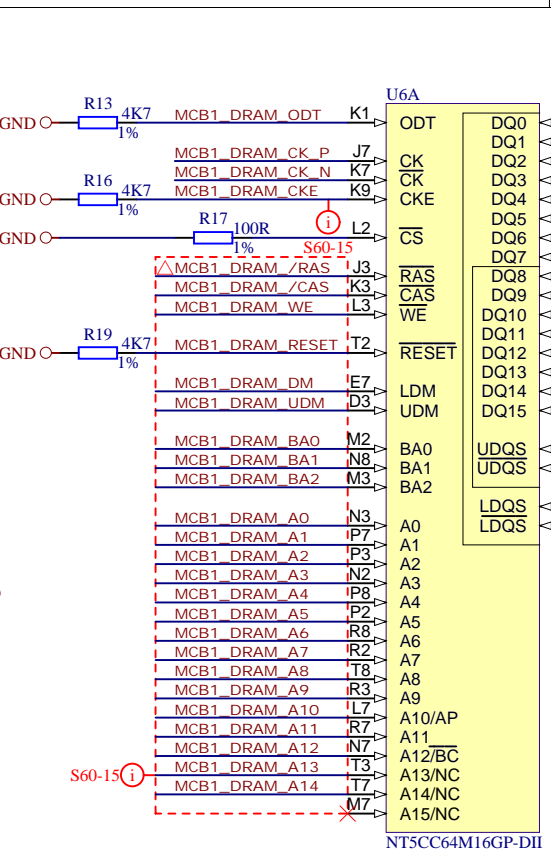
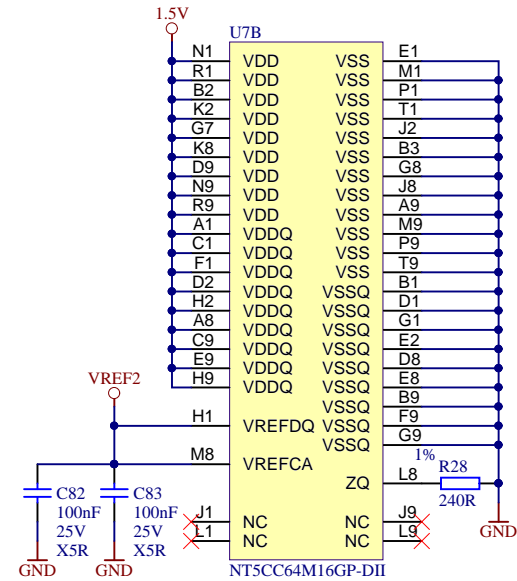
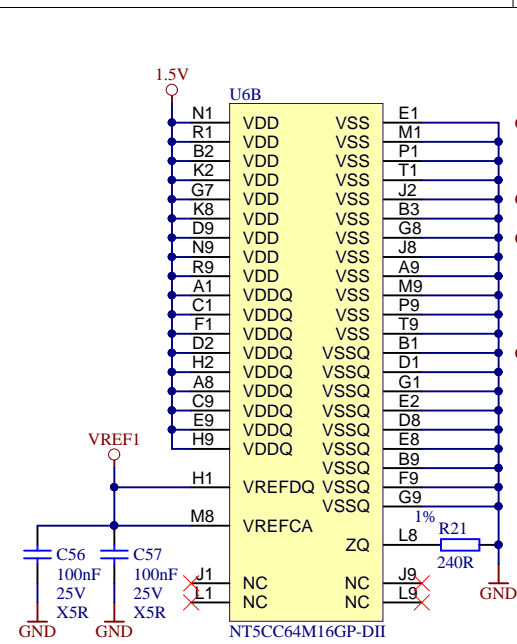
D

A

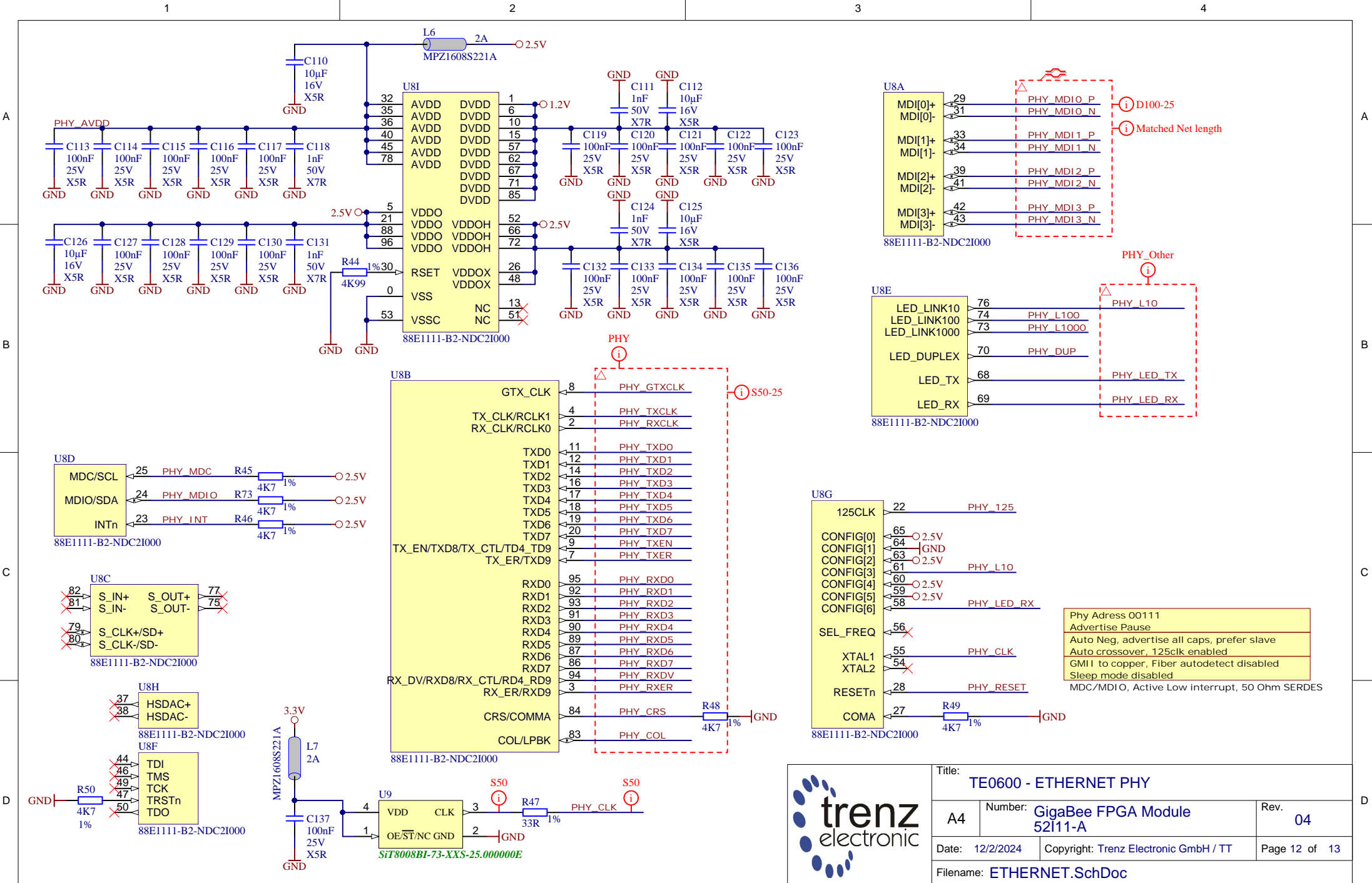
B

C

D



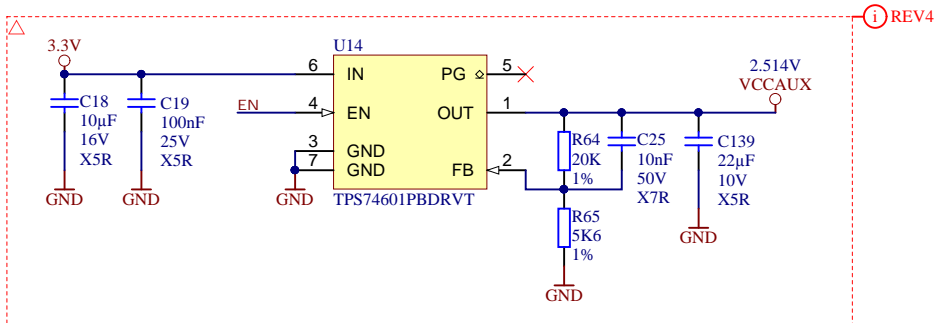
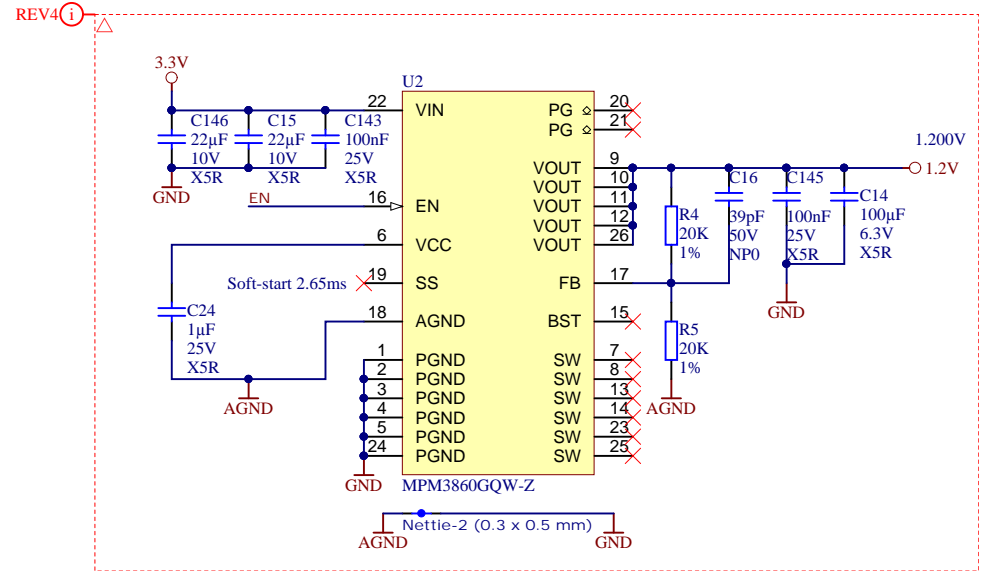
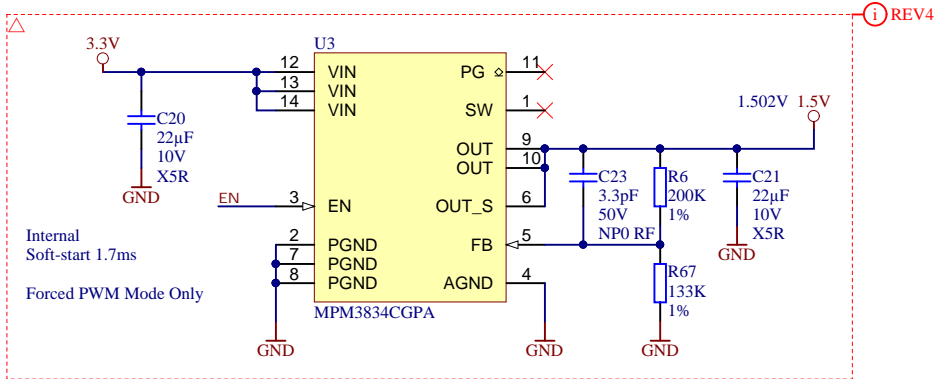
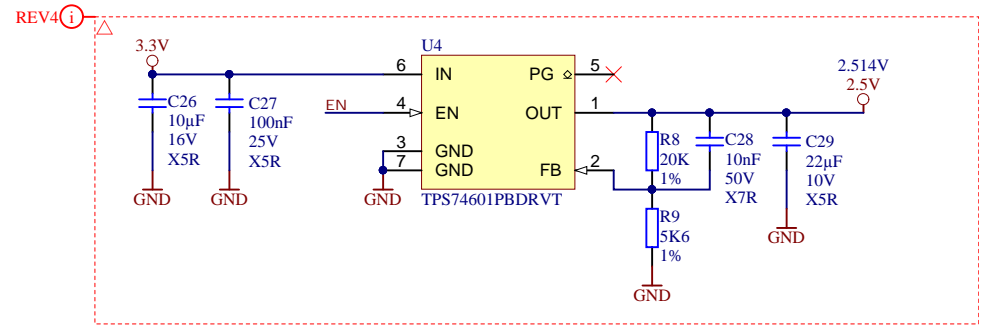
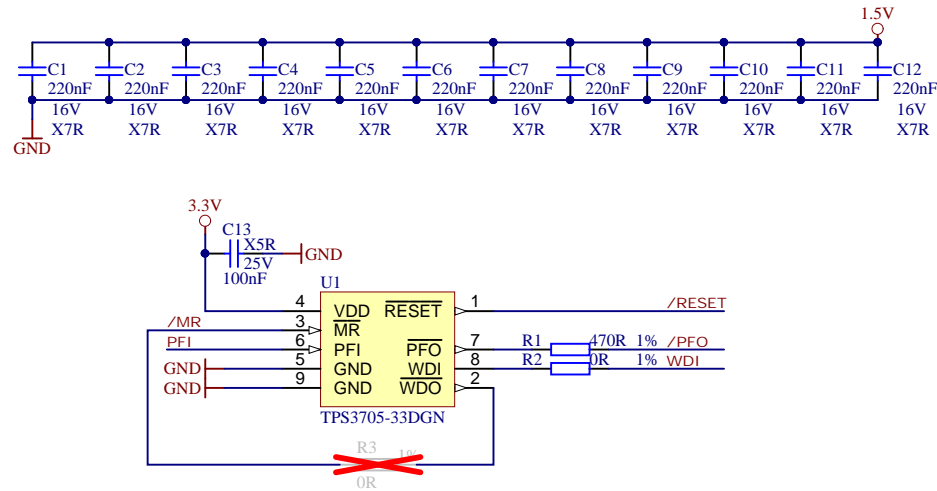
Title: TE0600 - DDR3 RAM		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 11 of 13
Filename: DDR3.SchDoc		




Phy Adress 00111
 Advertise Pause
 Auto Neg, advertise all caps, prefer slave
 Auto crossover, 125clk enabled
 GMII to copper, Fiber autotdetect disabled
 Sleep mode disabled
 MDC/MDIO, Active Low interrupt, 50 Ohm SERDES



Title: TE0600 - ETHERNET PHY		
A4	Number: GigaBee FPGA Module 52111-A	Rev. 04
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Page 12 of 13		
Filename: ETHERNET.SchDoc		



			Title: TE0600 - POWER	
			A4	Number: GigaBee FPGA Module 52111-A
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Filename: POWER.SchDoc				