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Schematics and other handouts serve for informational purposes only!

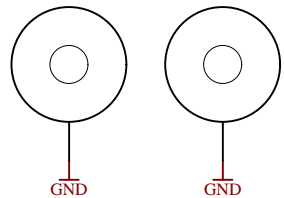


Title: <b>TE0600 - Legal Notices</b>		
A4	Number: <b>TE0600 83C21-A</b>	Rev. <b>04</b>
Date: <b>12/2/2024</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>13</b>
Filename: <b>Legal_Notices.SchDoc</b>		

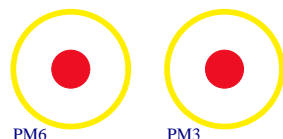
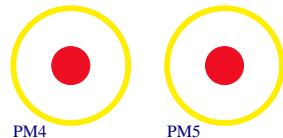
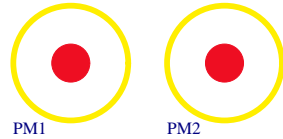
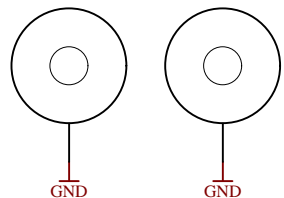
REV	Description	
-01	Initial revision	
-03	<ul style="list-style-type: none"> <li>1) added NetTie (board revision 03)</li> <li>2) optimized placement and routing pwr DCDC</li> <li>3) added tespoints</li> <li>4) changed OSC U9 (AN25008, SiT8008AI-73-XXS-25.000000E)</li> <li>5) update Razorbeam Connectors, full update lib</li> <li>6) added serial number (traceability pad)</li> <li>7) added thermal vias to mounting holes</li> <li>8) changed SPI flash (AN26012,W25Q128FVEIG 3V 128MBit Serial Flash)</li> <li>9) changed DDR3 (AN27202, AN27039)</li> <li>10) U13 (DS2432P+) is not populated</li> </ul>	
-04	<ul style="list-style-type: none"> <li>1) Leds @ {"Id": "DPKOIGIM\SYAXGYNW"} , @ {"Id": "NFAQWINK\BHTRJHLT"} were changed to SML-P11MTT86</li> <li>2) @ {"Id": "RXCWTMNI\KSNDNHO"} was added. @ {"Id": "RXCWTMNI\BJDDGYEG"} was changed from 2.2k to 100</li> <li>3) @ {"Id": "NFAQWINK\WAVCSPUH"} was changed from single BAT54VV,115 to pair BAT54A,215</li> <li>4) @ {"Id": "BSVLPKXO\WVYNQEAZ"} was changed from EN6347QI to MPM3860GQW-Z</li> <li>5) @ {"Id": "BSVLPKXO\BKMDLTRS"} was changed from EP53F8QI to MPM3834CGPA</li> <li>6) Stacked vias were removed</li> <li>7) Net BR0 was connected to GND</li> <li>8) B2B signal groups information was added</li> <li>9) Field filename was renamed for all schematic pages</li> <li>10) Legal Notices page was added</li> <li>11) System overview and power-on sequencing were added for TE0600.SchDoc page</li> <li>12) Testpoints @ {"Id": "GTKBAXHQ\YOBNRKRX"} - @ {"Id": "GTKBAXHQ\VIYNLZMN"} , @ {"Id": "GTKBAXHQ\ODTFOUWM"} - @ {"Id": "GTKBAXHQ\PNEPKLPC"} were added</li> </ul>	MT

	Title: TE0600 - Changes list		
	A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
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	Filename: Revision_Changes.SchDoc		

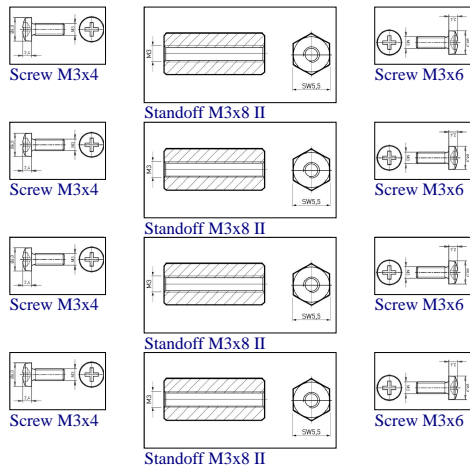
Mount.Hole 3.2mm Mount.Hole 3.2mm



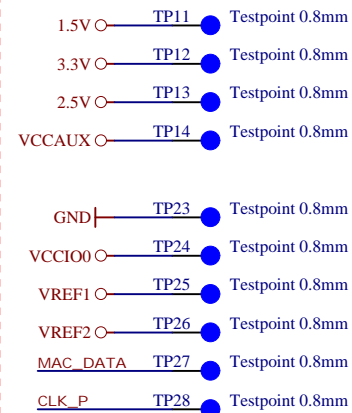
GND Mount.Hole 3.2mm Mount.Hole 3.2mm



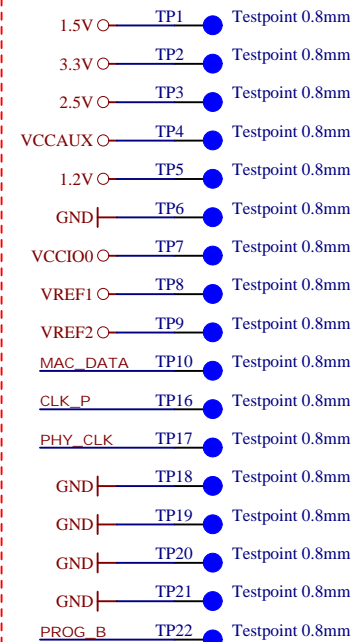
Top of Board



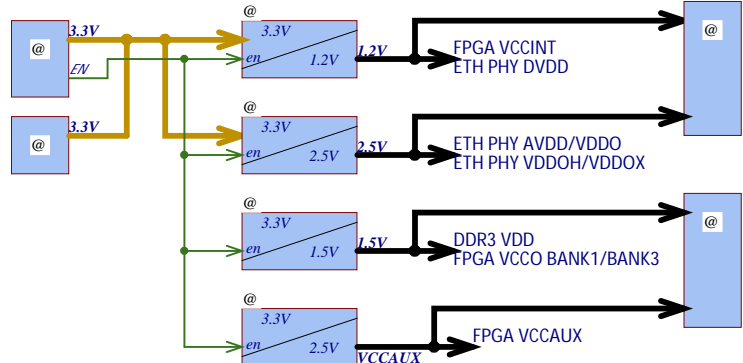
Top side testpoints:



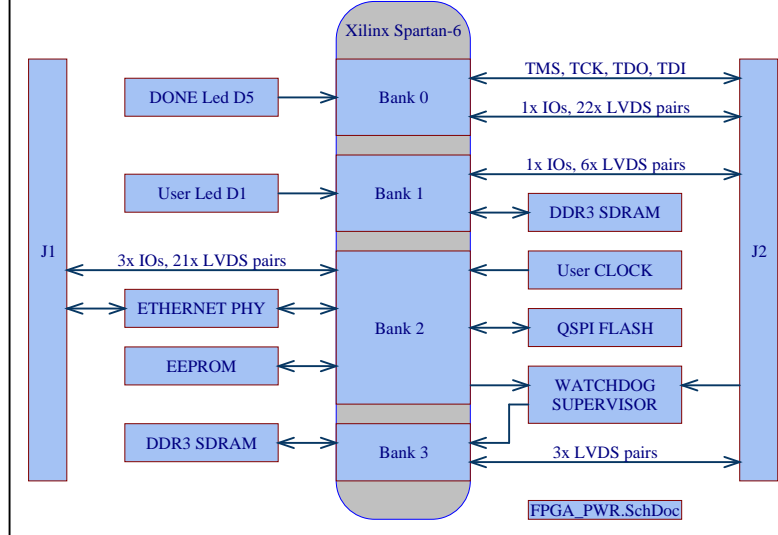
Bottom side testpoints:



Power-on sequencing



System Overview



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO0	IN	1.1 - 3.45V	+/-5%	IO Bank0	-
1.2V	OUT	1.2V	+/-3%	Power for Carrier	-
1.5V	OUT	1.5V	+/-3%	Power for Carrier	-
2.5V	OUT	2.5V	+/-3%	Power for Carrier	-
VCCAUX	OUT	2.5V	+/-3%	Power for Carrier	-

Special notes:

VariantNote1  
VariantNote2

CE  
CE-TOPOVERLAY  
RoHS  
RoHS-TOPOVERLAY  
WEEE  
WEEE-TOPOVERLAY  
Serial  
Serialnumber 6,3 x 6.3mm



Title: TE0600		
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B2: 45 Pins: 21 Differential; 3.3V Fixed VCCIO  
 ETHERNET PHY 10/100/1G

B0: 45 Pins: 22 Differential; variable VCCIO  
 B1: 13 Pins: 6 Differential; 1.5V Fixed  
 B3: 6 Pins: 3 Differential; 1.5V Fixed  
 JTAG: 3.3V Level

A

A

B

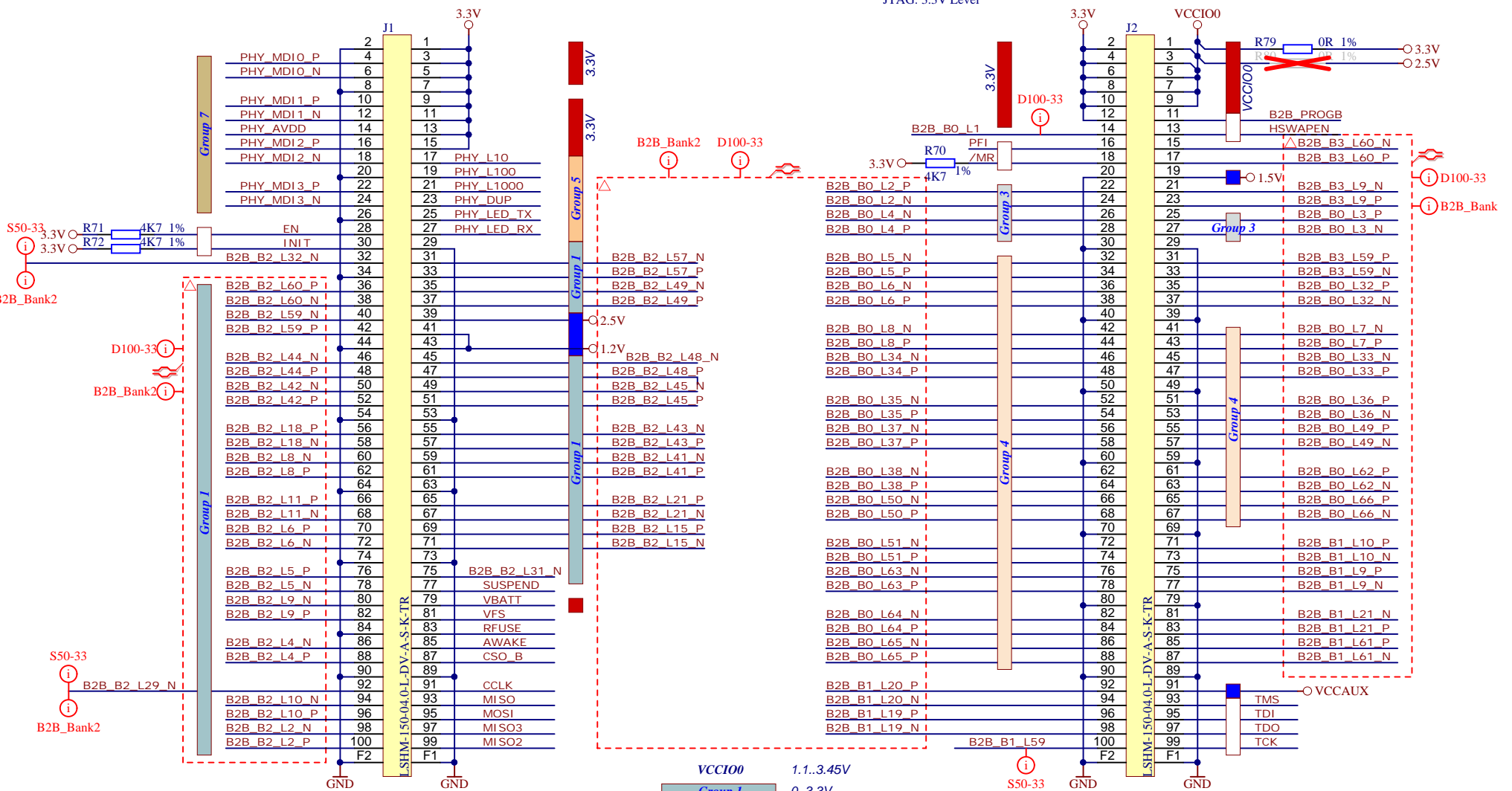
B

C

C

D

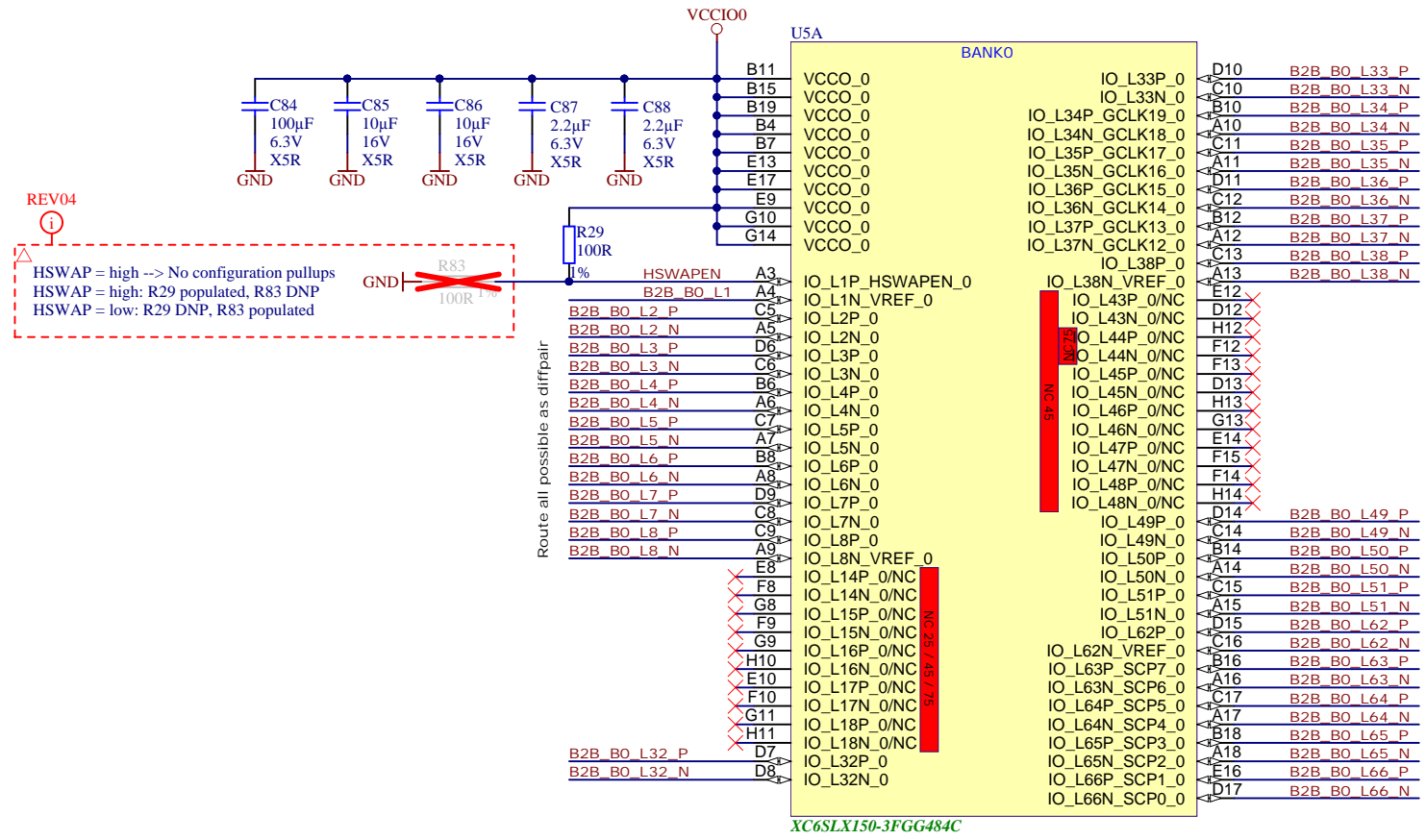
D



VCCIO0	1.1...3.45V
Group 1	0..3.3V
Group 3	0..VCCIO0
Group 4	0..VCCIO0
Group 5	0..VCCIO0
Group 7	ETHERNET
Special	
	PWR_in
	PWR_out



Title: TE0600 - B2B Connectors		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
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Filename: B2B.SchDoc		



Title: TE0600 - FPGA BANK0		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 5 of 13
Filename: BANK0.SchDoc		

A

B

C

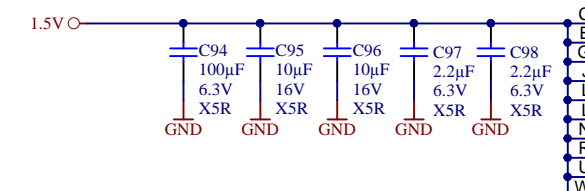
D

A

B

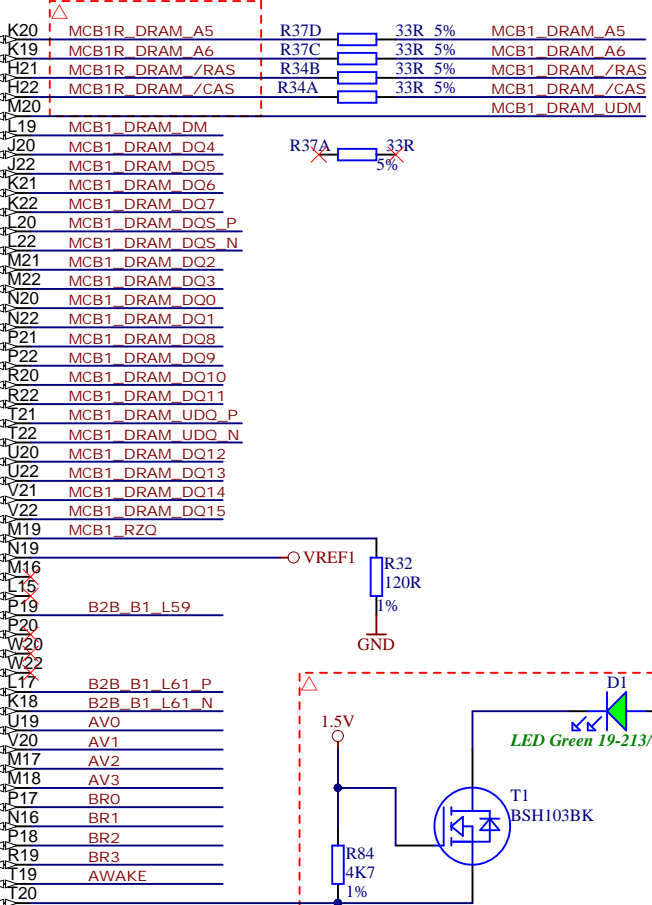
C

D



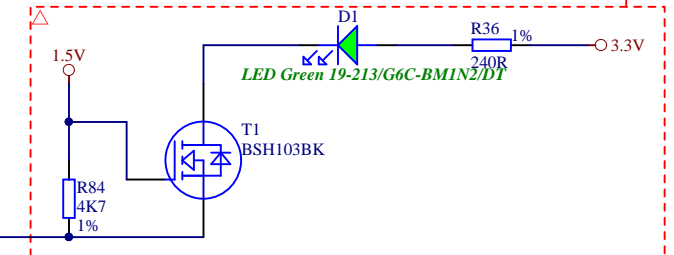
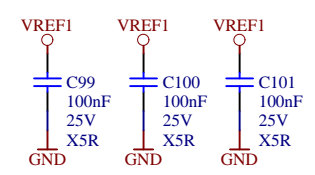
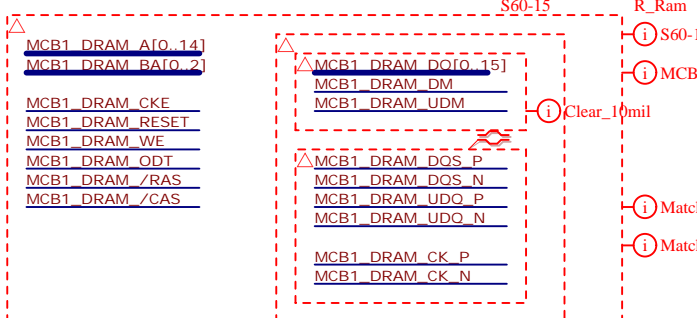
U5B

BANK1	
VCCO_1	IO_L40P_GCLK11_M1A5_1
VCCO_1	IO_L40N_GCLK10_M1A6_1
VCCO_1	IO_L41P_GCLK9_IRDY1_M1RASN_1
VCCO_1	IO_L41N_GCLK8_M1CASN_1
VCCO_1	IO_L42P_GCLK7_M1UDM_1
VCCO_1	IO_L42N_GCLK6_TRDY1_M1LDM_1
VCCO_1	IO_L43P_GCLK5_M1DQ4_1
VCCO_1	IO_L43N_GCLK4_M1DQ5_1
VCCO_1	IO_L44P_A3_M1DQ6_1
VCCO_1	IO_L44N_A2_M1DQ7_1
VCCO_1	IO_L45P_A1_M1LDQS_1
VCCO_1	IO_L45N_A0_M1LDQSN_1
VCCO_1	IO_L46P_FCS_B_M1DQ2_1
VCCO_1	IO_L46N_FOE_B_M1DQ3_1
VCCO_1	IO_L47P_FWE_B_M1DQ0_1
VCCO_1	IO_L47N_LDC_M1DQ1_1
VCCO_1	IO_L48P_HDC_M1DQ8_1
VCCO_1	IO_L48N_M1DQ9_1
VCCO_1	IO_L49P_M1DQ10_1
VCCO_1	IO_L49N_M1DQ11_1
VCCO_1	IO_L50P_M1UDQS_1
VCCO_1	IO_L50N_M1UDQSN_1
VCCO_1	IO_L51P_M1DQ12_1
VCCO_1	IO_L51N_M1DQ13_1
VCCO_1	IO_L52P_M1DQ14_1
VCCO_1	IO_L52N_M1DQ15_1
VCCO_1	IO_L53P_1
VCCO_1	IO_L53N_VREF_1
VCCO_1	IO_L58P_1/NC
VCCO_1	IO_L58N_1/NC
VCCO_1	IO_L59P_1
VCCO_1	IO_L59N_1
VCCO_1	IO_L60P_1
VCCO_1	IO_L60N_1
VCCO_1	IO_L61P_1
VCCO_1	IO_L61N_1
VCCO_1	IO_L70P_1/NC
VCCO_1	IO_L70N_1/NC
VCCO_1	IO_L71P_1/NC
VCCO_1	IO_L71N_1/NC
VCCO_1	IO_L72P_1/NC
VCCO_1	IO_L72N_1/NC
VCCO_1	IO_L73P_1/NC
VCCO_1	IO_L73N_1/NC
VCCO_1	IO_L74P_AWAKE_1
VCCO_1	IO_L74N_DOUT_BUSY_1
VCCO_1	IO_L39P_M1A3_1
VCCO_1	IO_L39N_M1ODT_1



MCB1_DRAM_A13	R31D	5%	33R	MCB1R_DRAM_A13	D19
MCB1_DRAM_A14	R31B	5%	33R	MCB1R_DRAM_A14	D20
MCB1_DRAM_RESET				MCB1_DRAM_RESET	F18
MCB1_DRAM_A11	R31C	5%	33R	MCB1R_DRAM_A11	F19
MCB1_DRAM_CKE	R33B	5%	33R	MCB1R_DRAM_CKE	D21
MCB1_DRAM_A12	R33A	5%	33R	MCB1R_DRAM_A12	D22
MCB1_DRAM_A8	R33D	5%	33R	MCB1R_DRAM_A8	C20
MCB1_DRAM_A9	R33C	5%	33R	MCB1R_DRAM_A9	C22
MCB1_DRAM_A10	R35D	5%	33R	MCB1R_DRAM_A10	G19
MCB1_DRAM_A4	R31A	5%	33R	MCB1R_DRAM_A4	F20
MCB1_DRAM_WE	R35B	5%	33R	MCB1R_DRAM_WE	H19
MCB1_DRAM_BA2	R35C	5%	33R	MCB1R_DRAM_BA2	H18
MCB1_DRAM_A7	R30D	5%	33R	MCB1R_DRAM_A7	E20
MCB1_DRAM_A2	R30C	5%	33R	MCB1R_DRAM_A2	E22
MCB1_DRAM_BA0	R35A	5%	33R	MCB1R_DRAM_BA0	J17
MCB1_DRAM_BA1	R37B	5%	33R	MCB1R_DRAM_BA1	K17
MCB1_DRAM_A0	R30B	5%	33R	MCB1R_DRAM_A0	F21
MCB1_DRAM_A1	R30A	5%	33R	MCB1R_DRAM_A1	F22
MCB1_DRAM_CK_P				MCB1_DRAM_CK_P	H20
MCB1_DRAM_CK_N				MCB1_DRAM_CK_N	J19
MCB1_DRAM_A3	R34D	5%	33R	MCB1R_DRAM_A3	G20
MCB1_DRAM_ODT	R34C	5%	33R	MCB1R_DRAM_ODT	G22

XC6SLX150-3FGG484C

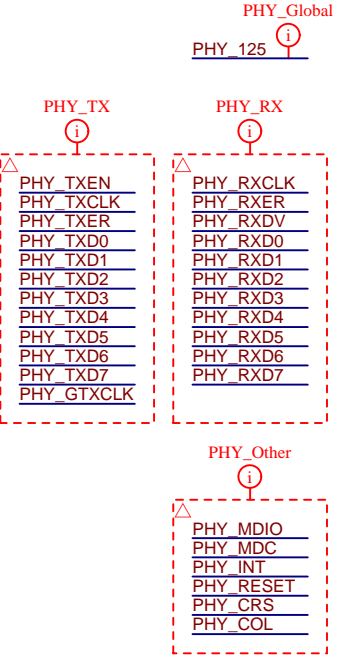
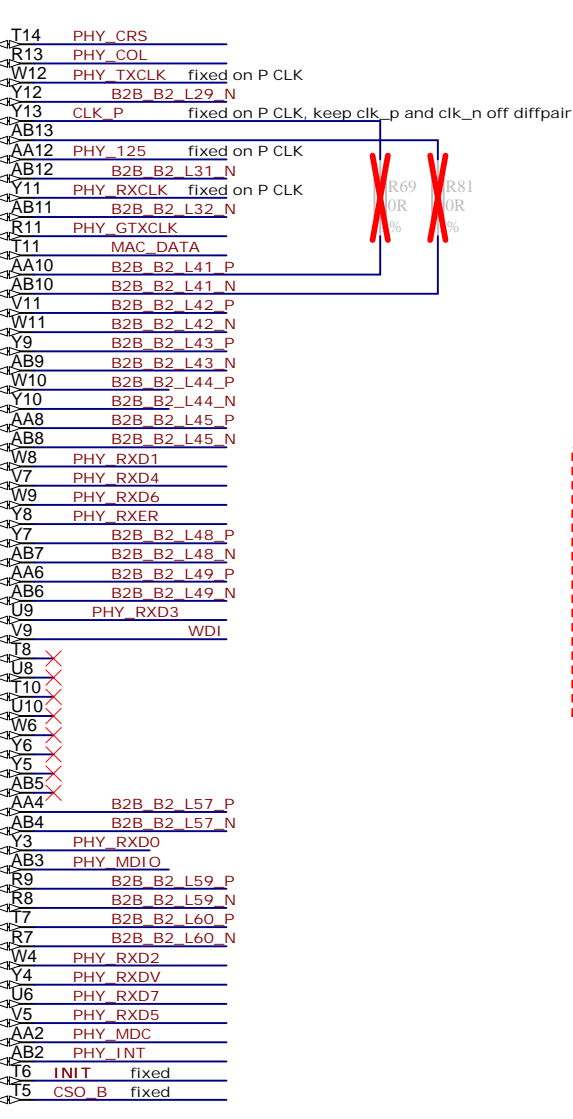
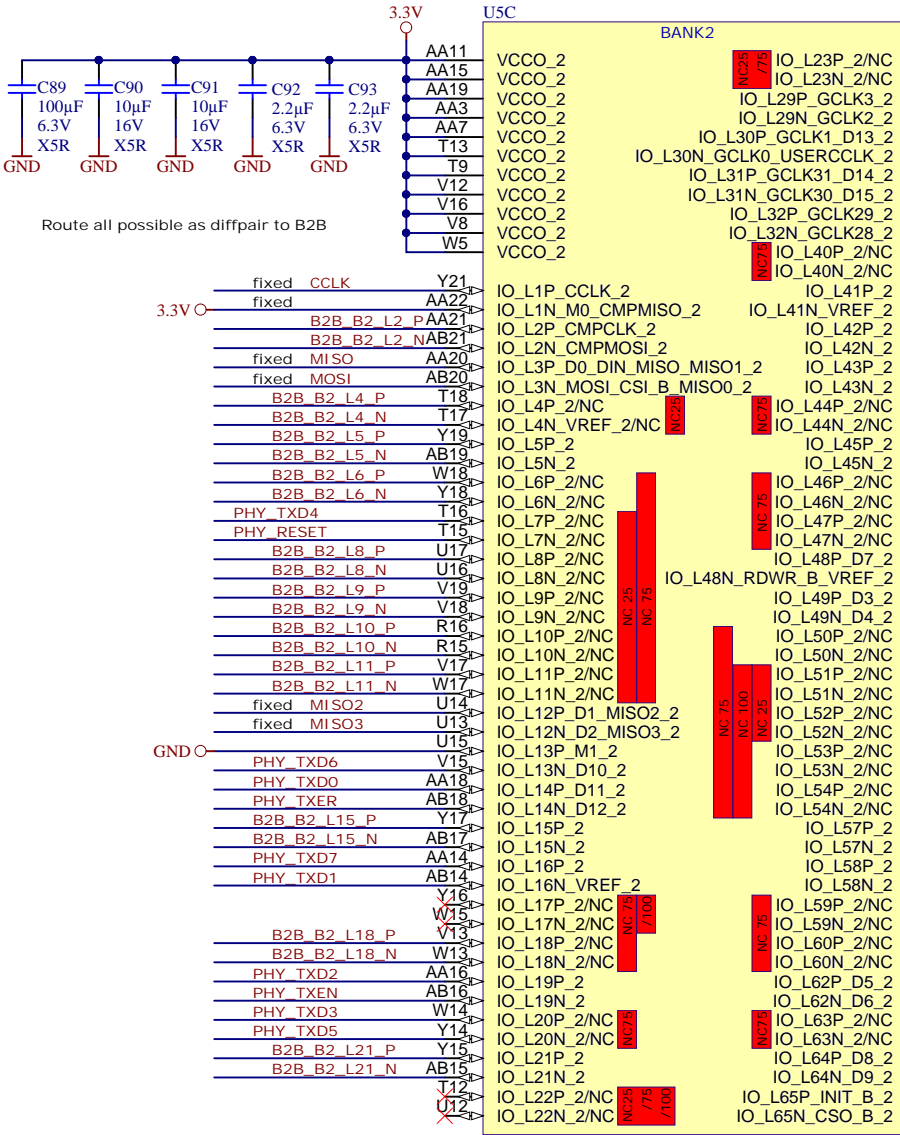


Title: TE0600 - FPGA BANK1 DDR		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 6 of 13
Filename: BANK1_DDR.SchDoc		

B2B\_Bank2 S50-33

D100-33

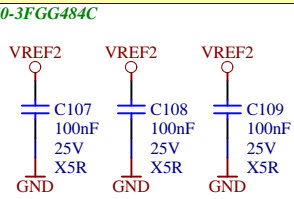
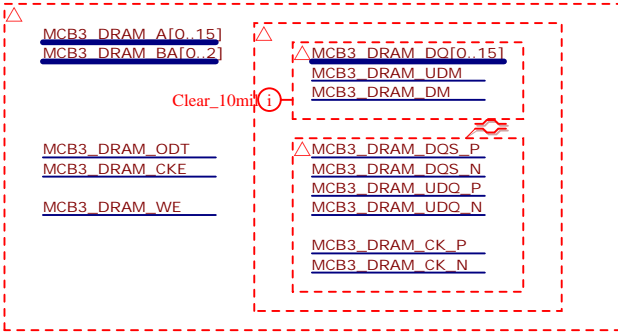
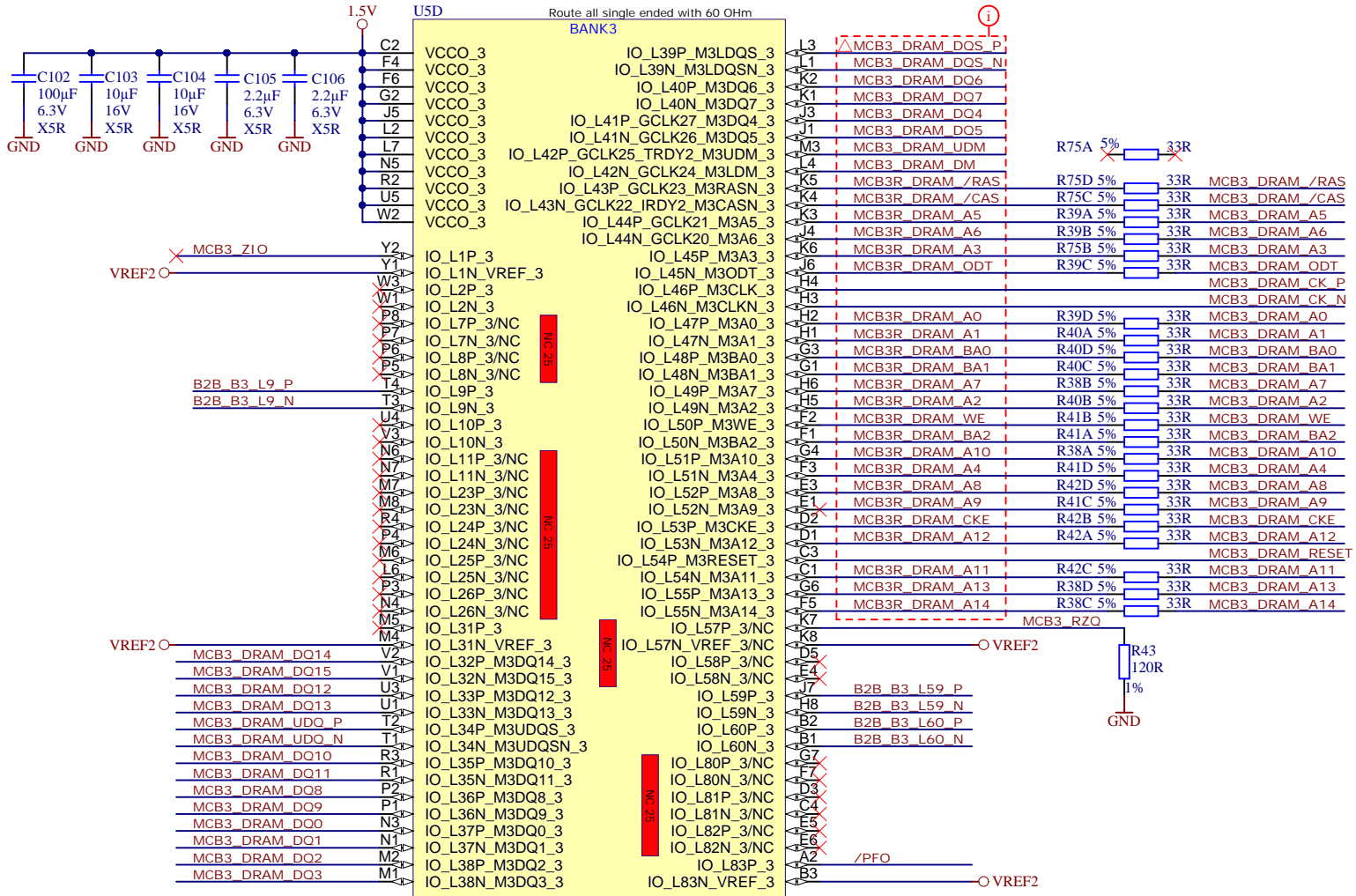
△ B2B B2 L2 P
B2B B2 L2 N
B2B B2 L4 P
B2B B2 L4 N
B2B B2 L5 P
B2B B2 L5 N
B2B B2 L6 P
B2B B2 L6 N
B2B B2 L8 P
B2B B2 L8 N
B2B B2 L9 P
B2B B2 L9 N
B2B B2 L10 P
B2B B2 L10 N
B2B B2 L11 P
B2B B2 L11 N
B2B B2 L15 N
B2B B2 L15 P
B2B B2 L18 P
B2B B2 L18 N
B2B B2 L21 P
B2B B2 L21 N
B2B B2 L41 P
B2B B2 L41 N
B2B B2 L42 P
B2B B2 L42 N
B2B B2 L43 P
B2B B2 L43 N
B2B B2 L44 P
B2B B2 L44 N
B2B B2 L45 P
B2B B2 L45 N
B2B B2 L48 P
B2B B2 L48 N
B2B B2 L49 P
B2B B2 L49 N
B2B B2 L57 P
B2B B2 L57 N
B2B B2 L59 P
B2B B2 L59 N
B2B B2 L60 P
B2B B2 L60 N
B2B B2 L29 N
B2B B2 L31 N
B2B B2 L32 N



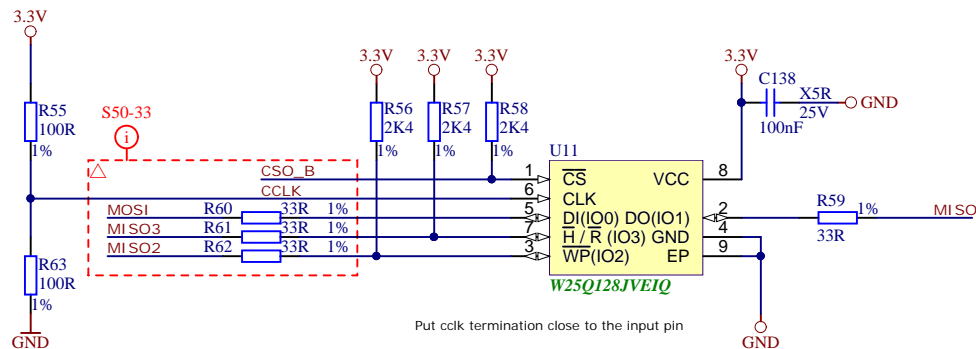
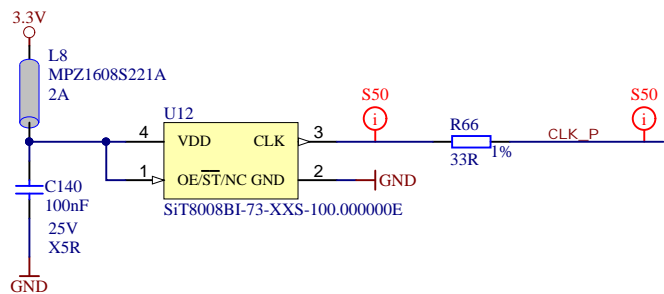
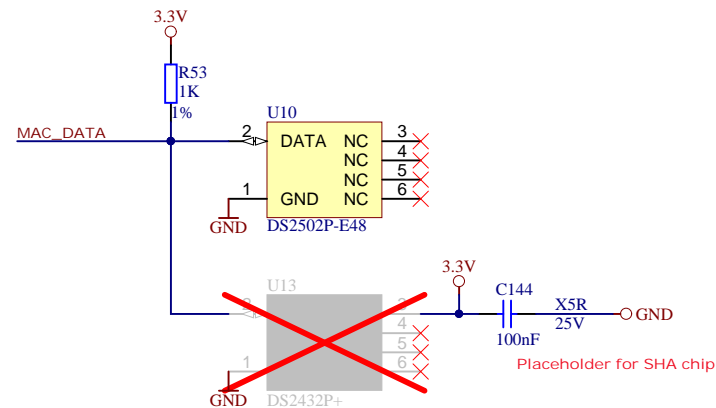
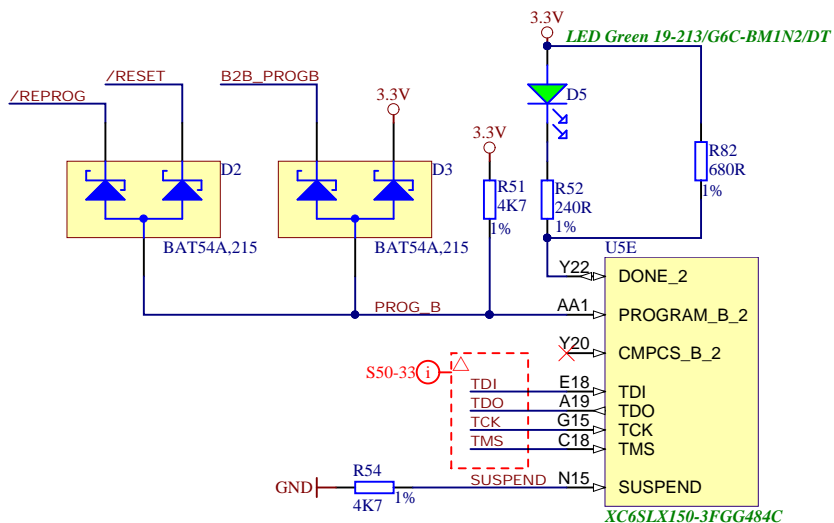
Don't use pins, which are marked NC100



Title: TE0600 - FPGA BANK2		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 7 of 13
Filename: BANK2.SchDoc		



Title: <b>TE0600 - FPGA BANK3 DDR</b>		
A4	Number: <b>GigaBee FPGA Module 83C21-A</b>	Rev. <b>04</b>
Date: <b>12/2/2024</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>13</b>
Filename: <b>BANK3_DDR.SchDoc</b>		



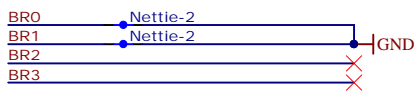
AV0 = 0 -> commercial AV0 = 1 -> Industrial  
 AV1 = 0 -> speedgrade 2 AV1 = 1 -> speedgrade 3  
 AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte  
 AV3 = Open -> Customized variants

BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02
1	1	0	1	-03
1	1	0	0	-04

Assembly Variants

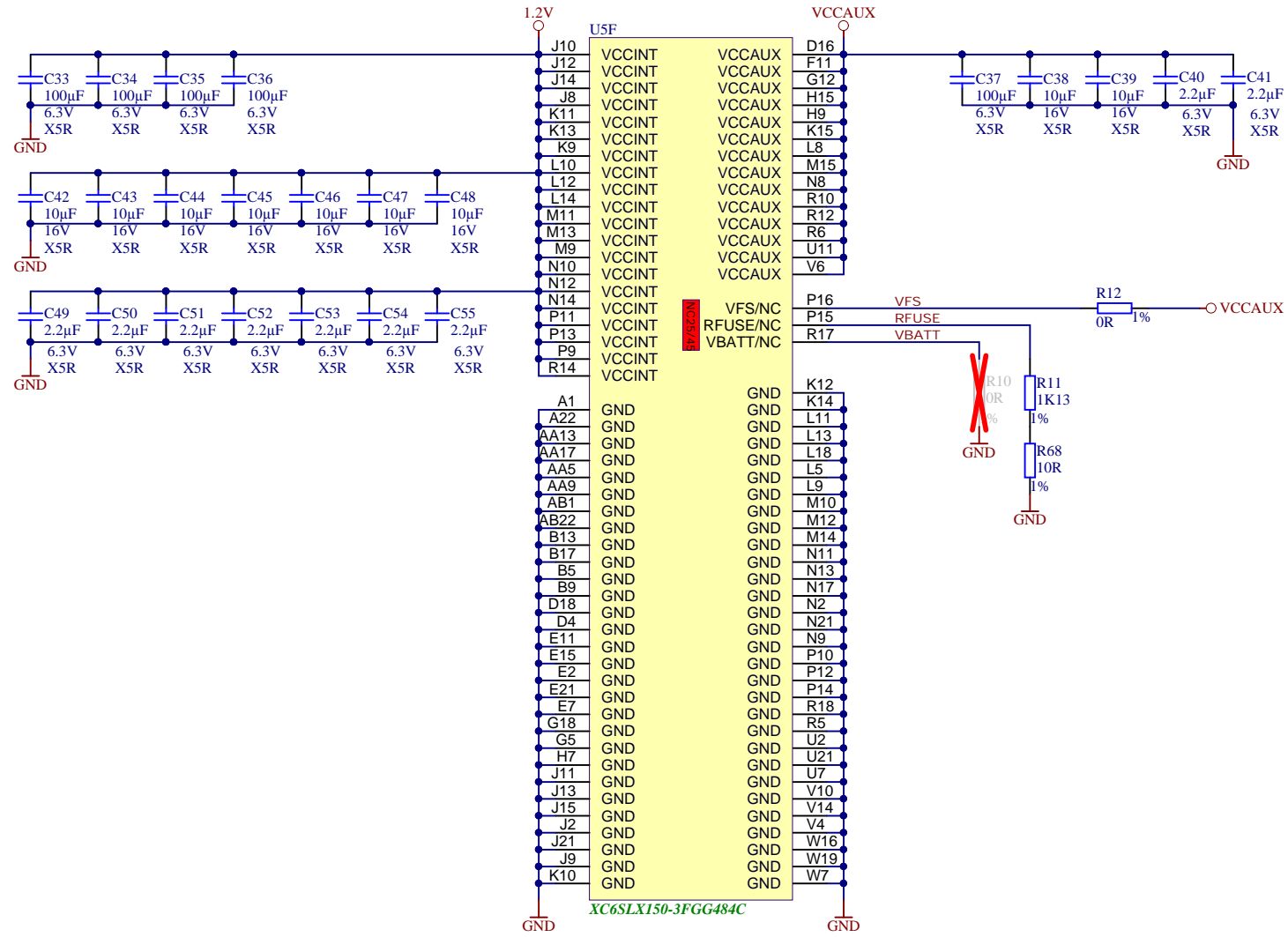


Board Revisions



Enable pullups in FPGA

Title: TE0600 - FPGA CFG		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 9 of 13
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Title: TE0600 - FPGA_PWR		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 10 of 13
Filename: FPGA_PWR.SchDoc		

A

B

C

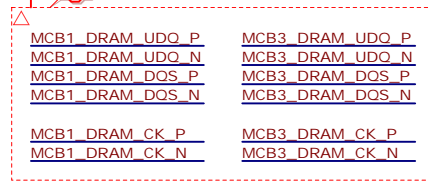
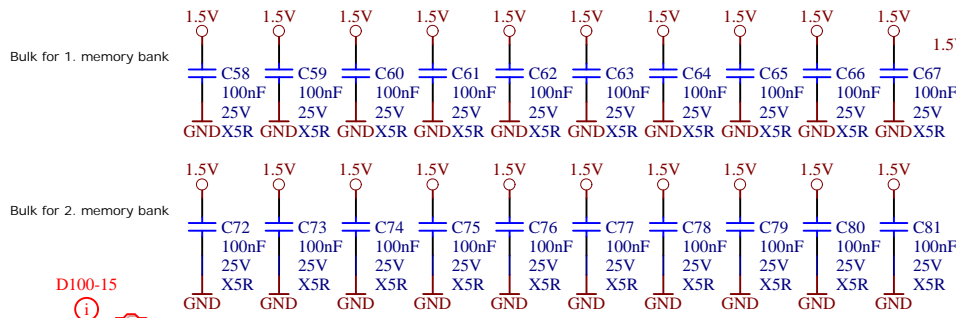
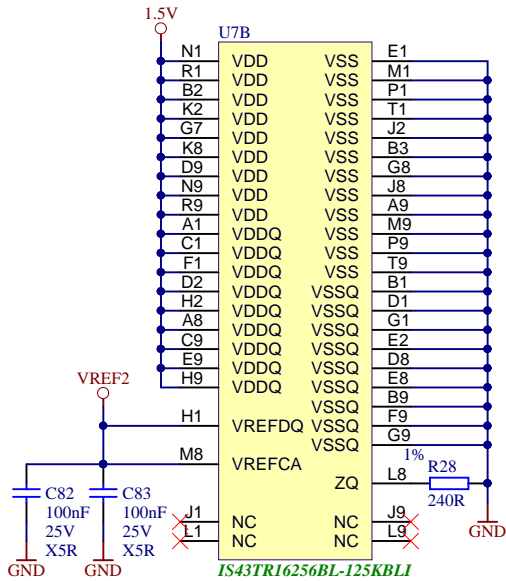
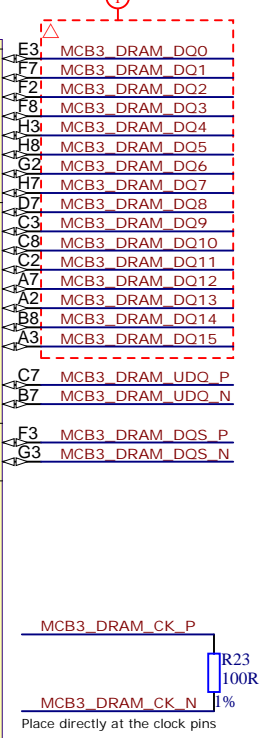
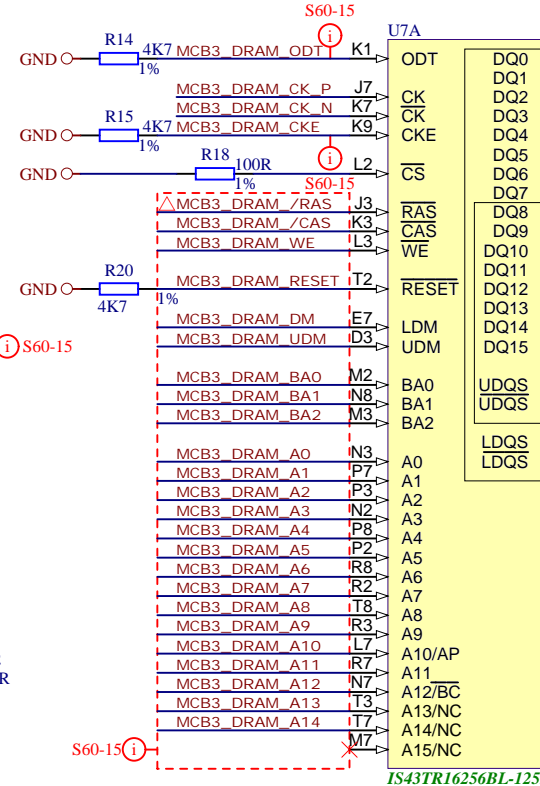
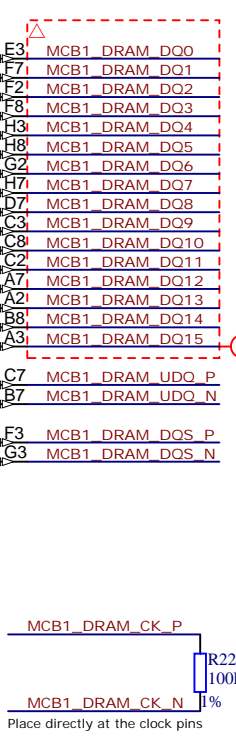
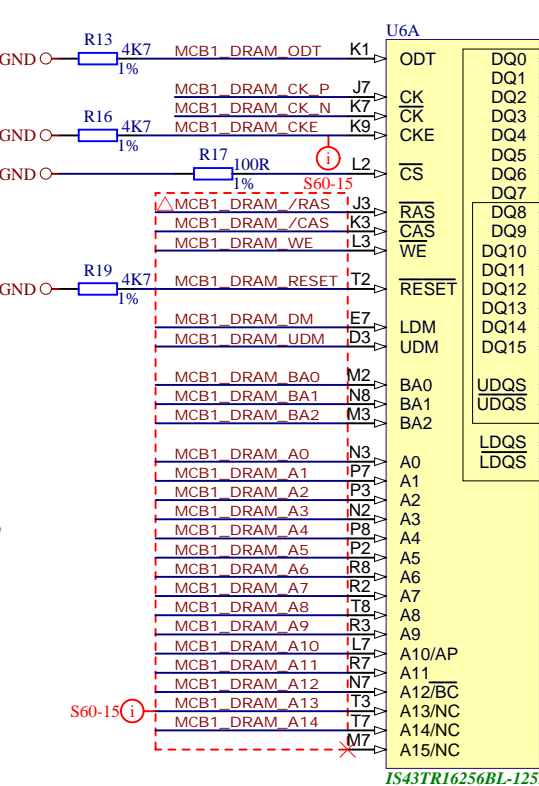
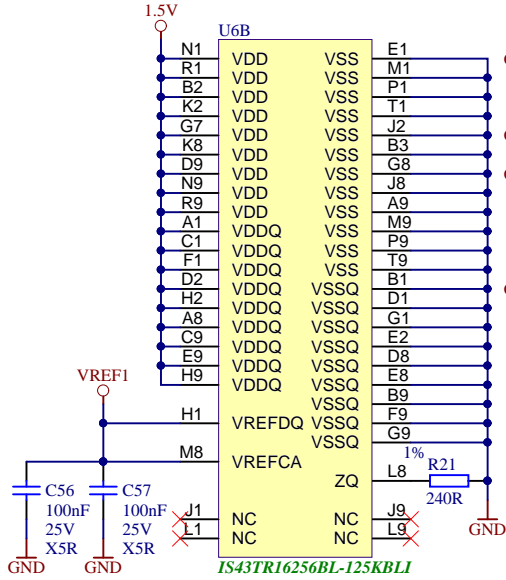
D

A

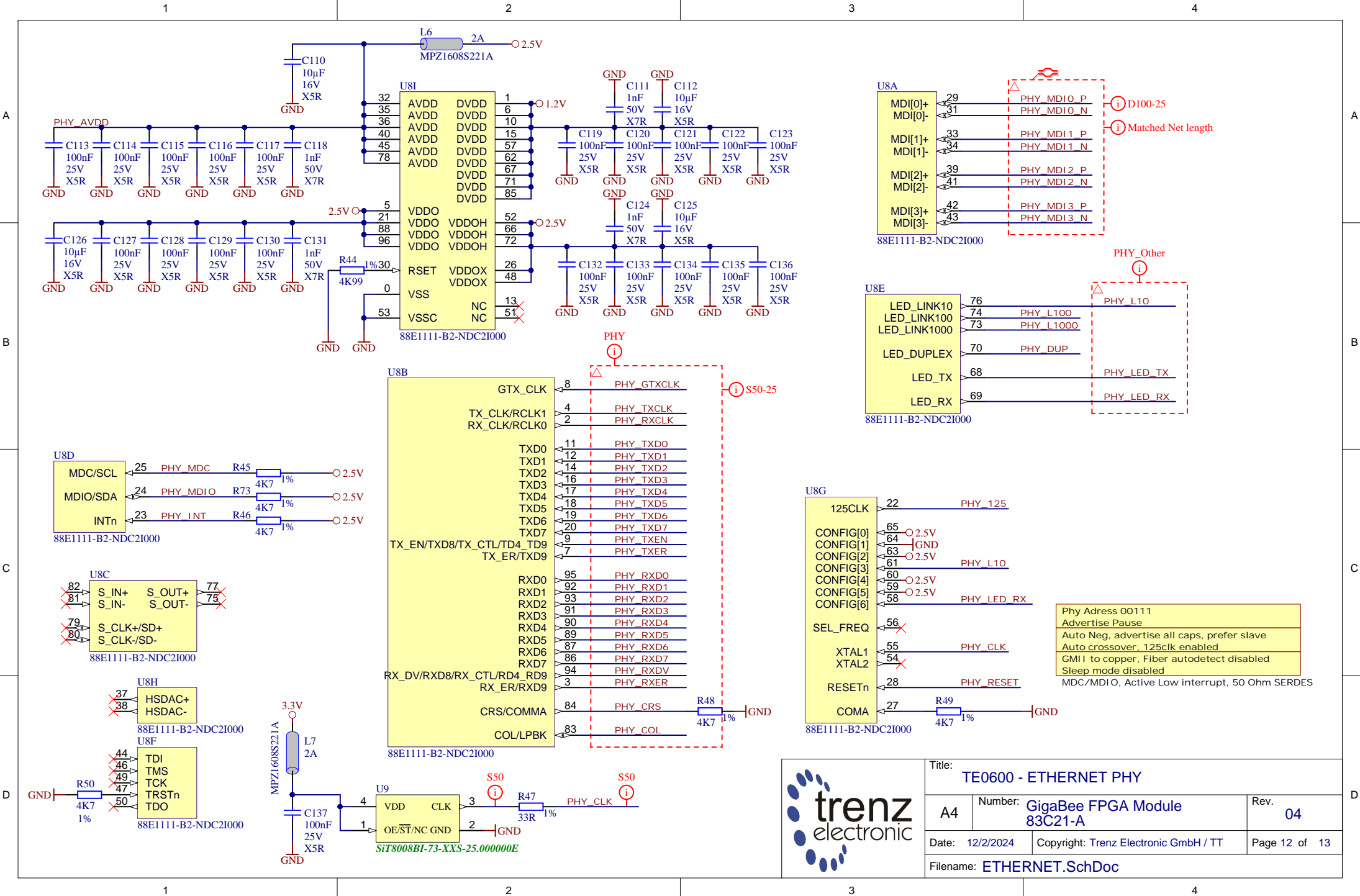
B

C

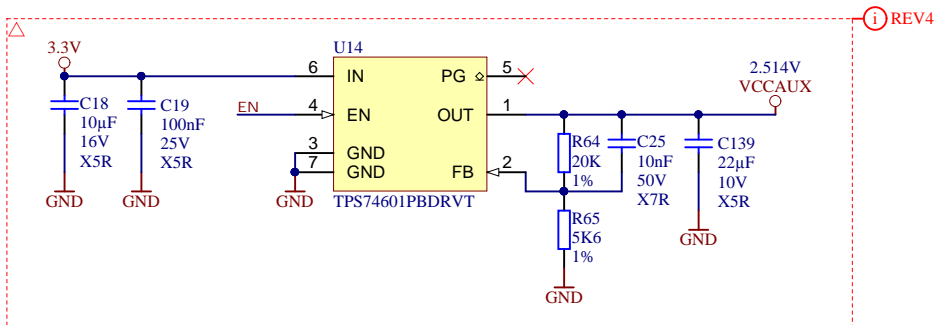
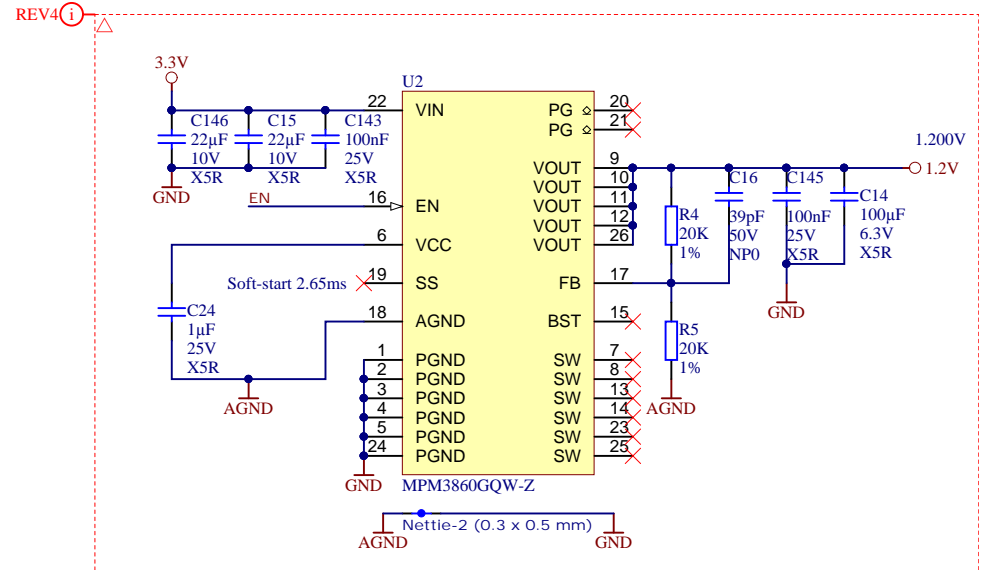
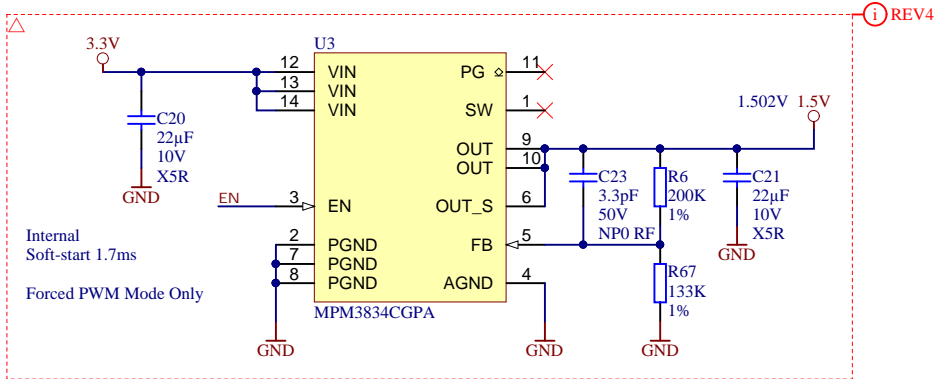
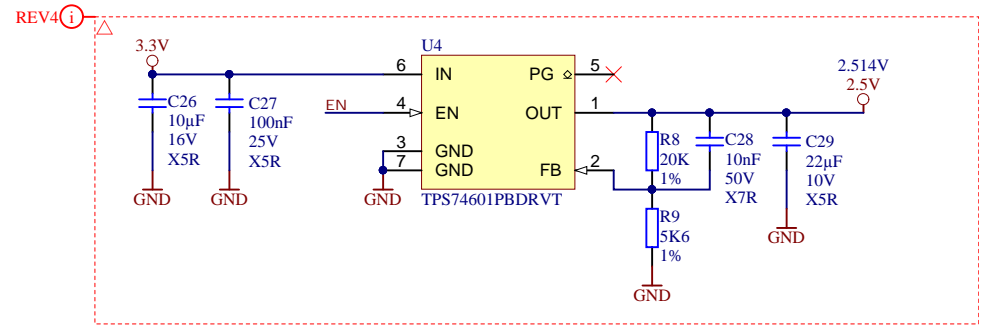
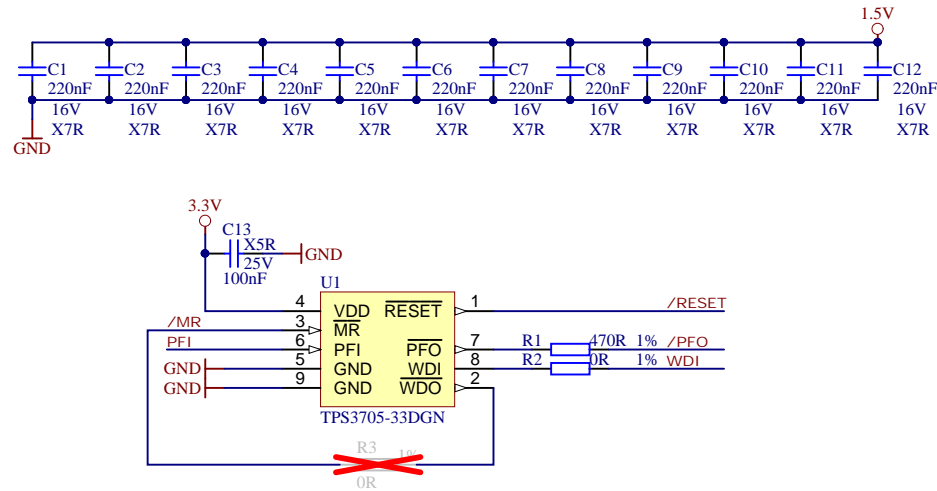
D




Title: TE0600 - DDR3 RAM		
A4	Number: GigaBee FPGA Module 83C21-A	Rev. 04
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			Title: TE0600 - POWER	
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