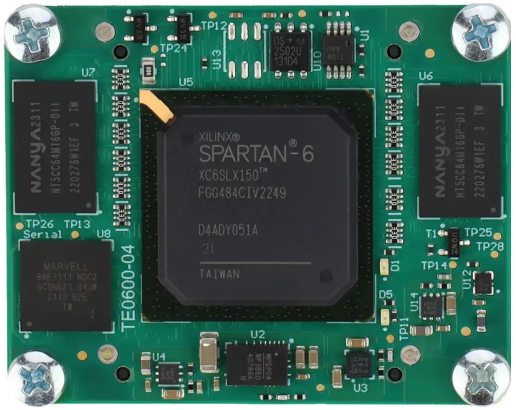

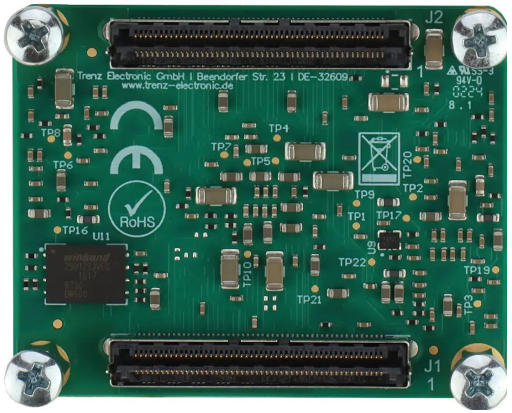

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0600 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0600 - Legal Notices		
A4	Number: TE0600 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH		Page 1 of 13
Filename: Legal_Notices.SchDoc			

REV	Description	
-01	Initial revision	
-03	1) added NetTie (board revision 03) 2) optimized placement and routing pwr DCDC 3) added tespoints 4) changed OSC U9 (AN25008, SiT8008AI-73-XXS-25.000000E) 5) update Razorbeam Connectors, full update lib 6) added serial number (tracebility pad) 7) added thermal vias to mounting holes 8) changed SPI flash (AN26012,W25Q128FVEIG 3V 128MBit Serial Flash) 9) changed DDR3 (AN27202, AN27039) 10) U13 (DS2432P+) is not populated	
-04	1) Leds @{"Id":"DPKOIGIM\SYAXGYNW"} , @{"Id":"NFAQWINK\BHTRJHLT"} were changed to SML-P11MTT86 2) @{"Id":"RXCWTMNI\KSNDDNHO"} was added. @{"Id":"RXCWTMNI\BJDDGYEG"} was changed from 2.2k to 100 3) @{"Id":"NFAQWINK\WAVCSPUH"} was changed from single BAT54VV,115 to pair BAT54A,215 4) @{"Id":"BSVLPKXO\WVYNQEAZ"} was changed from EN6347QI to MPM3860GQW-Z 5) @{"Id":"BSVLPKXO\BKMDDTRS"} was changed from EP53F8QI to MPM3834CGPA 6) Stacked vias were removed 7) Net BR0 was connected to GND 8) B2B signal groups information was added 9) Field filename was renamed for all schematic pages 10) Legal Notices page was added 11) System overview and power-on sequencing were added for TE0600.SchDoc page 12) Testpoints @{"Id":"GTKBAXHQ\YOBNRKRX"} - @{"Id":"GTKBAXHQ\VIYNLZMN"} , @{"Id":"GTKBAXHQ\ODTFOUWM"} - @{"Id":"GTKBAXHQ\PNEPKLPC"} were added	MT

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Title: TE0600 - Changes list		
A4	Number: GigaBee FPGA Module 83I11-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH	Page 2 of 13
Filename: Revision_Changes.SchDoc		

Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND

PM1
PM2
PM4
PM5
PM6
PM3

Top of Board

Screw M3x4
Standoff M3x8 II
Screw M3x6

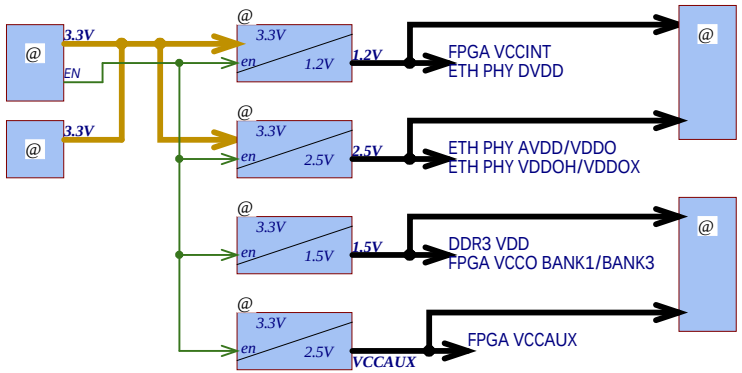
Top side testpoints:

1.5V	TP11	Testpoint 0.8mm
3.3V	TP12	Testpoint 0.8mm
2.5V	TP13	Testpoint 0.8mm
VCCAUX	TP14	Testpoint 0.8mm
GND	TP23	Testpoint 0.8mm
VCCIO0	TP24	Testpoint 0.8mm
VREF1	TP25	Testpoint 0.8mm
VREF2	TP26	Testpoint 0.8mm
MAC_DATA	TP27	Testpoint 0.8mm
CLK_P	TP28	Testpoint 0.8mm

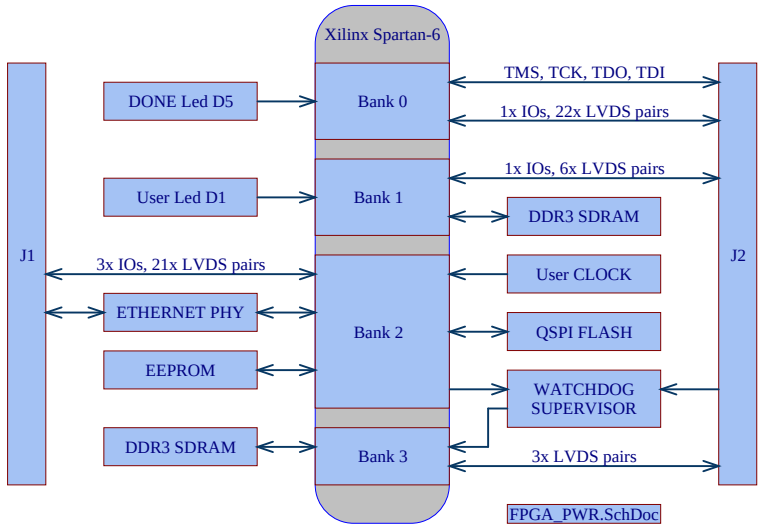
Bottom side testpoints:

1.5V	TP1	Testpoint 0.8mm
3.3V	TP2	Testpoint 0.8mm
2.5V	TP3	Testpoint 0.8mm
VCCAUX	TP4	Testpoint 0.8mm
1.2V	TP5	Testpoint 0.8mm
GND	TP6	Testpoint 0.8mm
VCCIO0	TP7	Testpoint 0.8mm
VREF1	TP8	Testpoint 0.8mm
VREF2	TP9	Testpoint 0.8mm
MAC_DATA	TP10	Testpoint 0.8mm
CLK_P	TP16	Testpoint 0.8mm
PHY_CLK	TP17	Testpoint 0.8mm
GND	TP18	Testpoint 0.8mm
GND	TP19	Testpoint 0.8mm
GND	TP20	Testpoint 0.8mm
GND	TP21	Testpoint 0.8mm
PROG_B	TP22	Testpoint 0.8mm

Power-on sequencing



System Overview



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3V	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO0	IN	1.1 - 3.45V	+/-5%	IO Bank0	-
1.2V	OUT	1.2V	+/-3%	Power for Carrier	-
1.5V	OUT	1.5V	+/-3%	Power for Carrier	-
2.5V	OUT	2.5V	+/-3%	Power for Carrier	-
VCCAUX	OUT	2.5V	+/-3%	Power for Carrier	-

Special notes:

VariantNote1

VariantNote2

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

Serial

Serial

Serialnumber 6,3 x 6.3mm

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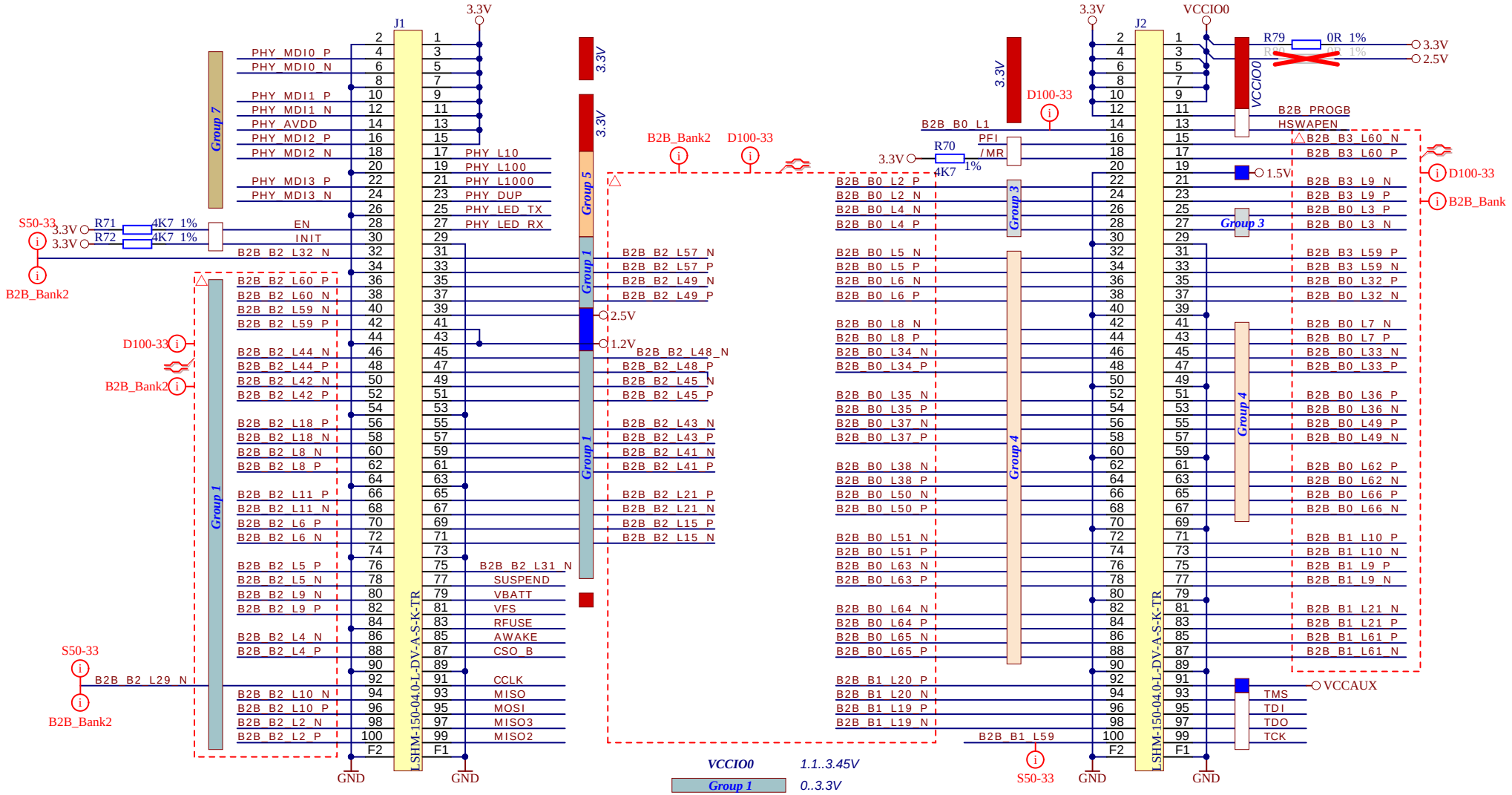
Title: TE0600			
A4	Number: GigaBee FPGA Module 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT		Page 3 of 13
Filename: TE0600.SchDoc			

B2: 45 Pins: 21 Differential; 3.3V Fixed VCCIO
ETHERNET PHY 10/100/1G

B0: 45 Pins: 22 Differential; variable VCCIO
B1: 13 Pins: 6 Differential; 1.5V Fixed
B3: 6 Pins: 3 Differential; 1.5V Fixed
JTAG: 3.3V Level



VCCIO0	*1.1..3.45V*
Group 1	*0..3.3V*
Group 3	*0..VCCIO0*
Group 4	*0..VCCIO0*
Group 5	
Group 7	*ETHERNET*
Special	
	PWR_in
	PWR_out

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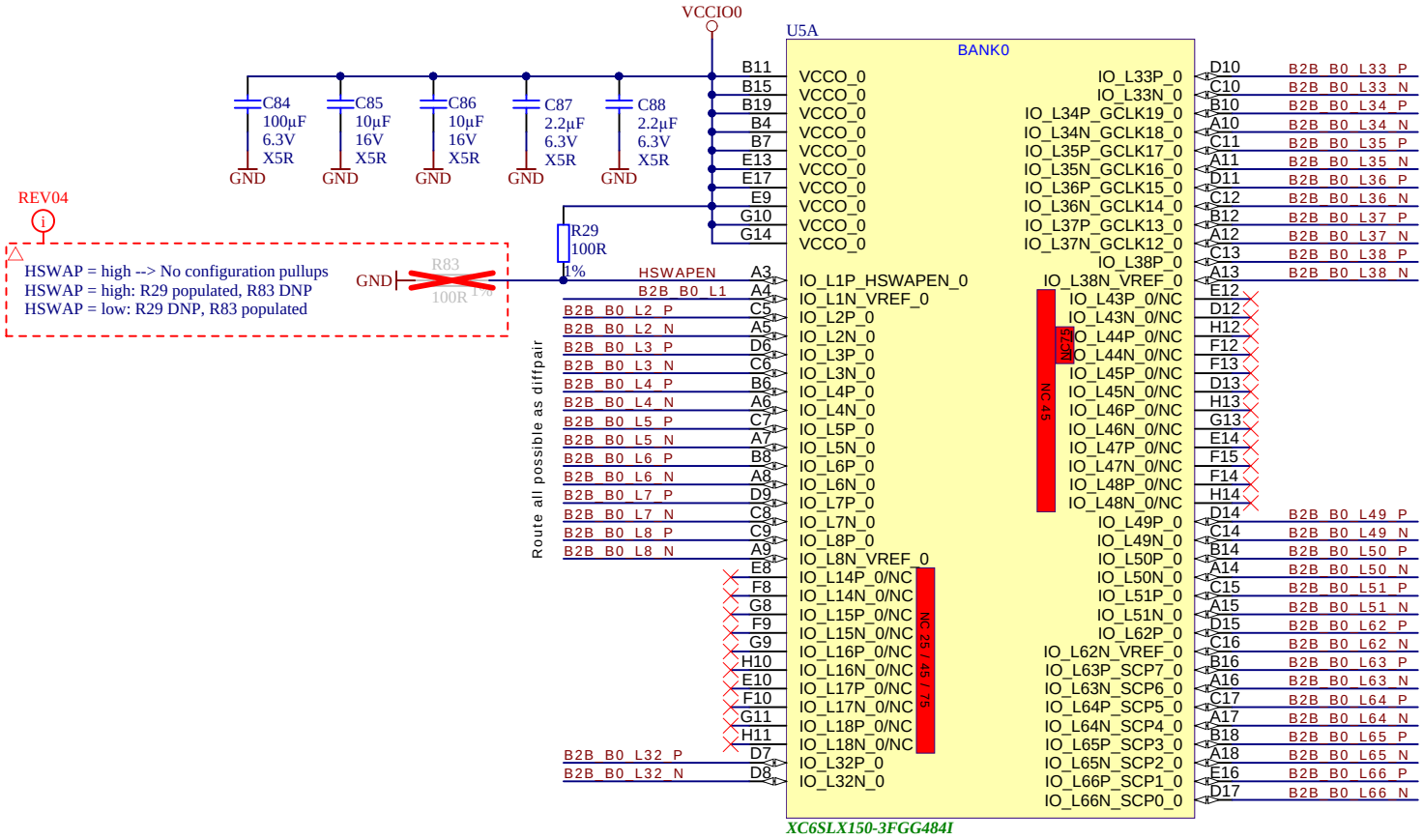
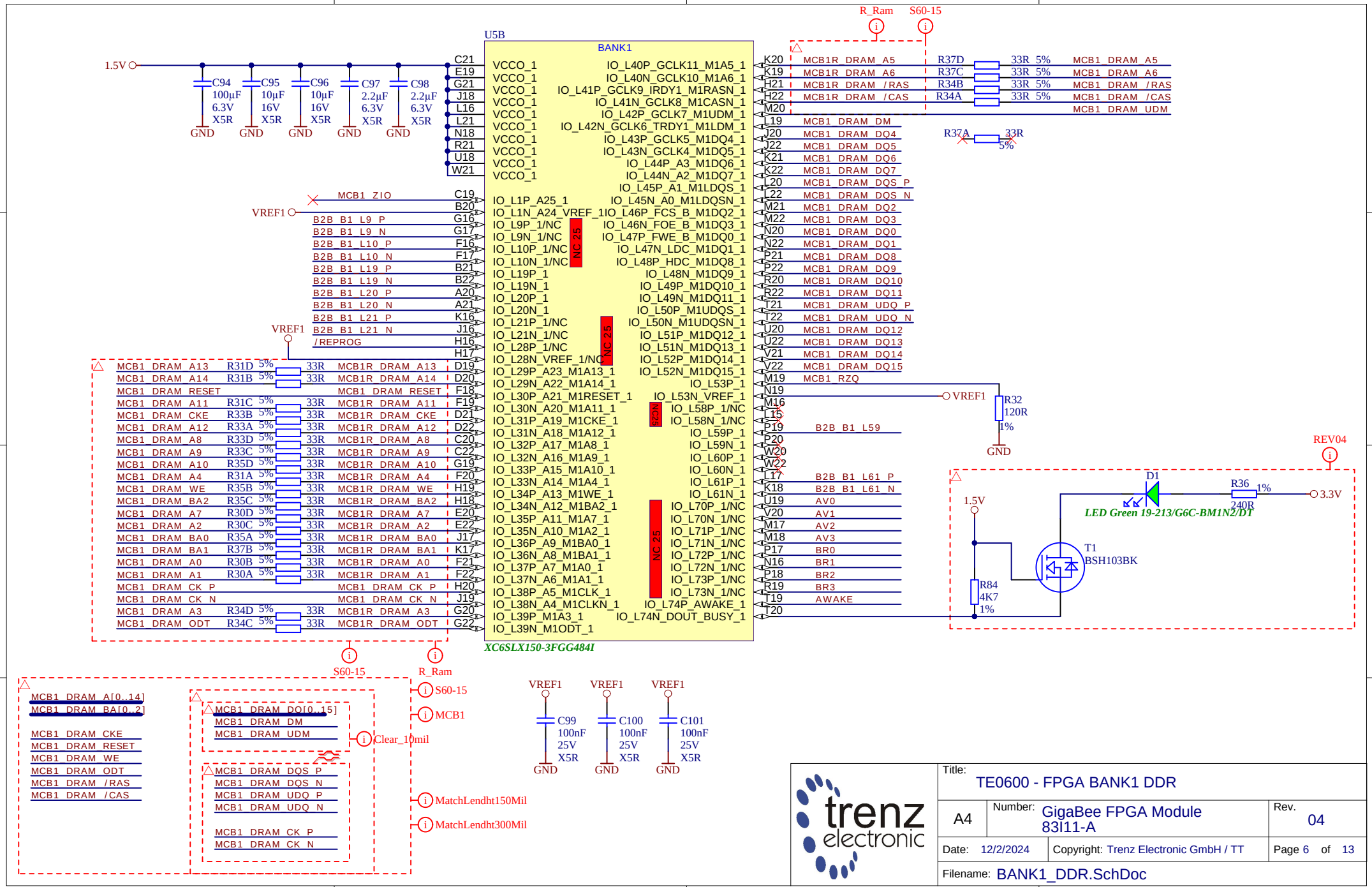
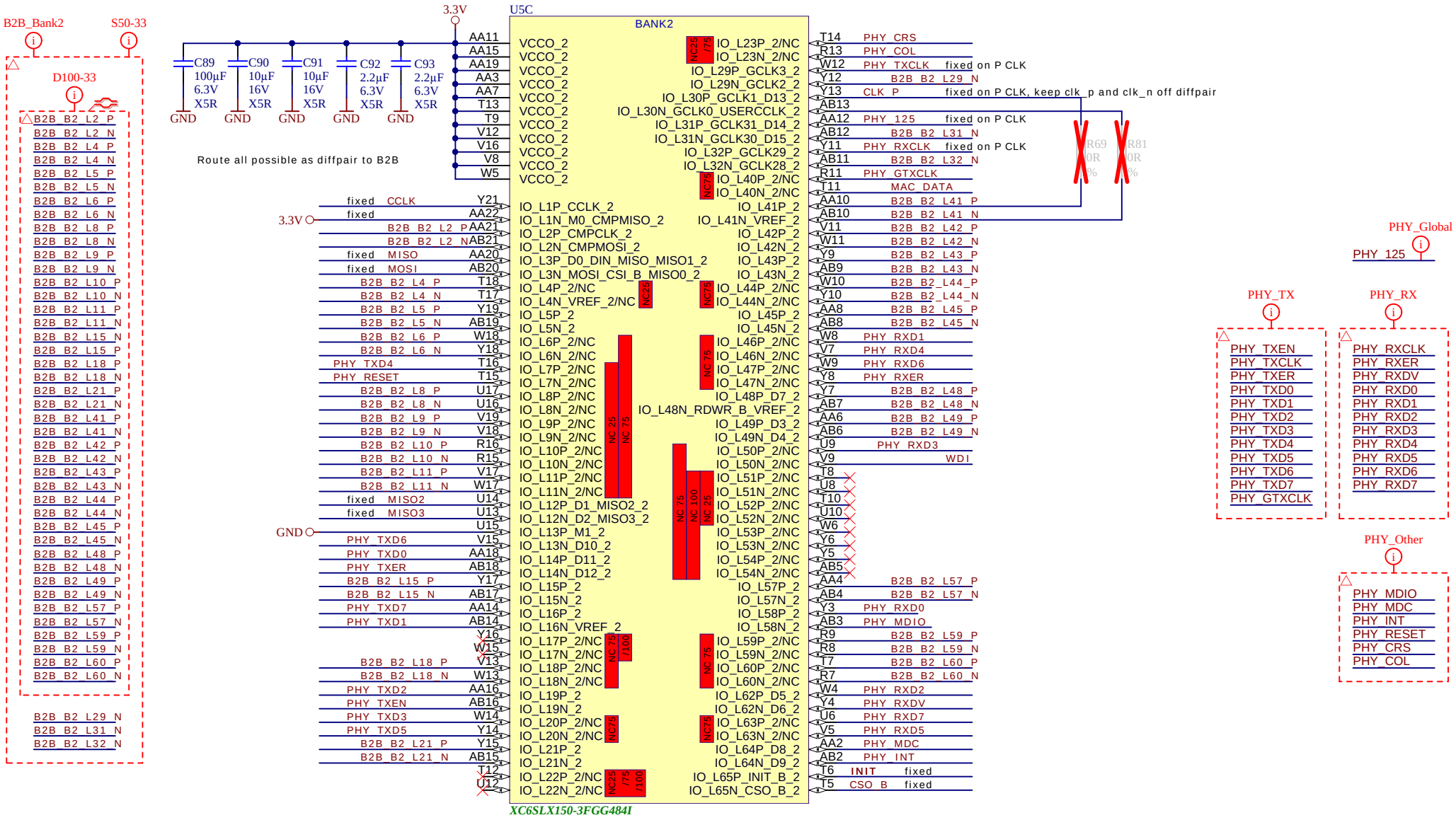
Title: TE0600 - B2B Connectors		
A4	Number: GigaBee FPGA Module 83I11-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 4 of 13
Filename: B2B.SchDoc		



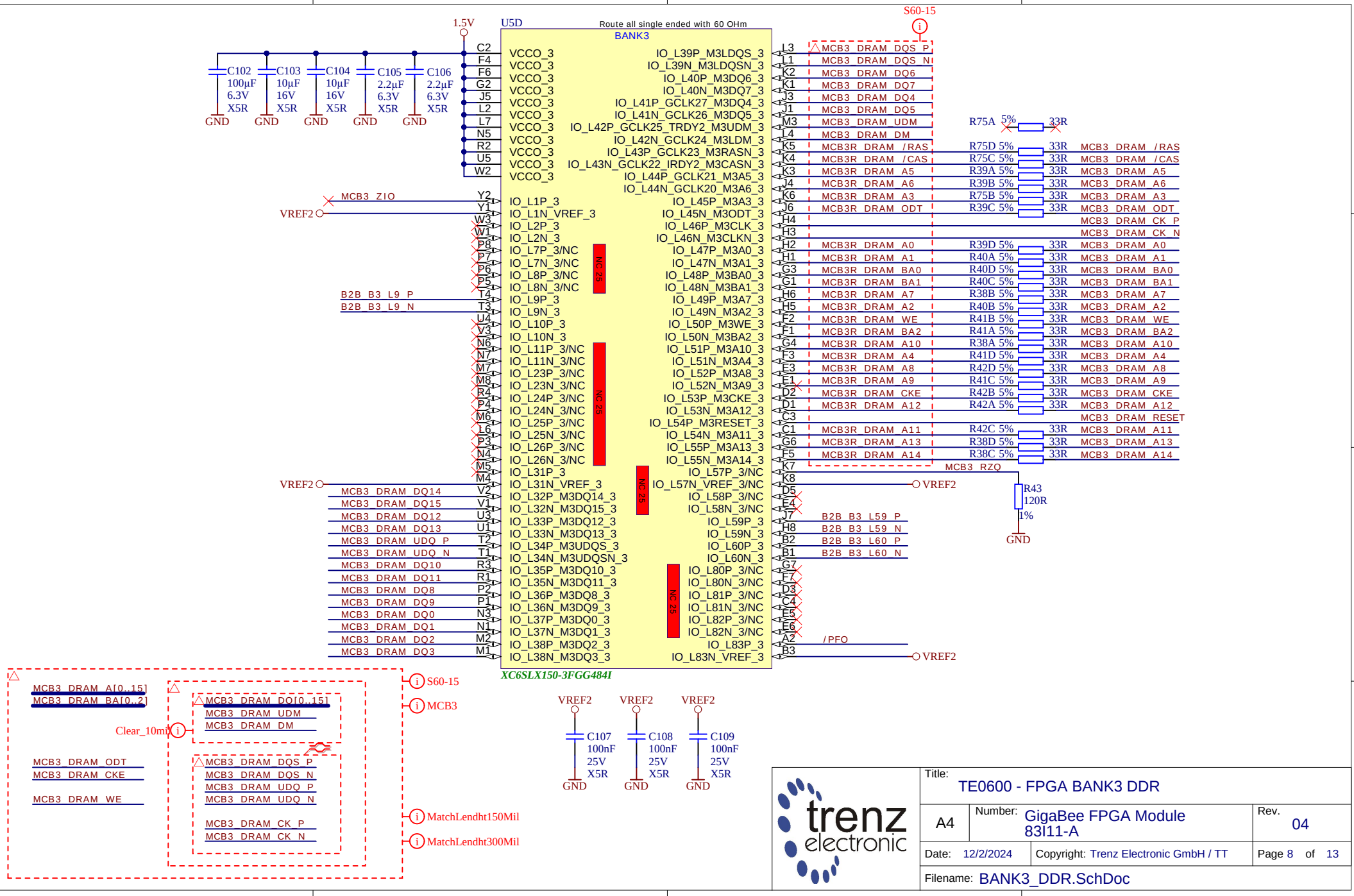
trenz electronic	Title: TE0600 - FPGA BANK0		
A4	Number: GigaBee FPGA Module 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT		Page 5 of 13
Filename: BANK0.SchDoc			



trenz electronic	Title: TE0600 - FPGA BANK1 DDR		
A4	Number: GigaBee FPGA Module 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT		Page 6 of 13
Filename: BANK1_DDR.SchDoc			



Title:	TE0600 - FPGA BANK2
A4	Number: GigaBee FPGA Module 83I11-A
	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT
	Page 7 of 13
Filename:	BANK2.SchDoc


Route all single ended with 60 OHm
U5D
BANK3
1.5V
S60-15
C102 100µF 6.3V X5R
C103 10µF 16V X5R
C104 10µF 16V X5R
C105 2.2µF 6.3V X5R
C106 2.2µF 6.3V X5R
GND
VCCO_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L45P_M3A3_3
IO_L45N_M3ODT_3
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L49P_M3A7_3
IO_L49N_M3A2_3
IO_L50P_M3WE_3
IO_L50N_M3BA2_3
IO_L51P_M3A10_3
IO_L51N_M3A4_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L53P_M3CKE_3
IO_L53N_M3A12_3
IO_L54P_M3RESET_3
IO_L54N_M3A11_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L57P_3/NC
IO_L57N_VREF_3/NC
IO_L58P_3/NC
IO_L58N_3/NC
IO_L59P_3
IO_L59N_3
IO_L60P_3
IO_L60N_3
IO_L80P_3/NC
IO_L80N_3/NC
IO_L81P_3/NC
IO_L81N_3/NC
IO_L82P_3/NC
IO_L82N_3/NC
IO_L83P_3
IO_L83N_VREF_3
IO_L1P_3
IO_L1N_VREF_3
IO_L2P_3
IO_L2N_3
IO_L7P_3/NC
IO_L7N_3/NC
IO_L8P_3/NC
IO_L8N_3/NC
IO_L9P_3
IO_L9N_3
IO_L10P_3
IO_L10N_3
IO_L11P_3/NC
IO_L11N_3/NC
IO_L23P_3/NC
IO_L23N_3/NC
IO_L24P_3/NC
IO_L24N_3/NC
IO_L25P_3/NC
IO_L25N_3/NC
IO_L26P_3/NC
IO_L26N_3/NC
IO_L31P_3
IO_L31N_VREF_3
IO_L32P_M3DQ14_3
IO_L32N_M3DQ15_3
IO_L33P_M3DQ12_3
IO_L33N_M3DQ13_3
IO_L34P_M3UDQS_3
IO_L34N_M3UDQSN_3
IO_L35P_M3DQ10_3
IO_L35N_M3DQ11_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
NC 25
MCB3_ZIO
VREF2
B2B_B3_L9_P
B2B_B3_L9_N
MCB3_DRAM_DQ14
MCB3_DRAM_DQ15
MCB3_DRAM_DQ12
MCB3_DRAM_DQ13
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_DQ10
MCB3_DRAM_DQ11
MCB3_DRAM_DQ8
MCB3_DRAM_DQ9
MCB3_DRAM_DQ0
MCB3_DRAM_DQ1
MCB3_DRAM_DQ2
MCB3_DRAM_DQ3
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_DQ6
MCB3_DRAM_DQ7
MCB3_DRAM_DQ4
MCB3_DRAM_DQ5
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3R_DRAM_/RAS
MCB3R_DRAM_/CAS
MCB3R_DRAM_A5
MCB3R_DRAM_A6
MCB3R_DRAM_A3
MCB3R_DRAM_ODT
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3R_DRAM_A0
MCB3R_DRAM_A1
MCB3R_DRAM_BA0
MCB3R_DRAM_BA1
MCB3R_DRAM_A7
MCB3R_DRAM_A2
MCB3R_DRAM_WE
MCB3R_DRAM_BA2
MCB3R_DRAM_A10
MCB3R_DRAM_A4
MCB3R_DRAM_A8
MCB3R_DRAM_A9
MCB3R_DRAM_CKE
MCB3R_DRAM_A12
MCB3_DRAM_RESET
MCB3R_DRAM_A11
MCB3R_DRAM_A13
MCB3R_DRAM_A14
MCB3_RZQ
R43 120R 1%
/PFO
B2B_B3_L59_P
B2B_B3_L59_N
B2B_B3_L60_P
B2B_B3_L60_N
R75A 5% 33R
R75D 5% 33R
R75C 5% 33R
R39A 5% 33R
R39B 5% 33R
R75B 5% 33R
R39C 5% 33R
R39D 5% 33R
R40A 5% 33R
R40D 5% 33R
R40C 5% 33R
R38B 5% 33R
R40B 5% 33R
R41B 5% 33R
R41A 5% 33R
R38A 5% 33R
R41D 5% 33R
R42D 5% 33R
R41C 5% 33R
R42B 5% 33R
R42A 5% 33R
R42C 5% 33R
R38D 5% 33R
R38C 5% 33R
XC6SLX150-3FGG484I
C107 100nF 25V X5R
C108 100nF 25V X5R
C109 100nF 25V X5R
MCB3_DRAM_A[0..15]
MCB3_DRAM_BA[0..2]
MCB3_DRAM_DQ[0..15]
MCB3_DRAM_UDM
MCB3_DRAM_DM
Clear_10mil
MCB3_DRAM_ODT
MCB3_DRAM_CKE
MCB3_DRAM_WE
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
S60-15
MCB3
MatchLendht150Mil
MatchLendht300Mil
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Title: TE0600 - FPGA BANK3 DDR
A4
Number: GigaBee FPGA Module 83I11-A
Rev. 04
Date: 12/2/2024
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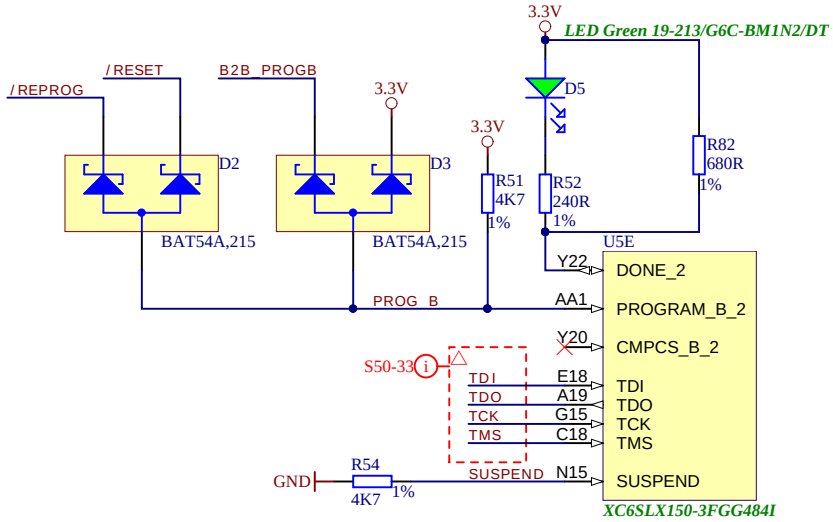
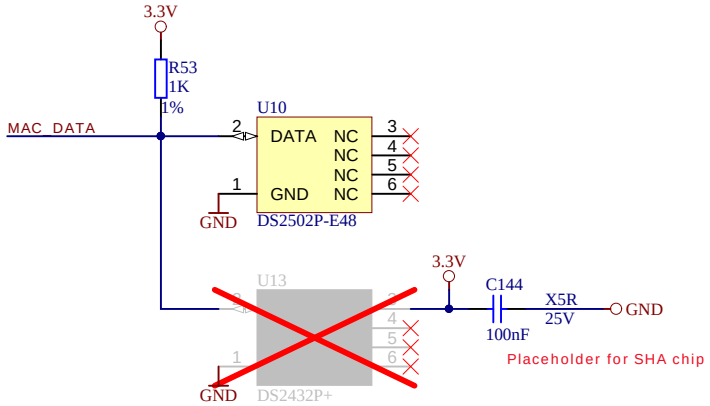
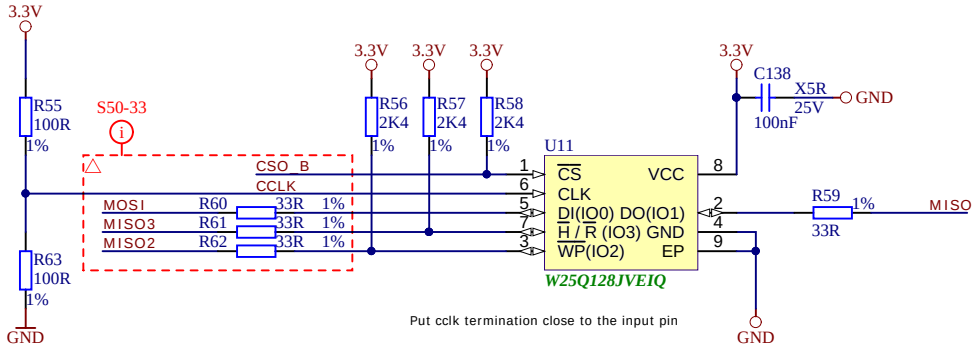
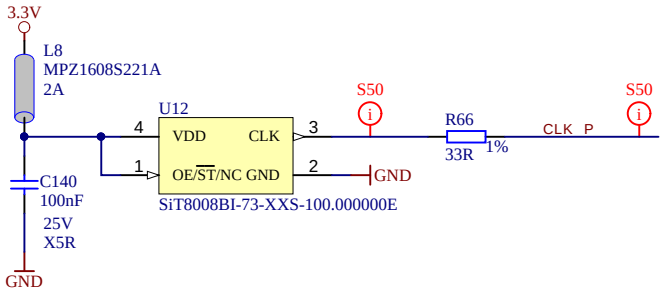
Filename: BANK3_DDR.SchDoc





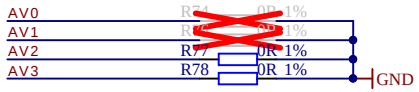




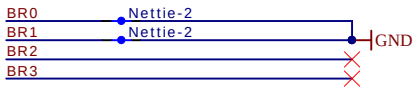

```
AV0 = 0 -> commercial    AV0 = 1 -> Industrial
AV1 = 0 -> speedgrade 2  AV1 = 1 -> speedgrade 3
AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte
AV3 = Open -> Customized variants
```

```
BR3 BR2 BR1 BR0
----------------------------------------
  1   1   1   1 | -01 Initial revision
  1   1   1   0 | -02
  1   1   0   1 | -03
  1   1   0   0 | -04
```

Assembly Variants



Board Revisions



Enable pullups in FPGA

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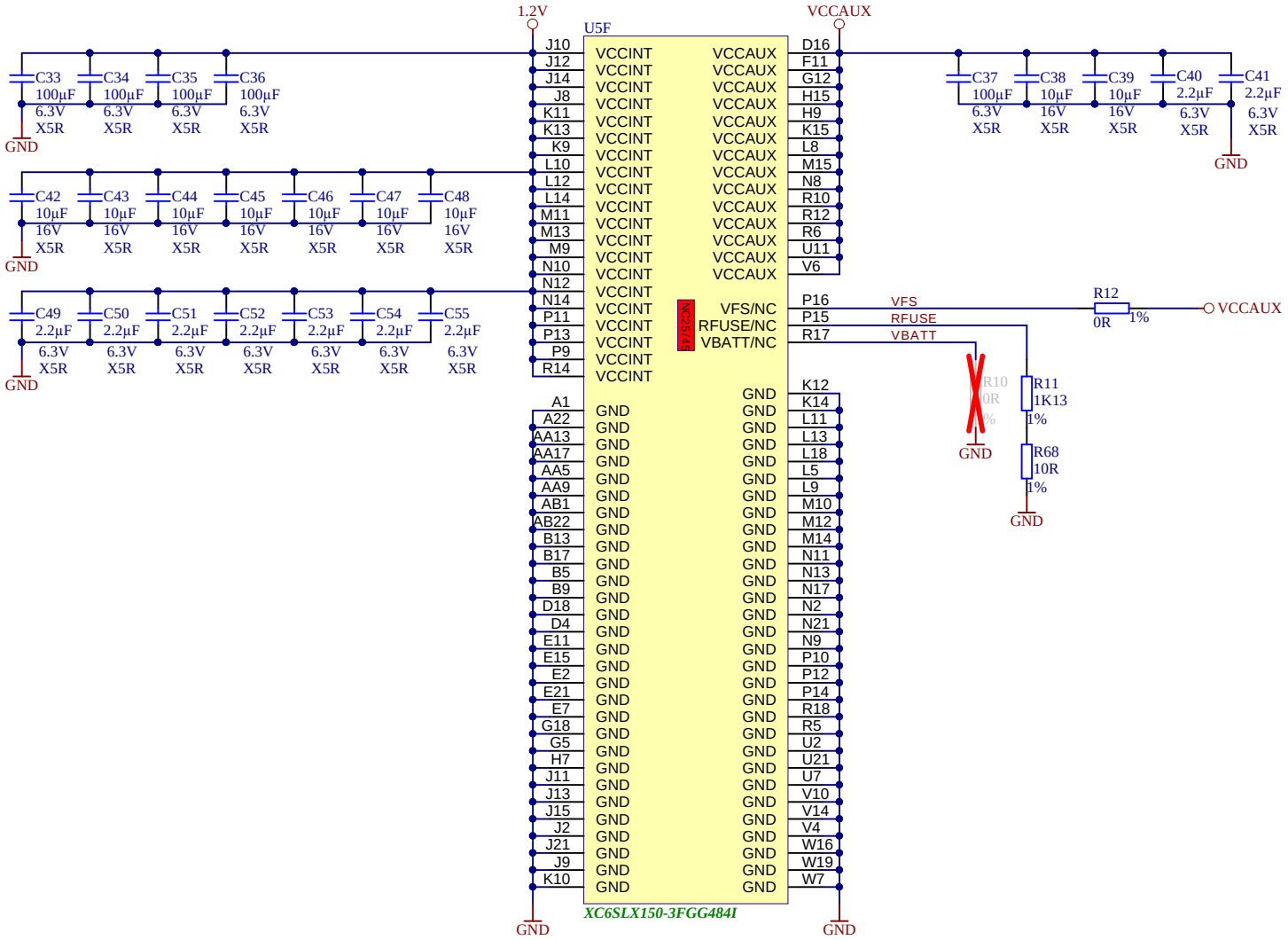
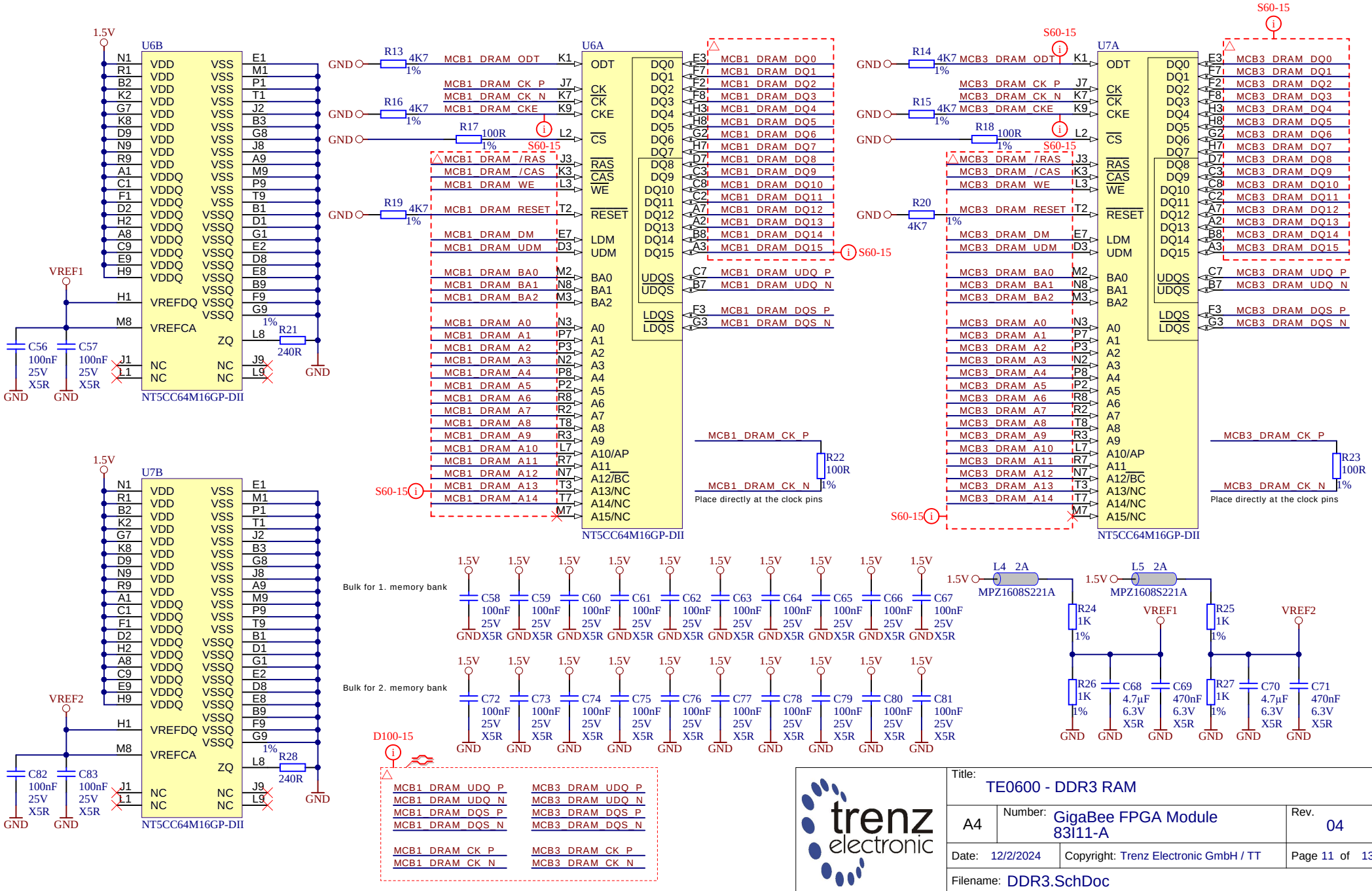
Title: TE0600 - FPGA CFG		
A4	Number: GigaBee FPGA Module 83I11-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 9 of 13
Filename: FPGA_CFG.SchDoc		



Title: TE0600 - FPGA_PWR		
A4	Number: GigaBee FPGA Module 83I11-A	Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT	Page 10 of 13
Filename: FPGA_PWR.SchDoc		



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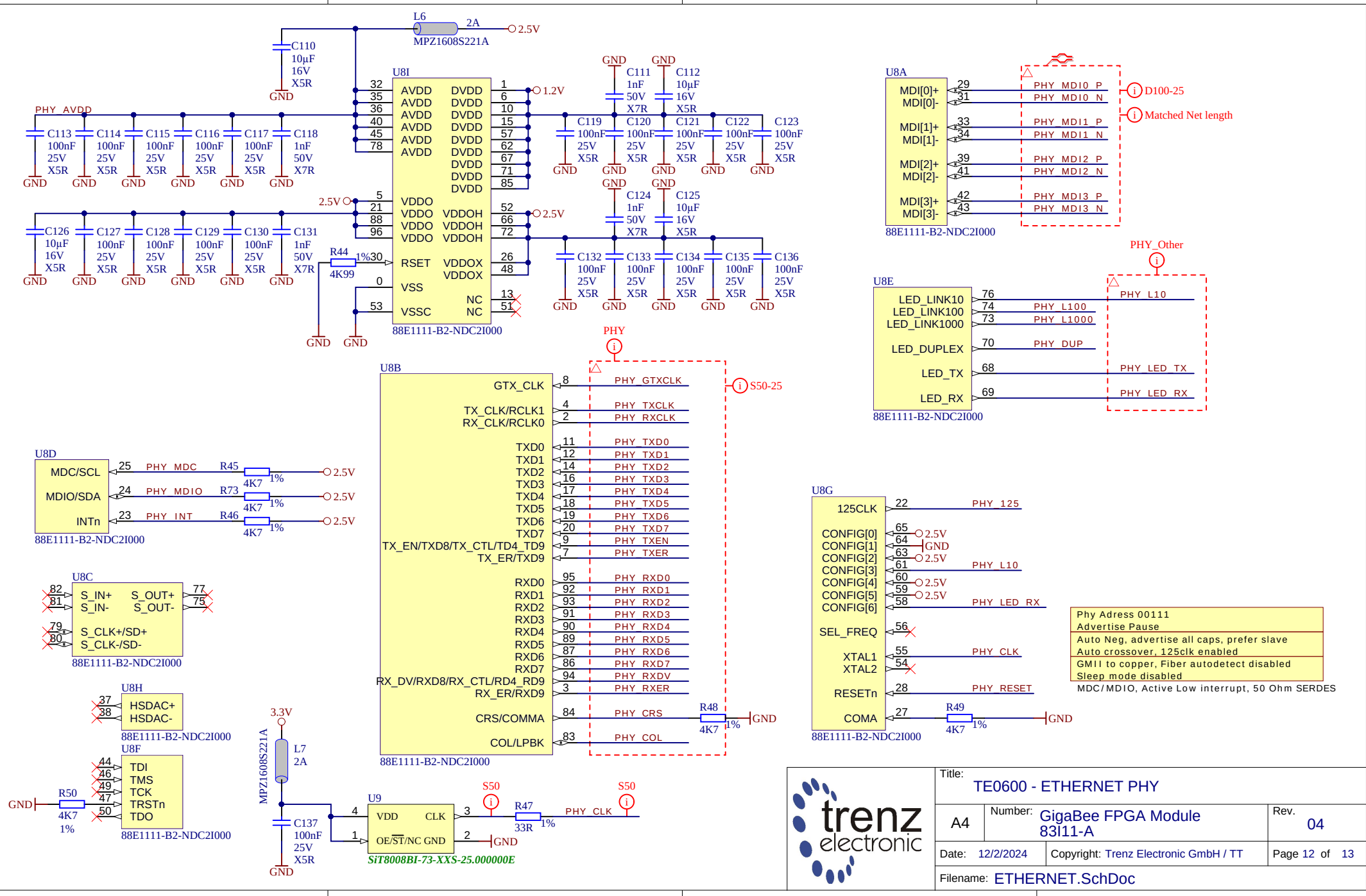
Title: TE0600 - DDR3 RAM			
A4	Number: GigaBee FPGA Module 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT		Page 11 of 13
Filename: DDR3.SchDoc			


L6
2A
2.5V
MPZ1608S221A
C110
10µF
16V
X5R
U8I
AVDD
DVDD
VDDO
VDDOH
VDDOX
RSET
VSS
VSSC
NC
1.2V
2.5V
R44
4K99
1%
88E1111-B2-NDC2I000
PHY_AVDD
C113 C114 C115 C116 C117 C118
C119 C120 C121 C122 C123
C124 C125
C126 C127 C128 C129 C130 C131
C132 C133 C134 C135 C136
100nF 1nF 10µF
25V 50V 16V
X5R X7R
GND
U8A
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-25
Matched Net length
U8E
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_TX
LED_RX
PHY_L100
PHY_L1000
PHY_DUP
PHY_LED_TX
PHY_LED_RX
PHY_L10
PHY_Other
PHY
U8B
GTX_CLK
TX_CLK/RCLK1
RX_CLK/RCLK0
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TX_EN/TXD8/TX_CTL/TD4_TD9
TX_ER/TXD9
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RX_DV/RXD8/RX_CTL/RD4_RD9
RX_ER/RXD9
CRS/COMMA
COL/LPBK
PHY_GTXCLK
PHY_TXCLK
PHY_RXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_CRS
PHY_COL
S50-25
R48
4K7
1%
U8D
MDC/SCL
MDIO/SDA
INTn
PHY_MDC
PHY_MDIO
PHY_INT
R45
R73
R46
U8C
S_IN+
S_IN-
S_OUT+
S_OUT-
S_CLK+/SD+
S_CLK-/SD-
U8H
HSDAC+
HSDAC-
U8F
TDI
TMS
TCK
TRSTn
TDO
R50
U8G
125CLK
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
CONFIG[6]
SEL_FREQ
XTAL1
XTAL2
RESETn
COMA
PHY_125
PHY_L10
PHY_LED_RX
PHY_CLK
PHY_RESET
R49
3.3V
L7
2A
MPZ1608S221A
C137
100nF
25V
X5R
U9
VDD
CLK
OE/ST/NC
GND
SiT8008BI-73-XXS-25.000000E
S50
R47
33R
Phy Adress 00111
Advertise Pause
Auto Neg, advertise all caps, prefer slave
Auto crossover, 125clk enabled
GMII to copper, Fiber autodetect disabled
Sleep mode disabled
MDC/MDIO, Active Low interrupt, 50 Ohm SERDES
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Title: TE0600 - ETHERNET PHY
A4
Number: GigaBee FPGA Module 83I11-A
Rev. 04
Date: 12/2/2024
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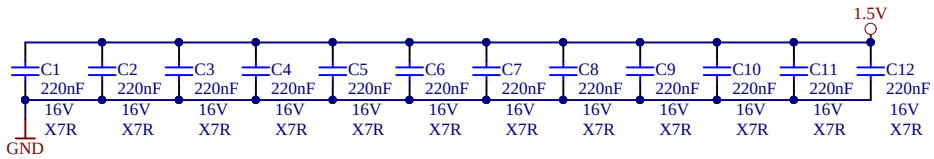

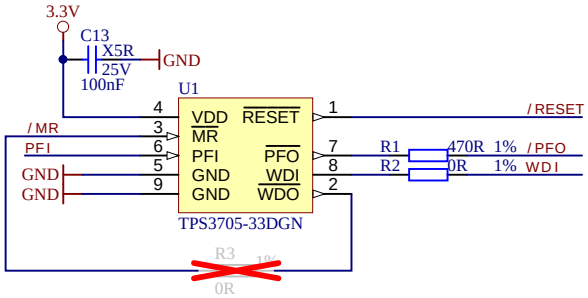

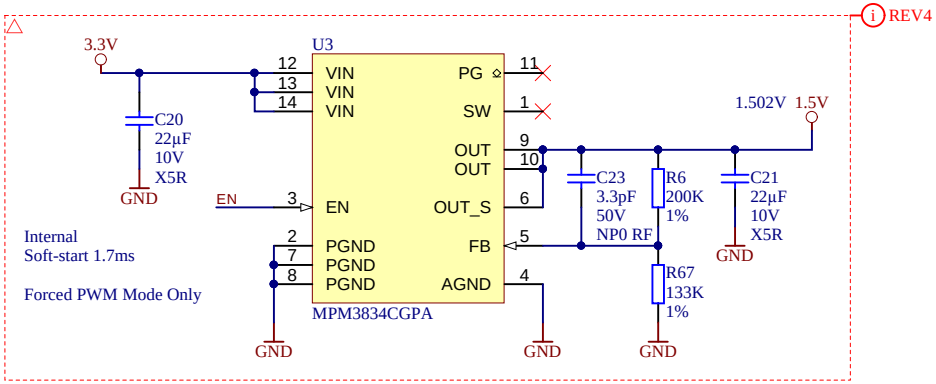

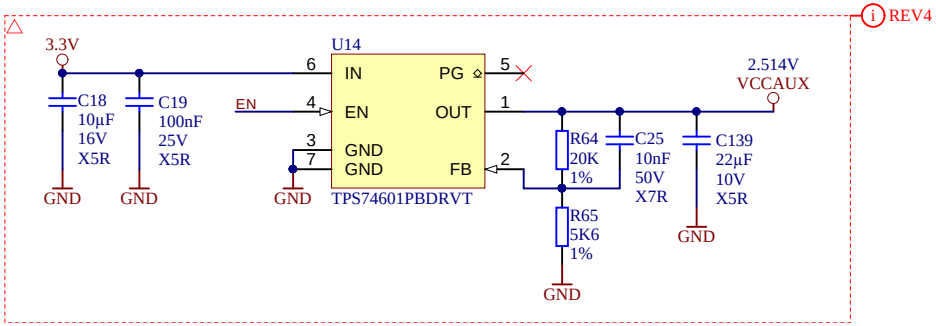

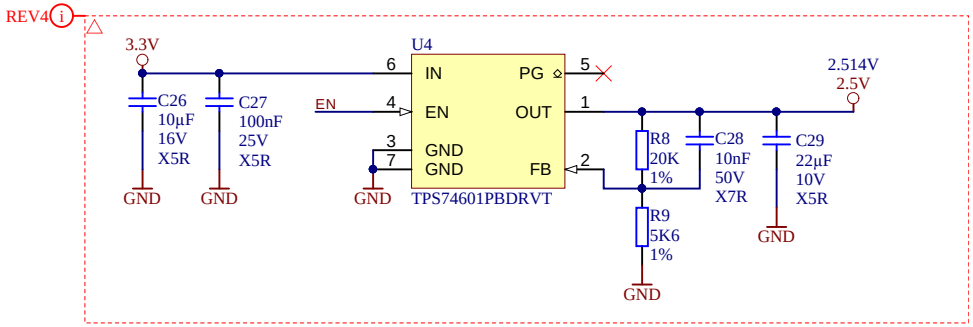

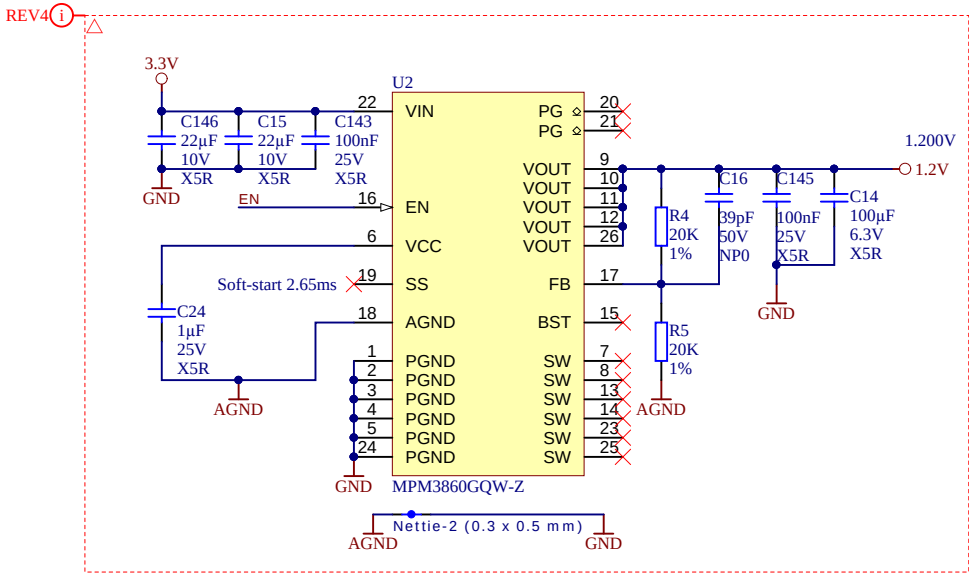

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Title: TE0600 - POWER			
A4	Number: GigaBee FPGA Module 83I11-A		Rev. 04
Date: 12/2/2024	Copyright: Trenz Electronic GmbH / TT		Page 13 of 13
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