



## TE0600 TRM

Revision v.39

Exported on 2025-06-05

# 1 Table of Contents

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1	Table of Contents .....	2
2	Table of Figures .....	3
3	Table of Tables .....	4
4	Overview .....	6
4.1	Key Features .....	6
4.2	Block Diagram .....	7
4.3	Main Components .....	8
4.4	Initial Delivery State .....	8
5	Signals, Interfaces and Pins .....	9
5.1	Connectors .....	9
5.2	Test Points .....	9
6	On-board Peripherals .....	12
7	Configuration and System Control Signals .....	13
8	Power and Power-On Sequence .....	15
8.1	Power Rails .....	15
8.2	Recommended Power up Sequencing .....	15
9	Board to Board Connectors .....	17
9.1	Connector Mating height .....	17
9.2	Connector Speed Ratings .....	18
9.3	Current Rating .....	18
9.4	Connector Mechanical Ratings .....	18
10	Technical Specifications .....	19
10.1	Absolute Maximum Ratings *) .....	19
10.2	Recommended Operating Conditions .....	19
10.2.1	Temperature range .....	20
10.2.2	Voltage rails .....	20
10.3	Physical Dimensions .....	20
11	Currently Offered Variants .....	22
12	Revision History .....	23
12.1	Hardware Revision History .....	23
12.2	Document Change History .....	26
13	Disclaimer .....	29
13.1	Data Privacy .....	29
13.2	Document Warranty .....	29
13.3	Limitation of Liability .....	29
13.4	Copyright Notice .....	29
13.5	Technology Licenses .....	29
13.6	Environmental Protection .....	29
13.7	REACH, RoHS and WEEE .....	30

## 2 Table of Figures

---

Figure 1: TE0600 block diagram .....	7
Figure 2: TE0600 main components .....	8
Figure 3: Physical Dimension .....	21
Figure 4: Board hardware revision number .....	23

## 3 Table of Tables

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Table 1: Initial delivery state of programmable devices on the module.....	8
Table 2: Board Connectors .....	9
Table 3: Test Points Information .....	9
Table 4: On board peripherals.....	12
Table 5: Controller signal.....	13
Table 6: Module power rails.....	15
Table 7: Baseboard Design Hints.....	16
Table 8: Connectors.....	17
Table 9: Speed rating.....	18
Table 10: Absolute maximum ratings .....	19
Table 11: Recommended operating conditions.....	20
Table 12: Trenz Electronic Shop Overview .....	22
Table 13: Hardware Revision History .....	24
Table 14: Document change history.....	26

[Current online version of this document.](#)

## 4 Overview

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Trenz Electronic GigaBee also known as TE0600 series are industrial-grade FPGA micromodules integrating an [AMD Spartan-6 LX FPGA](#), Gigabit Ethernet transceiver, two independent banks of 16-bit-wide DDR3 SDRAM, QSPI Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors.

Refer to <http://trenz.org/te0600-info> for current online available documentation.

### 4.1 Key Features

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- **SoC/FPGA/Module**
  - AMD FPGA: XC6SLX25 / XC6SLX45 / XC6SLX75 / XC6SLX100 / XC6SLX150 <sup>1)</sup>
  - Speedgrade: -1L / -2 / -3 / -N3 <sup>1)</sup>
  - Temperature Range: Commercial / Industrial <sup>1)</sup>
  - Package: FGG484
- **RAM/Storage**
  - 512 MByte DDR3 SDRAM <sup>1)</sup>
  - 16 Mbyte QSPI Flash <sup>1)</sup>
  - EEPROM with unique MAC/EUI-48 Ethernet address and 768 bit usable storage.
  - Optional EEPROM (DS2432P+) with unique MAC/EUI-48 Ethernet address and 1024 bit usable storage, 104 bit special storage and SHA-1 Engine.
- **On Board**
  - 10/100/1000 Mbit Ethernet PHY
  - 100 MHz oscillator
  - 1x LED for FPGA configuration status
  - 1x LED user configurable
- **Interface**
  - 3 x B2B Connector (LSHM) for Trenz 4 x 5 SoM socket
    - 104x SE / 52x DIFF
    - 5x SE
- **Power**
  - DCDC converters for all on-board voltage rails
- **Dimension**
  - 50 mm x 40 mm
- **Notes**
  - <sup>1)</sup> Assembly variant dependent.

## 4.2 Block Diagram

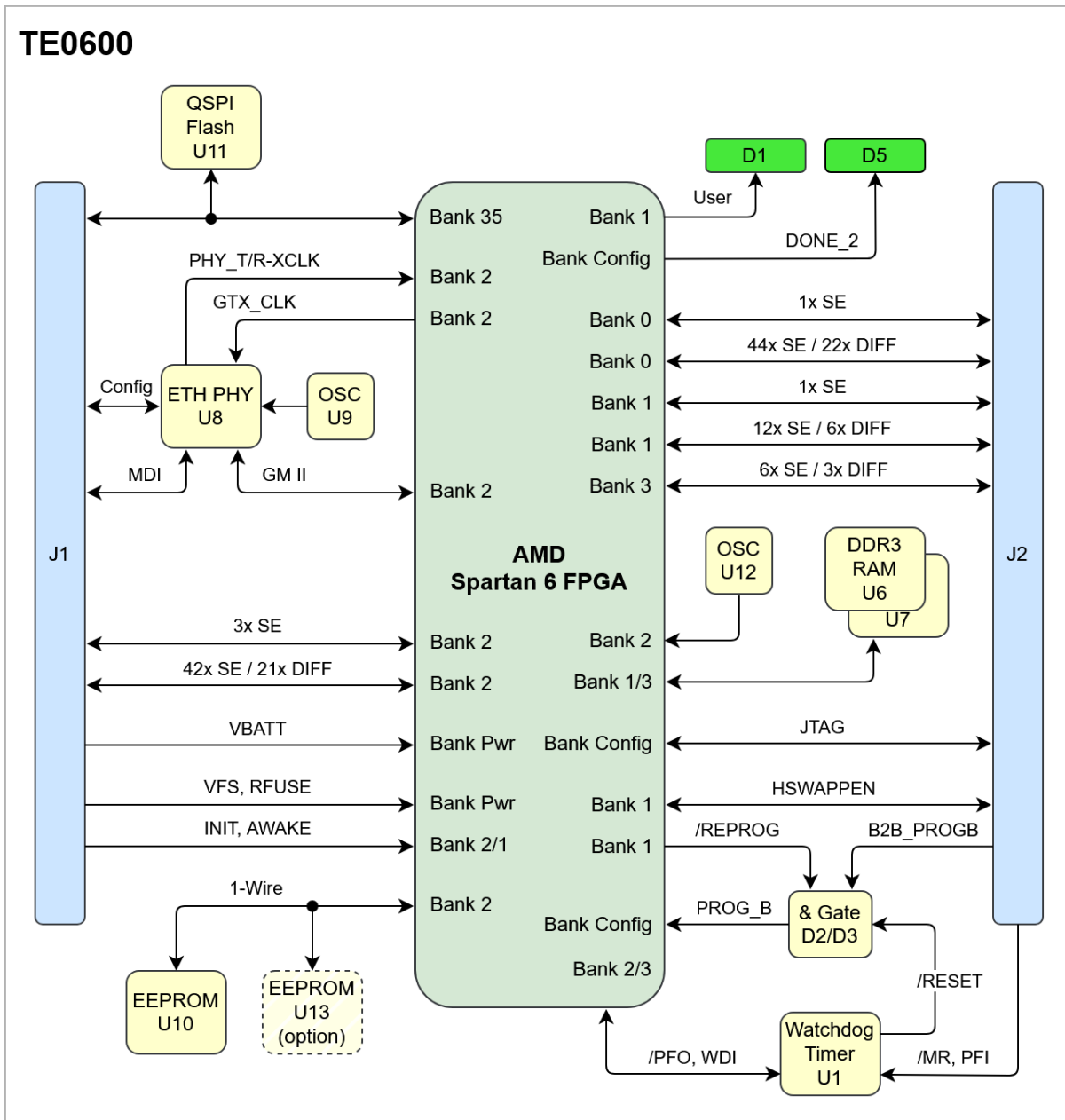
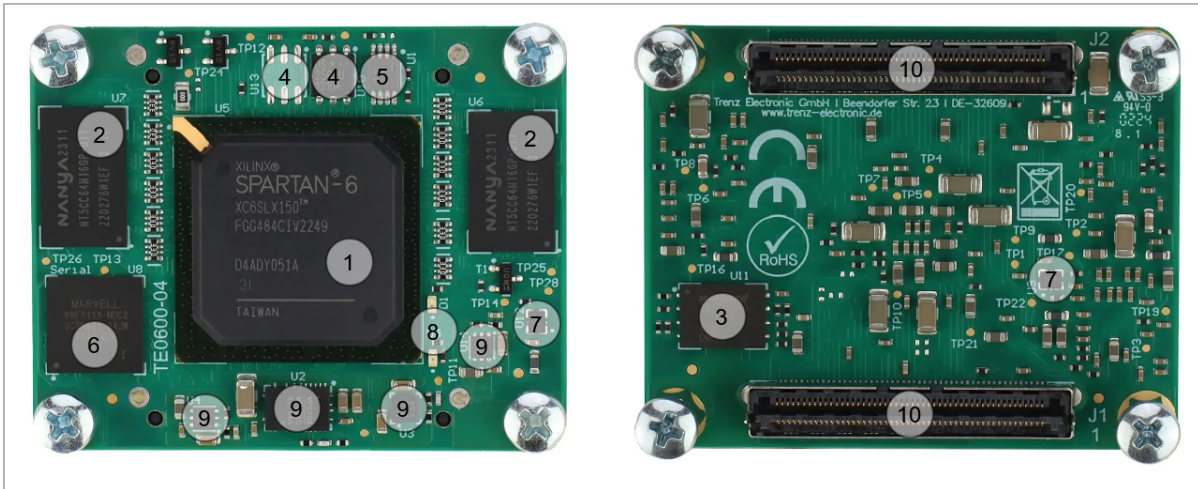


Figure 1: TE0600 block diagram

### 4.3 Main Components



**Figure 2: TE0600 main components**

1. Spartan 6 FPGA, U5
2. DDR3 SDRAM, U6, U7
3. QSPI Flash, U11
4. EEPROM, U10, U13
5. Watchdog, U1
6. Ethernet PHY, U8
7. Oscillators, U9, U12
8. Green LEDs, D1, D5
9. DCDCs, U2, U3, U4, U14
10. B2B connectors, J1, J2

### 4.4 Initial Delivery State

Storage device name	Content	Notes
QSPI Flash U11	Not programmed	
EEPROM, U10	Not programmed	Contains write protected Unique Node ID / MAC .
Optional EEPROM, U13	Not programmed	Contains write protected Unique Node ID / MAC and SHA-1 engine.
DDR3 SDRAM, U6, U7	Not programmed	

**Table 1: Initial delivery state of programmable devices on the module**

## 5 Signals, Interfaces and Pins

### 5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	J1	QSPI	6	Connects to FPGA U5 and QSPI flash U11.
B2B	J1	IO	3 SE	FPGA IO BANK 2.
B2B	J1	IO	42 SE / 21 DIFF	FPGA IO BANK 2.
B2B	J1	Ethernet MDI	9	4x DIFF data.
B2B	J2	IO	1 SE	FPGA IO BANK 0.
B2B	J2	IO	44 SE / 22 DIFF	FPGA IO BANK 0.
B2B	J2	IO	1 SE	FPGA IO BANK 1.
B2B	J2	IO	12 SE / 6 DIFF	FPGA IO BANK 1.
B2B	J2	IO	6 SE	FPGA IO BANK 3.
B2B	J2	JTAG	4	

**Table 2: Board Connectors**

### 5.2 Test Points

Test Point	Signal	Notes
TP1	1.5V	

Test Point	Signal	Notes
TP2	3.3V	
TP3	2.5V	
TP4	VCCAUX	
TP5	1.2V	
TP6	GND	
TP7	VCCIO0	
TP8	VREF1	
TP9	VREF2	
TP10	MAC_DATA	
TP11	1.5V	
TP12	3.3V	
TP13	2.5V	
TP14	VCCAUX	
TP16	CLK_P	
TP17	PHY_CLK	
TP18	GND	
TP19	GND	
TP20	GND	
TP21	GND	

Test Point	Signal	Notes
TP22	PROG_B	
TP23	GND	
TP24	VCCIO0	
TP25	VREF1	
TP26	VREF2	
TP27	MAC_DATA	
TP28	CLK_P	

**Table 3: Test Points Information**

## 6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
Spartan 6 FPGA	U5	<ul style="list-style-type: none"> <li>• DDR3 RAM</li> <li>• OSPI Flash</li> <li>• EEPROM U10</li> <li>• EEPROM U13</li> <li>• Watch dog U1</li> <li>• Ethernet PHY U8</li> </ul>	
DDR3 SDRAM	U6 / U7	<ul style="list-style-type: none"> <li>• FPGA U5</li> </ul>	
QSPI Flash	U11	<ul style="list-style-type: none"> <li>• FPGA U5</li> <li>• B2B connector J1</li> </ul>	Accessible via FPGA and B2B.
EEPROM	U10	<ul style="list-style-type: none"> <li>• FPGA U5</li> </ul>	
EEPROM	U13	<ul style="list-style-type: none"> <li>• FPGA U5</li> </ul>	
Watchdog	U1	<ul style="list-style-type: none"> <li>• FPGA U5</li> <li>• B2B connector J1</li> <li>• B2B connector J2</li> </ul>	
Ethernet PHY	U8	<ul style="list-style-type: none"> <li>• B2B connector J1</li> <li>• SoC MIO</li> </ul>	Gigabit ETH PHY
Oscillator	U12	<ul style="list-style-type: none"> <li>• FPGA U5</li> </ul>	100 MHz
<b>Oscillator</b>	U9	<ul style="list-style-type: none"> <li>• Ethernet PHY U8</li> </ul>	25 MHz

**Table 4: On board peripherals**

## 7 Configuration and System Control Signals

Signal Name	Connector.Pin	Direction <sup>1)</sup>	Description
EN	J1.28	IN	Enables all voltage converters.
INIT	J1.30	INOUT	Bidirectional pin for configuration. <sup>2)</sup>
SUSPEND	J1.77	IN	Dedicated Active-High control pin for power saving. <sup>2)</sup>
VFS	J1.81	IN	Power supply pin for eFUSE / decryptor key programming. <sup>2)</sup>
RFUSE	J1.83	IN	Auxiliary pin for eFUSE programming. <sup>2)</sup>
AWAKE	J1.85	INOUT	Status output pin for the power-saving Suspend mode or IO pin. <sup>2)</sup>
B2B_PROG B	J2.11	IN	Reset signal. Signal to manipulate the PROGRAM_B_2 signal/pin. Active-Low asynchronous reset to configuration logic. <sup>2)</sup>
HSWAPPEN	J2.13	IN	IO Pullup state before and during configuration. <sup>2)</sup>
CSO_B / CCLK / MISO / MOSI / MISO3 / MISO2	J1.17 / J1.19 / J1.21 / J1.23 / J1.25 / J1.27	Signal dependent	QSPI interface. <sup>2)</sup> Refer to <a href="#">Winbond W25Q128JV</a> .
JTAG	J2.93 / J2.95 / J2.97 / J2.99	Signal dependent	JTAG interface. <sup>2)</sup>

Signal Name	Connector.Pin	Direction <sup>1)</sup>	Description
PHY_L10 / PHY_L100 / PHY_L1000 / PHY_DUPLEX / PHY_LED_TX / PHY_LED_RX	J1.17 / J1.19 / J1.21 / J1.23 / J1.25 / J1.27	Signal dependent	Ethernet PHY configuration pins for Link Speed, Duplex Mode, MDI crossover and other features.  See <a href="#">Marvell Alaska 88E1111 Datasheet</a> .
PFI	J2.16	IN	Power-fail comparator input.  Refer to watchdog datasheet <a href="#">TPS3705-33DGN</a> .
/MR	J2.18	IN	Manual reset input.  Refer to watchdog datasheet <a href="#">TPS3705-33DGN</a> .

**Table 5: Controller signal.**

<sup>1)</sup> Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

<sup>2)</sup> See [AMD UG380 / UG385](#).

## 8 Power and Power-On Sequence

### 8.1 Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction <sup>1)</sup>	Notes
3.3V	J1.1 / J1.3 / J1.5 / J1.7 / J1.9 / J1.11 / J1.13 / J1.15  J2.2 / J2.4 / J2.6 / J2.8 / J2.10 / J2.12	IN	SoM supply.
VCCIO0	J2.1 / J2.3 / J2.5 / J2.7 / J2.9	IN	FPGA IO Bank 0 supply.
VBATT	J1.79	IN	Decryptor key RAM memory backup supply.
1.2V	J1.41 / J1.43	OUT	FPGA and Ethernet PHY supply.
1.5V	J2.19	OUT	FPGA DDR Bank 1/3 and DDR RAM supply.
2.5V	J1.39	OUT	Ethernet PHY supply.
VCCAUX	J2.91	OUT	JTAG reference voltage.

**Table 6: Module power rails.**

<sup>1)</sup> Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

### 8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
1	-	-	-	Configuration signal setup.	See <a href="#">Configuration and System Control Signals</a> .
	3.3V	_ 1)	-	Main Power supply.	
2	VCCIO0	_ 1)	-	Bank IO Power supply.	
3	EN	3.3 V ( $\pm 5\%$ )	-	Enable SoM.	

**Table 7: Baseboard Design Hints**

<sup>1)</sup> Refer to [Recommended Operating Conditions](#).

For more information refer to [DS162](#).

## 9 Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three [Samtec Razor Beam LSHM connectors](#) on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

### 9.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

**Table 8: Connectors.**

The module can be manufactured using other connectors upon request.

## 9.2 Connector Speed Ratings

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The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

**Table 9: Speed rating.**

## 9.3 Current Rating

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Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

## 9.4 Connector Mechanical Ratings

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- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

## 10 Technical Specifications

This TRM is generic for all variants.

- The voltage ranges are generally the same across variants (exceptions are possible, depending on custom requests).
- The temperature range can differ depending on the assembly version.
- The combination of a carrier and a SoM might have different requirements.

Variants of modules are described here: [Article Number Information](#). Please contact us for options.

### 10.1 Absolute Maximum Ratings <sup>\*)</sup>

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
3.3V	Supply power from carrier.	-0.5	3.75	V
VCCIO0	IO Bank 0 supply power from carrier.	-0.5	3.75	V
VBATT	Decryptor key RAM memory backup supply.	-0.5	4.05	V
VFS	eFUSE Programming voltage supply.	-0.5	3.75	V

**Table 10: Absolute maximum ratings**

<sup>\*)</sup> Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Condition". Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

### 10.2 Recommended Operating Conditions

Trenz Electronic classifies modules into temperature range categories by subsumption of its component data (PCB, ICs, connectors, passive components). The temperature ranges are values for ambient air temperature and do not reflect the junction temperature of individual components.

The categories are:

- Modules with commercial temperature grade are equipped with components that cover at least the ambient temperature range of 0°C to 75°C.
- Modules with extended temperature grade are equipped with components that cover at least the ambient temperature range of 0°C to 85°C.
- Modules with industrial temperature grade are equipped with components that cover at least the ambient temperature range of -40°C to 85°C.

These categories do not take into account the entire custom system consisting of:

- Customer SoC/FPGA design.
- Cooling solution, active and or passive cooling.
- Climate or enviromental conditions besides ambient temperature range.
- Module orientation, neighboring assemblies, neither other heat sources nor the SoC/FPGA as heat source to other components.

### 10.2.1 Temperature range

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The SoM components are capable of being operated at industrial-grade temperatures, which cover at least the range of -40 °C to +85 °C.

The actual operating temperature range will depend on the customer design, usage and cooling solution. Consult [Cooling Solutions](#) for more information.

### 10.2.2 Voltage rails

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Parameter	Min	Max	Units	Reference Document
3.3V	3.135	3.465	V	
VCCIO0	1.1	3.45	V	
VBATT	1.0	3.6	V	
VFS	3.2	3.4	V	

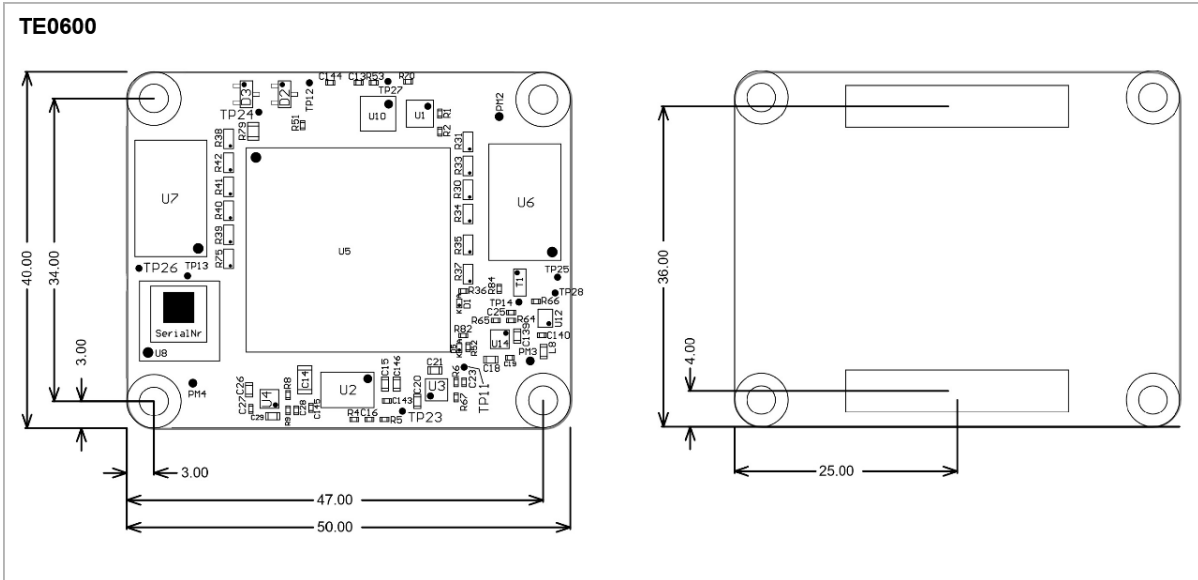
**Table 11: Recommended operating conditions.**

## 10.3 Physical Dimensions

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- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.
- PCB thickness: 1.724 ±10 % mm.

All dimensions are shown in millimeters.



**Figure 3: Physical Dimension**

## 11 Currently Offered Variants

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Trenz shop TE0600 overview page*	
<a href="#">English page</a>	<a href="#">German page</a>

**Table 12: Trenz Electronic Shop Overview**

\*) Module article name encoding table: 6 Series Spartan 6 modules

## 12 Revision History

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### 12.1 Hardware Revision History

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The hardware revision number is located on the PCB next to the module identifier, separated by a dash.




**Figure 4: Board hardware revision number.**

Date	Revision	Changes	Documentation Link
2024-01	04	<ol style="list-style-type: none"> <li>1. Leds D1, D5 were changed from 19-213/G6C-BM1N2/DT to SML-P11MTT86.</li> <li>2. R83 was added. Inserted internal pull-up IO resistor option for FPGA via external resistor (R83).</li> <li>3. D3 was changed from single BAT54VV,115 to pair BAT54A,215.</li> <li>4. U2 was changed from EN6347QI to MPM3860GQW-Z and adapted power circuit.</li> <li>5. U3 was changed from EP53F8QI to MPM3834CGPA and adapted power circuit.</li> <li>6. Testpoints TP11 - TP15 , TP23 - TP28 were added.</li> <li>7. Changed LDO LP3878SD-ADJ (U4, U14) to TPS74601PBDRVT and adapted power circuit.</li> <li>8. Assembled clock SiT8008BI-73-XXS-100.000000E (U12).</li> <li>9. Improved led (D1) driving circuit via adding MOSFET (T1) and resistor (R84) and changed 120 Ohm resistor (R36) to 240 Ohm.</li> <li>10. Changed 2.2 kOhm resistor (R29) to 100 Ohm.</li> <li>11. Changed 2.2 kOhm resistor (R56, R57, R58) to 2.4 kOhm.</li> <li>12. Pulled-down board revision signal "BR0" (FPGA U5, pin P17) and updated board revision documentation.</li> <li>13. Changed fiducials to standard fiducial type.</li> <li>14. Changed stacked vias to staggered vias.</li> <li>15. Signal trace lengths changed.</li> <li>16. Updated B2B documentation.</li> <li>17. Renamed document sheets.</li> <li>18. Updated legal notices, revision history, block and power diagram. Updated page count and order.</li> </ol>	<a href="#">REV04</a> <a href="#">PCN</a>

Date	Revision	Changes	Documentation Link
2016-08	03	<ol style="list-style-type: none"> <li>1. Added NetTie (board revision 03).</li> <li>2. Optimized placement and routing for DCDC converters.</li> <li>3. Added tespoints.</li> <li>4. Changed U9 from SIT1602AI-83-33E-25.0000 to SiT8008AI-73-XXS-25.000000E.</li> <li>5. Update Razorbeam Connectors, full update lib.</li> <li>6. Added serial number (Track-it™ Traceability Pad).</li> <li>7. Added thermal vias to mounting holes.</li> <li>8. DDR3 changed from IM4G16D3EABG-125I to IM4G16D3FABG-125I for the 4 GBit variants.</li> <li>9. Change SPI Flash from W25Q128BVEIG to W25Q128FVEIG (W25Q128FVEIG 3V 128MBit Serial Flash) .</li> <li>10. U13 (DS2432P+) is no longer populated by default.</li> <li>11. Changed Board revision identification to REV03.</li> <li>12. Changee SPI Flash from W25Q128FVEIG to W25Q128JVEIQ.</li> <li>13. Changed DDR3 RAM from IM4G16D3FABG-125I to IS43TR16256BL-125KBLI</li> <li>14. Clock Revision Change from SiT8008AI-73-XXS-25.000000E to SiT8008BI-73-XXS-25.000000E.</li> <li>15. LEDs D1 and D5 changed to 19-213/G6C-BM1N2/DT.</li> </ol>	<a href="#">REV03</a> <a href="#">PCN</a> <a href="#">PCN</a> <a href="#">PCN</a>
2013-08	02	<ol style="list-style-type: none"> <li>1. More powerful regulators for 1.2V and 1.5V rails.</li> <li>2. VCCAUX separated from 2.5V power rail.</li> <li>3. 128 Mbit SPI Flash.</li> <li>4. Additional secure 1 Kbit EEPROM.</li> <li>5. Optional B2B connection to bank 2 differential clock input.</li> <li>6. New memory options.</li> </ol>	<a href="#">REV02</a> <a href="#">PCN</a>
-	01	Initial release	<a href="#">REV01</a>

**Table 13: Hardware Revision History**

## 12.2 Document Change History

Date	Revision	Contributor	Description
 2025-05-13	v.39	Kilian Jahn	<ul style="list-style-type: none"> <li>• Updated to TRM version 4.3</li> <li>• Updated TRM to hardware revision 04</li> <li>• Minor error corrections</li> <li>• Fixed Inter Page Links</li> <li>• Updated PDF &amp; PDF-Web Link</li> </ul>
2024-03-21	v.28	VY	<ul style="list-style-type: none"> <li>• Updated SoM statuses in <i>Assembly variants pin coding</i> Table</li> </ul>
2024-03-11	v.27	MT	<ul style="list-style-type: none"> <li>• Added REV04 to assembly variant coding table</li> <li>• Added REV04 to revision coding table</li> <li>• Added main differences between 03 and 04 revisions</li> <li>• Updated nets lengths table</li> <li>• Added info about additional 3.3V single-ended oscillator (U12)</li> <li>• Updated supply diagram</li> <li>• Updated block diagram</li> </ul>
2017-04-03	v.26	TT	<ul style="list-style-type: none"> <li>• Added REV03 to assembly Variant Table</li> </ul>
2016-11-05	v.25	FDR	<ul style="list-style-type: none"> <li>• Document ported to wiki and adapted to web presentation.</li> </ul>
2016-01-29	v.24	AIK	<ul style="list-style-type: none"> <li>• Pause advertise correction</li> </ul>
2013-03-13	v.23	AIK	<ul style="list-style-type: none"> <li>• Changed Bank 1 power supply description and VCCIO0 sources description</li> </ul>
2013-03-13	v.22	AIK	<ul style="list-style-type: none"> <li>• Connectors current chapter moved to separate document</li> </ul>
2013-01-21	v.21	AIK	<ul style="list-style-type: none"> <li>• Added PHY reset note</li> </ul>

Date	Revision	Contributor	Description
2012-12-19	v.20	AIK	<ul style="list-style-type: none"> <li>Fixed SPI Flash size on block diagram</li> </ul>
2012-11-30	v.19	AIK	<ul style="list-style-type: none"> <li>Added Ethernet disable note</li> </ul>
2012-11-21	v.18	AIK	<ul style="list-style-type: none"> <li>Updated module diagram</li> </ul>
2012-11-06	v.17	AIK	<ul style="list-style-type: none"> <li>Fixed bank 1 power options</li> </ul>
2012-10-30	v.16	AIK	<ul style="list-style-type: none"> <li>Fork to 01 and 02 board revisions</li> </ul>
2012-07-18	v.15	AIK	<ul style="list-style-type: none"> <li>Added table with B2B signals summary per FPGA bank</li> </ul>
2012-06-18	v.14	FDR	<ul style="list-style-type: none"> <li>Removed junction temperature limits under connector current ratings.</li> </ul>
2012-05-18	v.13	AIK	<ul style="list-style-type: none"> <li>Corrected cross-reference in section 3.2. Corrected LED description.</li> </ul>
2012-04-17	v.12	FDR	<ul style="list-style-type: none"> <li>Updated documentation link.</li> <li>Replaced obsolete EIDesI and RedMine links with current GitHub links.</li> <li>Updated dating convention.</li> </ul>
2012-04-12	v.11	AIK	<ul style="list-style-type: none"> <li>Added FPGA banks VCCIO voltages table.</li> </ul>
2012-01-20	v.10	AIK	<ul style="list-style-type: none"> <li>Added pin compatibility note and manual reference.</li> </ul>
2011-11-11	v.9	AIK	<ul style="list-style-type: none"> <li>Added pin numbering description for B2B connectors</li> </ul>
2011-10-12	v.8	AIK	<ul style="list-style-type: none"> <li>Fix in eFUSE section.</li> </ul>
2011-10-08	v.7	AIK	<ul style="list-style-type: none"> <li>Little fixes after FDR audit.</li> </ul>

Date	Revision	Contributor	Description
2011-10-06	v.6	AIK	<ul style="list-style-type: none"> <li>Added power consumption section.</li> </ul>
2011-10-06	v.5	AIK	<ul style="list-style-type: none"> <li>Removed net length information for nets which can't be measured right.</li> </ul>
2011-10-06	v.4	AIK	<ul style="list-style-type: none"> <li>Added board photos. Additions to eFUSE section.</li> </ul>
2011-10-06	v.3	AIK	<ul style="list-style-type: none"> <li>Reformatted pin-out tables. Added eFUSE programming section.</li> </ul>
2011-10-05	v.2	AIK	<ul style="list-style-type: none"> <li>Added B2B pin-out section.</li> </ul>
2011-10-01	v.1	AIK	<ul style="list-style-type: none"> <li>Release.</li> </ul>
--	all	Maksim Tserabei , Ali Naseri , Fabio De Riccardis , John Hartfiel , Kilian Jahn , Susanne Kunath , Thorsten Trenz , Vadim Yunitski	<ul style="list-style-type: none"> <li>--</li> </ul>

**Table 14: Document change history.**

## 13 Disclaimer

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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 2019-06-07