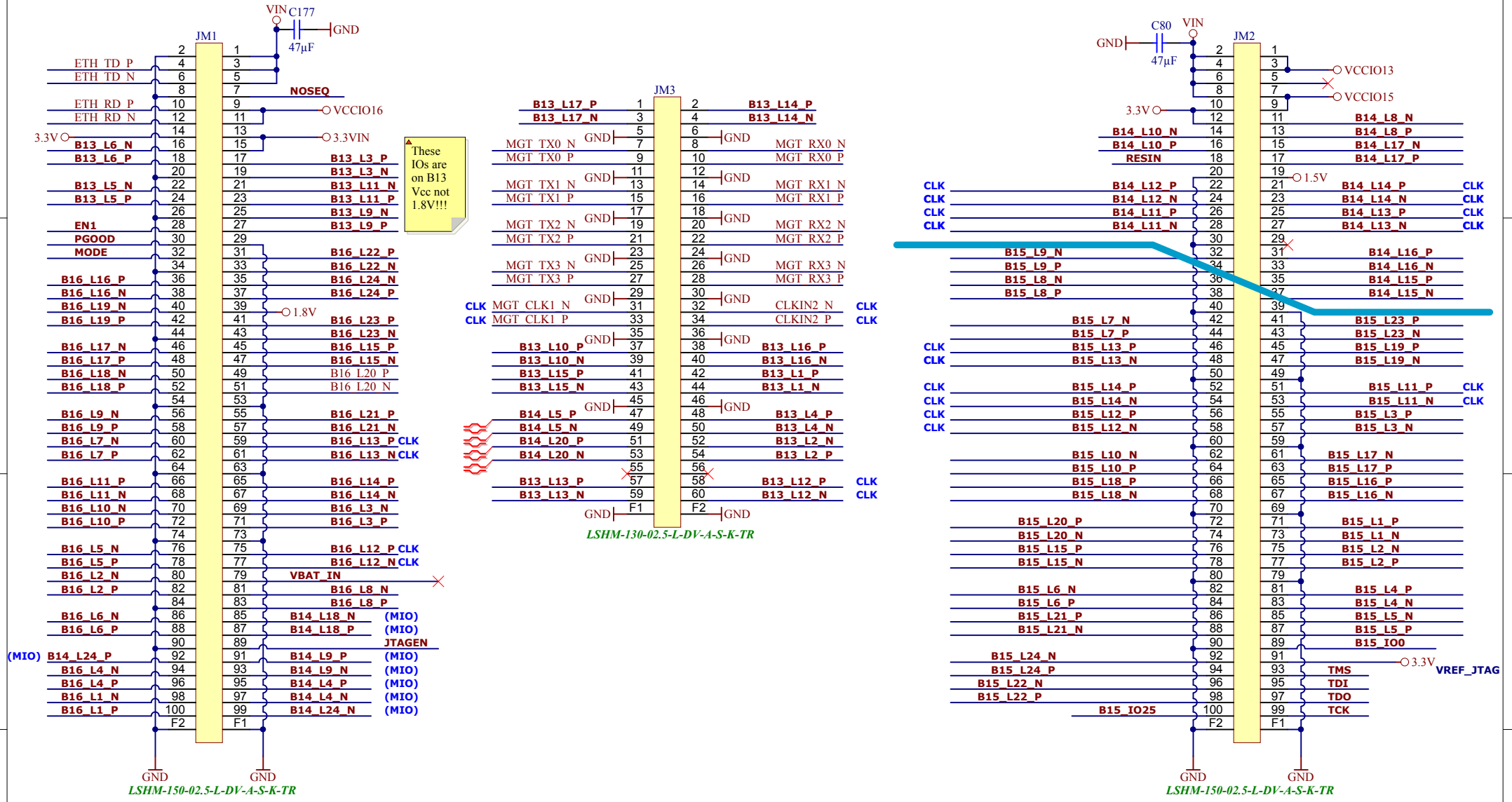

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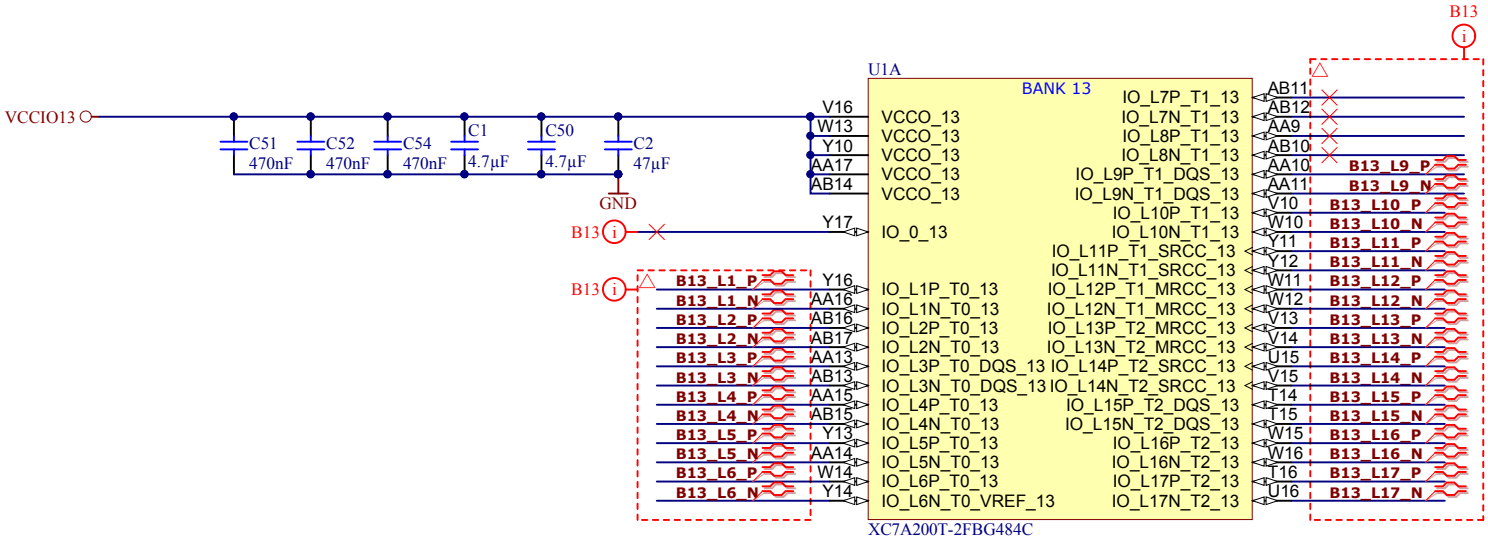
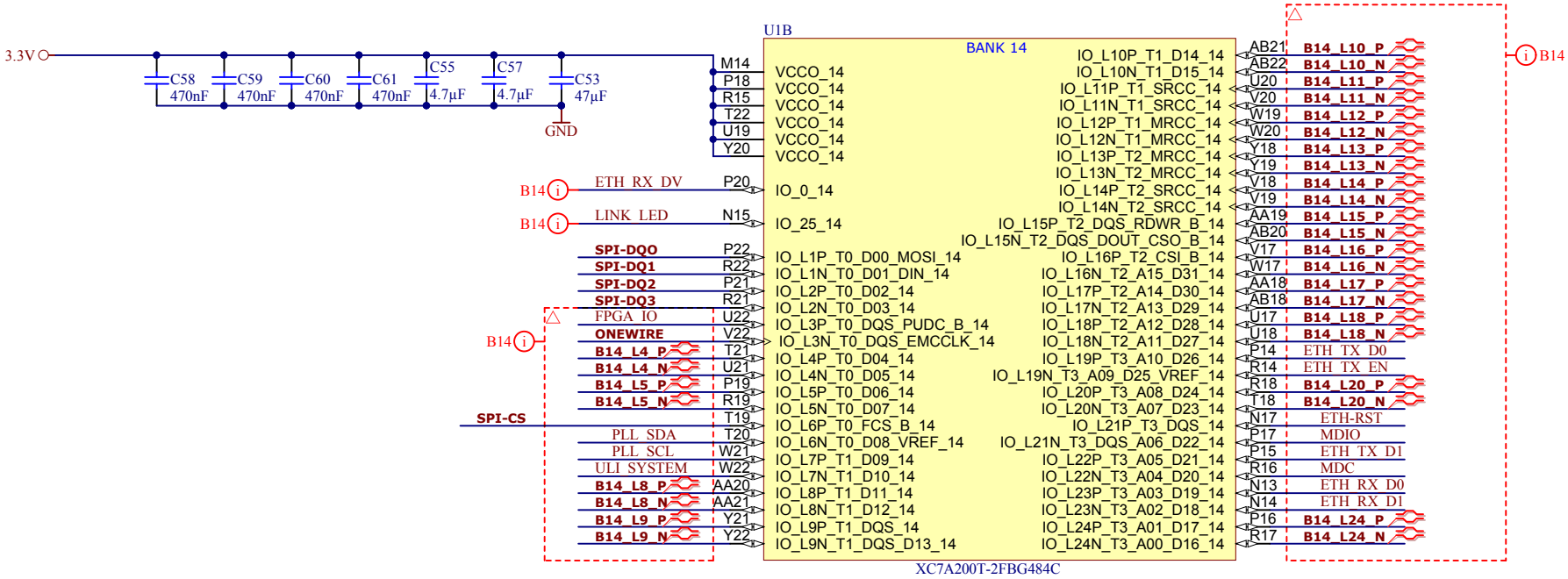
Title: B2B			
A4	Number: TE0712 200_2C3		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page1 of 16
Filename: B2B-Connectors.SchDoc			



trenz electronic	Title: B13		
A4	Number: TE0712 200_2C3		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page2 of 16
Filename: B13.SchDoc			



trenz electronic	Title: B14		
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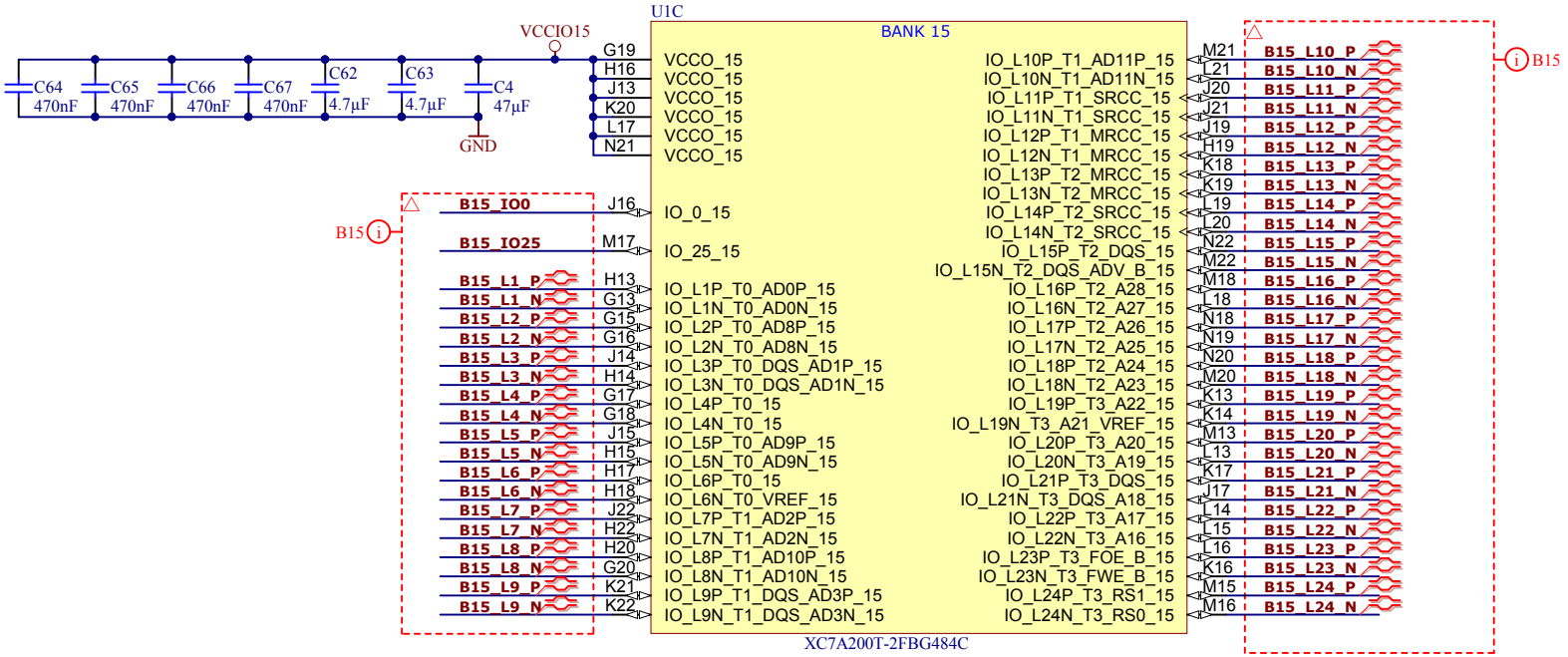
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page3 of 16
	Filename: B14.SchDoc		



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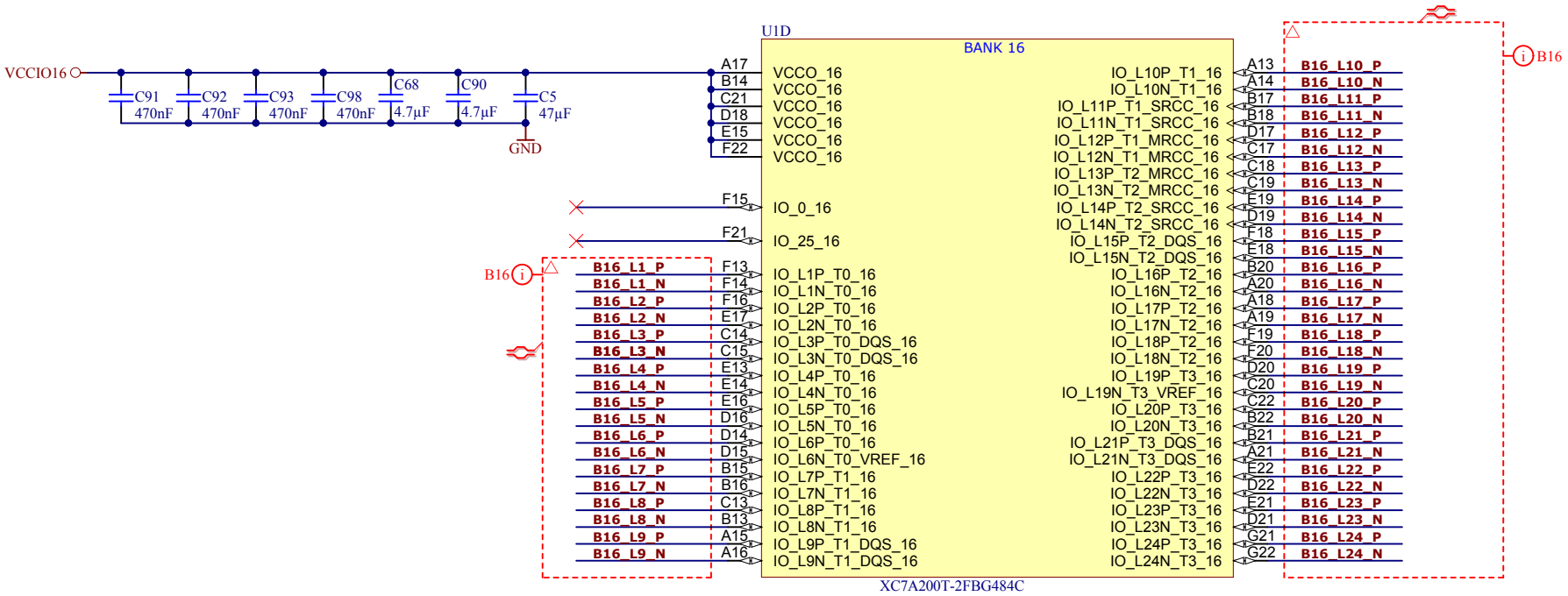
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page4 of 16
	Filename: B15.SchDoc		



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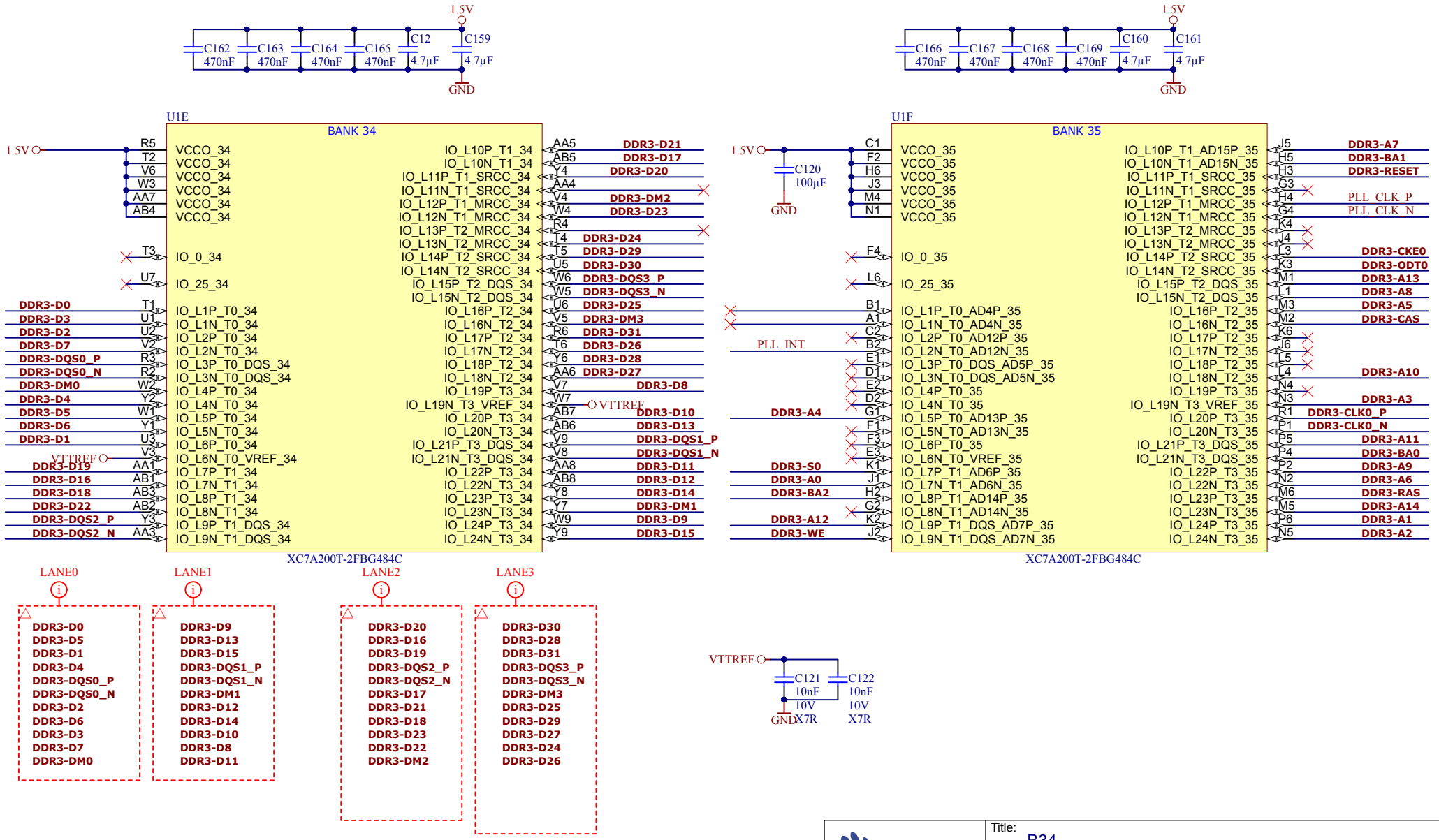
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page5 of 16
Filename: B16.SchDoc			



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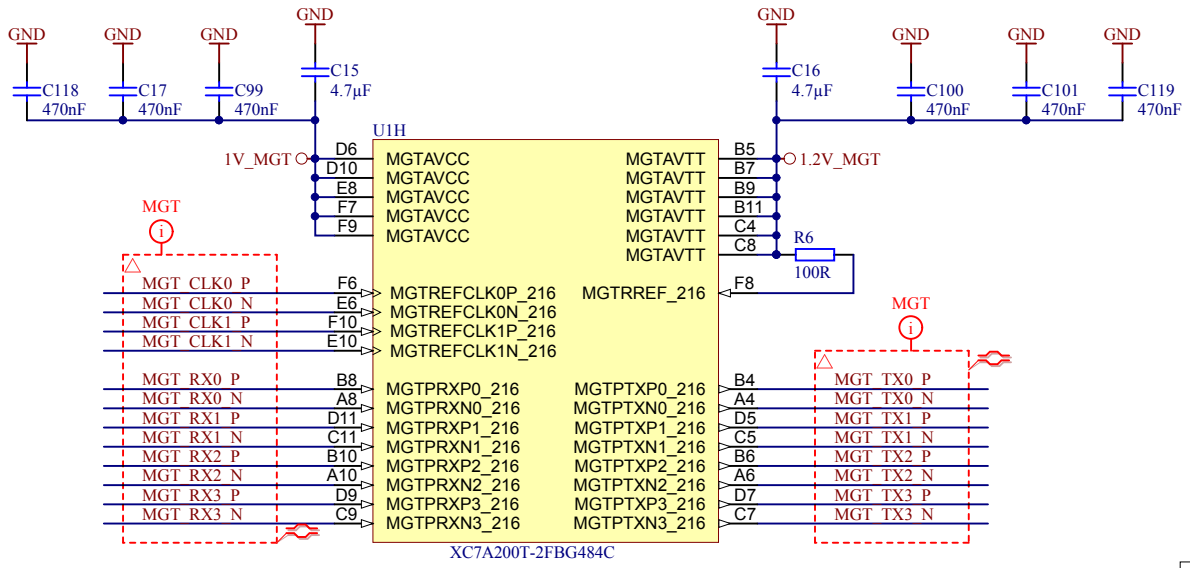
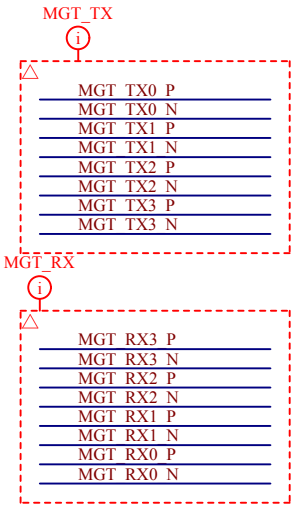
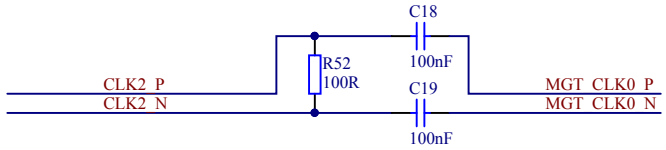
Rev.	01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH
Page6 of 16	
Filename:	B34.SchDoc







trenz electronic	Title: MGT		
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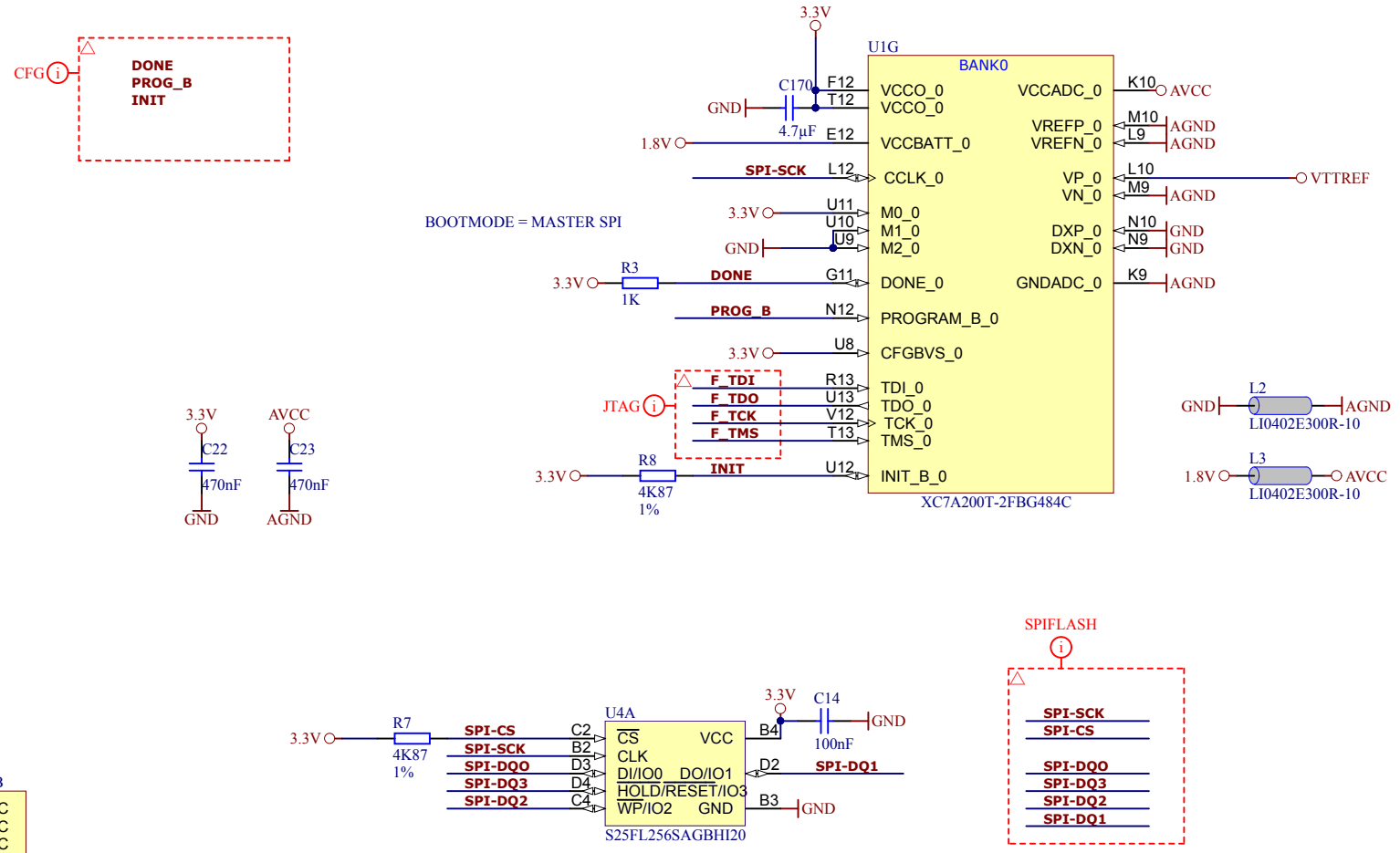
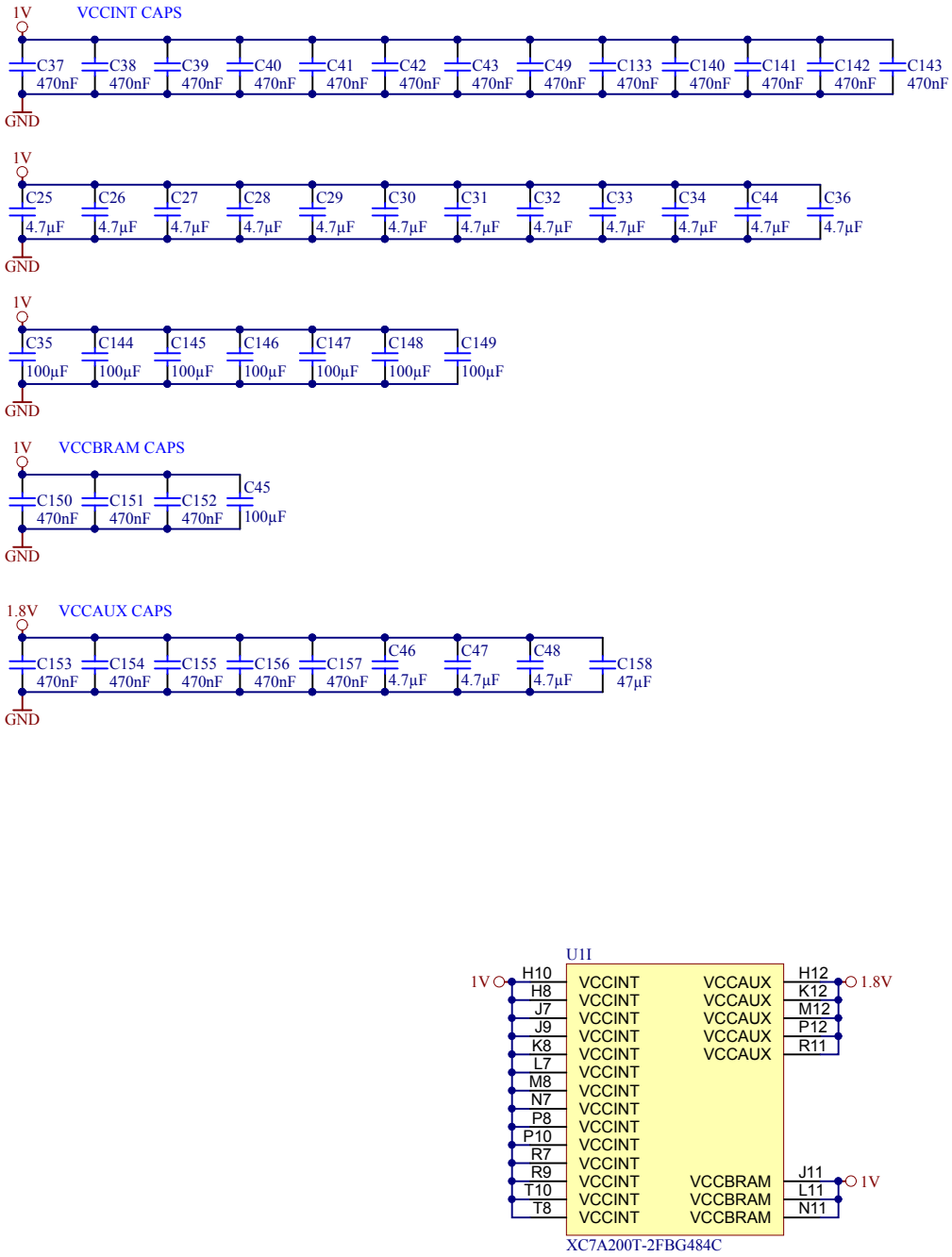
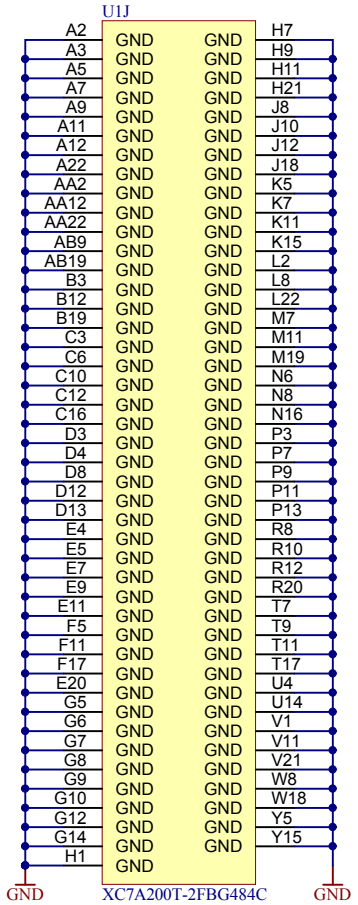
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page7 of 16
Filename: FPGA-MGT.SchDoc			



trenz electronic	Title: CFG		
	A4	Number: TE0712 200_2C3	Rev. 01
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page8 of 16
	Filename: FPGA-CFG.SchDoc		





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Title: PWR			
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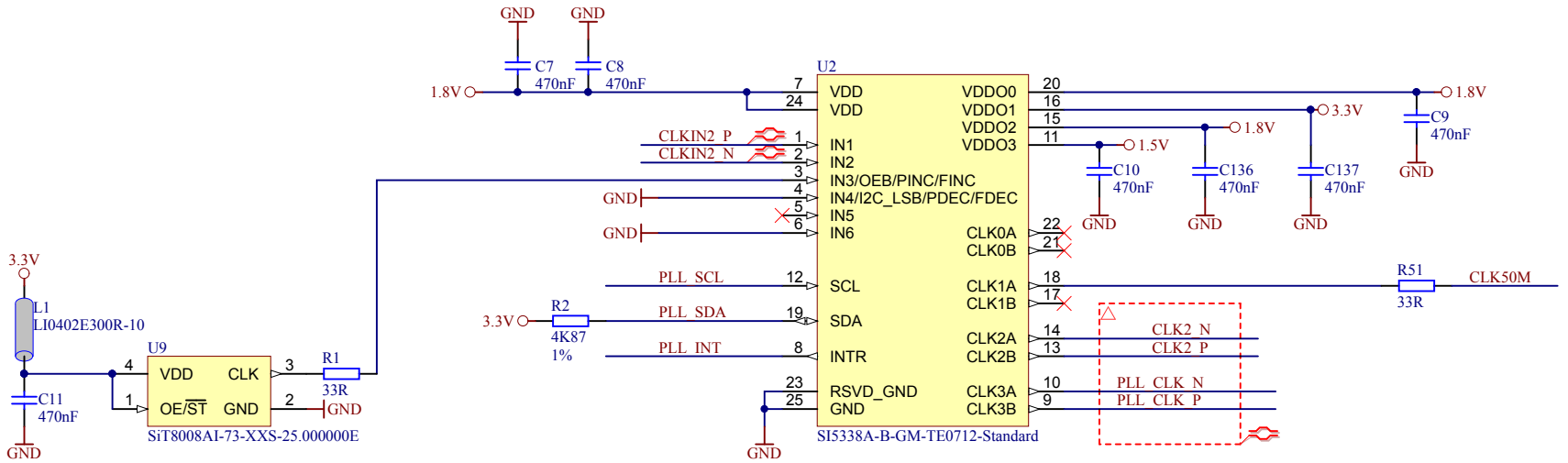
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page9 of 16
Filename: FPGA-PWR.SchDoc			



trenz electronic	Title: Clock		
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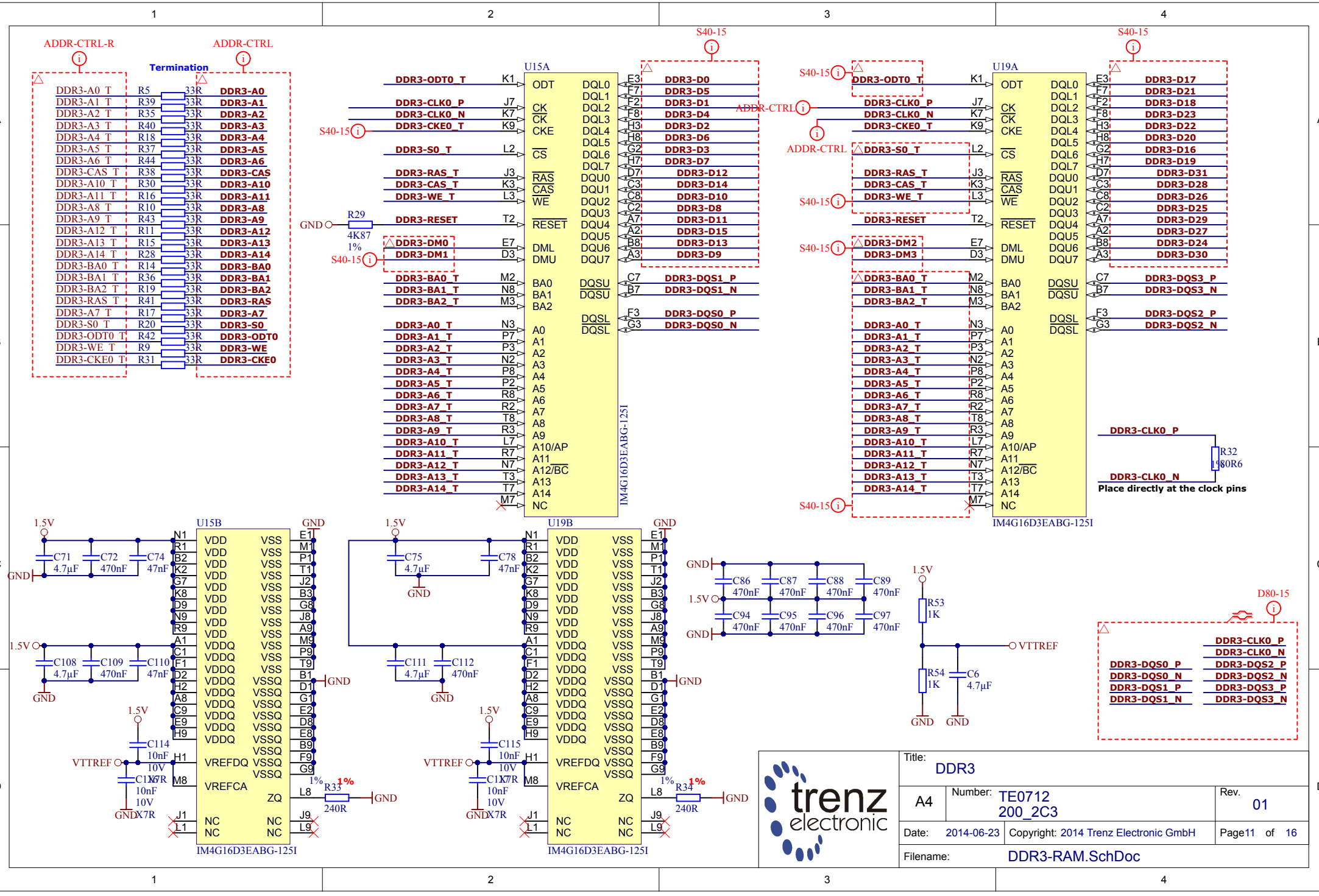
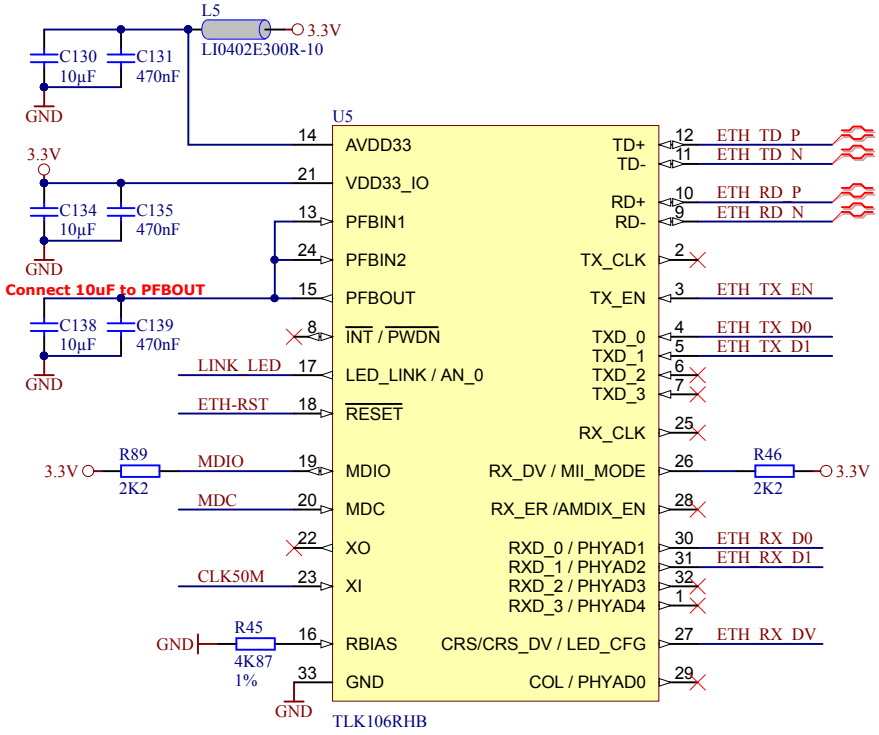
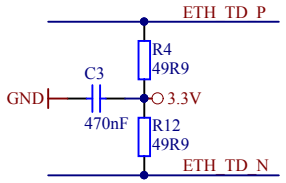
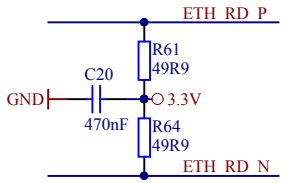
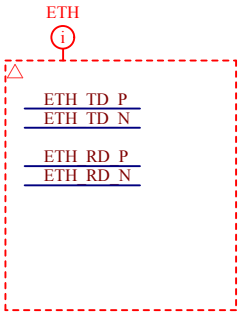
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page10 of 16
Filename: Clock.SchDoc			


ADDR-CTRL-R
ADDR-CTRL
Termination
DDR3-A0_T R5 33R DDR3-A0
DDR3-A1_T R39 33R DDR3-A1
DDR3-A2_T R35 33R DDR3-A2
DDR3-A3_T R40 33R DDR3-A3
DDR3-A4_T R18 33R DDR3-A4
DDR3-A5_T R37 33R DDR3-A5
DDR3-A6_T R44 33R DDR3-A6
DDR3-CAS_T R38 33R DDR3-CAS
DDR3-A10_T R30 33R DDR3-A10
DDR3-A11_T R16 33R DDR3-A11
DDR3-A8_T R10 33R DDR3-A8
DDR3-A9_T R43 33R DDR3-A9
DDR3-A12_T R11 33R DDR3-A12
DDR3-A13_T R15 33R DDR3-A13
DDR3-A14_T R28 33R DDR3-A14
DDR3-BA0_T R14 33R DDR3-BA0
DDR3-BA1_T R36 33R DDR3-BA1
DDR3-BA2_T R19 33R DDR3-BA2
DDR3-RAS_T R41 33R DDR3-RAS
DDR3-A7_T R17 33R DDR3-A7
DDR3-S0_T R20 33R DDR3-S0
DDR3-ODT0_T R42 33R DDR3-ODT0
DDR3-WE_T R9 33R DDR3-WE
DDR3-CKE0_T R31 33R DDR3-CKE0
U15A
U19A
S40-15
ADDR-CTRL
IM4G16D3EABG-125I
R29 4K87 1%
GND
DDR3-RESET
DDR3-ODT0_T
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-CKE0_T
DDR3-S0_T
DDR3-RAS_T
DDR3-CAS_T
DDR3-WE_T
DDR3-DM0
DDR3-DM1
DDR3-DM2
DDR3-DM3
DDR3-BA0_T
DDR3-BA1_T
DDR3-BA2_T
DDR3-A0_T
DDR3-A1_T
DDR3-A2_T
DDR3-A3_T
DDR3-A4_T
DDR3-A5_T
DDR3-A6_T
DDR3-A7_T
DDR3-A8_T
DDR3-A9_T
DDR3-A10_T
DDR3-A11_T
DDR3-A12_T
DDR3-A13_T
DDR3-A14_T
DDR3-D0
DDR3-D5
DDR3-D1
DDR3-D4
DDR3-D2
DDR3-D6
DDR3-D3
DDR3-D7
DDR3-D12
DDR3-D14
DDR3-D10
DDR3-D8
DDR3-D11
DDR3-D15
DDR3-D13
DDR3-D9
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-D17
DDR3-D21
DDR3-D18
DDR3-D23
DDR3-D22
DDR3-D20
DDR3-D16
DDR3-D19
DDR3-D31
DDR3-D28
DDR3-D26
DDR3-D25
DDR3-D29
DDR3-D27
DDR3-D24
DDR3-D30
DDR3-DQS3_P
DDR3-DQS3_N
DDR3-DQS2_P
DDR3-DQS2_N
R32 1%80R6
Place directly at the clock pins
U15B
U19B
1.5V
GND
C71 4.7µF
C72 470nF
C74 47nF
C108 4.7µF
C109 470nF
C110 47nF
C114 10nF 10V X7R
C115 10nF 10V X7R
C75 4.7µF
C78 47nF
C111 4.7µF
C112 470nF
C86 470nF
C87 470nF
C88 470nF
C89 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
R53 1K
R54 1K
C6 4.7µF
VTTREF
R33 240R 1%
R34 240R 1%
D80-15
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
trenz electronic
Title: DDR3
A4
Number: TE0712 200_2C3
Rev. 01
Date: 2014-06-23
Copyright: 2014 Trenz Electronic GmbH
Page11 of 16
Filename: DDR3-RAM.SchDoc

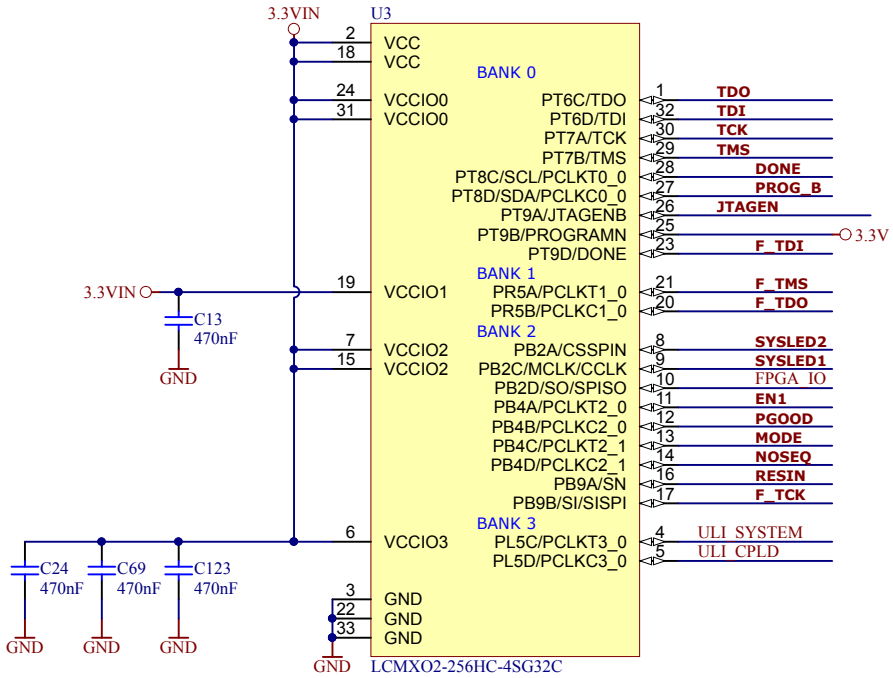


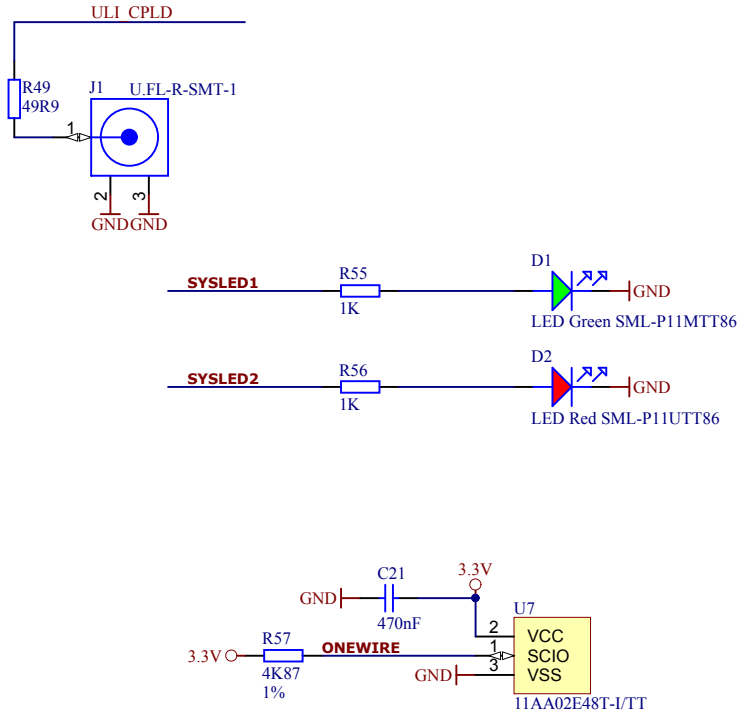




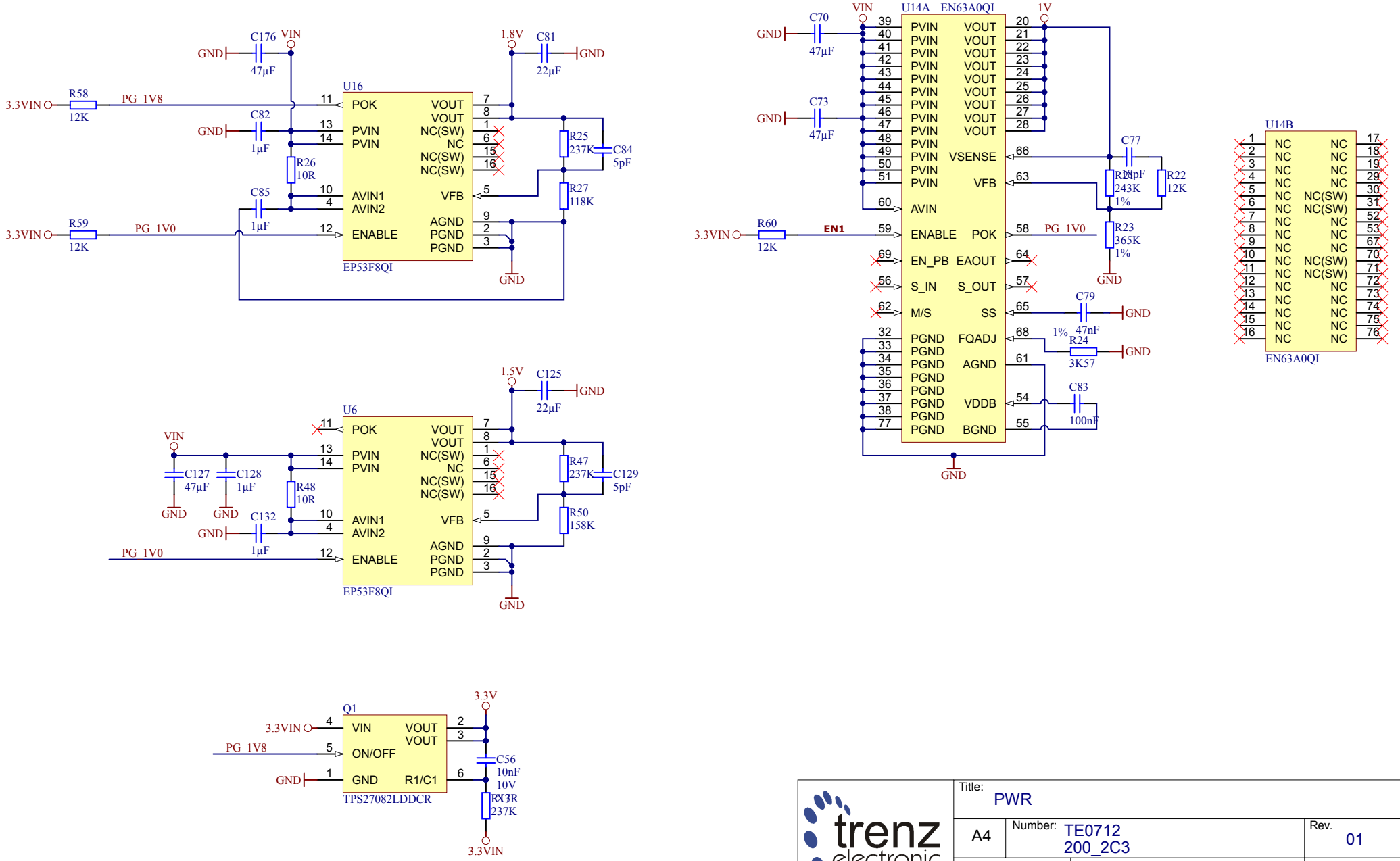


trenz electronic	Title: ETH		
	A4	Number: TE0712 200_2C3	Rev. 01
	Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page12 of 16
	Filename: ETHERNET.SchDoc		

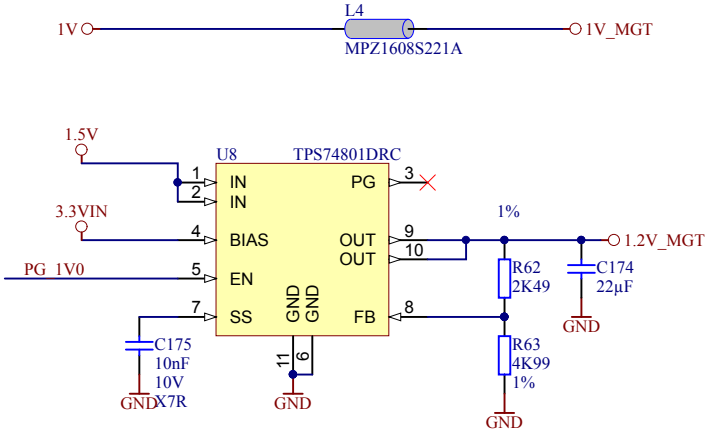




trenz electronic	Title: CPLD		
A4	Number: TE0712 200_2C3		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page13 of 16
Filename: CPLD.SchDoc			



Title: PWR			
A4	Number: TE0712 200_2C3		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page14 of 16
Filename: PWR1.SchDoc			



Title: PWR			
A4	Number: TE0712 200_2C3		Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH		Page 15 of 16
Filename: PWR2.SchDoc			

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

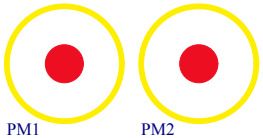
U_DDR3-RAM
DDR3-RAM.SchDoc

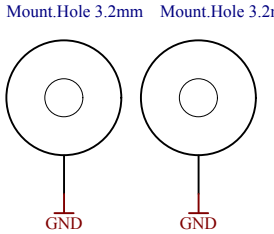
U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

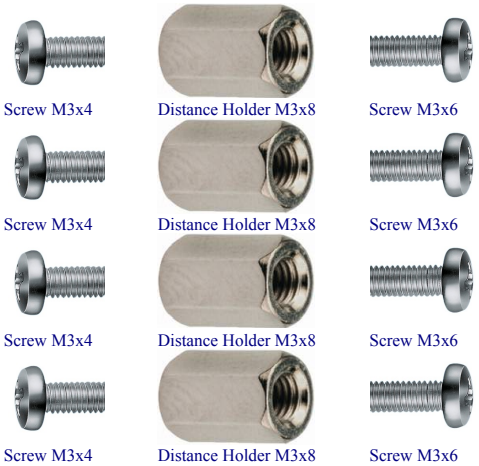
U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc





Top of Board



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Title: TE0712		
A4	Number: TE0712 200_2C3	Rev. 01
Date: 2014-06-23	Copyright: 2014 Trenz Electronic GmbH	Page16 of 16
Filename: TE0712.SchDoc		