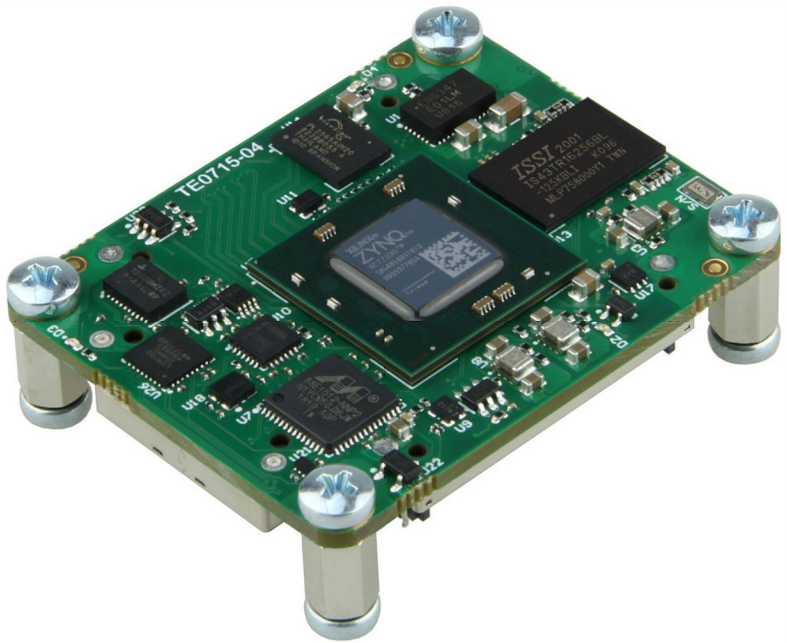
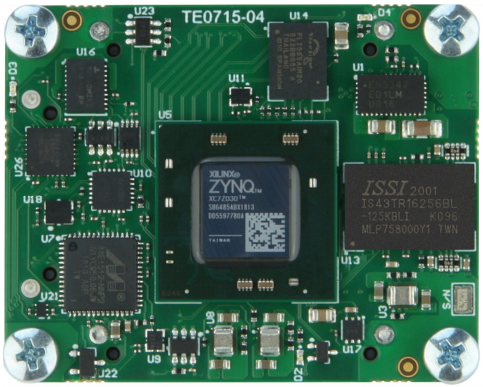
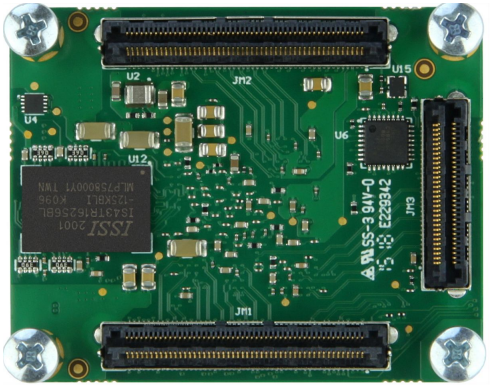






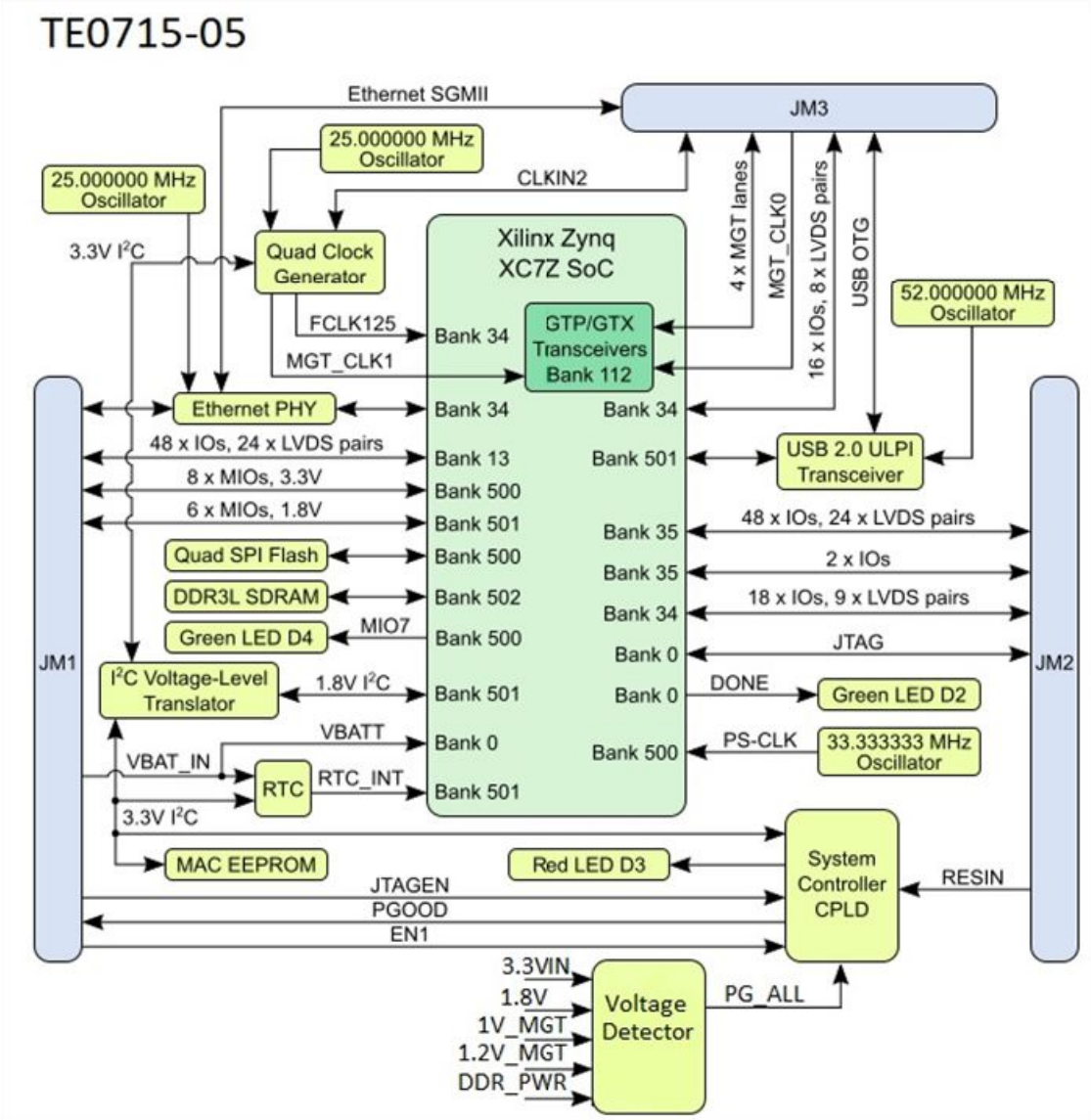
Regarding the usage of our schematics and alike documentation for Trenz module .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0715 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0715 - Legal Notices Modules		
	A4	Number: TE0715 71I33-A	Rev. 05
	Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

TE0715-05



trenz electronic	Title: TE0715 - System Overview		
	A4	Number: TE0715 71I33-A	Rev. 05
	Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 2 of 20
	Filename: Overview.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03		
-04		
-05	1. Revised power supply circuit: replaced obsolete parts U1, U2, U3,U8,U24, Q1 2. Added power supervisor BD39040MUF (U25). Signal PG_DDR_PWR renamed to PG_All (U25) and connected to system controller (U26.27) 3. Signal MIO8 (U5.E18) connected to system controller (U26.8) 4. Power supervisor U23 connected to 3.3VIN power rail (was 3.3V). Added protection diode D5 to U23.3 (#MR input) 5. Revised quantity of decoupling capacitors regarding Xilinx Spec (UG933, v1.13.1) 6. Auxiliary information has been added on Overview, Power_diagram, Legal_Notices pages 7. PCB: Revised layout of power supplies 8. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected 9. SCH & PCB: Full LIB update	VT

trenz electronic

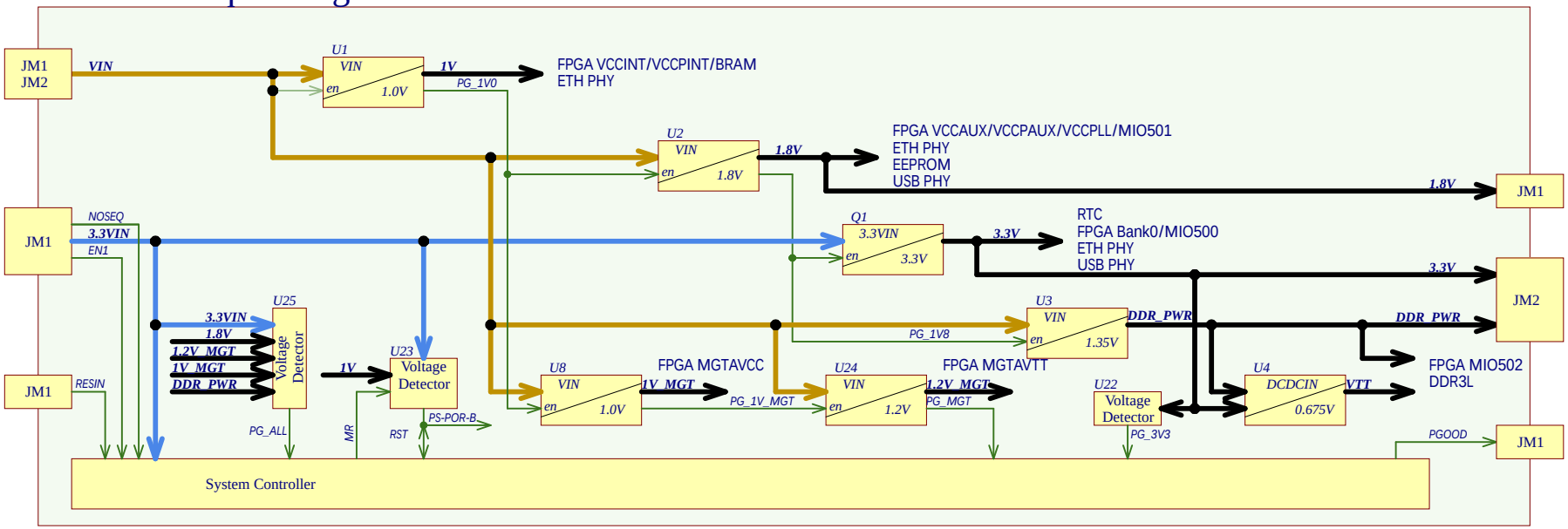
Title: TE0715 - Revision History

A4 | Number: TE0715 71I33-A | Rev. 05

Date: 2022-03-14 | Copyright: Trenz Electronic GmbH |

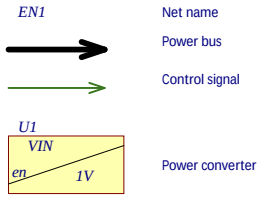
Filename: Revision Changes.SchDoc

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO34	IN	1.2 - 3.3V	+/-3%	HR IO Bank34	for XC7Z012/XC7Z015
VCCIO34	IN	1.2 - 1.8V	+/-3%	HP IO Bank34	for XC7Z030
VCCIO35	IN	1.2 - 3.3V	+/-3%	HR IO Bank35	for XC7Z012/XC7Z015
VCCIO35	IN	1.2 - 1.8V	+/-3%	HP IO Bank35	for XC7Z030
VBAT_IN	IN	3.0V	+/-3%	RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-
DDR_PWR	OUT	1.35V	+/-3%	Power for Carrier	-



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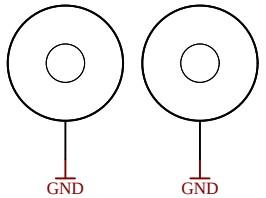
Title: TE0715 - Power Diagram			
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 4 of 20
Filename: Power_Diagram.SchDoc			

FPGA-MISC
FPGA-MISC.SchDoc
B13
B13.SchDoc
B34
B34.SchDoc
B35
B35.SchDoc
MIO-BANKS
MIO-BANKS.SchDoc
MGT
MGT.SchDoc
DDR-BANK
DDR-BANK.SchDoc

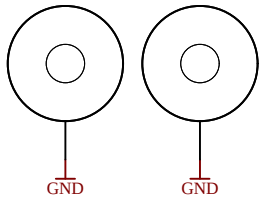
FPGA-POWER
FGPA-POWER.SchDoc
DDR3-RAM
DDR3-RAM.SchDoc
B2B_Connector
B2B_Connector.SchDoc
Clock
Clock.SchDoc
ETH-PHY
ETH-PHY.SchDoc
USB-PHY
USB-PHY.SchDoc
POWER
POWER.SchDoc
POWER_2
POWER_2.SchDoc

Special notes:

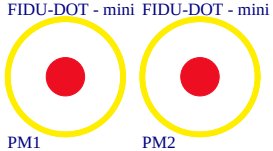
Mount.Hole 3.2mm
Mount.Hole 3.2mm



Mount.Hole 3.2mm
Mount.Hole 3.2mm

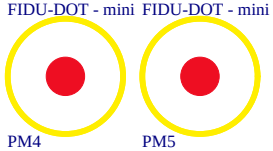


FIDU-DOT - mini
FIDU-DOT - mini



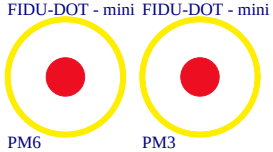
PM1
PM2

FIDU-DOT - mini
FIDU-DOT - mini



PM4
PM5

FIDU-DOT - mini
FIDU-DOT - mini



PM6
PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant:	71I33-A
Created by:	VT
Modified by:	VT
Modified at:	2022-02-21

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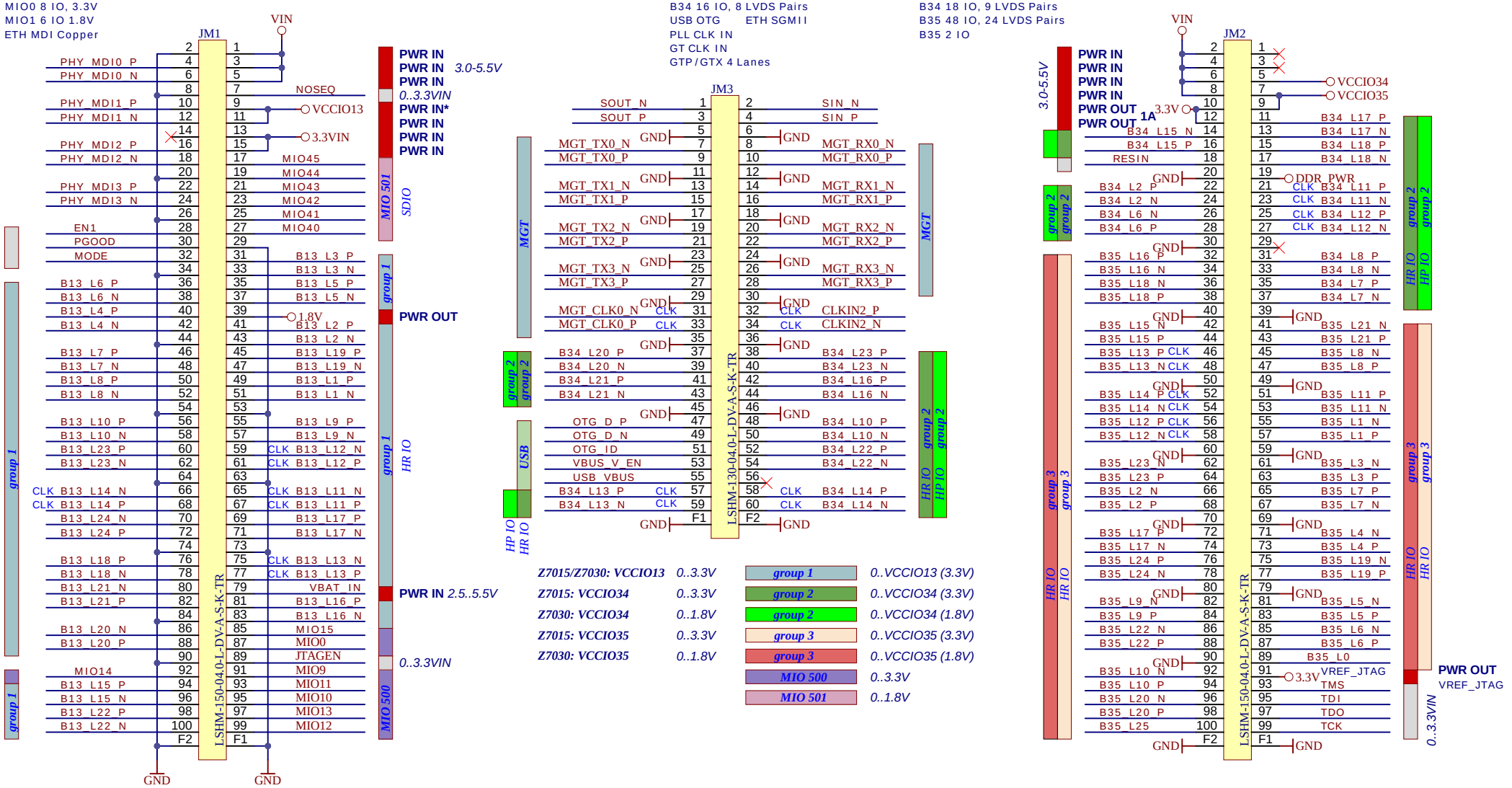
Title: TE0715 - Overview		
A4	Number: TE0715 71I33-A	Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 5 of 20
Filename: TE0715.SchDoc		

B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

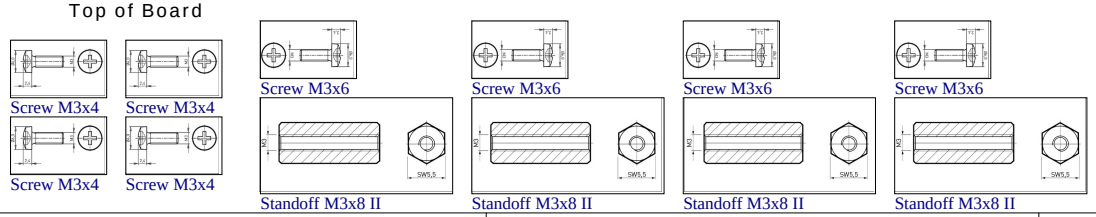
B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO



Z7015/Z7030: VCCIO13	0..3.3V	group 1	0..VCCIO13 (3.3V)
Z7015: VCCIO34	0..3.3V	group 2	0..VCCIO34 (3.3V)
Z7030: VCCIO34	0..1.8V	group 2	0..VCCIO34 (1.8V)
Z7015: VCCIO35	0..3.3V	group 3	0..VCCIO35 (3.3V)
Z7030: VCCIO35	0..1.8V	group 3	0..VCCIO35 (1.8V)
		MIO 500	0..3.3V
		MIO 501	0..1.8V

Top of Board



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Title: TE0715 - B2B_Connectors			
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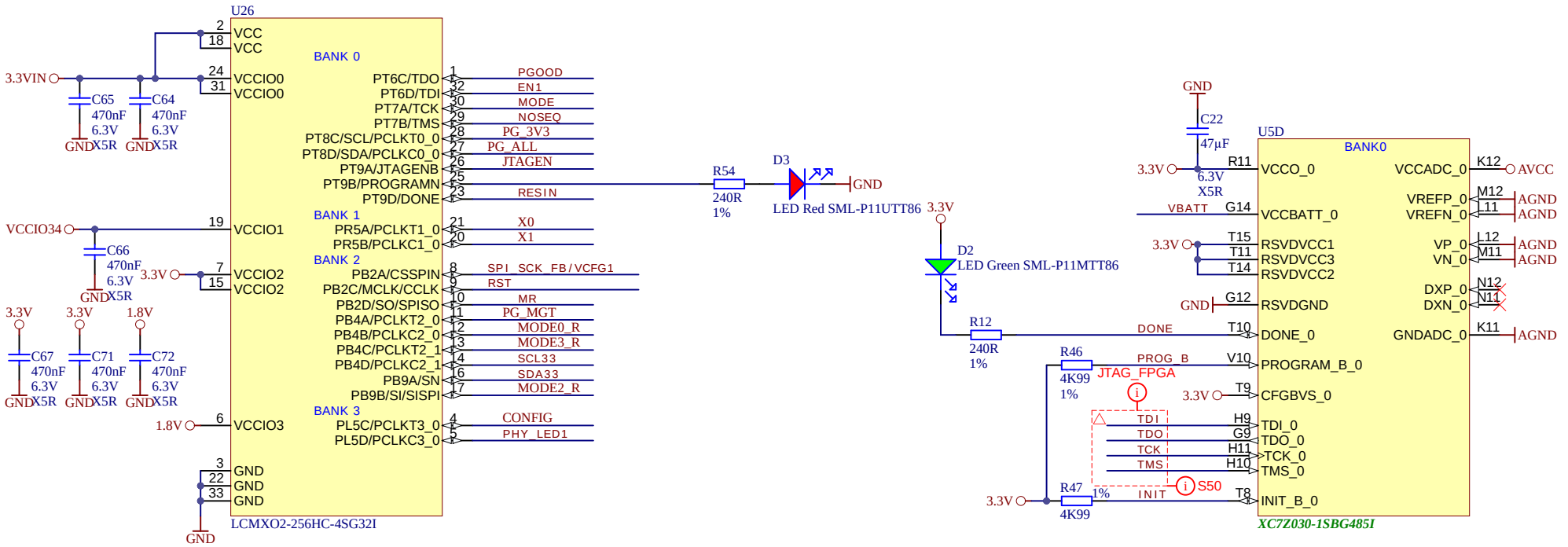
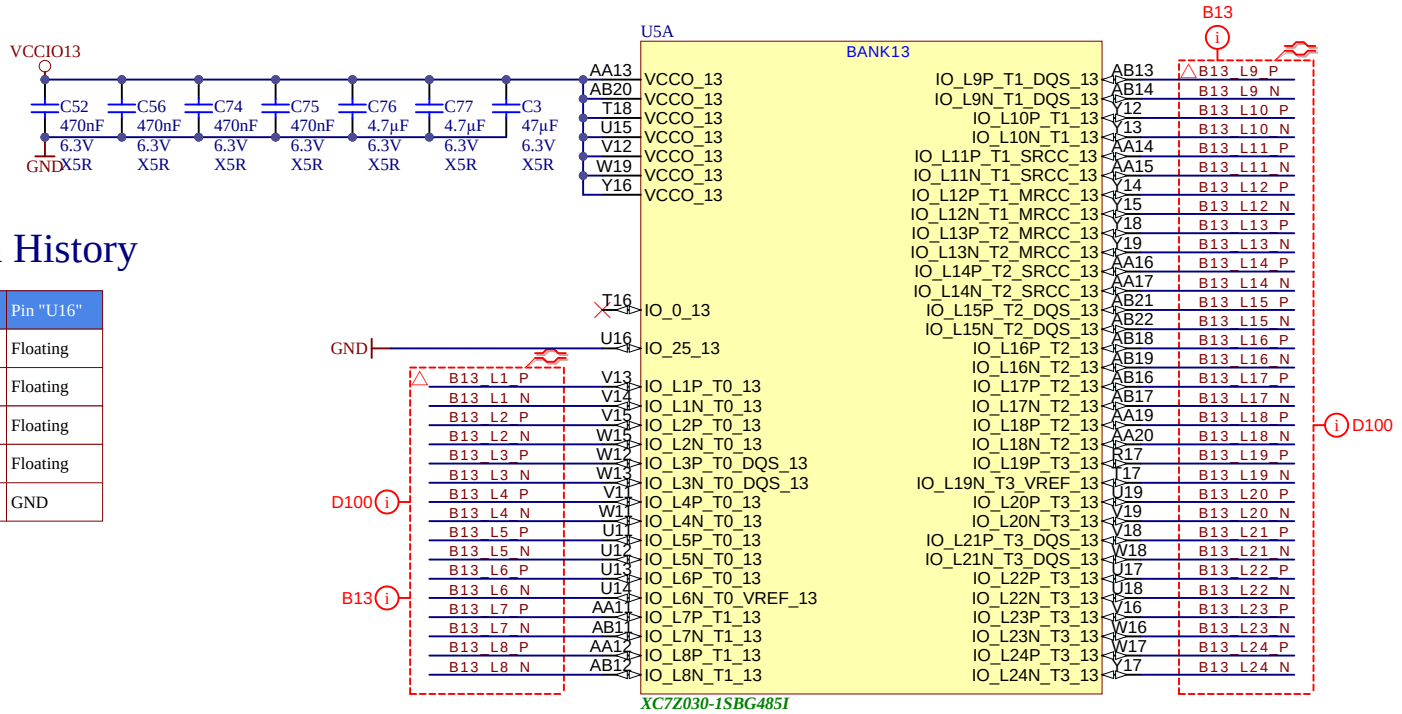
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 6 of 20
Filename: B2B_Connector.SchDoc			



Title: TE0715 - Config-MISC			
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 7 of 20
Filename: FPGA-MISC.SchDoc			



HW Revision History

Revision	Pin "T16"	Pin "U16"
REV01	Floating	Floating
REV02	Floating	Floating
REV03	Floating	Floating
REV04	GND	Floating
REV05	Floating	GND

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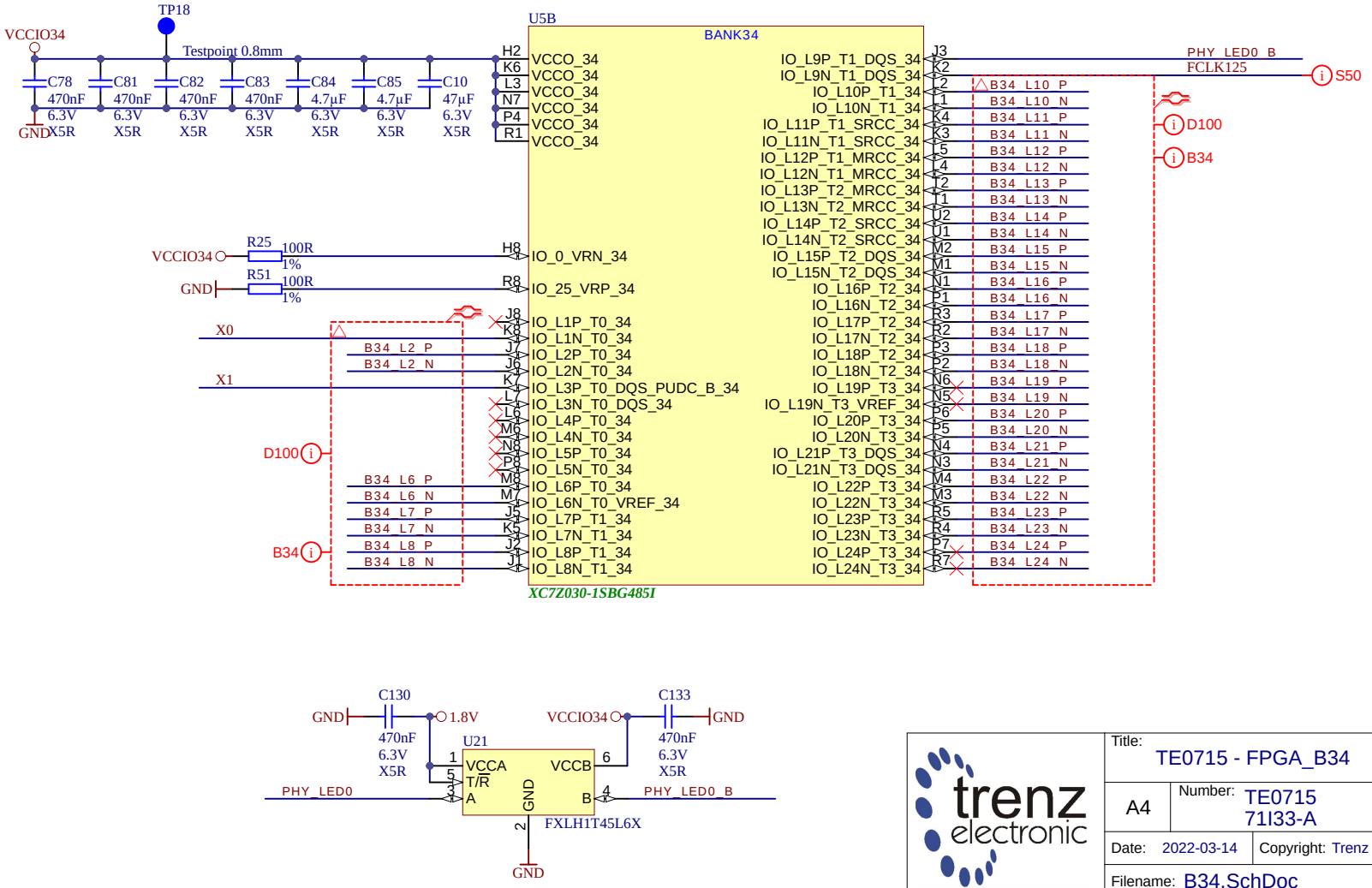
Title: TE0715 - FPGA_B12		
A4	Number: TE0715 71I33-A	Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 8 of 20
Filename: B13.SchDoc		



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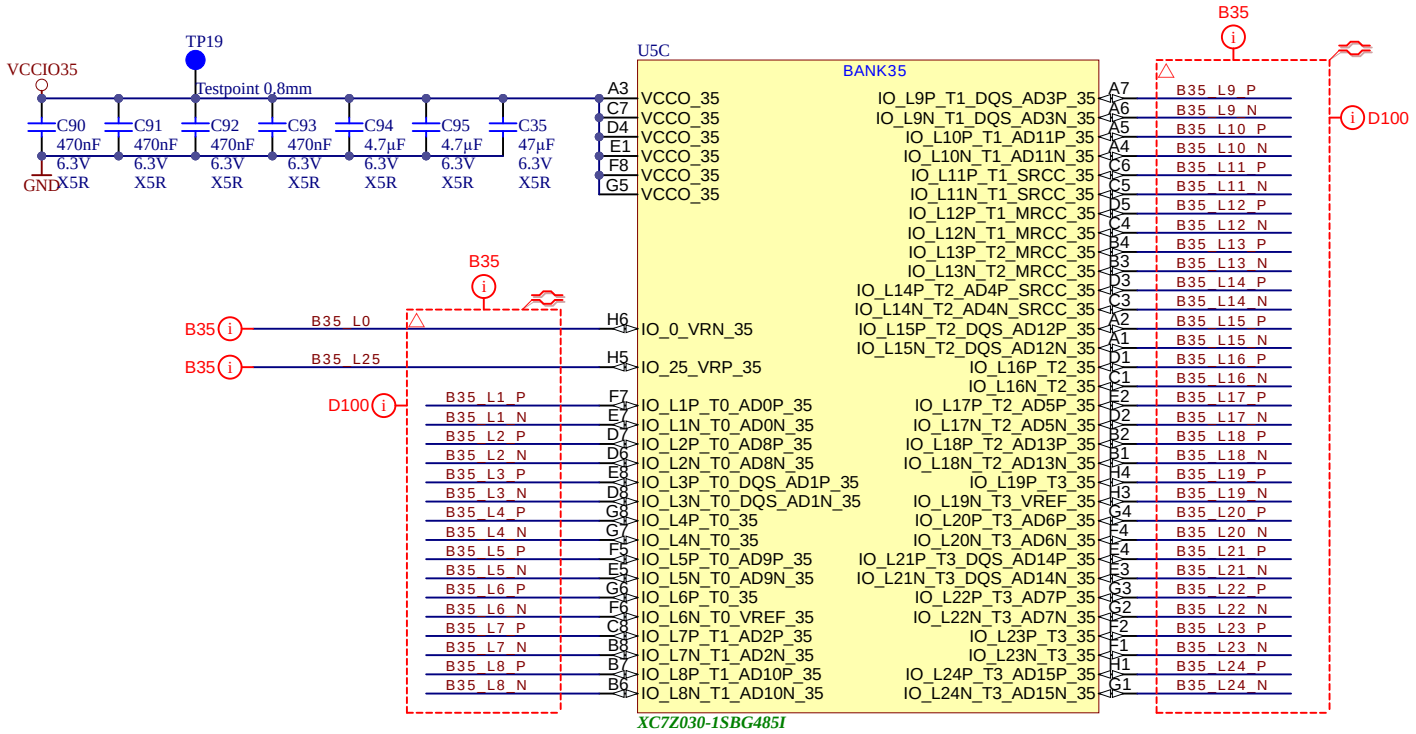
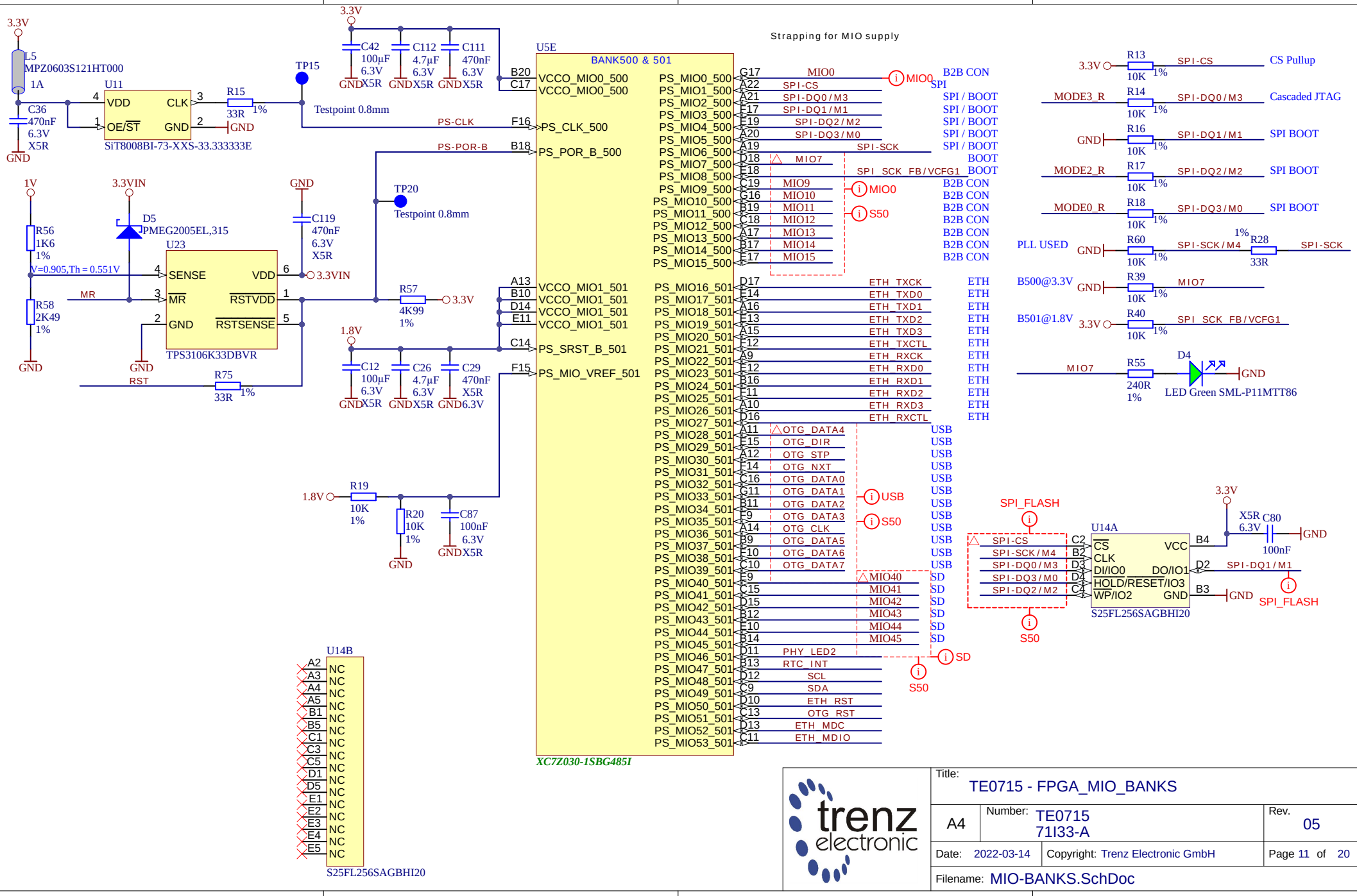
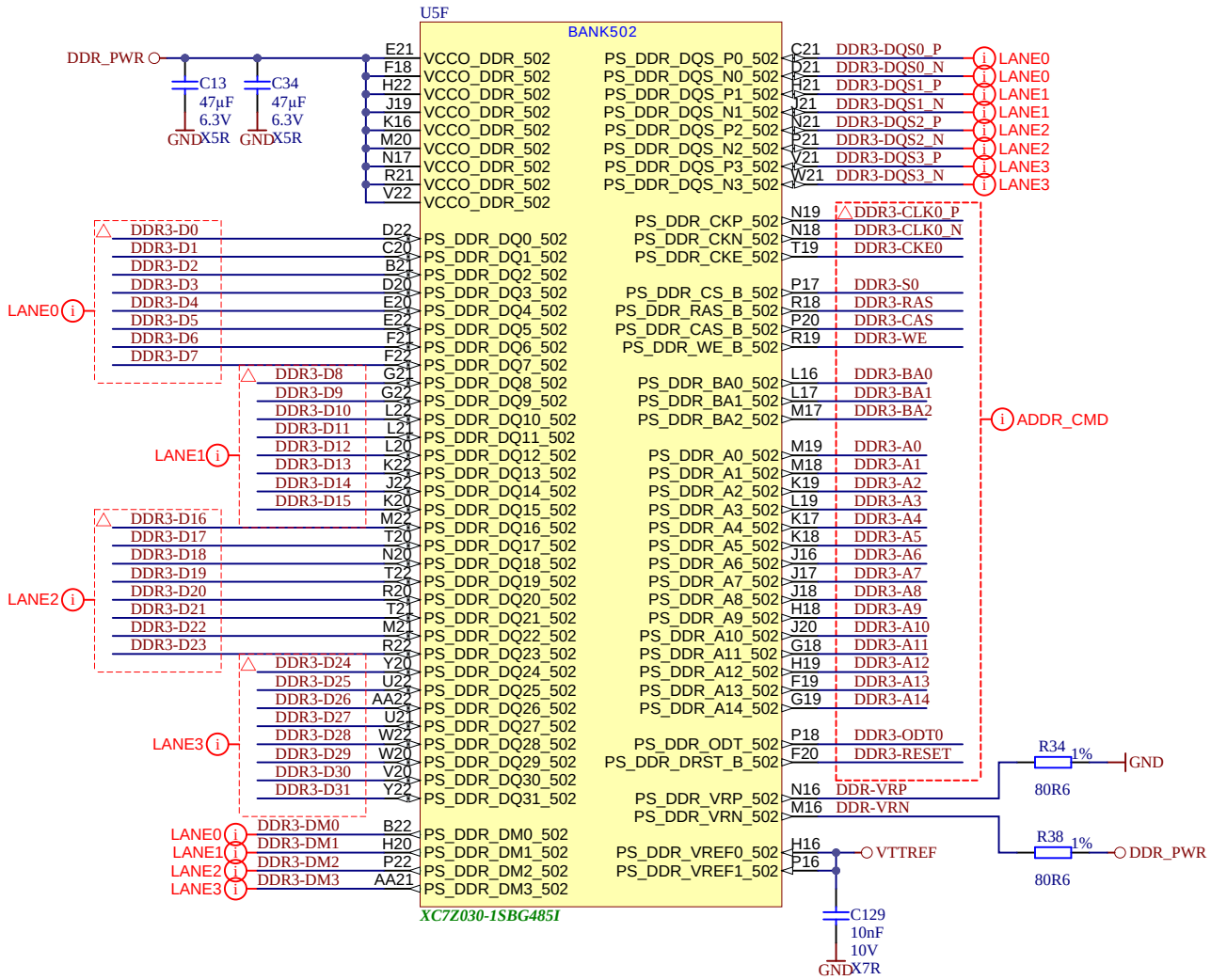
Title: TE0715 - FPGA_B34			
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 9 of 20
Filename: B34.SchDoc			



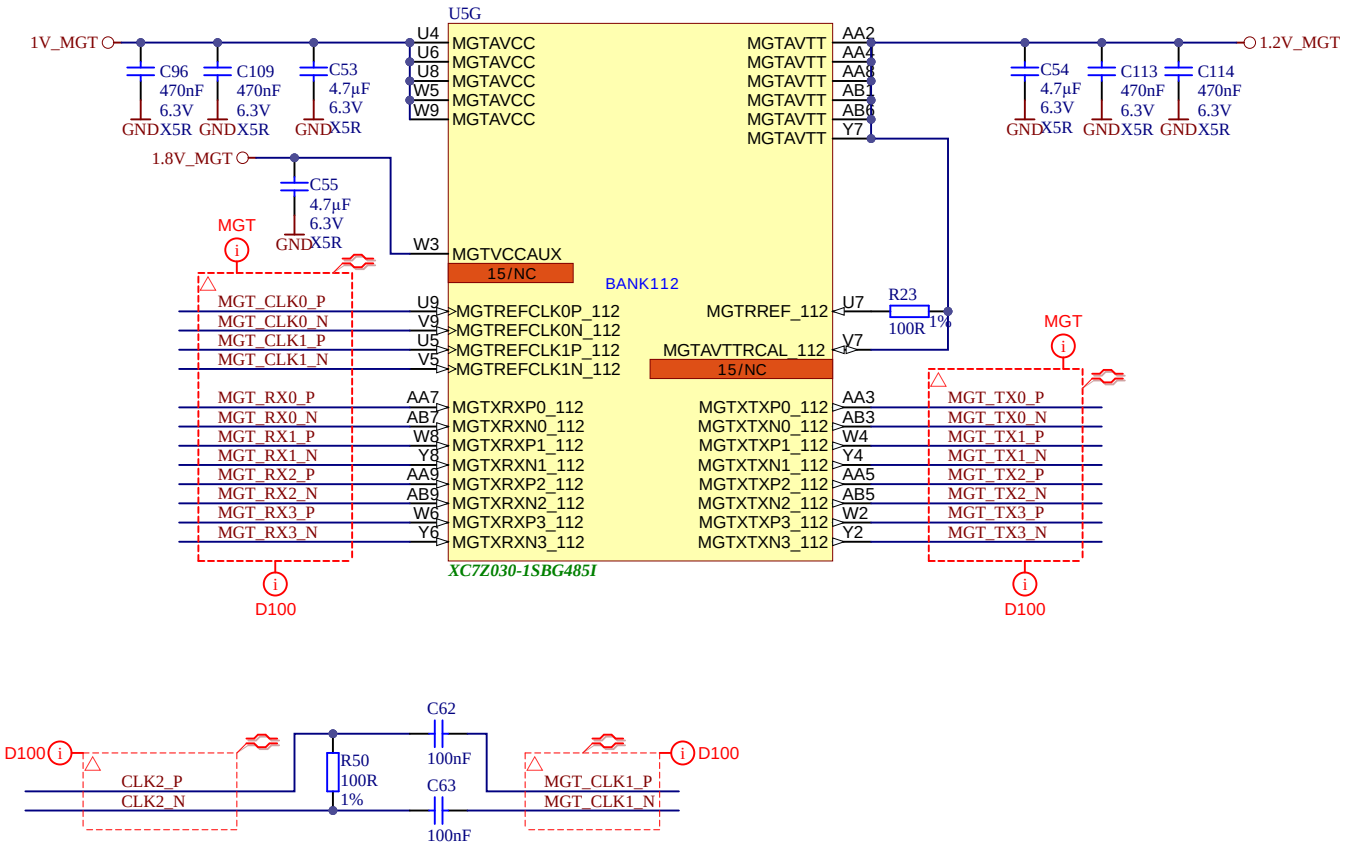
trenz electronic	Title: TE0715 - FPGA_B35		
	A4	Number: TE0715 71I33-A	Rev. 05
	Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 10 of 20
	Filename: B35.SchDoc		



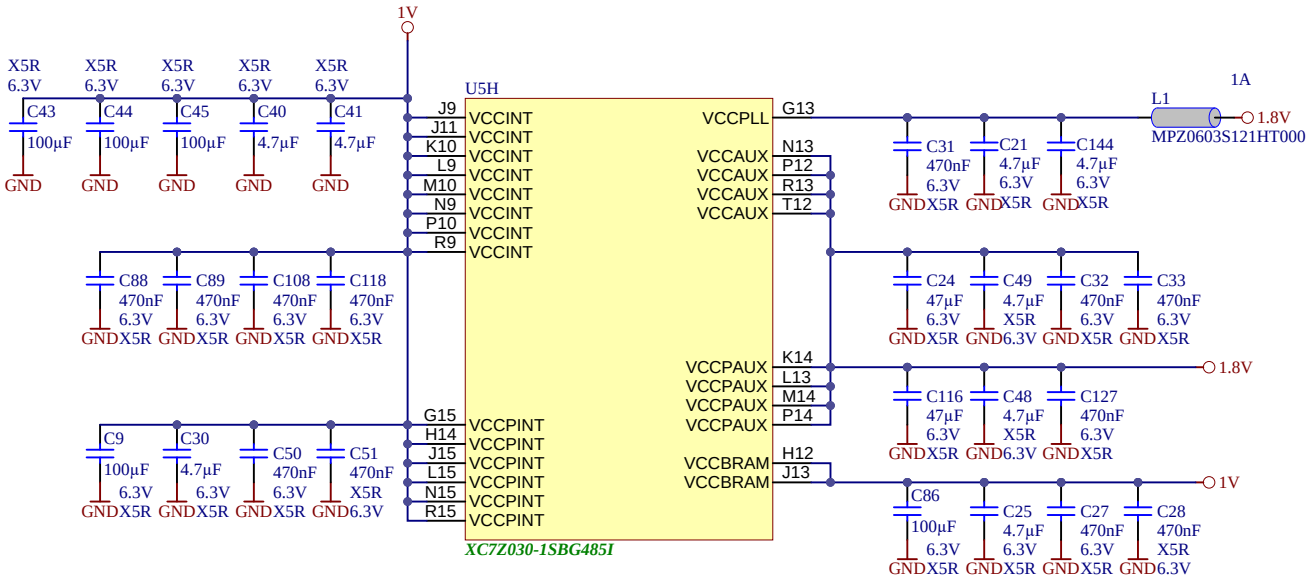
Title: TE0715 - FPGA_MIO_BANKS		
A4	Number: TE0715 71I33-A	Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 11 of 20
Filename: MIO-BANKS.SchDoc		

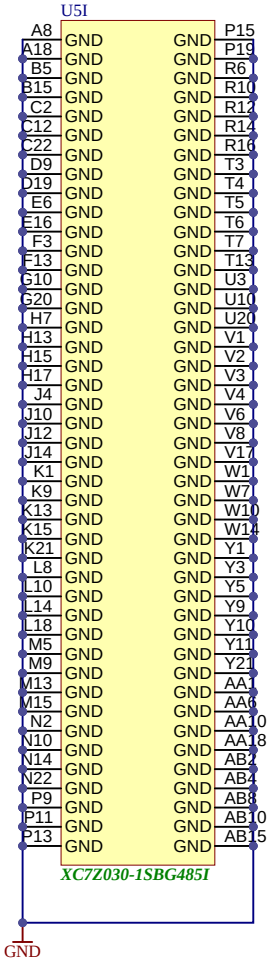


trenz electronic	Title: TE0715 - FPGA_PS-DDR		
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 12 of 20
Filename: DDR-BANK.SchDoc			

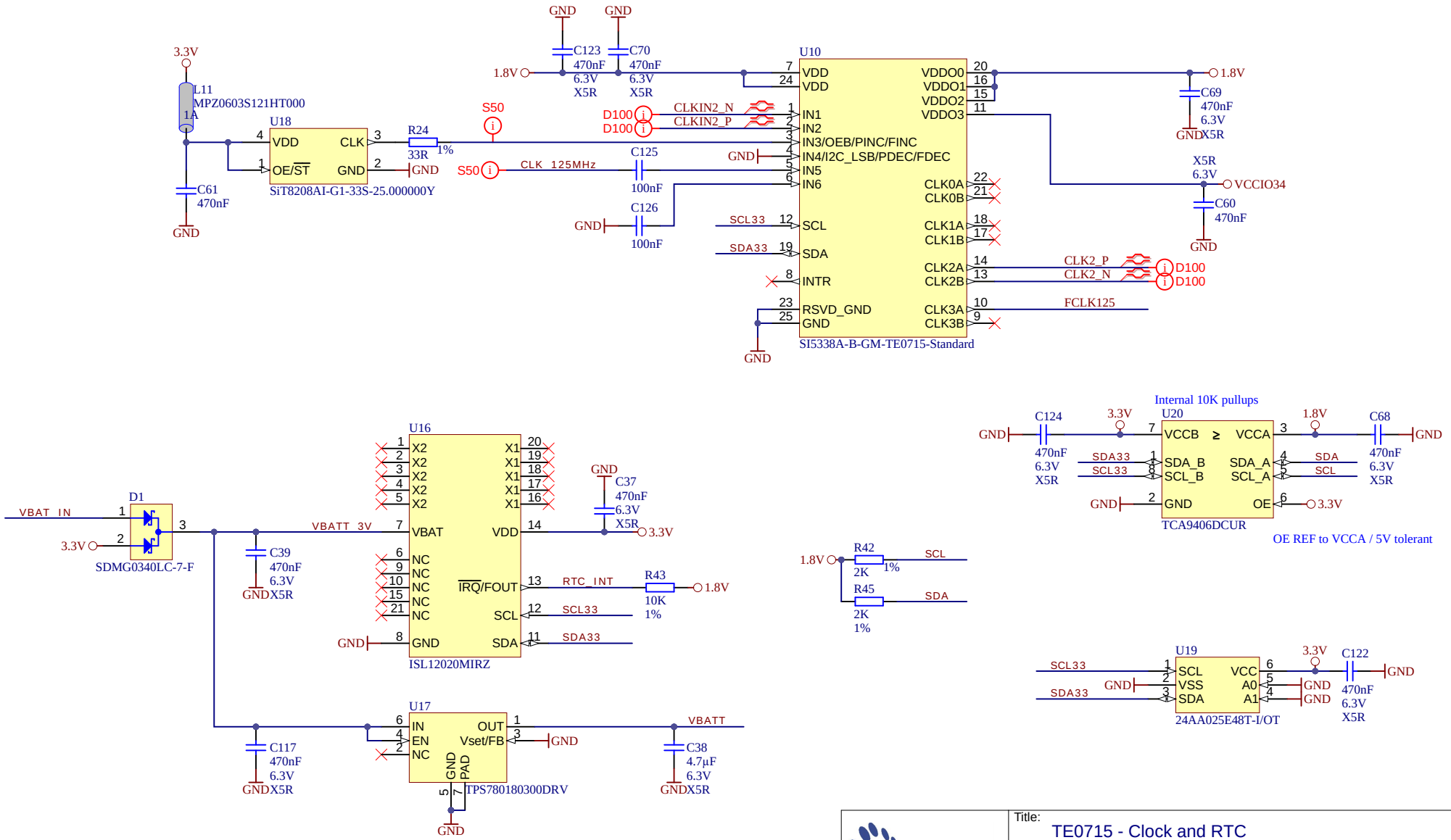


Title: TE0715 - FPGA_MGT			
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 13 of 20
Filename: MGT.SchDoc			





trenz electronic	Title: TE0715 - FPGA_Power		
A4	Number: TE0715 71I33-A		Rev. 05
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 14 of 20
Filename: FGPA-POWER.SchDoc			



Title: TE0715 - Clock and RTC			
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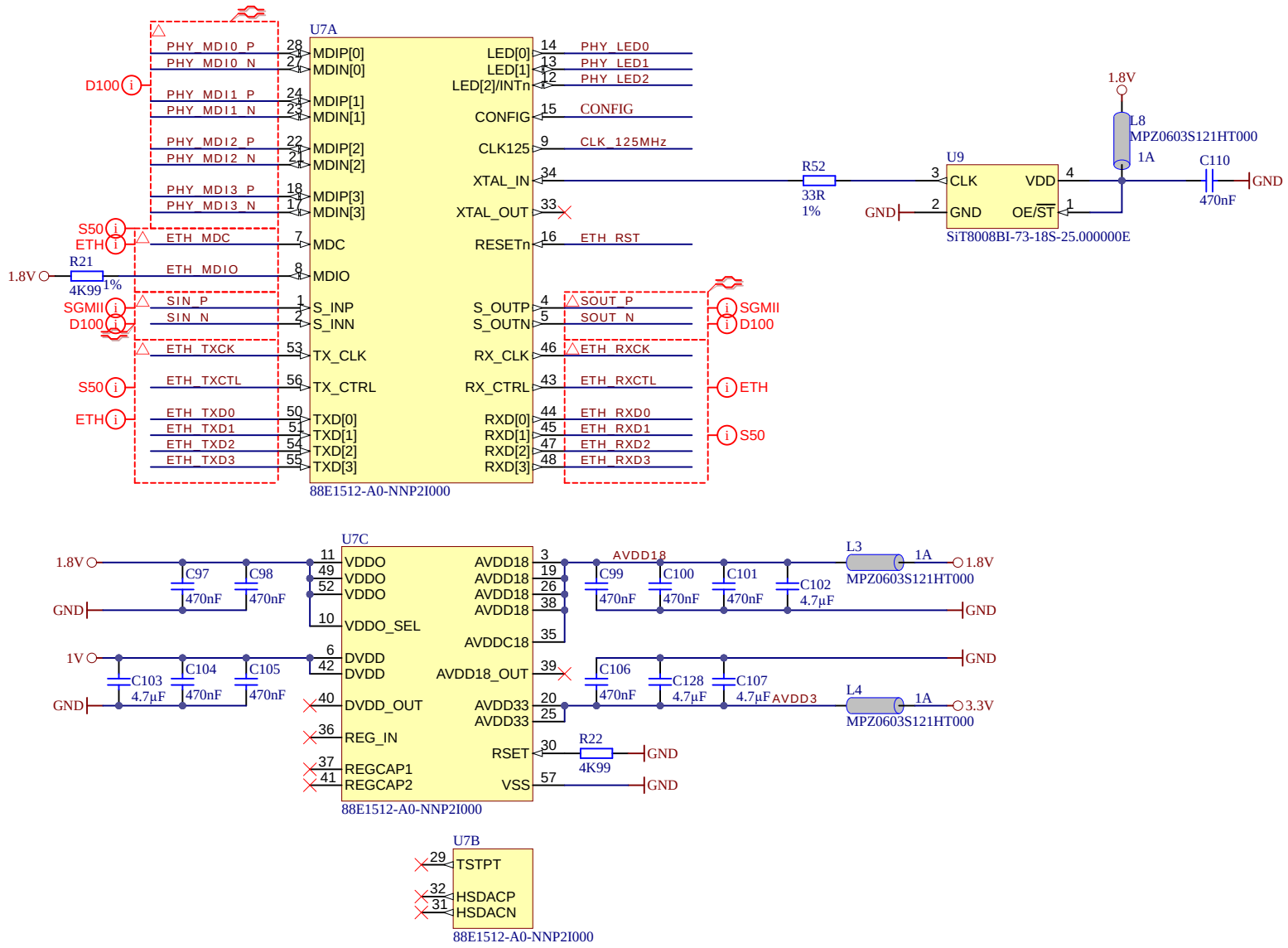
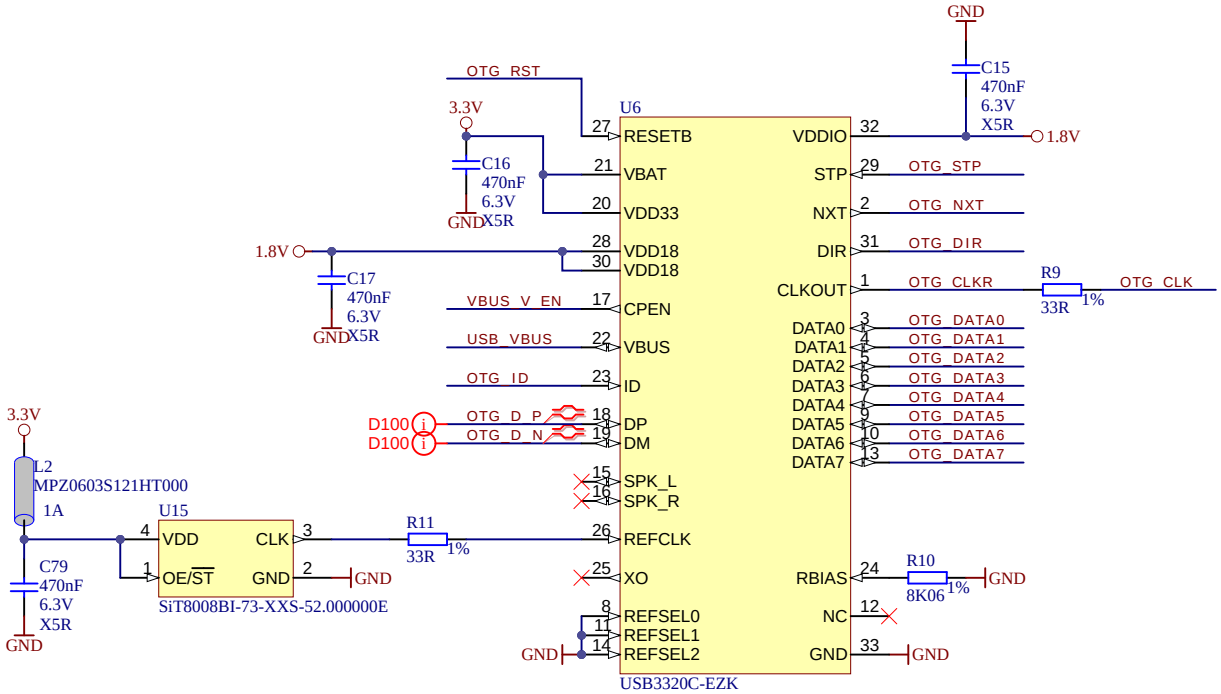
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 15 of 20
Filename: Clock.SchDoc			



trenz electronic	Title: TE0715 - ETH_PHY		
	A4	Number: TE0715 71I33-A	Rev. 05
	Date: 2022-03-14	Copyright: Trenz Electronic GmbH	Page 16 of 20
	Filename: ETH-PHY.SchDoc		



trenz electronic	Title: TE0715 - USB_PHY		
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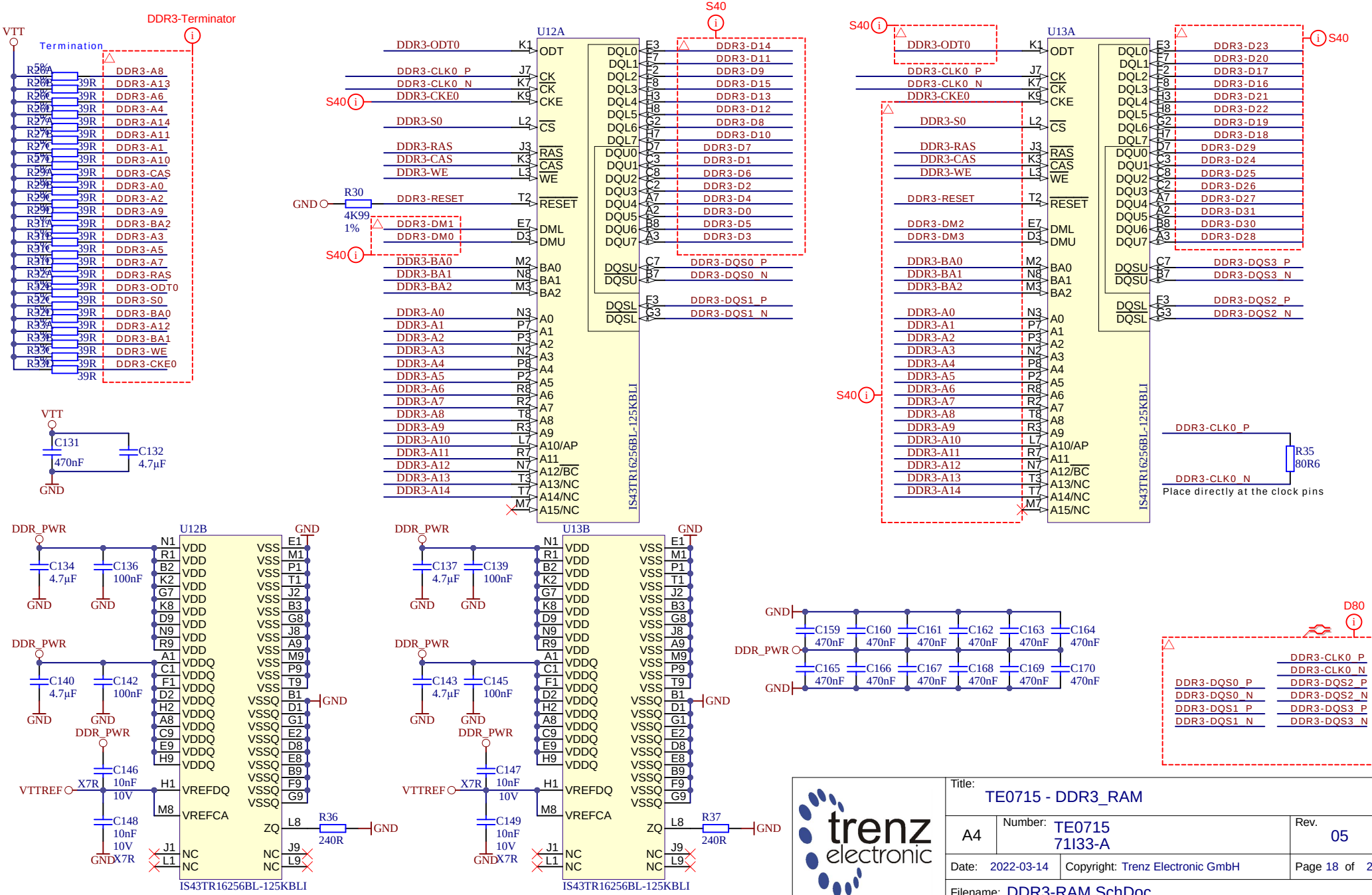
Date: 2022-03-14	Copyright: Trenz Electronic GmbH		Page 17 of 20
Filename: USB-PHY.SchDoc			


DDR3-Terminator
Termination
VTT
DDR3-A8
DDR3-A13
DDR3-A6
DDR3-A4
DDR3-A14
DDR3-A11
DDR3-A1
DDR3-A10
DDR3-CAS
DDR3-A0
DDR3-A2
DDR3-A9
DDR3-BA2
DDR3-A3
DDR3-A5
DDR3-A7
DDR3-RAS
DDR3-ODT0
DDR3-S0
DDR3-BA0
DDR3-A12
DDR3-BA1
DDR3-WE
DDR3-CKE0
39R
C131
470nF
C132
4.7µF
GND
U12A
S40
DDR3-ODT0
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-CKE0
DDR3-S0
DDR3-RAS
DDR3-CAS
DDR3-WE
R30
4K99
1%
DDR3-RESET
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DDR3-DM0
DDR3-BA0
DDR3-BA1
DDR3-BA2
DDR3-A0
DDR3-A1
DDR3-A2
DDR3-A3
DDR3-A4
DDR3-A5
DDR3-A6
DDR3-A7
DDR3-A8
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DDR3-A11
DDR3-A12
DDR3-A13
DDR3-A14
ODT
CK
CKE
CS
RAS
CAS
WE
RESET
DML
DMU
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13/NC
A14/NC
A15/NC
DQL0
DQL1
DQL2
DQL3
DQL4
DQL5
DQL6
DQL7
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7
DQSU
DQSU
DQSL
DQSL
DDR3-D14
DDR3-D11
DDR3-D9
DDR3-D15
DDR3-D13
DDR3-D12
DDR3-D8
DDR3-D10
DDR3-D7
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DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
IS43TR16256BL-125KBLI
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DDR3-D23
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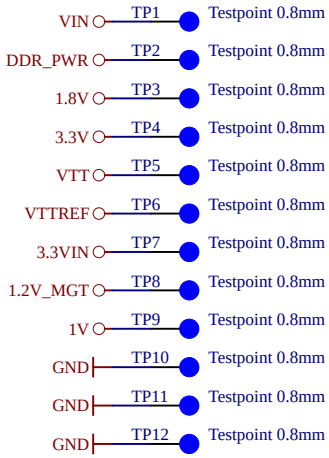
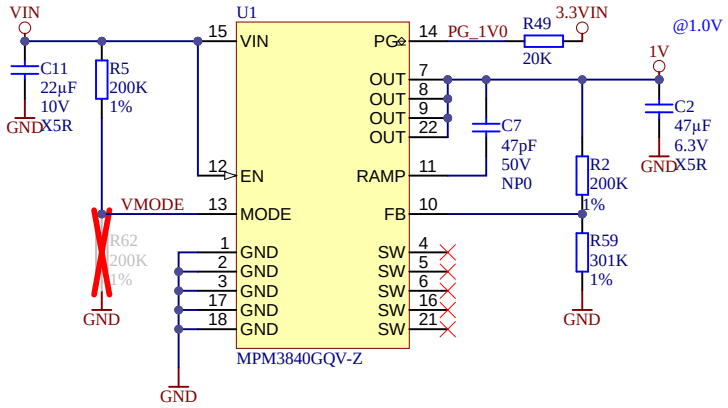
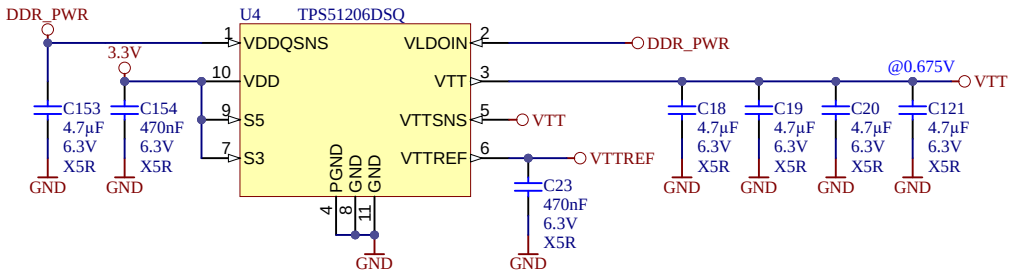
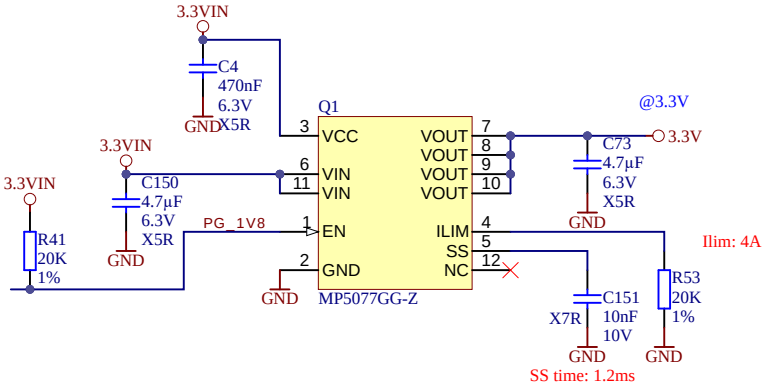
DDR3-D22
DDR3-D19
DDR3-D18
DDR3-D29
DDR3-D24
DDR3-D25
DDR3-D26
DDR3-D27
DDR3-D31
DDR3-D30
DDR3-D28
DDR3-DQS3_P
DDR3-DQS3_N
DDR3-DQS2_P
DDR3-DQS2_N
R35
80R6
Place directly at the clock pins
U12B
U13B
DDR_PWR
C134
4.7µF
C136
100nF
C140
4.7µF
C142
100nF
C146
10nF
10V
X7R
C148
10nF
10V
X7R
VTTREF
VDD
VDDQ
VREFDQ
VREFCA
VSS
VSSQ
ZQ
NC
R36
240R
C137
4.7µF
C139
100nF
C143
4.7µF
C145
100nF
C147
10nF
10V
X7R
C149
10nF
10V
X7R
R37
240R
C159
C160
C161
C162
C163
C164
C165
C166
C167
C168
C169
C170
470nF
D80
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
trenz electronic
Title: TE0715 - DDR3_RAM
A4
Number: TE0715 71I33-A
Rev. 05
Date: 2022-03-14
Copyright: Trenz Electronic GmbH
Page 18 of 20
Filename: DDR3-RAM.SchDoc









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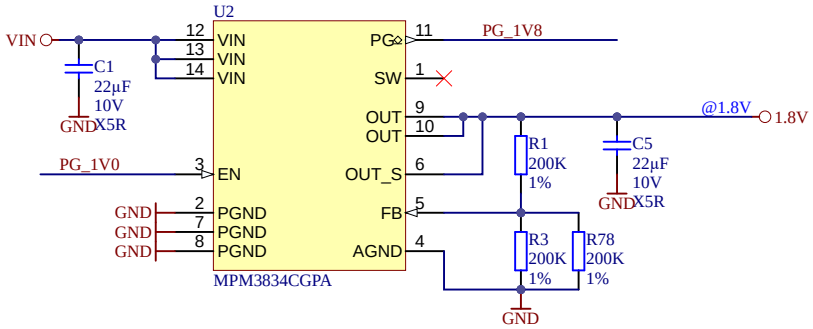

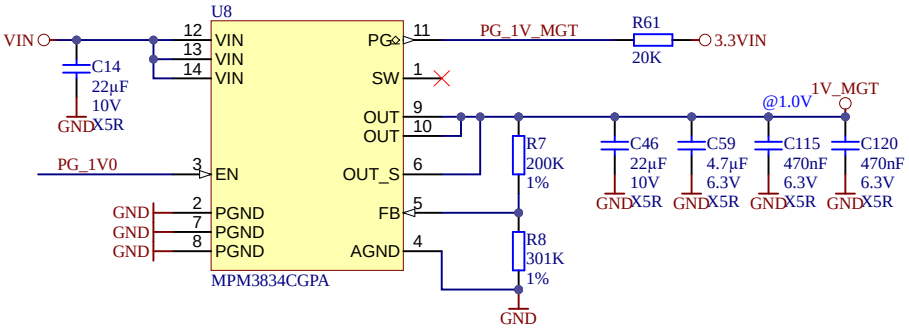

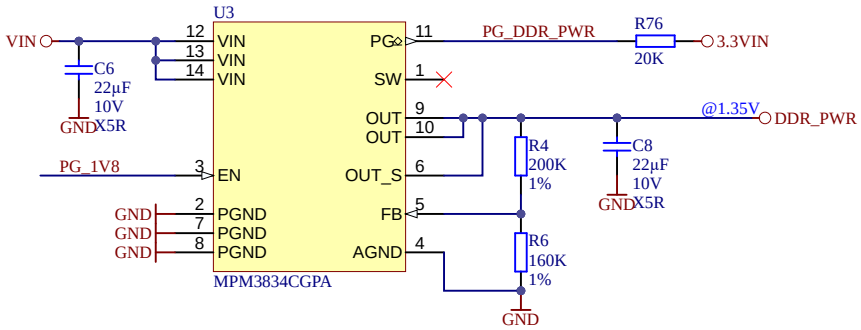

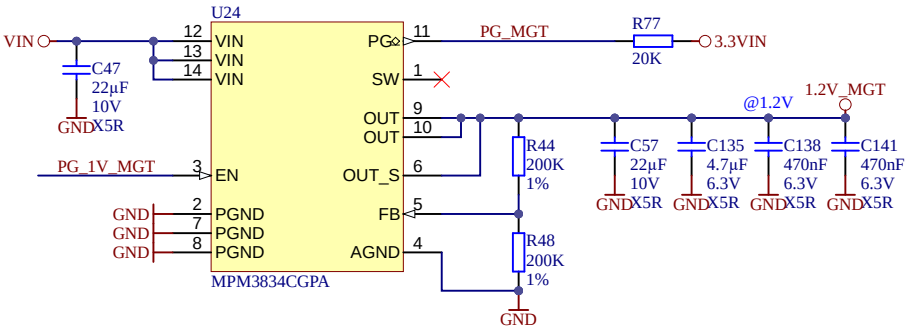

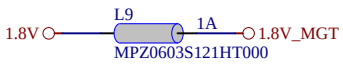

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