



TE0715 Test Board

Revision: v.31

Date: 09.05.2019 07:48

Table of Contents

Overview	5
Key Features	5
Revision History	5
Release Notes and Know Issues	6
Requirements	6
Software	6
Hardware	6
Content	7
Design Sources	7
Additional Sources	7
Prebuilt	7
Download	8
Design Flow	9
Launch	11
Programming	11
QSPI	11
SD	11
JTAG	11
Usage	11
Linux	12
Vivado HW Manager	12
System Design - Vivado	13
Block Design	13
PS Interfaces	13
Constrains	14
Basic module constrains	14
Design specific constrain	14
Software Design - SDK/HSI	15
Application	15
zynq_fsbl	15
zynq_fsbl_flash	15
U-Boot	15
Software Design - PetaLinux	16
Config	16
U-Boot	16
Device Tree	17
Kernel	18
Rootfs	18
Applications	18
startup	18
Additional Software	19
SI5338	19

Appx. A: Change History and Legal Notices	20
Document Change History	20
Legal Notices	20
Data privacy	20
Document Warranty	21
Limitation of Liability	21
Copyright Notice	21
Technology Licenses	21
Environmental Protection	21
REACH, RoHS and WEEE	22

Online version of this manual and other related documents can be found at <https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation>

Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager.

Key Features

- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- SI5338 Initialisation with FSBL (optional)
- Special FSBL for QSPI Programming

Revision History

Date	Vivado	Project Built	Authors	Description
2018-04-26	2017.4	TE0715-test_board-vivado_2017.4-build_07_20180426171530.zip TE0715-test_board_noprebuilt-vivado_2017.4-build_07_20180426171546.zip	John Hartfiel	<ul style="list-style-type: none"> • new assembly variant
2018-03-27	2017.4	te0715-test_board-vivado_2017.4-build_07_20180327223552.zip te0715-test_board_noprebuilt-vivado_2017.4-build_07_20180327223606.zip	John Hartfiel	<ul style="list-style-type: none"> • Board Part Bug fix with UART 1
2018-01-05	2017.4	te0715-test_board-vivado_2017.4-build_01_20180105195436.zip te0715-test_board_noprebuilt-vivado_2017.4-build_01_20180105195452.zip	John Hartfiel	<ul style="list-style-type: none"> • No Design changes • Add FSBL for Flash Programming
2017-11-10	2017.2	te0715-test_board-vivado_2017.2-build_05_20171110134232.zip te0715-test_board_noprebuilt-vivado_2017.2-build_05_20171110134247.zip	John Hartfiel	<ul style="list-style-type: none"> • New Web Link on Board Part Files • Add optional FSBL Code to reprogram SI5338
2017-10-19	2017.2	te0715-test_board-vivado_2017.2-build_04_20171019141808.zip te0715-test_board_noprebuilt-vivado_2017.2-build_04_20171019141825.zip	John Hartfiel	<ul style="list-style-type: none"> • changed Flash typ on TE0715_board_files.csv (older one is not supported on Vivado 2017.2)
2017-09-22	2017.2	te0715-test_board-vivado_2017.2-build_02_20170927143412.zip te0715-test_board_noprebuilt-vivado_2017.2-build_02_20170927143427.zip	John Hartfiel	<ul style="list-style-type: none"> • initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Timing problems with Frequency counter	can be ignored	---	---

Requirements

Software

Software	Version	Note
Vivado	2017.4	needed
SDK	2017.4	needed
PetaLinux	2017.4	needed

Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0715-03-15-1C	03_15_1c	REV01,02,03	1GB	32		
TE0715-03-15-1I	03_15_1i	REV01,02,03	1GB	32		
TE0715-03-15-2I	03_15_2i	REV01,02,03	1GB	32		
TE0715-03-30-1C	03_30_1c	REV01,02,03	1GB	32		
TE0715-03-30-1I	03_30_1i	REV01,02,03	1GB	32		
TE0715-03-30-3E	03_30_3e	REV01,02,03	1GB	32		
TE0715-04-15-1C	04_15_1c	REV04	1GB_L	32		
TE0715-04-15-1I	04_15_1i	REV04	1GB_L	32		
TE0715-04-15-2I	04_15_2i	REV04	1GB_L	32		
TE0715-04-30-1C	04_30_1c	REV04	1GB_L	32		
TE0715-04-30-1I	04_30_1i	REV04	1GB_L	32		
TE0715-04-30-3E	04_30_3e	REV04	1GB_L	32		
TE0715-04-12s-1C	12s	REV04	1GB_L	32		
TE0715-04-30-1IA	04_30_1i	REV04	1GB_L	32		Micron instead of Spansion Flash

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703	used as reference carrier
TE0705	
TE0706	
TEBA0841	

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Content

For general structure and of the reference design, see [Project Delivery](#)

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Additional Sources

Type	Location	Notes
SI5338 Project	<design_name>/misc/si5338	---

Prebuilt

Only on ZIP file with Prebuilt content.

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File

File	File-Extension	Description
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0715 "Test Board" Reference Design](#)

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

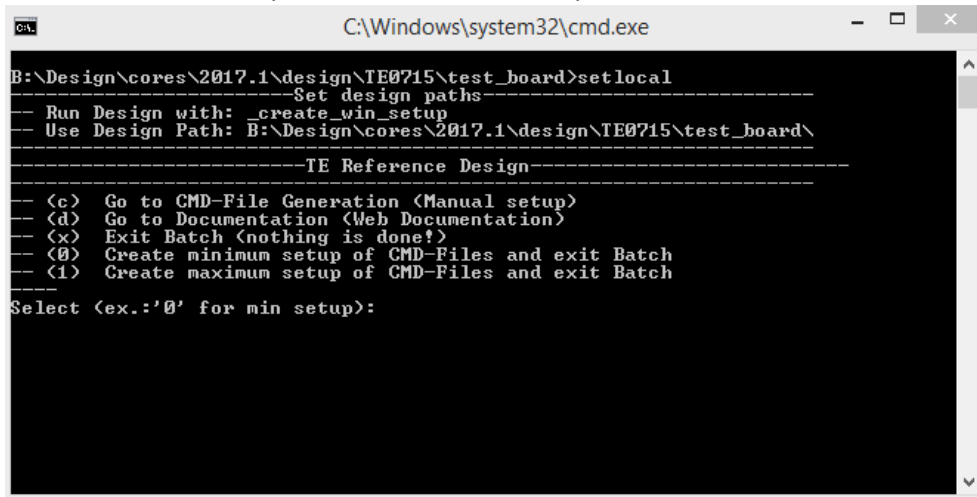
See also:

- [Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects](#)
- [Project Delivery](#).

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



```

C:\Windows\system32\cmd.exe

B:\Design\cores\2017.1\design\TE0715\test_board>setlocal
-----Set design paths-----
Run Design with: _create_win_setup
Use Design Path: B:\Design\cores\2017.1\design\TE0715\test_board\
-----TE Reference Design-----
(c) Go to CMD-File Generation (Manual setup)
(d) Go to Documentation (Web Documentation)
(x) Exit Batch (nothing is done!)
(0) Create minimum setup of CMD-Files and exit Batch
(1) Create maximum setup of CMD-Files and exit Batch
Select (ex.:\'0\' for min setup):
  
```

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
 - a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guiemode.cmd"

Note: Select correct one, see [TE Board Part Files](#)

5. Create HDF and export to prebuilt folder
 - a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`
Note: Script generate design and export files into `\prebuilt\hardware\<short dir>`. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported HDF
 - a. HDF is exported to `"prebuilt\hardware\<short name>"`
Note: HW Export from Vivado GUI create another path as default workspace.
 - b. Create Linux images on VM, see [PetaLinux KICKstart](#)
 - i. Use TE Template from `/os/petalinux`
Note: run `init_config.sh` before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
 - a. `"prebuilt\os\petalinux\default"` or `"prebuilt\os\petalinux\<short name>"`
Notes: Scripts select `"prebuilt\os\petalinux\<short name>"`, if exist, otherwise `"prebuilt\os\petalinux\default"`
8. Generate Programming Files with HSI/SDK
 - a. Run on Vivado TCL: `TE::sw_run_hsi`
Note: Scripts generate applications and bootable files, which are defined in `"sw_lib\apps_list.csv"`
 - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_sdk`
Note: See [SDK Projects](#)

Launch



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first lunch.

TE0715-0x-30-xx only: HP IO Banks max power supply voltage is 1.8V.

Programming

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
Note: To program with SDK/Vivado GUI, use special FSBL (zynq_fsbl_flash) on setup
4. Copy image.ub on SD-Card
5. Insert SD-Card

SD

1. Copy image.ub and Boot.bin on SD-Card.
 - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
 - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
Note: See TRM of the Carrier, which is used.

4. Power On PCB

Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

Linux

1. Open Serial Console (e.g. putty)

- Speed: 115200
- COM Port: Win OS, see device manager, Linux OS see dmesg | grep tty (UART is *USB1)

2. Linux Console:

Note: Wait until Linux boot finished For Linux Login use:

- User Name: root
- Password: root

3. You can use Linux shell now.

- I2C 1 Bus type: i2cdetect -y -r 1
- RTC check: dmesg | grep rtc
- ETH0 works with udhcpc

Vivado HW Manager

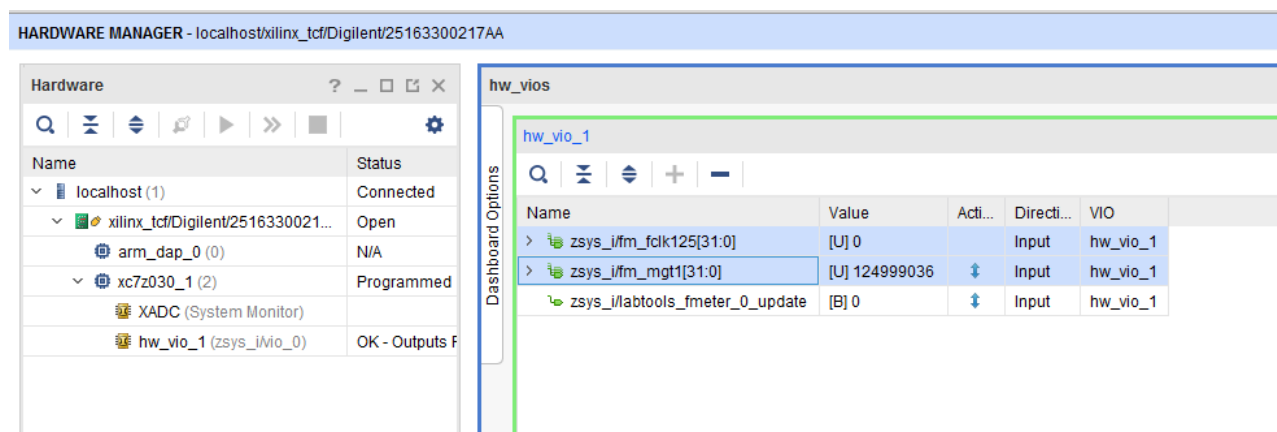
MGT Reference CLK Counter:

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- Set radix from VIO signals to unsigned integer.

Note: Frequency Counter is inaccurate and displayed unit is Hz

MGT CLK is configured to 125MHz by default, FCLK is not configured by default (optional possible see FSBL description).



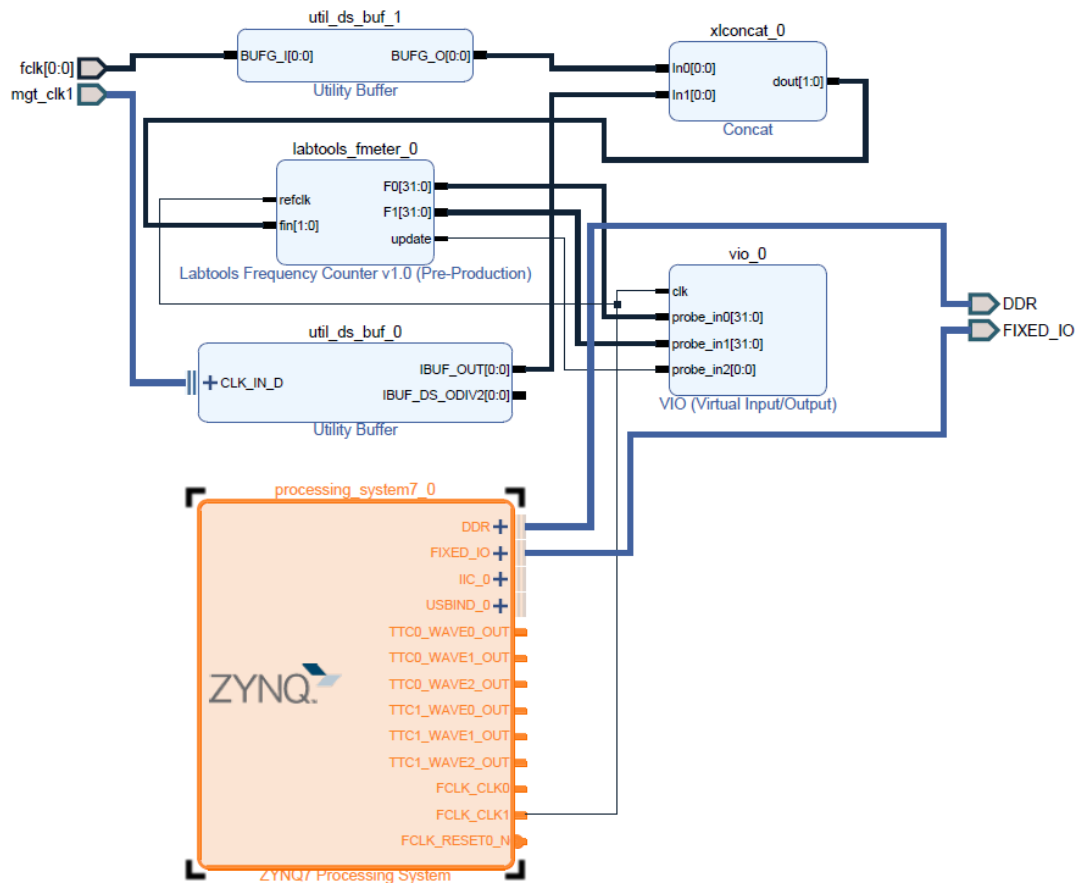
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/25163300217AA

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/2516330021...	Open
arm_dap_0 (0)	N/A
xc7z030_1 (2)	Programmed
XADC (System Monitor)	
hw_vio_1 (zsys_i/vio_0)	OK - Outputs F

Name	Value	Acti...	Directi...	VIO
> zsys_i/fm_fclk125[31:0]	[U] 0		Input	hw_vio_1
> zsys_i/fm_mgt1[31:0]	[U] 124999036	↑	Input	hw_vio_1
zsys_i/labtools_fmeter_0_update	[B] 0	↑	Input	hw_vio_1

System Design - Vivado

Block Design



PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
I2C0	EMIO- NC
I2C1	MIO
UART0	MIO
GPIO	MIO
SD0	MIO

Type	Note
USB0	MIO
ETH0	MIO
TTC	EMIO

Constraints

Basic module constraints

`_i_bitgen_common.xdc`

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFBVSS VCCO [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS_TIMESTAMP [current_design]
```

`_i_unused_io.xdc`

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

`_i_io.xdc`

```
set_property PACKAGE_PIN K2 [get_ports {fclk[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {fclk[0]}]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets fclk_IBUF[0]]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

- [SDK Projects](#)

Application

zynq_fsbl

TE modified 2017.4 FSBL

Changes:

- Si5338 Configuration see fsbl_hooks.c
add define RECONFIGURE_SI5338 to enable PLL programming with given register_map.h setup
- Add register_map.h, si5338.c, si5338.h

zynq_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)

Config

No changes.

U-Boot

No changes.

Device Tree

```

/include/ "system-conf.dtsi"
/ {
};

/* default */

/* ETH PHY */
&gem0 {

    status = "okay";
    ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
        reg = <0>;
    };
};

/* USB PHY */
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/* I2C */
// i2c PLL: 0x70, i2c eeprom: 0x50

&i2c1 {
    rtc@6F {          // Real Time Clock
        compatible = "isl12022";
        reg = <0x6F>;
    };
};
};

```

Kernel

Activate:

- RTC_DRV_ISL12022

Rootfs

Activate:

- i2c-tools

Applications

startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

Additional Software

SI5338


Download [ClockBuilder Desktop for SI5338](#)

1. Install and start ClockBuilder
2. Select SI5338
3. Options Open register map file
Note: File location <design name>/misc/SI5338/RegisterMap.txt
4. Modify settings
5. Options save C code header files
6. Replace Header files from FSBL template with generated file

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2018-10-01	v.31  Unbekanntes Makro: 'metadata'	John Hartfiel	<ul style="list-style-type: none"> New assembly variant
27.03.2018	v.29	John Hartfiel	<ul style="list-style-type: none"> Bugfix Board Part Files
2018-02-13	v.28	John Hartfiel	<ul style="list-style-type: none"> Release 2017.4
2017-11-10	v.22	John Hartfiel	<ul style="list-style-type: none"> Design Update with new options Add Si5338 section Update FSBL section
2017-10-19	v.21	John Hartfiel	<ul style="list-style-type: none"> Download Update
2017-10-19	v.20	John Hartfiel	<ul style="list-style-type: none"> Document style update
2017-10-06	v.18	John Hartfiel	<ul style="list-style-type: none"> Text correction Update Launch section Supported PCBs
2017-10-02	v.14	John Hartfiel	<ul style="list-style-type: none"> Document update on Prebuilt section
2017-09-28	v.13	John Hartfiel	Release 2017.2
2017-09-11	v.1	John Hartfiel	Initial release
	All	John Hartfiel	

Legal Notices

Data privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2018-09-18