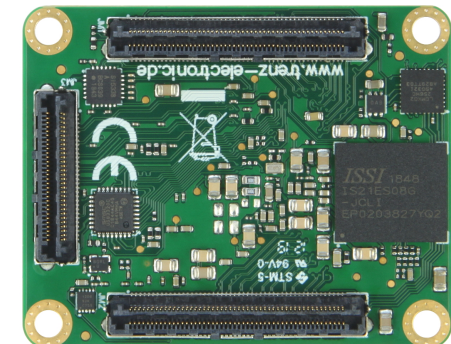




Regarding the usage of our schematics and alike documentation for Trenz module TE0821.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0821 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

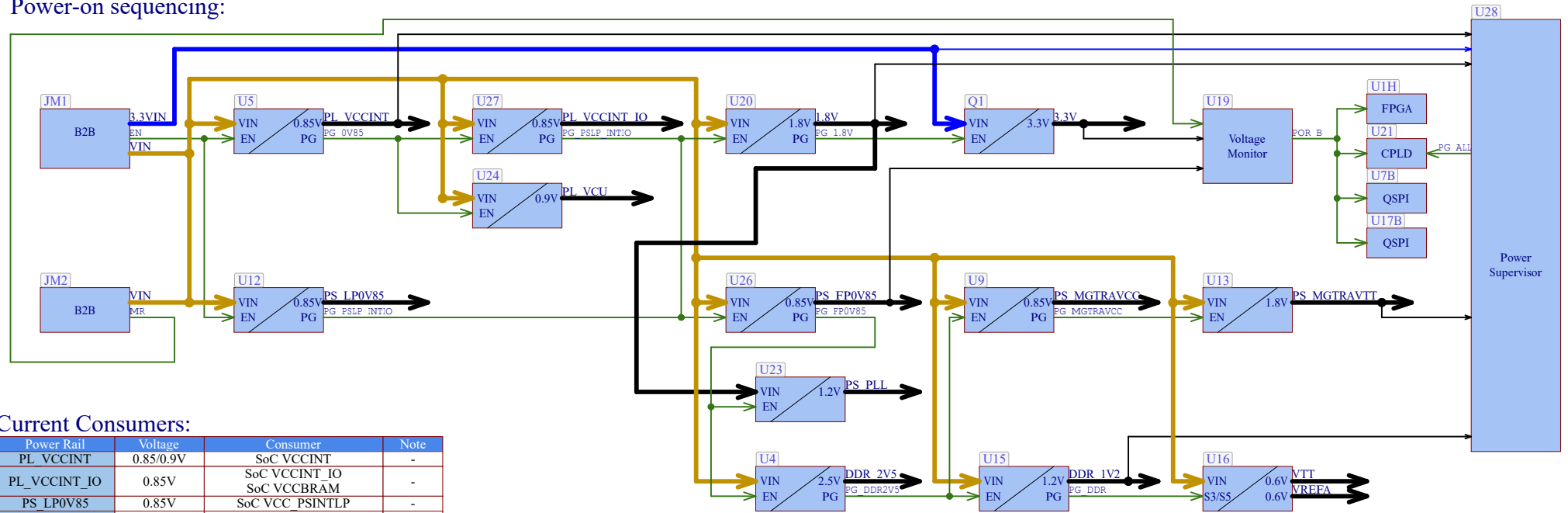
	Title: TE0821 - Legal Notices		
	A4	Number: TE0821 2AI51NA	Rev. 02
	Date: 02.12.2024	Copyright: Trenz Electronic GmbH	Page 1 of 25
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-01A	1) R38 value was changed to 20K (was: 40K2) to set VCU 0.9V	VY
-01B	1) Updated Block diagram	VY
-02	1) <u>Q1</u> was changed from TPS27081ADDCR to MP5077GG-Z 2) R82 was removed 3) <u>C143</u> and <u>C144</u> were added 4) Signal trace lengths were changed. PCB routing was improved 5) <u>D5</u> was added 6) Pins N9 (TEN) of <u>U2A</u> and <u>U3A</u> were connected together 7) <u>R100</u> was added 8) <u>U5</u> was changed from EN6363QI to MPM3860GQW-Z 9) <u>U28</u> was added 10) Net "PG_ALL" was connected to pin 5 of CPLD <u>U21</u> 11) <u>T2A</u> and <u>R113</u> - <u>R115</u> were added (<u>R113</u> DNP by default) 12) Net "RST_EN" was connected to pin 27 of CPLD <u>U21</u> 13) Net <u>EN</u> was connected to pin 16 of <u>U5</u> and pin 1 of <u>U12</u> 14) <u>R116</u> and <u>R117</u> were added (<u>R116</u> DNP by default) 15) All unconnected pins for Bank64 <u>U1D</u> were connected together 16) <u>TP17</u> , <u>TP18</u> , <u>TP21</u> , <u>TP22</u> were added. Some testpoints were moved 17) <u>C178</u> was added 18) <u>R118</u> - <u>R121</u> were added 19) <u>C179</u> - <u>C185</u> were added 20) <u>C136</u> , <u>C140</u> were changed from 22u to 47u 21) <u>C186</u> , <u>C187</u> , <u>C188</u> , <u>C189</u> were added 22) <u>C15</u> , <u>C16</u> were changed from 4.7u to 10u 23) <u>C48</u> was changed from 16V to 10V, <u>C45</u> was changed from 4.7u to 10u 24) <u>C49</u> , <u>C52</u> , <u>C53</u> , <u>C57</u> were changed from 4.7u to 10u 25) <u>C2</u> was changed from 16V to 10V 26) <u>C37</u> , <u>C41</u> , <u>C89</u> , <u>C94</u> , <u>C107</u> , <u>C130</u> , <u>C134</u> were changed from 16V 0603 to 10V 0402 27) FPGA speedgrade table was changed on page "POWER.SchDoc" 28) <u>C24</u> , <u>C25</u> , <u>C96</u> , <u>C110</u> were changed from 0805 to 0603 29) <u>C19</u> , <u>C21</u> , <u>C23</u> , <u>C67</u> , <u>C84</u> , <u>C93</u> , <u>C129</u> , <u>C133</u> , <u>C135</u> were changed from 6.3V to 10V 30) <u>C61</u> was changed from 16V 0402 to 6.3V 0201 31) Power Diagram page was added, System Overview was updated 32) Nets were renamed: "PS_AVCC" -> <u>PS_MGTRAVCC</u> , "PG_AVCC" -> <u>PG_MGTRAVCC</u> , "OTG-RCLK" -> <u>OTG-REFCLK</u> , "PS_AVTT" -> <u>PS_MGTRAVTT</u> , "PG_DDR" -> <u>PG_DDRIV2</u> 33) Connection for pin "SENSE" of <u>U19</u> was changed from net <u>PS_LP0V85</u> to net <u>PS_FP0V85</u> 34) Net <u>PG_0V85</u> was connected to pin 1 (EN) of <u>U27</u> 35) Net "PG_PS_LP" was renamed to <u>PG_PSLP_INTIO</u> and connected with pin 2 (PG) of <u>U27</u> , pin 1 (EN) of <u>U20</u> (instead net <u>PG_0V85</u>) 36) Net <u>PG_FP0V85</u> was created and connected to pin 2 (PG) of <u>U26</u> , pin 3 (EN) of <u>U23</u> (instead net "PG_PS_LP") and pin 1 (EN) of <u>U4</u> (instead net "PG_PS_LP") 37) Net <u>PG_DDR2V5</u> was created, pin 2 (PG) of <u>U4</u> was connected to pin 1 (EN) of <u>U9</u> (instead net "PG_PS_LP") 38) <u>R70</u> was unconnected from pin 1 of <u>U9</u> and connected to pin 1 of <u>U26</u> 39) <u>R122</u> was added 40) <u>U11</u> was changed from SiT8008BI-73-XXS-25.000000E to SiT8008BI-73-18S-25.000000E 41) VDD for <u>U10</u> and <u>U11</u> was changed from 3.3V to 1.8V	MT



Title: TE0821 - Revision Changes		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH	Page 2 of 25
Filename: Revision Changes.SchDoc		

Power-on sequencing:



Current Consumers:

Power Rail	Voltage	Consumer	Note
PL_VCCINT	0.85V/0.9V	SoC VCCINT	-
PL_VCCINT_IO	0.85V	SoC VCCINT_IO SoC VCCBRAM	-
PS_LP0V85	0.85V	SoC VCC_PSINTLP	-
1.8V	1.8V	CPLD VCCIO1/2 B2B JM1 SoC VCCO_66 QSPI FLASH QUAD CLK VDDO SoC VCCO_PS_503 eMMC VCCQ ETH PHY VDDO SoC VCCPSDDR_PLL USB PHY VDD18 SoC VCC_AUX SoC VCC_AUX_IO SoC VCC_PS_AUX	-
PL_VCU	0.9V	SoC VCCINT_VCU	-
PS_AVCC	0.85V	SoC PS_MGTRAVCC	-
PS_FP0V85	0.85V	SoC VCC_PS_INTFP_DDR SoC VCC_PS_INTFP	-
PS_PLL	1.2V	SoC VCC_PSPLL	-
DDR_2V5	2.5V	DDR VPP	-
3.3V	3.3V	B2B JM2 SoC VCCO_PSIO1_501 QUAD CLK VDD eMMC VCC EEPROM VCC CLK GEN 25M VDD USB PHY VDD33/VBAT CLK GEN 52M VDD	-
PS_AVTT	1.8V	SoC PS_MGTRAVTT	-
DDR_1V2	1.2V	DDR VDD/VDDQ	-
VREFA	0.6V	SoC VCCO_PSDDR_504 DDR VREFCA	-

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V-5.7V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
	OUT	3.3V	+/-5%	Power for JTAG	-
PSBATT	IN	1.2 - 1.5V	+/-3%	SoC Vbatt	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	IO Bank65	-
VCCO_HD25_26	IN	1.2 - 3.3V	+/-3%	IO Banks 25/26	-
VCCO_HD24_44	IN	1.2 - 3.3V	+/-3%	IO Banks 24/44	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-



Title: TE0821 - Power Diagram		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 24.10.2025	Copyright: Trenz Electronic GmbH	Page 4 of 25
Filename: Power Diagram.SchDoc		

Serial
Serialnumber 6,3 x 6.3mm

CE
CE Logo on Top Overlay

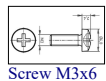
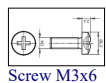
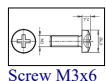
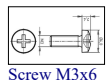
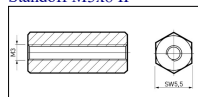
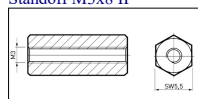
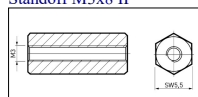
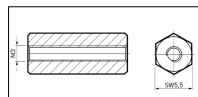
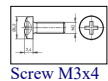
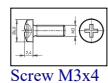
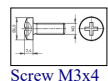
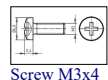
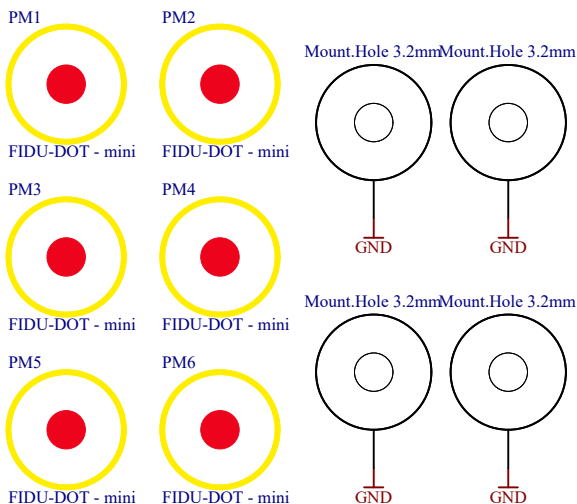
CE-TOPOVERLAY

UKCA
UKCA Logo on Top Overlay

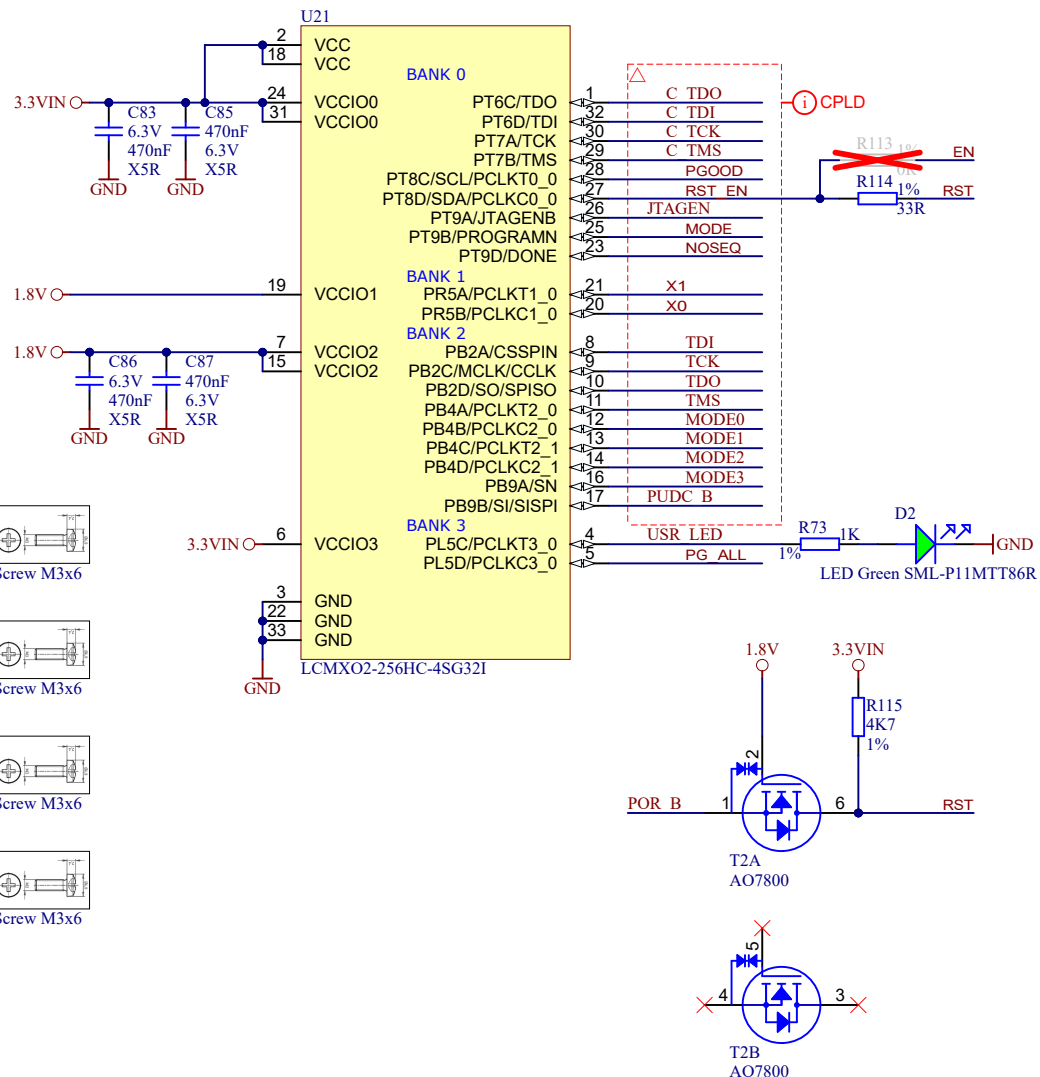
UKCA-TOPOVERLAY

RoHS
RoHS Logo on Top Overlay

RoHS-TOPOVERLAY



Special notes:



Title: TE0821		Rev. 02	
A4	Number: TE0821 2AI51NA	Page 5 of 25	
Date: 02.12.2024	Copyright: Trenz Electronic GmbH		Filename: TE0821.SchDoc

1

2

3

4

A

A

B

B

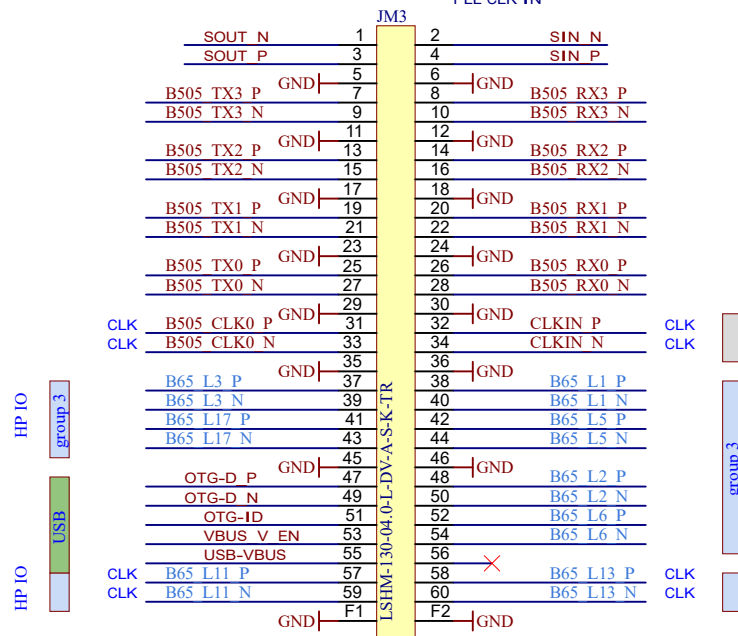
C

C

D

D

USB OTG
ETH SGMII
PS_GTR 4 Lanes
PS_GTR CLK IN
PLL CLK IN



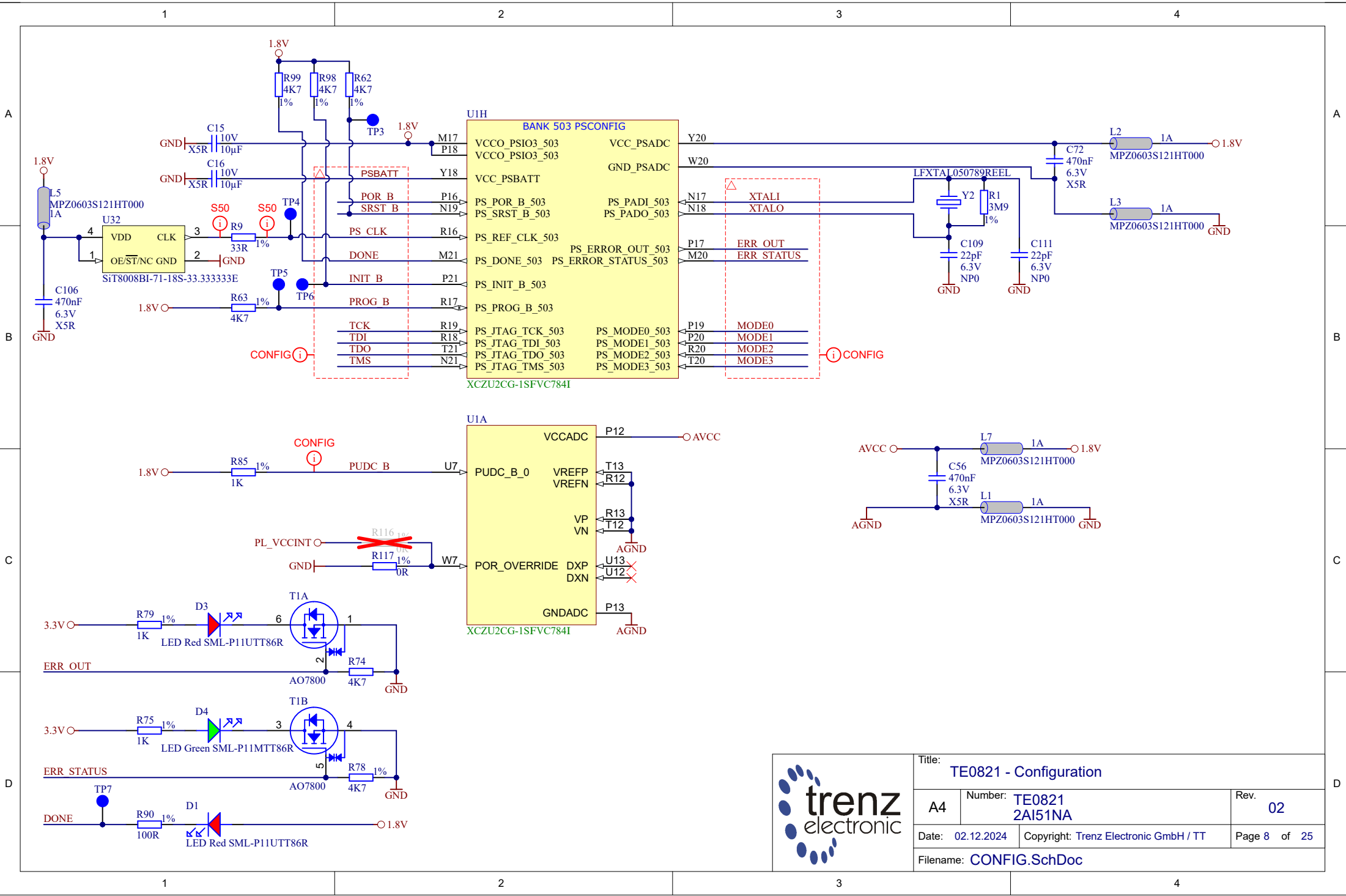
Title: TE0821 - B2B Connectors			
A4	Number: TE0821 2AI51NA		Rev. 02
Date: 02.12.2024		Copyright: 2015 Trenz Electronic GmbH	Page 7 of 25
Filename: B2B-Connectors_2.SchDoc			

1

2

3

4





Title: TE0821 - Configuration		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 8 of 25
Filename: CONFIG.SchDoc		

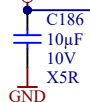
1

2

3

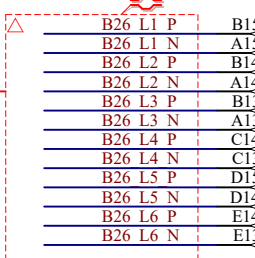
4

VCCO_HD25_26



U1C

BANK 26 HD (ZU4/5 BANK 46 HD)

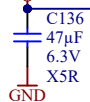
VCCO_26
VCCO_26

IO_L1P_AD11P_26
IO_L1N_AD11N_26
IO_L2P_AD10P_26
IO_L2N_AD10N_26
IO_L3P_AD9P_26
IO_L3N_AD9N_26
IO_L4P_AD8P_26
IO_L4N_AD8N_26
IO_L5P_HDGC_AD7P_26
IO_L5N_HDGC_AD7N_26
IO_L6P_HDGC_AD6P_26
IO_L6N_HDGC_AD6N_26

IO_L7P_HDGC_AD5P_26
IO_L7N_HDGC_AD5N_26
IO_L8P_HDGC_AD4P_26
IO_L8N_HDGC_AD4N_26
IO_L9P_AD3P_26
IO_L9N_AD3N_26
IO_L10P_AD2P_26
IO_L10N_AD2N_26
IO_L11P_AD1P_26
IO_L11N_AD1N_26
IO_L12P_AD0P_26
IO_L12N_AD0N_26

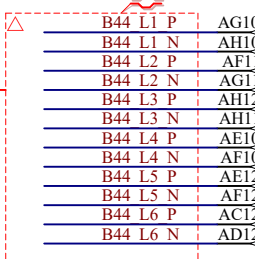
B26 L7 P
B26 L7 N
B26 L8 P
B26 L8 N
B26 L9 P
B26 L9 N
B26 L10 P
B26 L10 N
B26 L11 P
B26 L11 N
B26 L12 P
B26 L12 N

VCCO_HD24_44



U1C

BANK 44 HD (ZU4/5 BANK 43 HD)

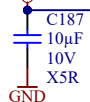
VCCO_44
VCCO_44

IO_L1P_AD11P_44
IO_L1N_AD11N_44
IO_L2P_AD10P_44
IO_L2N_AD10N_44
IO_L3P_AD9P_44
IO_L3N_AD9N_44
IO_L4P_AD8P_44
IO_L4N_AD8N_44
IO_L5P_HDGC_AD7P_44
IO_L5N_HDGC_AD7N_44
IO_L6P_HDGC_AD6P_44
IO_L6N_HDGC_AD6N_44

IO_L7P_HDGC_AD5P_44
IO_L7N_HDGC_AD5N_44
IO_L8P_HDGC_AD4P_44
IO_L8N_HDGC_AD4N_44
IO_L9P_AD3P_44
IO_L9N_AD3N_44
IO_L10P_AD2P_44
IO_L10N_AD2N_44
IO_L11P_AD1P_44
IO_L11N_AD1N_44
IO_L12P_AD0P_44
IO_L12N_AD0N_44

B44 L7 P
B44 L7 N
B44 L8 P
B44 L8 N
B44 L9 P
B44 L9 N
B44 L10 P
B44 L10 N
B44 L11 P
B44 L11 N
B44 L12 P
B44 L12 N

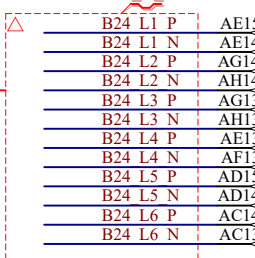
VCCO_HD24_44



U1B

XCZU2CG-1SFVC784I

BANK 24 HD (ZU4/5 BANK 44 HD)

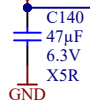
VCCO_24
VCCO_24

IO_L1P_AD15P_24
IO_L1N_AD15N_24
IO_L2P_AD14P_24
IO_L2N_AD14N_24
IO_L3P_AD13P_24
IO_L3N_AD13N_24
IO_L4P_AD12P_24
IO_L4N_AD12N_24
IO_L5P_HDGC_24
IO_L5N_HDGC_24
IO_L6P_HDGC_24
IO_L6N_HDGC_24

IO_L7P_HDGC_24
IO_L7N_HDGC_24
IO_L8P_HDGC_24
IO_L8N_HDGC_24
IO_L9P_AD11P_24
IO_L9N_AD11N_24
IO_L10P_AD10P_24
IO_L10N_AD10N_24
IO_L11P_AD9P_24
IO_L11N_AD9N_24
IO_L12P_AD8P_24
IO_L12N_AD8N_24

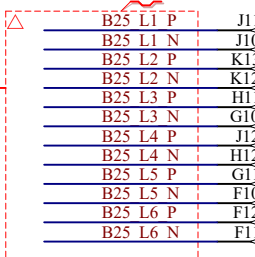
B24 L7 P
B24 L7 N
B24 L8 P
B24 L8 N
B24 L9 P
B24 L9 N
B24 L10 P
B24 L10 N
B24 L11 P
B24 L11 N
B24 L12 P
B24 L12 N

VCCO_HD25_26



U1C

BANK 25 HD (ZU4/5 BANK 45 HD)

VCCO_25
VCCO_25

IO_L1P_AD15P_25
IO_L1N_AD15N_25
IO_L2P_AD14P_25
IO_L2N_AD14N_25
IO_L3P_AD13P_25
IO_L3N_AD13N_25
IO_L4P_AD12P_25
IO_L4N_AD12N_25
IO_L5P_HDGC_25
IO_L5N_HDGC_25
IO_L6P_HDGC_25
IO_L6N_HDGC_25

IO_L7P_HDGC_25
IO_L7N_HDGC_25
IO_L8P_HDGC_25
IO_L8N_HDGC_25
IO_L9P_AD11P_25
IO_L9N_AD11N_25
IO_L10P_AD10P_25
IO_L10N_AD10N_25
IO_L11P_AD9P_25
IO_L11N_AD9N_25
IO_L12P_AD8P_25
IO_L12N_AD8N_25

B25 L7 P
B25 L7 N
B25 L8 P
B25 L8 N
B25 L9 P
B25 L9 N
B25 L10 P
B25 L10 N
B25 L11 P
B25 L11 N
B25 L12 P
B25 L12 N

XCZU2CG-1SFVC784I



Title:

TE0821 - HD Banks

A4

Number:

TE0821
2AI51NA

Rev.

02

Date: 02.12.2024

Copyright: Trenz Electronic GmbH / TT

Page 9 of 25

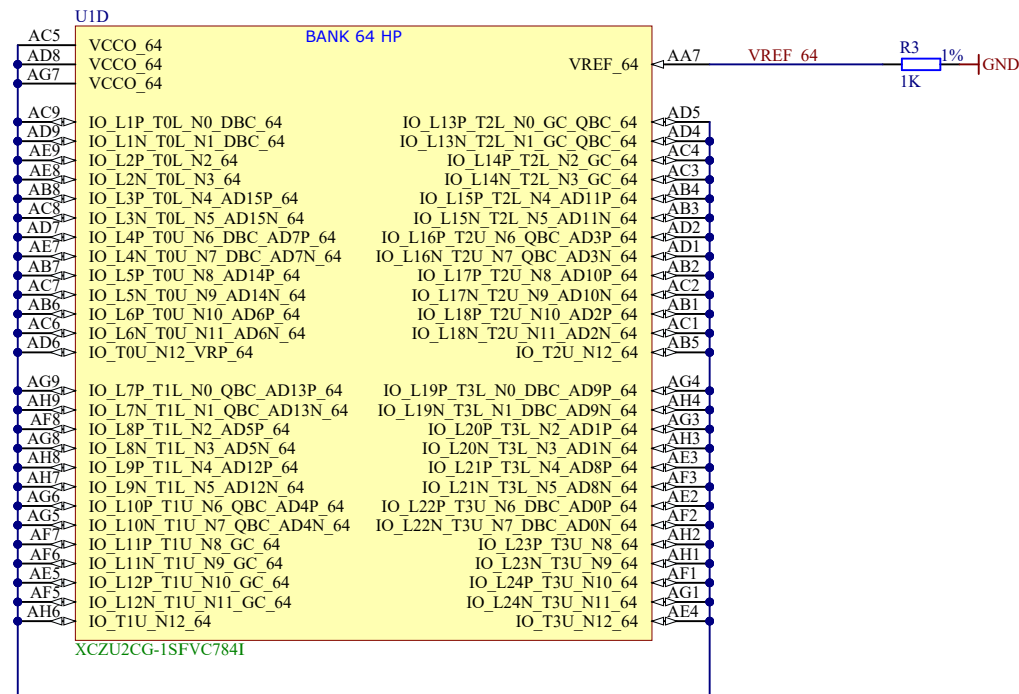
Filename: B_HD.SchDoc

1

2

3

4



Title: TE0821 - B64		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 10 of 25
Filename: B64.SchDoc		

1

2

3

4

A

A

B

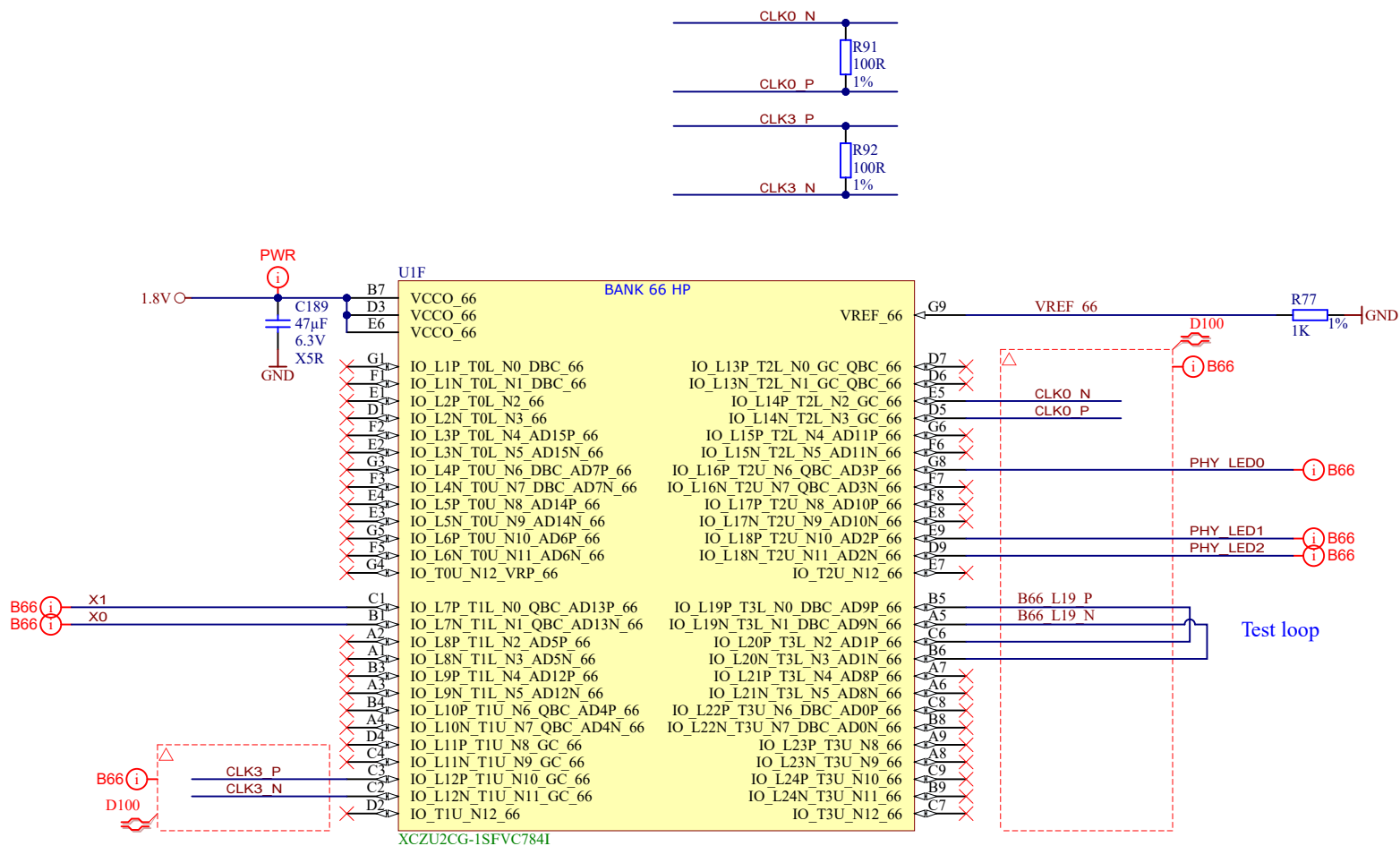
B

C

C

D

D



Title: TE0821 - B66		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 12 of 25
Filename: B66.SchDoc		

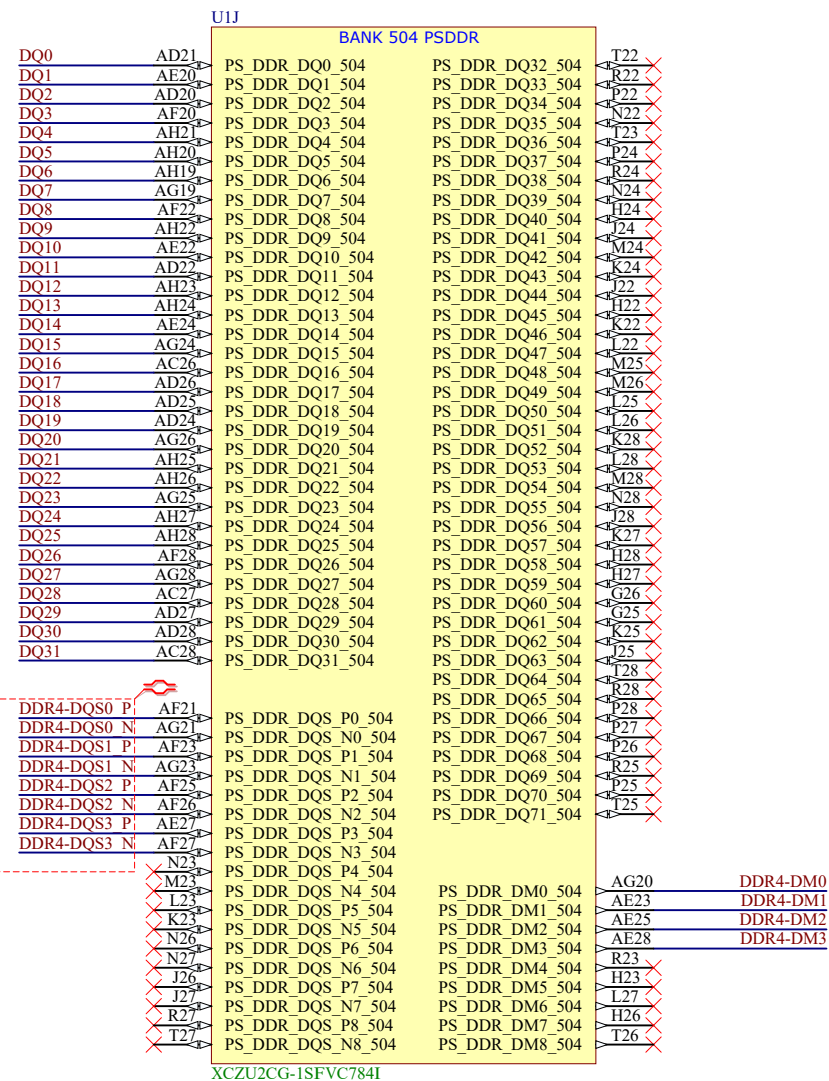
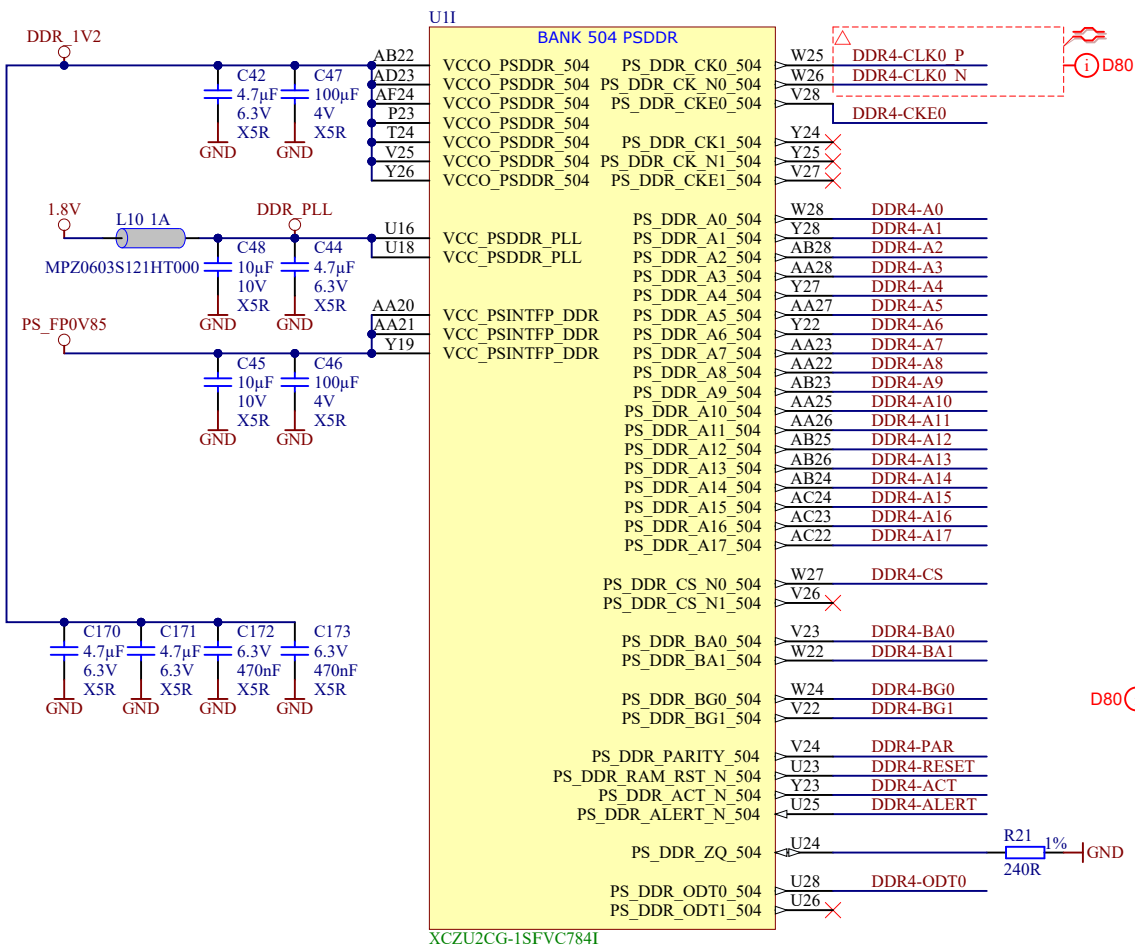
1

2

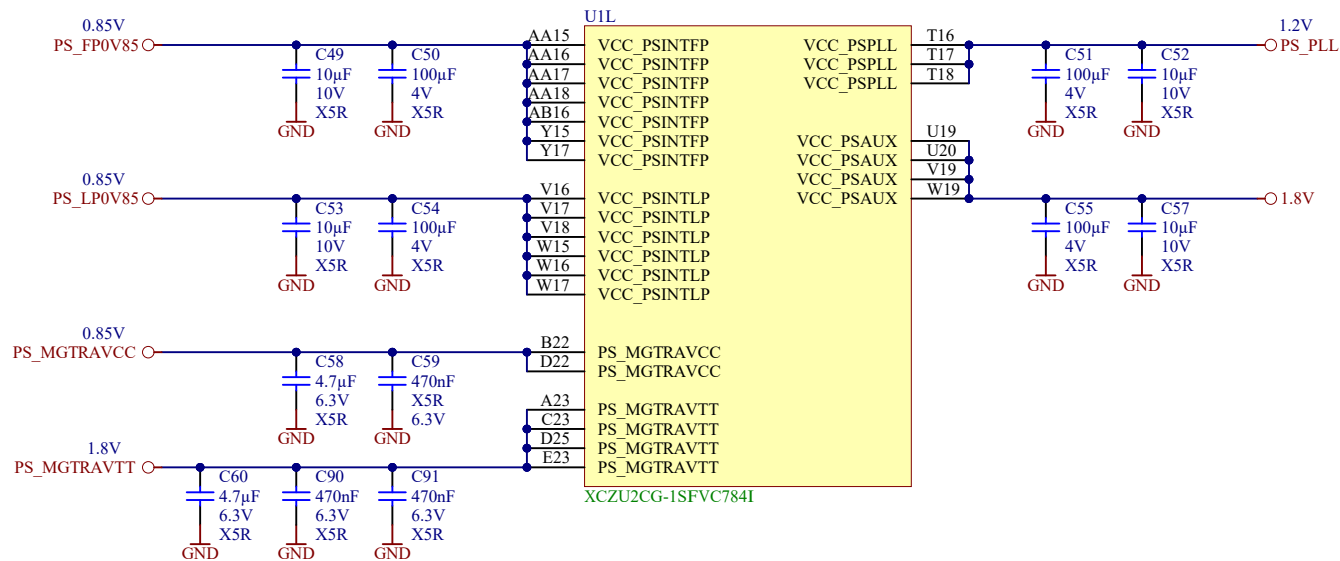
3

4

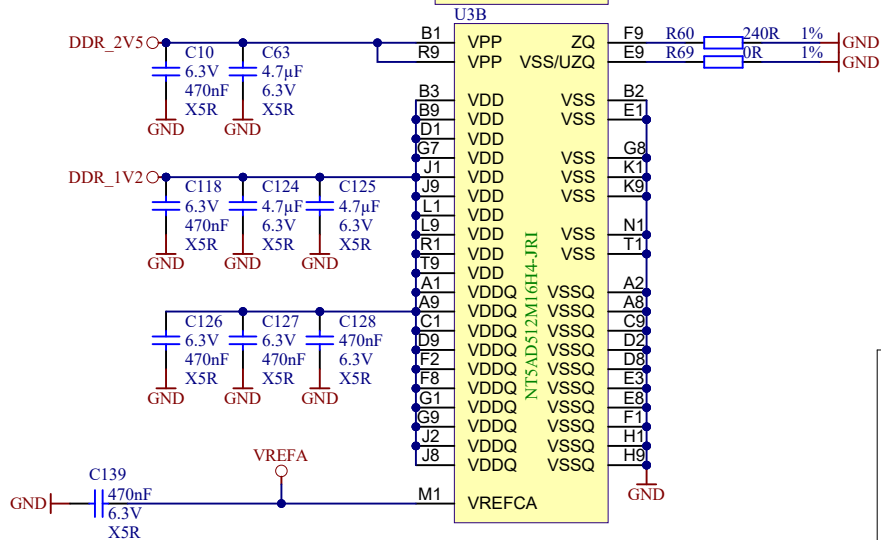




Title: TE0821 - PS DDR			
A4	Number: TE0821 2AI51NA		Rev. 02
Date: 02.12.2024		Copyright: Trenz Electronic GmbH / TT	Page 14 of 25
Filename: PS_DDR.SchDoc			



		Title: TE0821 - ZU PS POWER	
		A4	Rev. 02
Date: 02.12.2024		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 17 of 25	



Title: TE0821 - DDR4 RAM2			
A4	Number: TE0821 2AI51NA	Rev. 02	
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 20 of 25	
Filename: DDR4-RAM_2.SchDoc			

1

2

3

4

A

B

C

D

A

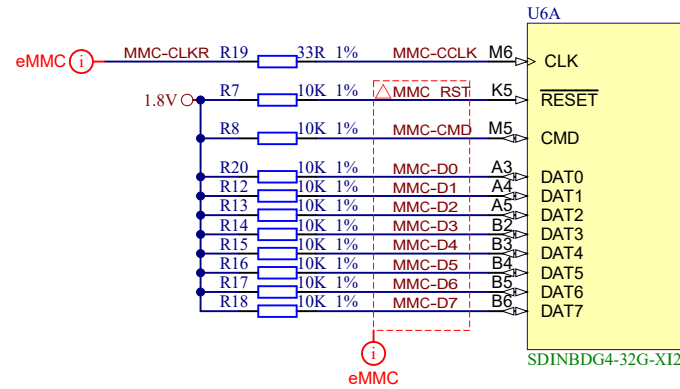
B

C

D

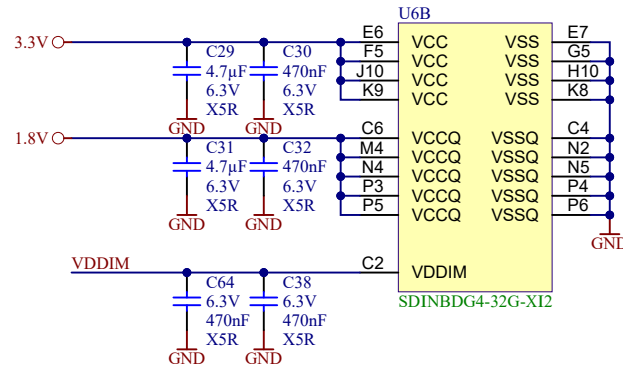
U6D			
A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M1
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

SDINBDG4-32G-X12



U6C	
A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

SDINBDG4-32G-X12



Title: TE0821 - eMMC		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 21 of 25
Filename: eMMC.SchDoc		

1

2

3

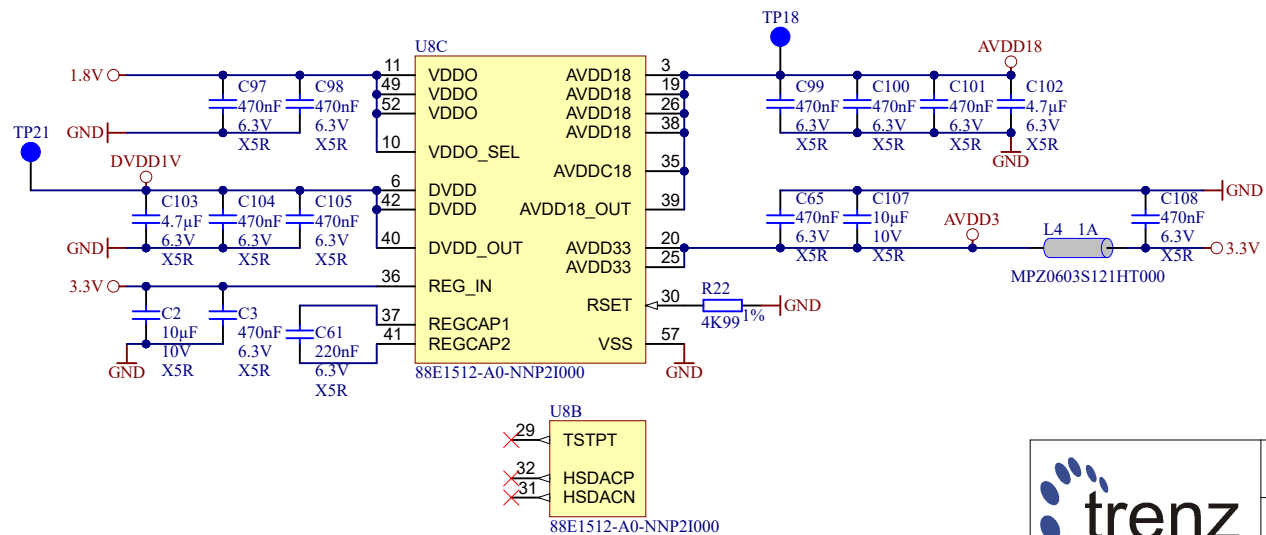
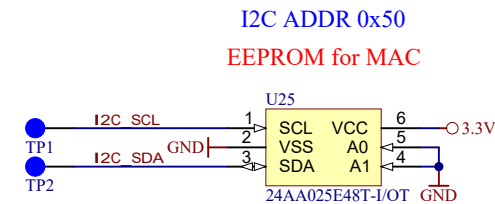
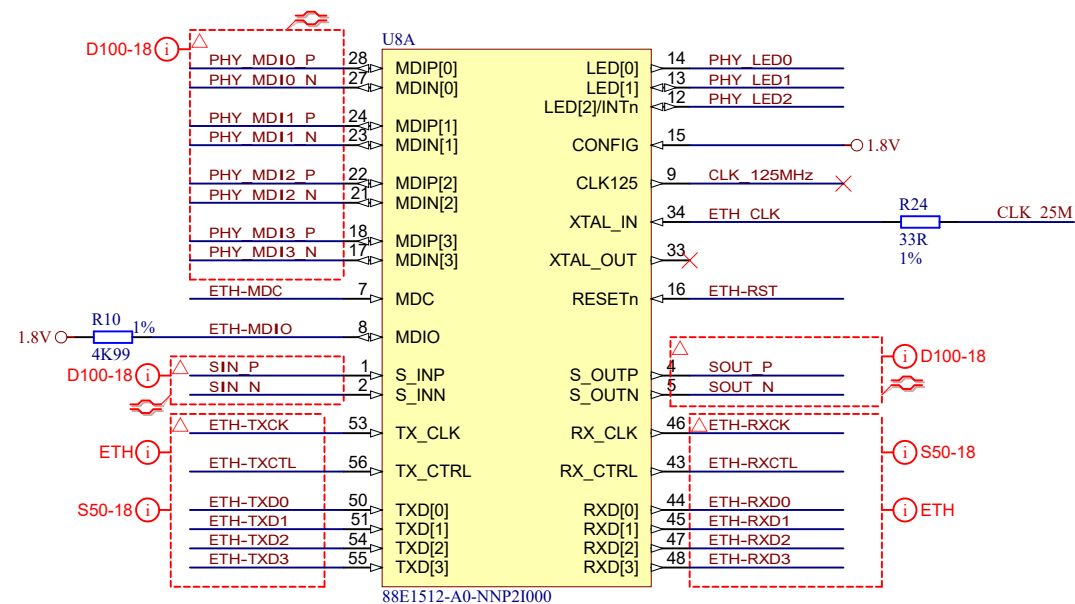
4

1

2

3

4



Title: TE0821 - Ethernet PHY			
A4	Number: TE0821 2A151NA		Rev. 02
Date: 02.12.2024		Copyright: 2015 Trenz Electronic GmbH	Page 22 of 25
Filename: ETH-PHY.SchDoc			

1

2

3

4

1

2

3

4

A

A

B

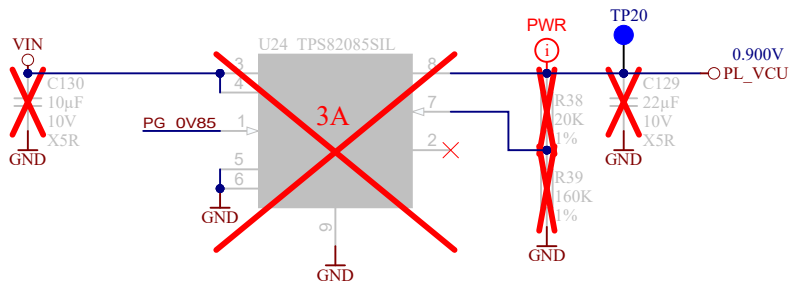
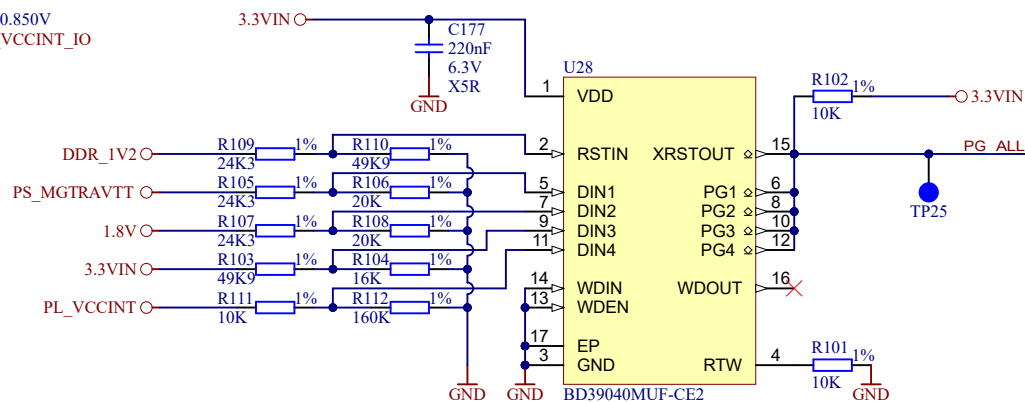
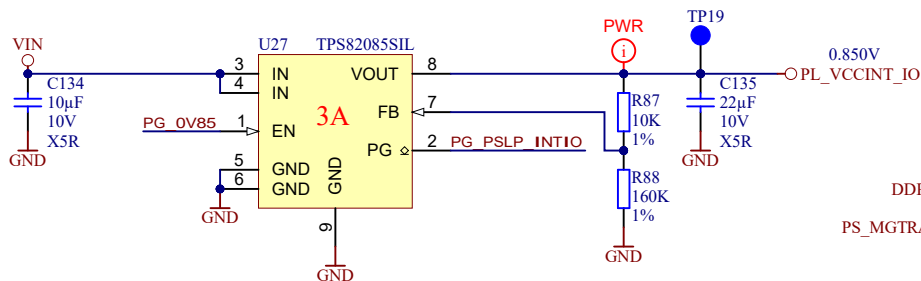
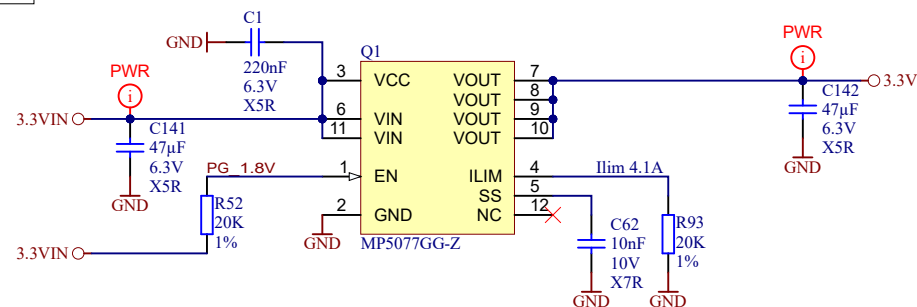
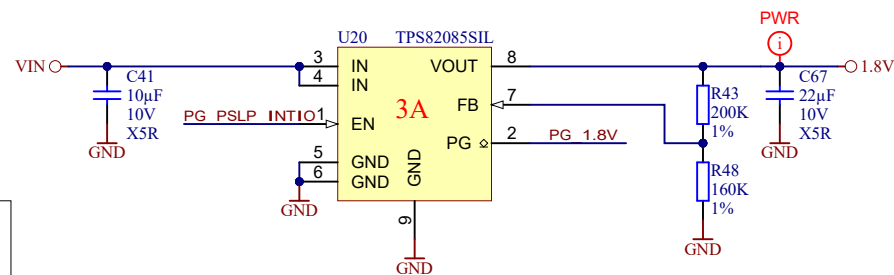
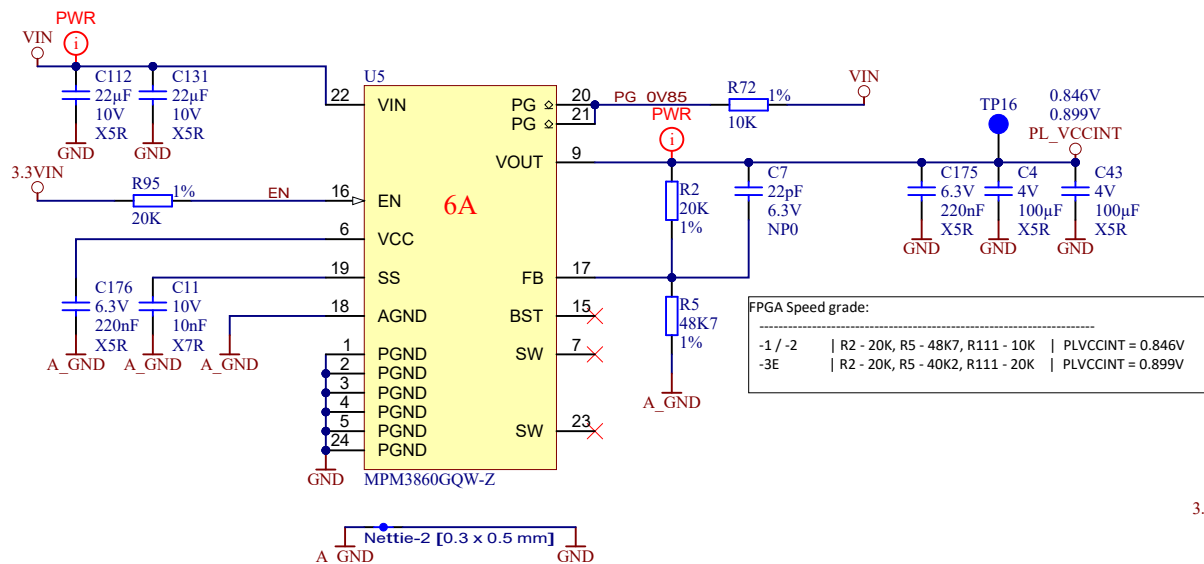
B

C

C

D

D



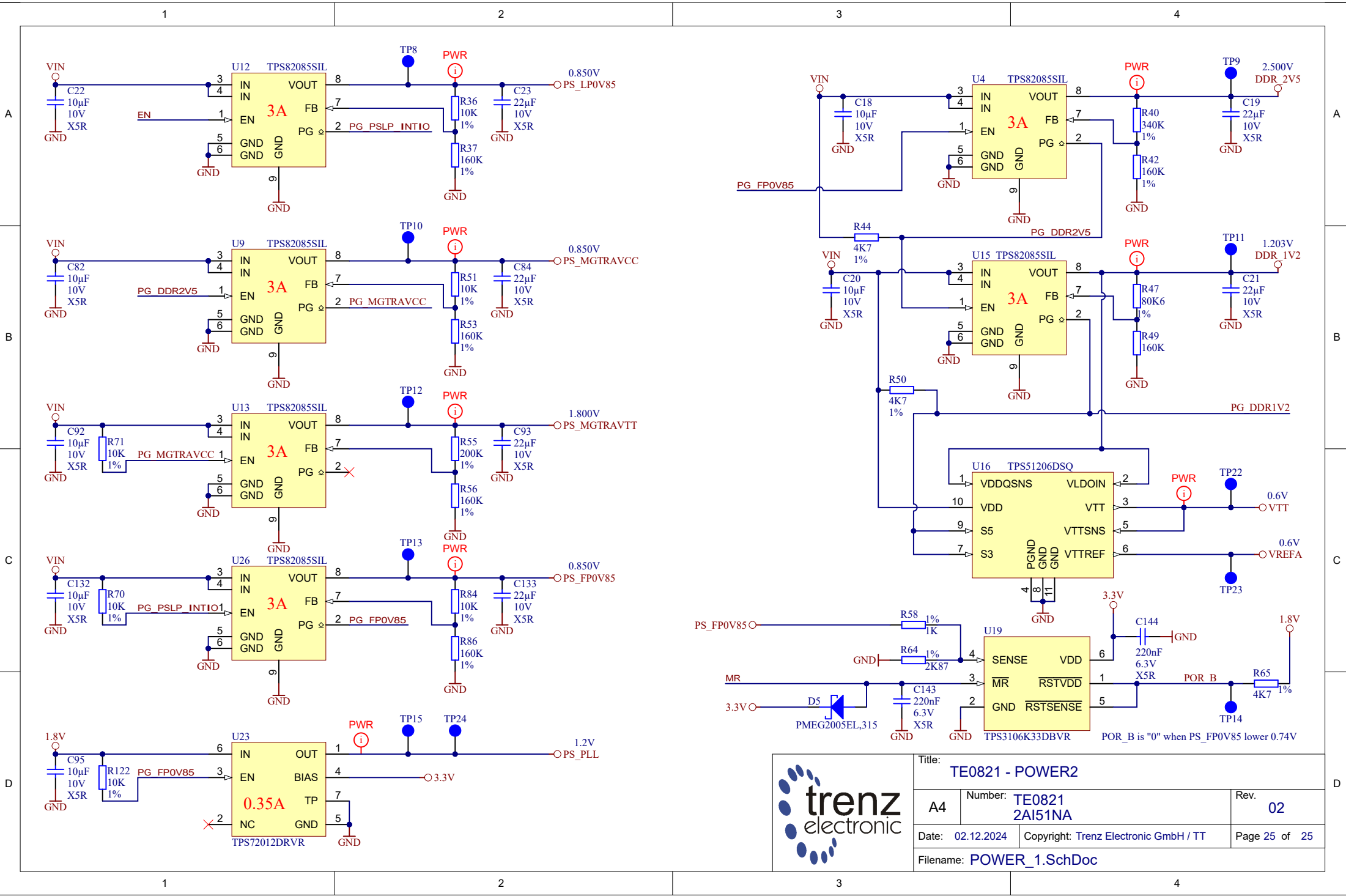
Title: TE0821 - POWER		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 24 of 25
Filename: POWER.SchDoc		

1

2

3

4





Title: TE0821 - POWER2		
A4	Number: TE0821 2AI51NA	Rev. 02
Date: 02.12.2024	Copyright: Trenz Electronic GmbH / TT	Page 25 of 25
Filename: POWER_1.SchDoc		