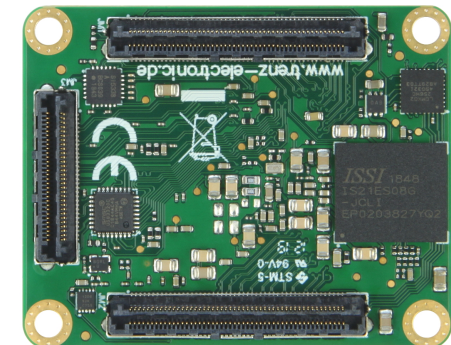




Regarding the usage of our schematics and alike documentation for Trenz module TE0821.

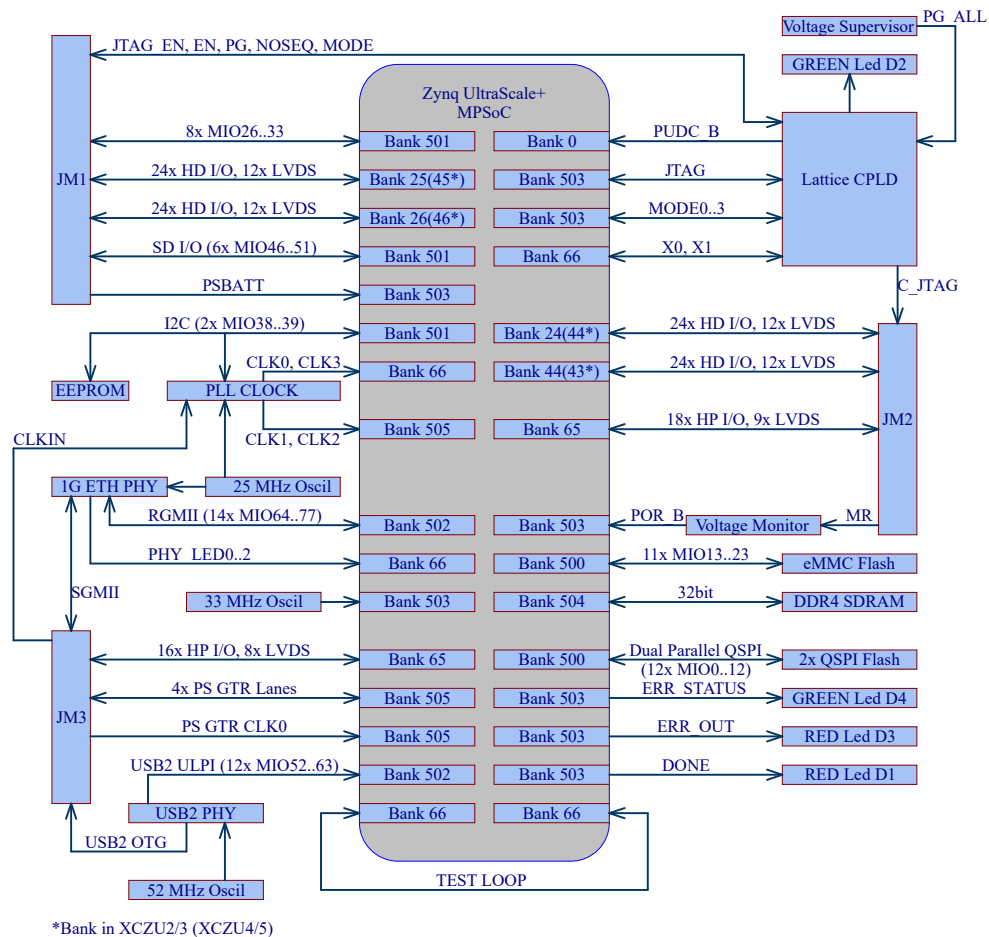
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0821 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0821 - Legal Notices		
	A4	Number: TE0821 3BE91ND	Rev. 02
	Date: 28-May-24	Copyright: Trenz Electronic GmbH	Page 1 of 25
	Filename: Legal Notices Modules.SchDoc		

1		2		3		4	
A	REV		Description				A
	-01		Initial revision				
	-01A		1) R38 value was changed to 20K (was: 40K2) to set VCU 0.9V		VY		
	-01B		1) Updated Block diagram		VY		
B	-02		1) Q1 was changed from TPS27081ADDCR to MP5077GG-Z 2) R82 was removed 3) C143 and C144 were added 4) Signal trace lengths were changed. PCB routing was improved 5) D5 was added 6) Pins N9 (TEN) of U2A and U3A were connected together 7) R100 was added 8) U5 was changed from EN6363Q1 to MPM3860GQW-Z 9) U28 was added 10) Net "PG_ALL" was connected to pin 5 of CPLD U21 11) T2A and R113 - R115 were added (R113 DNP by default) 12) Net "RST_EN" was connected to pin 27 of CPLD U21 13) Net EN was connected to pin 16 of U5 and pin 1 of U12 14) R116 and R117 were added (R116 DNP by default) 15) All unconnected pins for Bank64 U1D were connected together 16) TP17 , TP18 , TP21 , TP22 were added. Some testpoints were moved 17) C178 was added 18) R118 - R121 were added 19) C179 - C185 were added 20) C136 , C140 were changed from 22u to 47u 21) C186 , C187 , C188 , C189 were added 22) C15 , C16 were changed from 4.7u to 10u 23) C48 was changed from 16V to 10V, C45 was changed from 4.7u to 10u 24) C49 , C52 , C53 , C57 were changed from 4.7u to 10u 25) C2 was changed from 16V to 10V 26) C37 , C41 , C89 , C94 , C107 , C130 , C134 were changed from 16V 0603 to 10V 0402 27) FPGA speedgrade table was changed on page "POWER.SchDoc" 28) C24 , C25 , C96 , C110 were changed from 0805 to 0603 29) C19 , C21 , C23 , C67 , C84 , C93 , C129 , C133 , C135 were changed from 6.3V to 10V 30) C61 was changed from 16V 0402 to 6.3V 0201 31) Power Diagram page was added, System Overview was updated 32) Nets were renamed: "PS_AVCC" -> PS_MGTRAVCC , "PG_AVCC" -> PG_MGTRAVCC "OTG-RCLK" -> OTG-REFCLK , "PS_AVTT" -> PS_MGTRAVTT , "PG_DDR" -> PG_DDR1V2 33) Connection for pin "SENSE" of U19 was changed from net PS_LP0V85 to net PS_FP0V85 34) Net PG_0V85 was connected to pin 1 (EN) of U27 35) Net "PG_PS_LP" was renamed to PG_PSLP_INTIO and connected with pin 2 (PG) of U27 , pin 1 (EN) of U20 (instead net PG_0V85) 36) Net PG_FP0V85 was created and connected to pin 2 (PG) of U26 , pin 3 (EN) of U23 (instead net "PG_PS_LP") and pin 1 (EN) of U4 (instead net "PG_PS_LP") 37) Net PG_DDR2V5 was created, pin 2 (PG) of U4 was connected to pin 1 (EN) of U9 (instead net "PG_PS_LP") 38) R70 was unconnected from pin 1 of U9 and connected to pin 1 of U26 39) R122 was added 40) U11 was changed from SiT8008BI-73-XXS-25.000000E to SIT8008BI-73-18S-25.000000E 41) VDD for U10 and U11 was changed from 3.3V to 1.8V		MT		B
C							C
D							D
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		Title: TE0821 - Revision Changes		
		A4	Number: TE0821 3BE91ND	Rev. 02
		Date: 30-Sep-24	Copyright: Trenz Electronic GmbH	Page 2 of 25
		Filename: Revision Changes.SchDoc		



- U_B64
B64.SchDoc
- U_ZU_POWER
ZU_POWER.SchDoc
- U_ZU_PS_POWER
ZU_PS_POWER.SchDoc
- U_POWER
POWER.SchDoc
- U_POWER_1
POWER_1.SchDoc
- U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

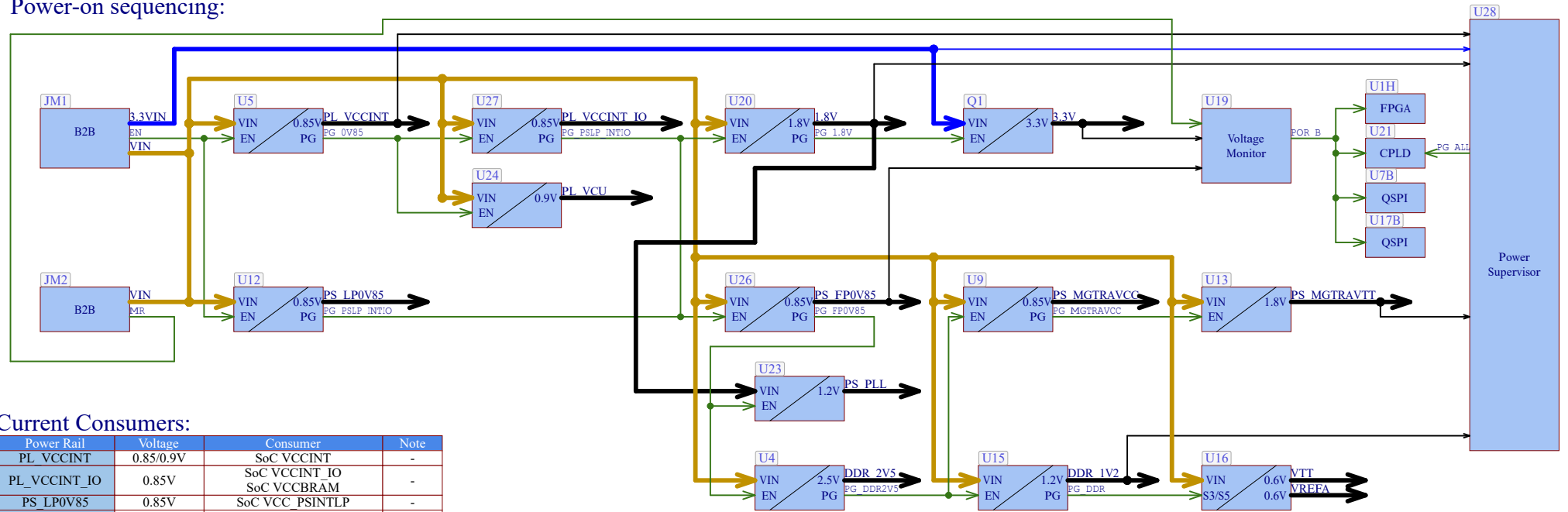
Table of I2C devices and addresses

Designator	I2C Address	Description
U25	0x50	I2C MAC EEPROM
U10	0x70	QUAD CLOCK GEN



Title: TE0821 - System Overview			
A4	Number: TE0821 3BE91ND		Rev. 02
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Filename: TE0821-Overview.SchDoc			

Power-on sequencing:



Current Consumers:

Power Rail	Voltage	Consumer	Note
PL_VCCINT	0.85V/0.9V	SoC VCCINT	-
PL_VCCINT_IO	0.85V	SoC VCCINT_IO SoC VCCBRAM	-
PS_LP0V85	0.85V	SoC VCC_PSINTLP	-
1.8V	1.8V	CPLD VCCIO1/2 B2B JM1 SoC VCCO_66 QSPI FLASH QUAD CLK VDDO SoC VCCO_PS_503 eMMC VCCQ ETH PHY VDDO SoC VCCPSDDR_PLL USB PHY VDD18 SoC VCC_AUX SoC VCC_AUX_IO SoC VCC_PS_AUX	-
PL_VCU	0.9V	SoC VCCINT_VCU	-
PS_AVCC	0.85V	SoC PS_MGTRAVCC	-
PS_FP0V85	0.85V	SoC VCC_PS_INTFP_DDR SoC VCC_PS_INTFP	-
PS_PLL	1.2V	SoC VCC_PSPLL	-
DDR_2V5	2.5V	DDR VPP	-
3.3V	3.3V	B2B JM2 SoC VCCO_PSI01_501 QUAD CLK VDD eMMC VCC EEPROM VCC CLK GEN 25M VDD USB PHY VDD33/VBAT CLK GEN 52M VDD	-
PS_AVTT	1.8V	SoC PS_MGTRAVTT	-
DDR_1V2	1.2V	DDR VDD/VDDQ	-
VREFA	0.6V	SoC VCCO_PSDDR_504 DDR VREFCA	-

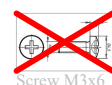
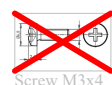
Supported Voltage Ranges:

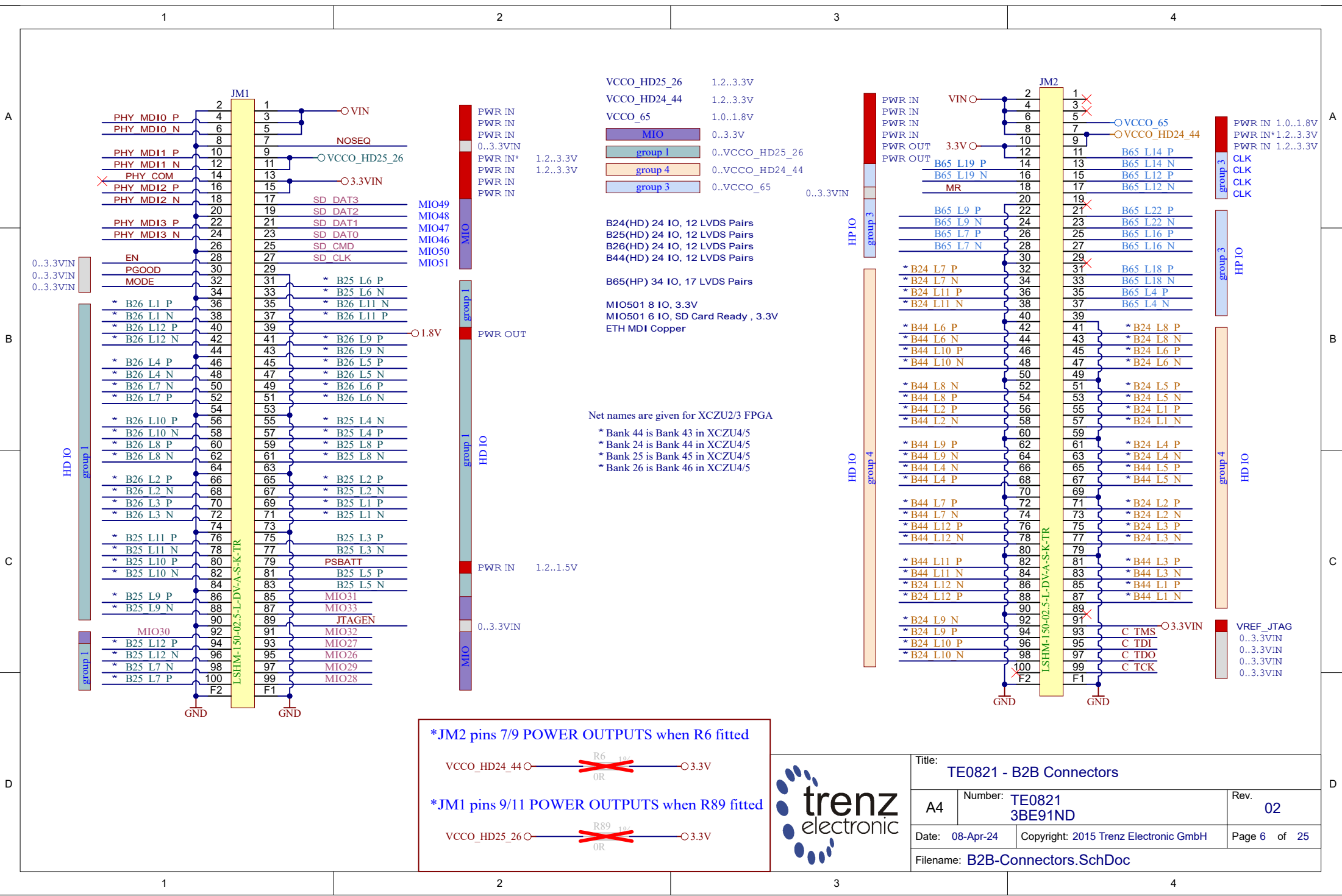
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V-5.7V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
	OUT	3.3V	+/-5%	Power for JTAG	-
PSBATT	IN	1.2 - 1.5V	+/-3%	SoC Vbatt	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	IO Bank65	-
VCCO_HD25_26	IN	1.2 - 3.3V	+/-3%	IO Banks 25/26	-
VCCO_HD24_44	IN	1.2 - 3.3V	+/-3%	IO Banks 24/44	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-



Title: TE0821 - Power Diagram		
A4	Number: TE0821 3BE91ND	Rev. 02
Date: 02-Oct-25	Copyright: Trenz Electronic GmbH	
Filename: Power_Diagram.SchDoc		Page 4 of 25

RoHS-TOPOVERLAY





Title: TE0821 - B2B Connectors			
A4	Number: TE0821 3BE91ND		Rev. 02
Date: 08-Apr-24	Copyright: 2015 Trenz Electronic GmbH		Page 6 of 25
Filename: B2B-Connectors.SchDoc			

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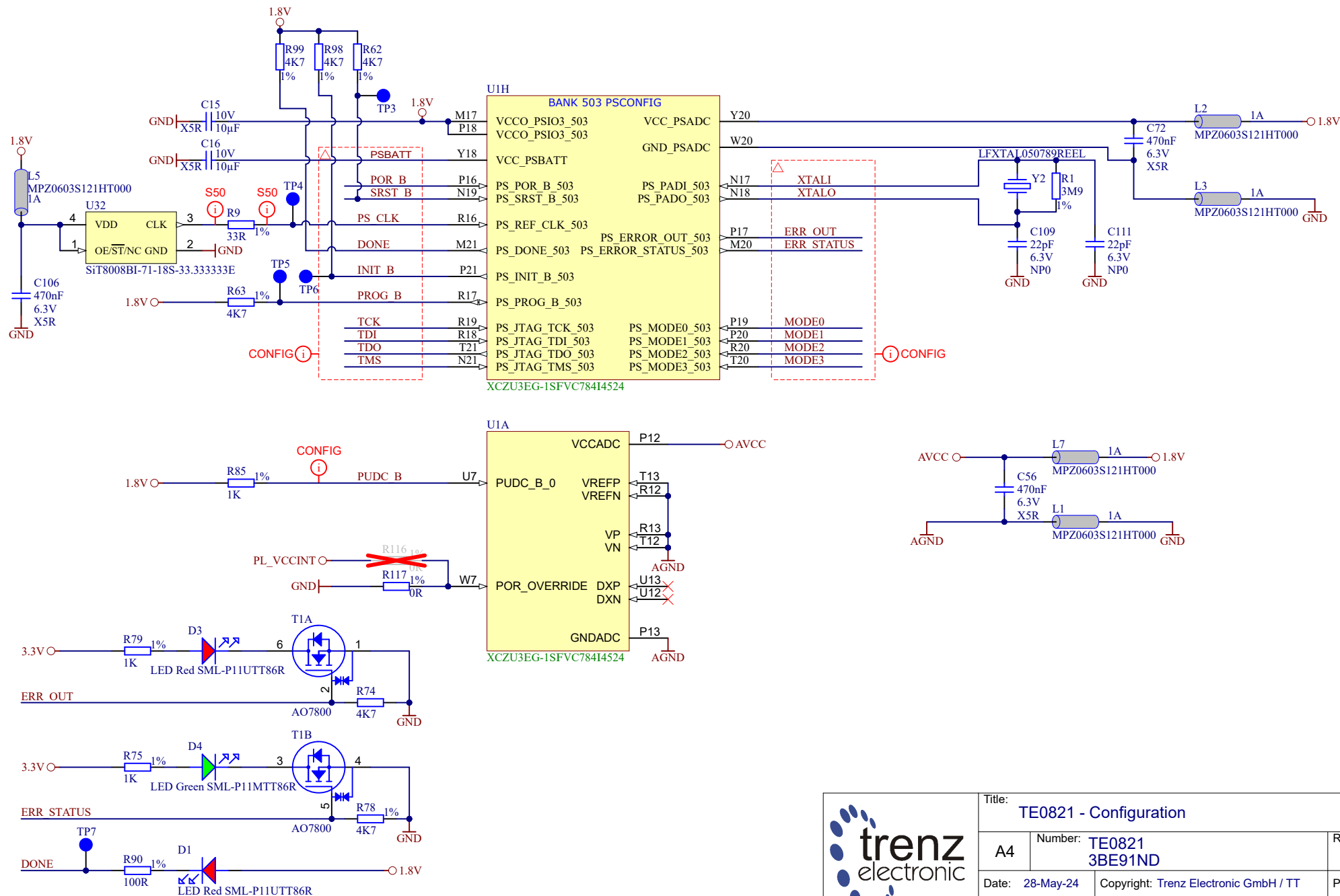
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Title: TE0821 - Configuration		
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Date: 28-May-24	Copyright: Trenz Electronic GmbH / TT	Page 8 of 25
Filename: CONFIG.SchDoc		

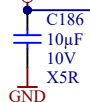
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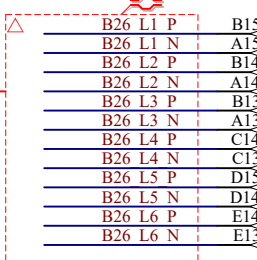
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VCCO_HD25_26



U1C

BANK 26 HD (ZU4/5 BANK 46 HD)

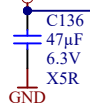
VCCO_26
VCCO_26

IO_L1P_AD11P_26
IO_L1N_AD11N_26
IO_L2P_AD10P_26
IO_L2N_AD10N_26
IO_L3P_AD9P_26
IO_L3N_AD9N_26
IO_L4P_AD8P_26
IO_L4N_AD8N_26
IO_L5P_HDGC_AD7P_26
IO_L5N_HDGC_AD7N_26
IO_L6P_HDGC_AD6P_26
IO_L6N_HDGC_AD6N_26

IO_L7P_HDGC_AD5P_26
IO_L7N_HDGC_AD5N_26
IO_L8P_HDGC_AD4P_26
IO_L8N_HDGC_AD4N_26
IO_L9P_AD3P_26
IO_L9N_AD3N_26
IO_L10P_AD2P_26
IO_L10N_AD2N_26
IO_L11P_AD1P_26
IO_L11N_AD1N_26
IO_L12P_AD0P_26
IO_L12N_AD0N_26

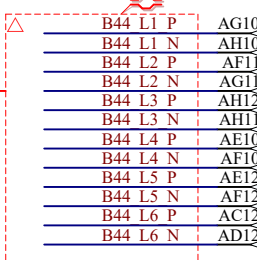
B26 L7 P
B26 L7 N
B26 L8 P
B26 L8 N
B26 L9 P
B26 L9 N
B26 L10 P
B26 L10 N
B26 L11 P
B26 L11 N
B26 L12 P
B26 L12 N

VCCO_HD24_44



U1B

BANK 44 HD (ZU4/5 BANK 43 HD)

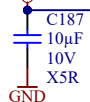
VCCO_44
VCCO_44

IO_L1P_AD11P_44
IO_L1N_AD11N_44
IO_L2P_AD10P_44
IO_L2N_AD10N_44
IO_L3P_AD9P_44
IO_L3N_AD9N_44
IO_L4P_AD8P_44
IO_L4N_AD8N_44
IO_L5P_HDGC_AD7P_44
IO_L5N_HDGC_AD7N_44
IO_L6P_HDGC_AD6P_44
IO_L6N_HDGC_AD6N_44

IO_L7P_HDGC_AD5P_44
IO_L7N_HDGC_AD5N_44
IO_L8P_HDGC_AD4P_44
IO_L8N_HDGC_AD4N_44
IO_L9P_AD3P_44
IO_L9N_AD3N_44
IO_L10P_AD2P_44
IO_L10N_AD2N_44
IO_L11P_AD1P_44
IO_L11N_AD1N_44
IO_L12P_AD0P_44
IO_L12N_AD0N_44

B44 L7 P
B44 L7 N
B44 L8 P
B44 L8 N
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B44 L10 N
B44 L11 P
B44 L11 N
B44 L12 P
B44 L12 N

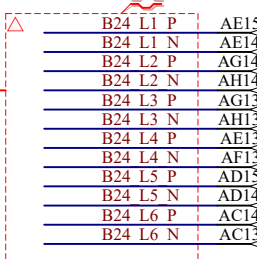
VCCO_HD24_44



U1B

XCZU3EG-1SFVC78414524

BANK 24 HD (ZU4/5 BANK 44 HD)

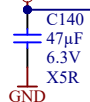
VCCO_24
VCCO_24

IO_L1P_AD15P_24
IO_L1N_AD15N_24
IO_L2P_AD14P_24
IO_L2N_AD14N_24
IO_L3P_AD13P_24
IO_L3N_AD13N_24
IO_L4P_AD12P_24
IO_L4N_AD12N_24
IO_L5P_HDGC_24
IO_L5N_HDGC_24
IO_L6P_HDGC_24
IO_L6N_HDGC_24

IO_L7P_HDGC_24
IO_L7N_HDGC_24
IO_L8P_HDGC_24
IO_L8N_HDGC_24
IO_L9P_AD11P_24
IO_L9N_AD11N_24
IO_L10P_AD10P_24
IO_L10N_AD10N_24
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IO_L11N_AD9N_24
IO_L12P_AD8P_24
IO_L12N_AD8N_24

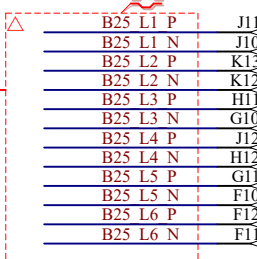
B24 L7 P
B24 L7 N
B24 L8 P
B24 L8 N
B24 L9 P
B24 L9 N
B24 L10 P
B24 L10 N
B24 L11 P
B24 L11 N
B24 L12 P
B24 L12 N

VCCO_HD25_26



U1C

BANK 25 HD (ZU4/5 BANK 45 HD)

VCCO_25
VCCO_25

IO_L1P_AD15P_25
IO_L1N_AD15N_25
IO_L2P_AD14P_25
IO_L2N_AD14N_25
IO_L3P_AD13P_25
IO_L3N_AD13N_25
IO_L4P_AD12P_25
IO_L4N_AD12N_25
IO_L5P_HDGC_25
IO_L5N_HDGC_25
IO_L6P_HDGC_25
IO_L6N_HDGC_25

IO_L7P_HDGC_25
IO_L7N_HDGC_25
IO_L8P_HDGC_25
IO_L8N_HDGC_25
IO_L9P_AD11P_25
IO_L9N_AD11N_25
IO_L10P_AD10P_25
IO_L10N_AD10N_25
IO_L11P_AD9P_25
IO_L11N_AD9N_25
IO_L12P_AD8P_25
IO_L12N_AD8N_25

B25 L7 P
B25 L7 N
B25 L8 P
B25 L8 N
B25 L9 P
B25 L9 N
B25 L10 P
B25 L10 N
B25 L11 P
B25 L11 N
B25 L12 P
B25 L12 N

XCZU3EG-1SFVC78414524



Title:

TE0821 - HD Banks

A4

Number:

TE0821
3BE91ND

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02

Date: 16-May-24

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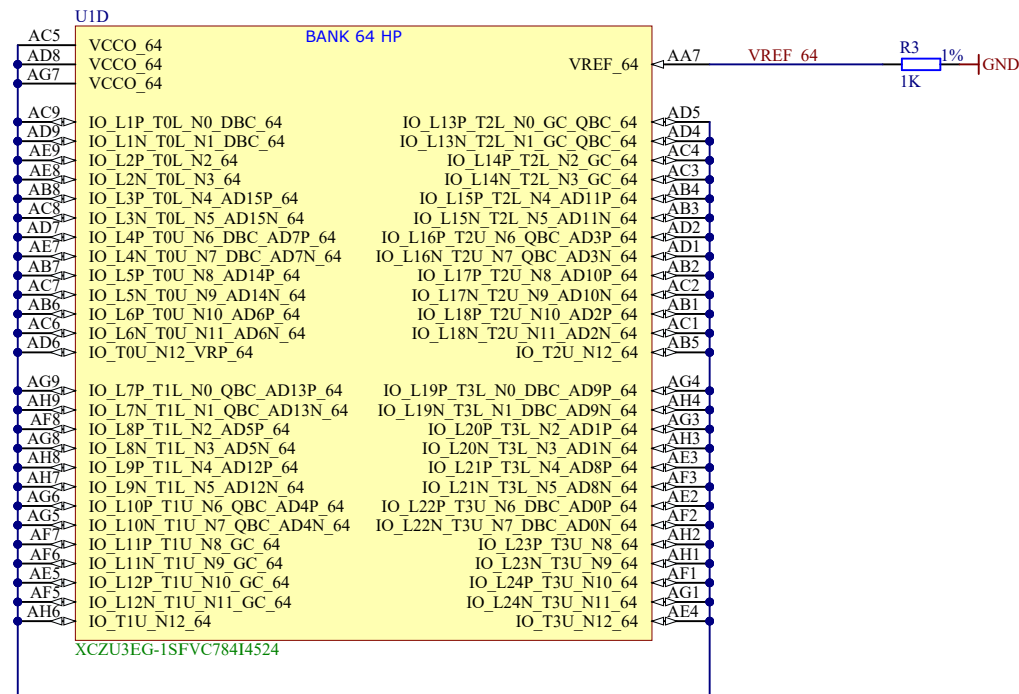
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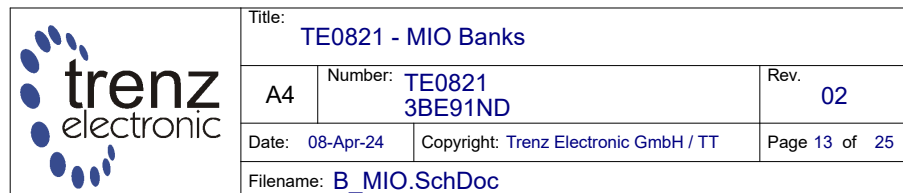
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Title: TE0821 - B64		
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Date: 08-Apr-24	Copyright: Trenz Electronic GmbH / TT	Page 10 of 25
Filename: B64.SchDoc		

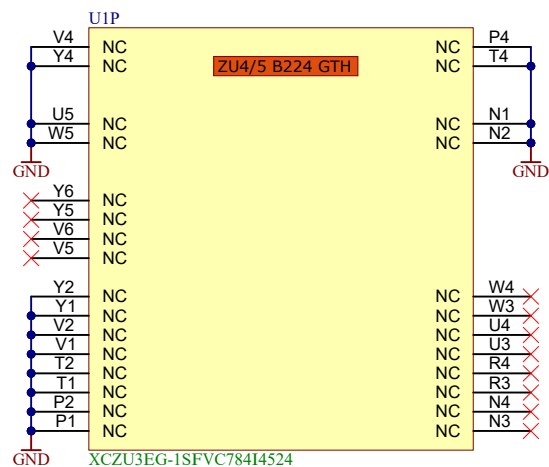
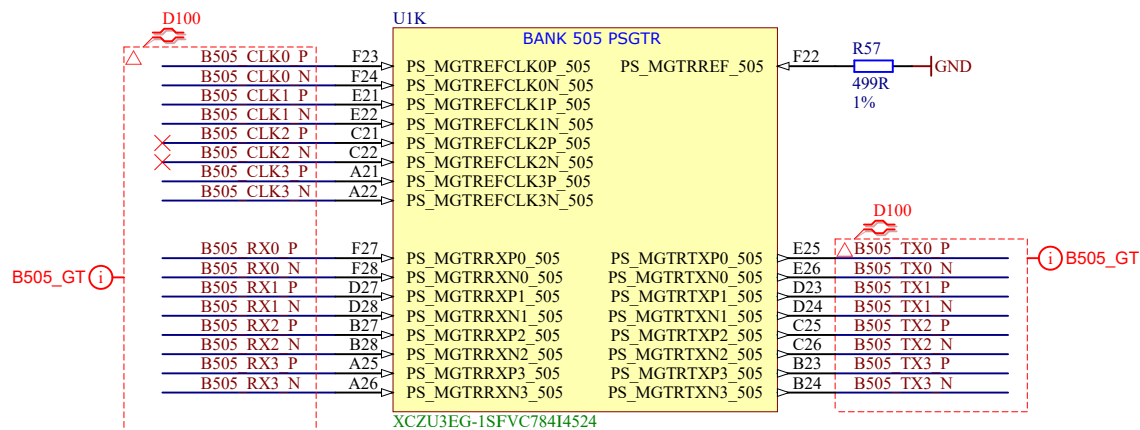


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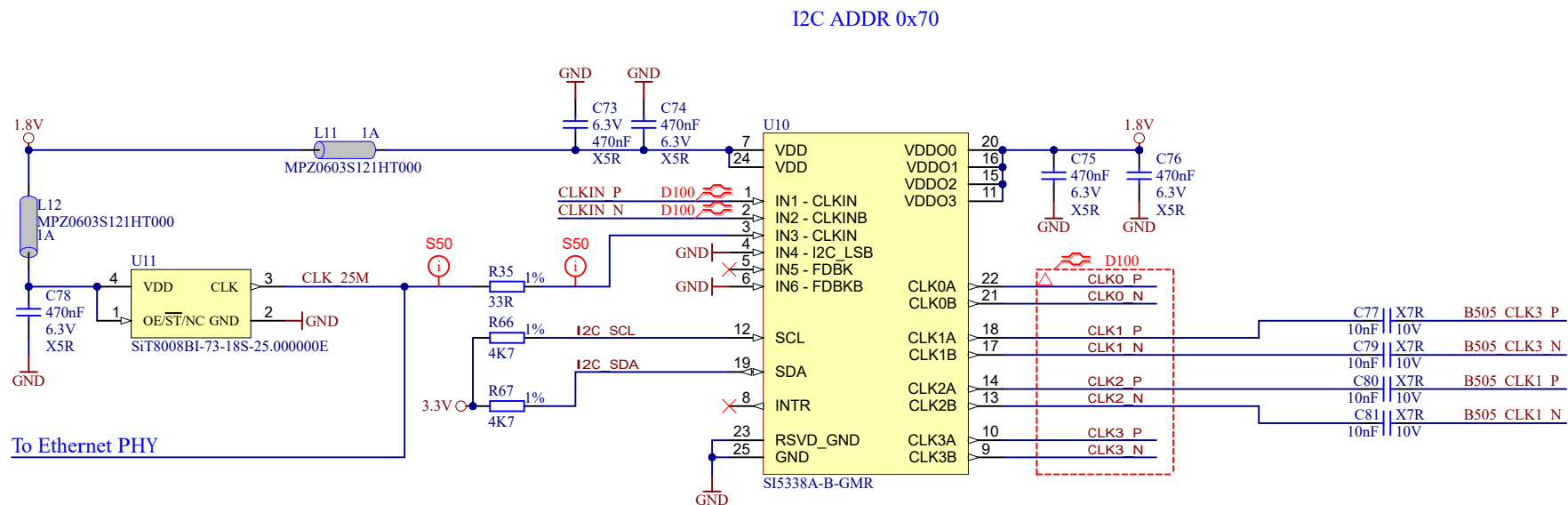
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		A4	Rev. 02
Date: 28-May-24		Copyright: Trenz Electronic GmbH / TT	
Filename: B_PS_GT.SchDoc		Page 15 of 25	

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		Title: TE0821 - CLK	
		A4 Number: TE0821 3BE91ND	Rev. 02
Date: 30-Sep-24		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 18 of 25	

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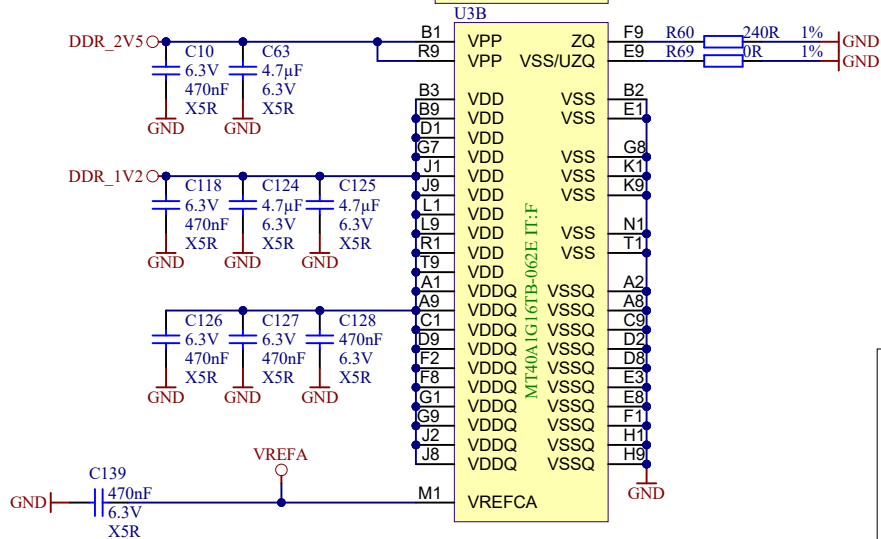
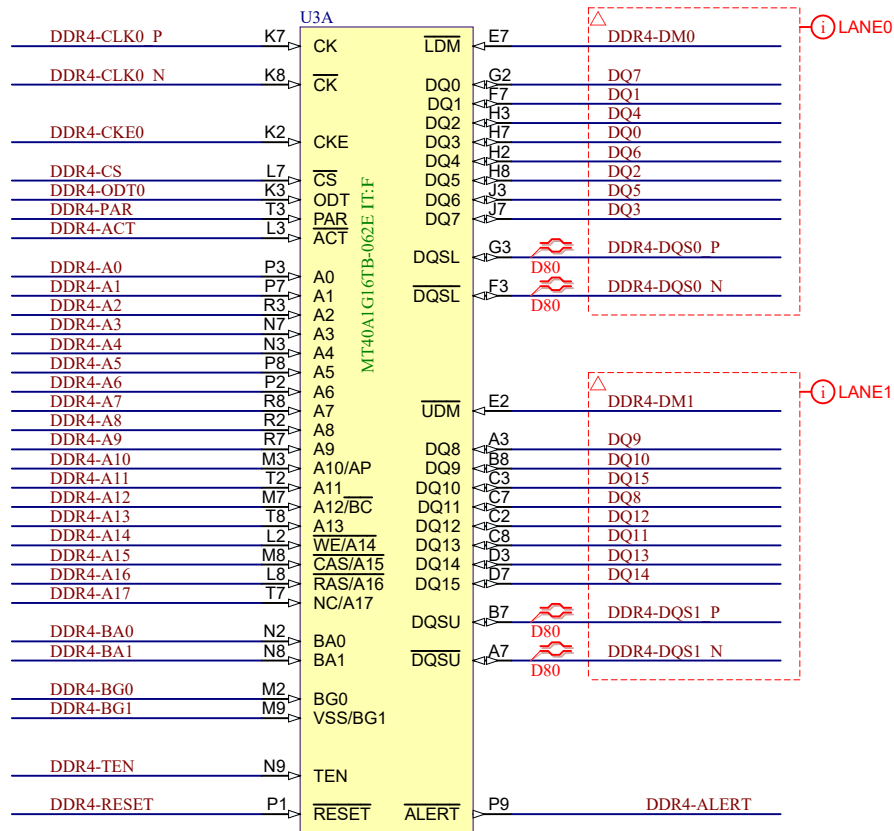
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Title: TE0821 - DDR4 RAM2		
A4	Number: TE0821 3BE91ND	Rev. 02
Date: 29-May-24	Copyright: Trenz Electronic GmbH / TT	Page 20 of 25
Filename: DDR4-RAM_2.SchDoc		

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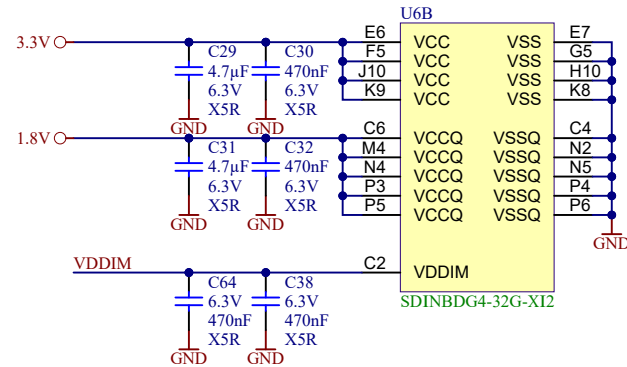
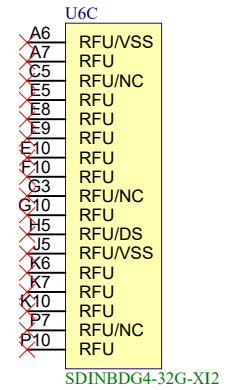
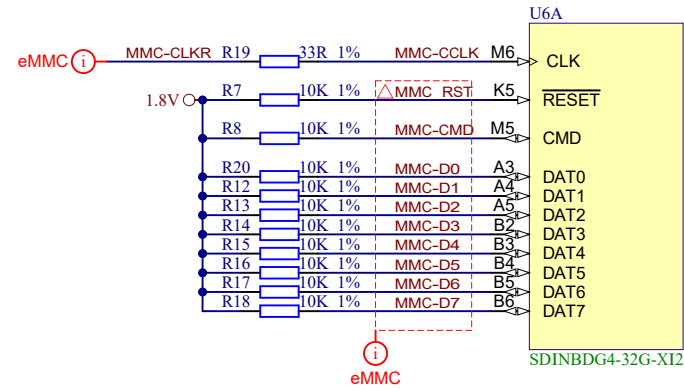
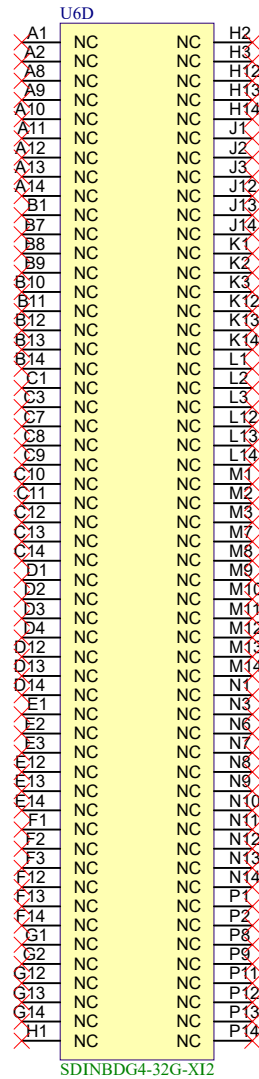
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Date: 15-Apr-24	Copyright: Trenz Electronic GmbH / TT	Page 21 of 25
Filename: eMMC.SchDoc		

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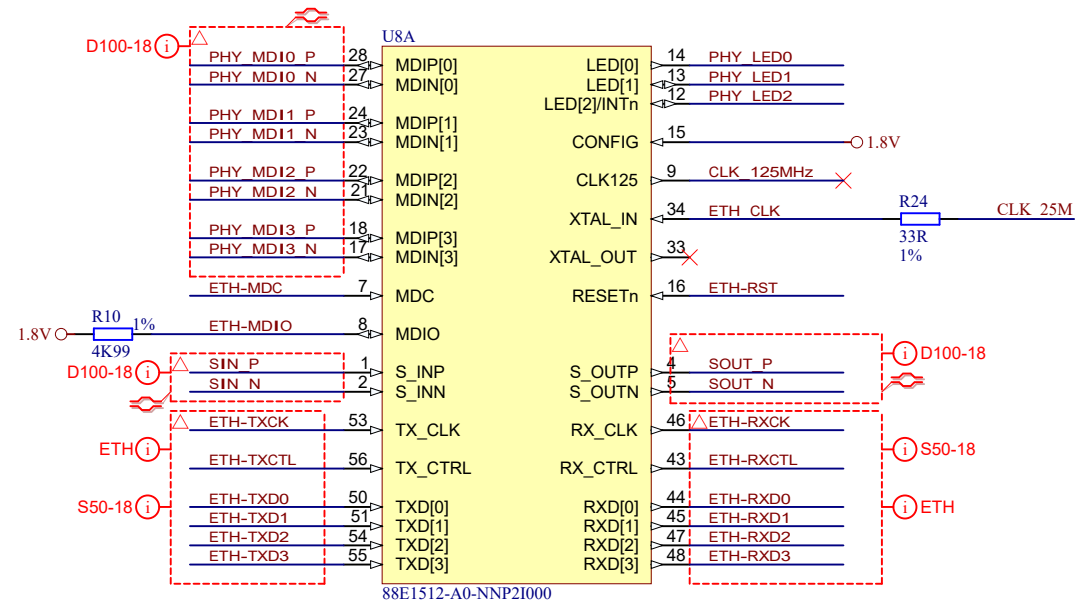
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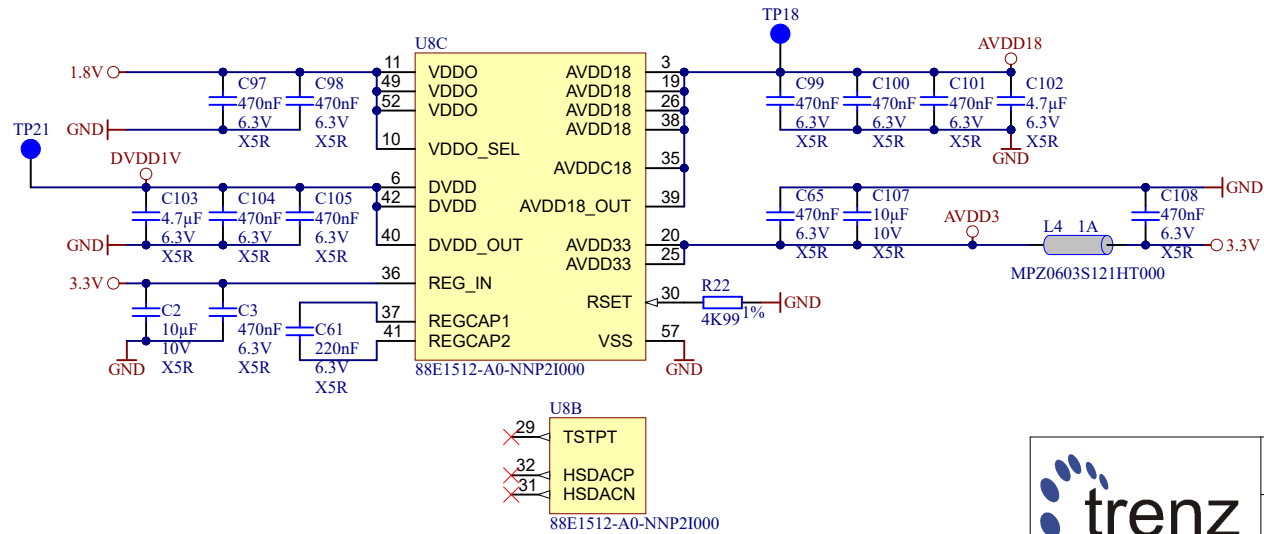
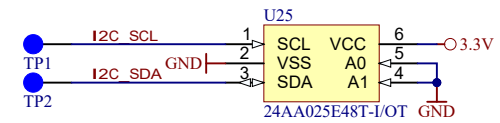
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I2C ADDR 0x50
EEPROM for MAC



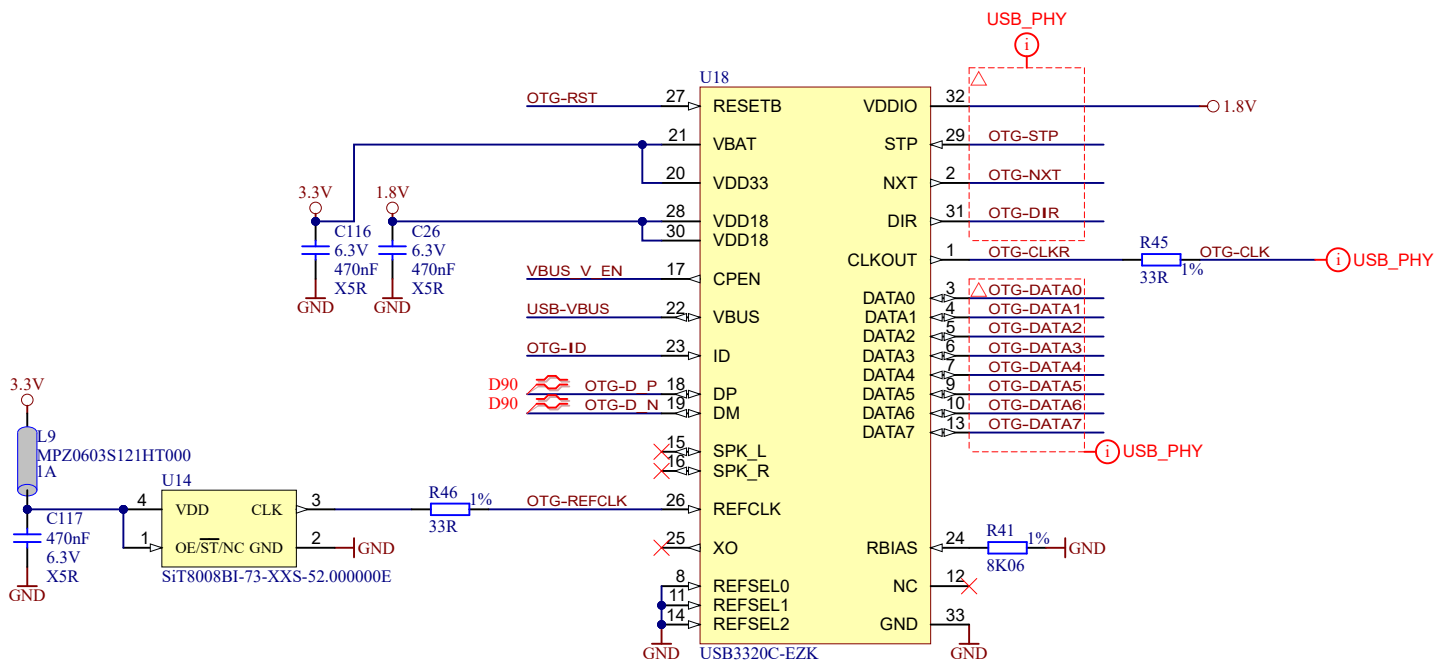
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A4	Number: TE0821 3BE91ND	Rev. 02
Date: 28-May-24	Copyright: 2015 Trenz Electronic GmbH	Page 22 of 25
Filename: ETH-PHY.SchDoc		

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		Title: TE0821 - USB PHY	
		Number: TE0821 3BE91ND	Rev. 02
Date: 16-May-24		Copyright: 2015 Trenz Electronic GmbH	
Filename: USB-PHY.SchDoc		Page 23 of 25	

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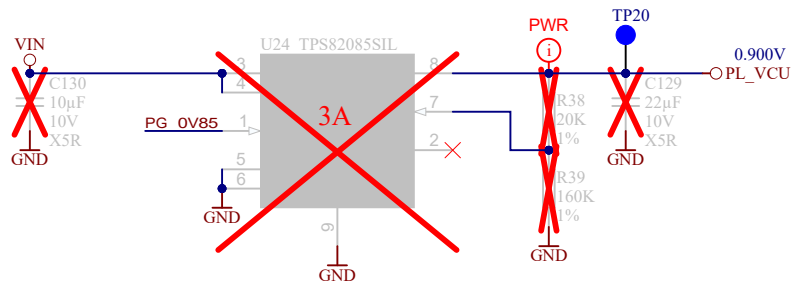
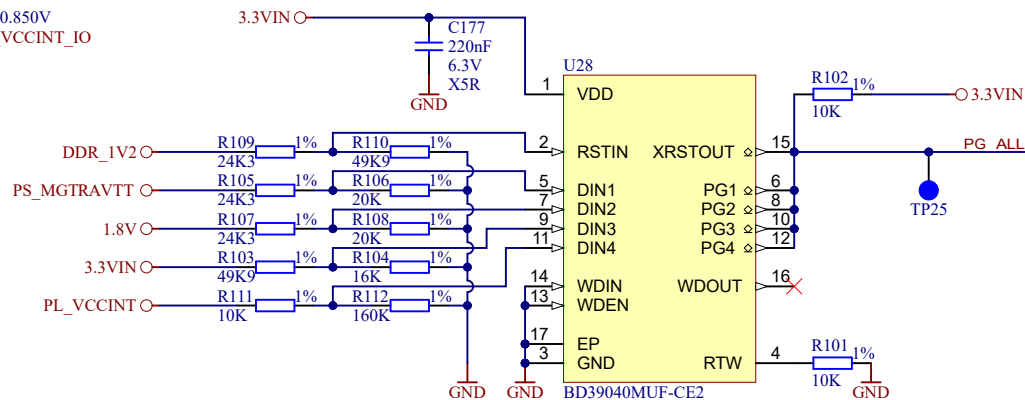
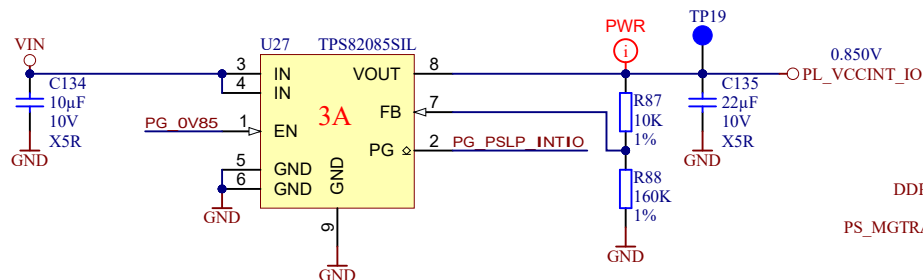
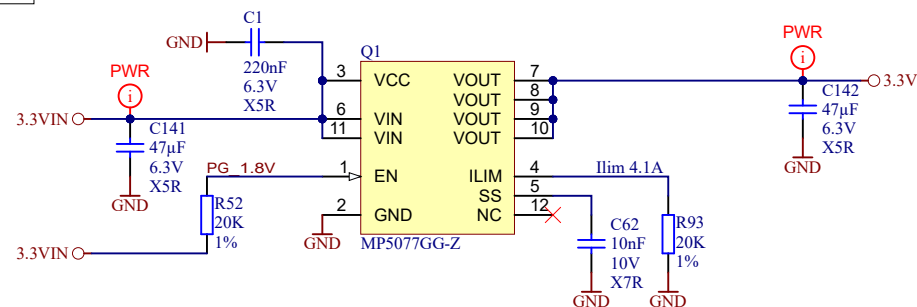
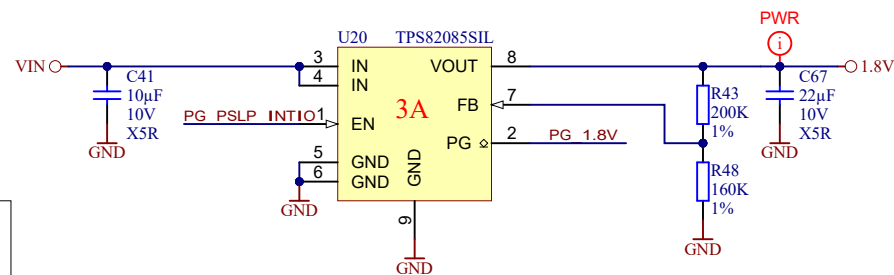
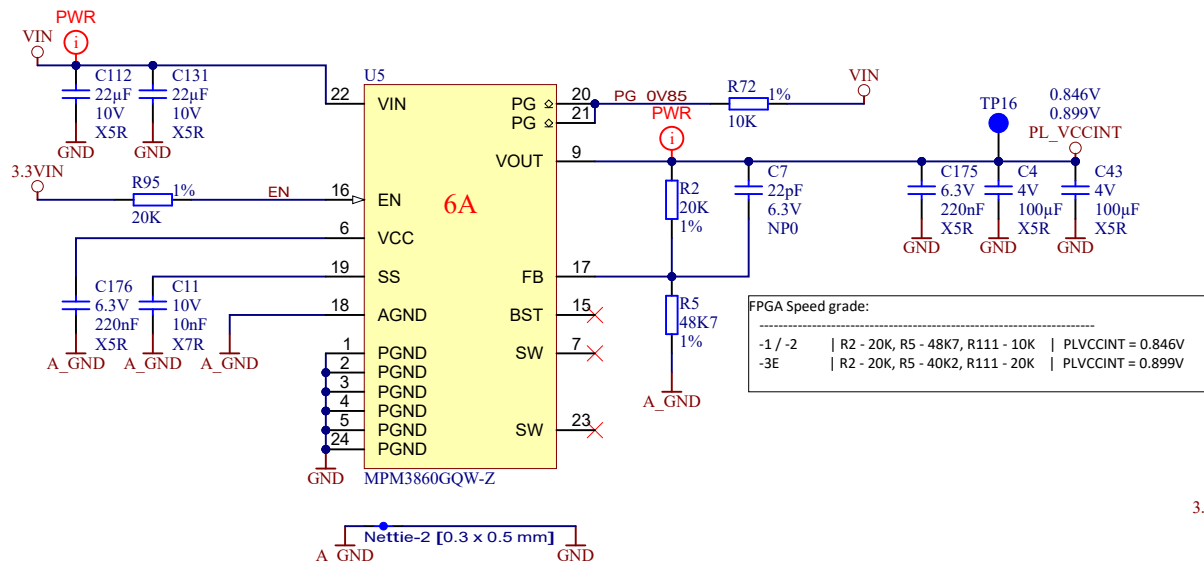
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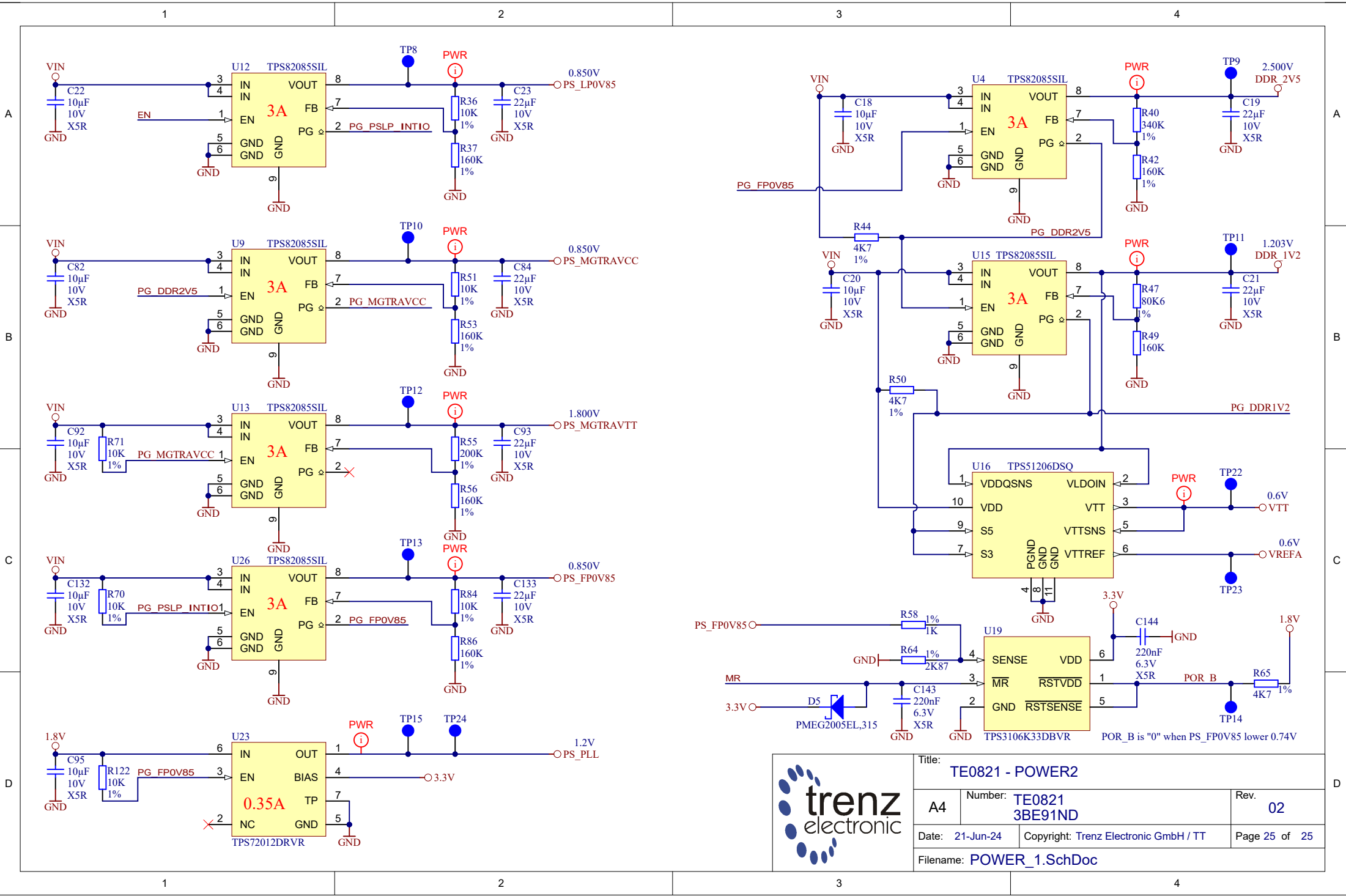
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