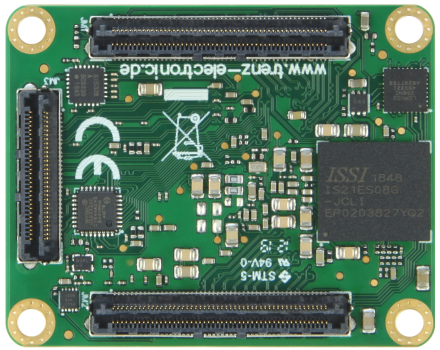

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0821 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0821 - Legal Notices		
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REV	Description	
-01	Initial revision	
-01A	1) R38 value was changed to 20K (was: 40K2) to set VCU 0.9V	VY
-01B	1) Updated Block diagram	VY
-02	1) Q1 was changed from TPS27081ADDCR to MP5077GG-Z 2) R82 was removed 3) C143 and C144 were added 4) Signal trace lengths were changed. PCB routing was improved 5) D5 was added 6) Pins N9 (TEN) of U2A and U3A were connected together 7) R100 was added 8) U5 was changed from EN6363QI to MPM3860GQW-Z 9) U28 was added 10) Net "PG_ALL" was connected to pin 5 of CPLD U21 11) T2A and R113 - R115 were added (R113 DNP by default) 12) Net "RST_EN" was connected to pin 27 of CPLD U21 13) Net EN was connected to pin 16 of U5 and pin 1 of U12 14) R116 and R117 were added (R116 DNP by default) 15) All unconnected pins for Bank64 U1D were connected together 16) TP17 , TP18 , TP21 , TP22 were added. Some testpoints were moved 17) C178 was added 18) R118 - R121 were added 19) C179 - C185 were added 20) C136 , C140 were changed from 22u to 47u 21) C186 , C187, C188, C189 were added 22) C15 , C16 were changed from 4.7u to 10u 23) C48 was changed from 16V to 10V, C45 was changed from 4.7u to 10u 24) C49 , C52 , C53 , C57 were changed from 4.7u to 10u 25) C2 was changed from 16V to 10V 26) C37 , C41 , C89 , C94 , C107 , C130 , C134 were changed from 16V 0603 to 10V 0402 27) FPGA speedgrade table was changed on page "POWER.SchDoc" 28) C24 , C25 , C96 , C110 were changed from 0805 to 0603 29) C19 , C21 , C23 , C67 , C84 , C93 , C129 , C133 , C135 were changed from 6.3V to 10V 30) C61 was changed from 16V 0402 to 6.3V 0201 31) Power Diagram page was added, System Overview was updated 32) Nets were renamed: "PS_AVCC" -> PS_MGTRAVCC , "PG_AVCC" -> PG_MGTRAVCC "OTG-RCLK" -> OTG-REFCLK , "PS_AVTT" -> PS_MGTRAVTT , "PG_DDR" -> PG_DDR1V2 33) Connection for pin "SENSE" of U19 was changed from net PS_LP0V85 to net PS_FP0V85 34) Net PG_0V85 was connected to pin 1 (EN) of U27 35) Net "PG_PS_LP" was renamed to PG_PSLP_INTIO and connected with pin 2 (PG) of U27 , pin 1 (EN) of U20 (instead net PG_0V85) 36) Net PG_FP0V85 was created and connected to pin 2 (PG) of U26 , pin 3 (EN) of U23 (instead net "PG_PS_LP") and pin 1 (EN) of U4 (instead net "PG_PS_LP") 37) Net PG_DDR2V5 was created, pin 2 (PG) of U4 was connected to pin 1 (EN) of U9 (instead net "PG_PS_LP") 38) R70 was unconnected from pin 1 of U9 and connected to pin 1 of U26 39) R122 was added 40) U11 was changed from SiT8008BI-73-XXS-25.000000E to SIT8008BI-73-18S-25.000000E 41) VDD for U10 and U11 was changed from 3.3V to 1.8V	MT

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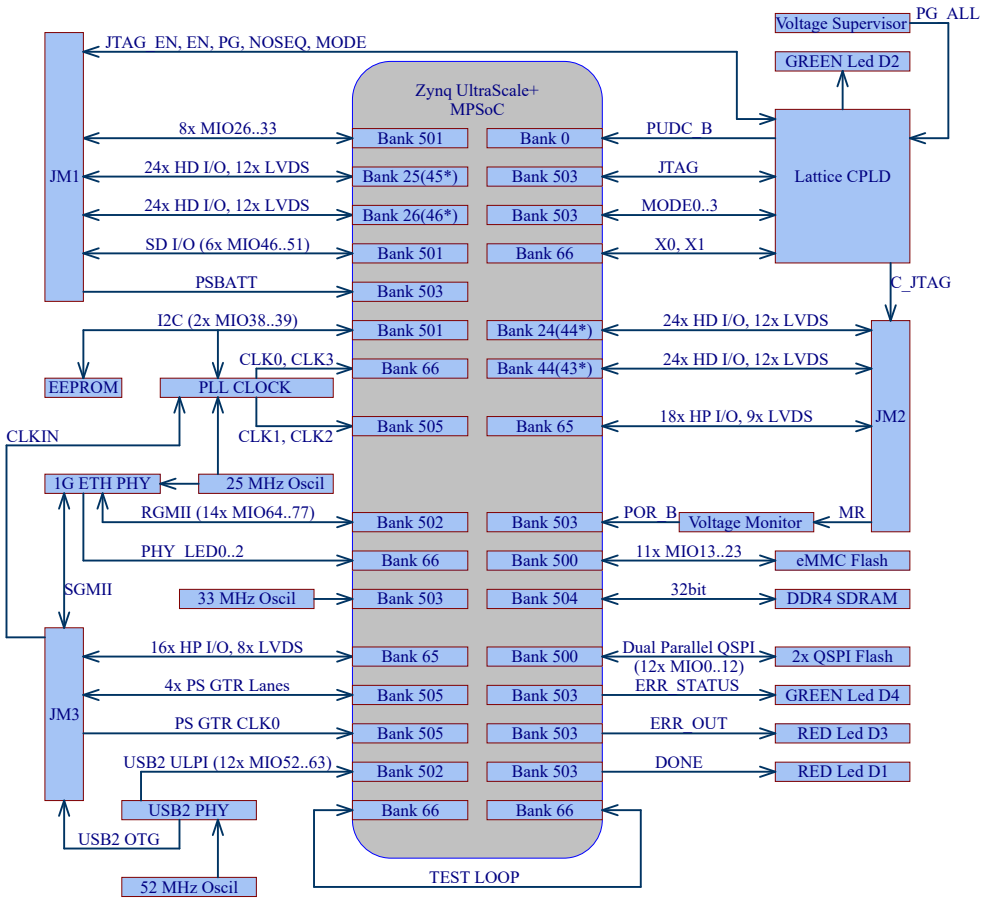

*Bank in XCZU2/3 (XCZU4/5)

U_B64
B64.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_POWER
POWER.SchDoc

U_POWER_1
POWER_1.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

Table of I2C devices and addresses

Designator	I2C Address	Description
U25	0x50	I2C MAC EEPROM
U10	0x70	QUAD CLOCK GEN

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Title: TE0821 - System Overview		
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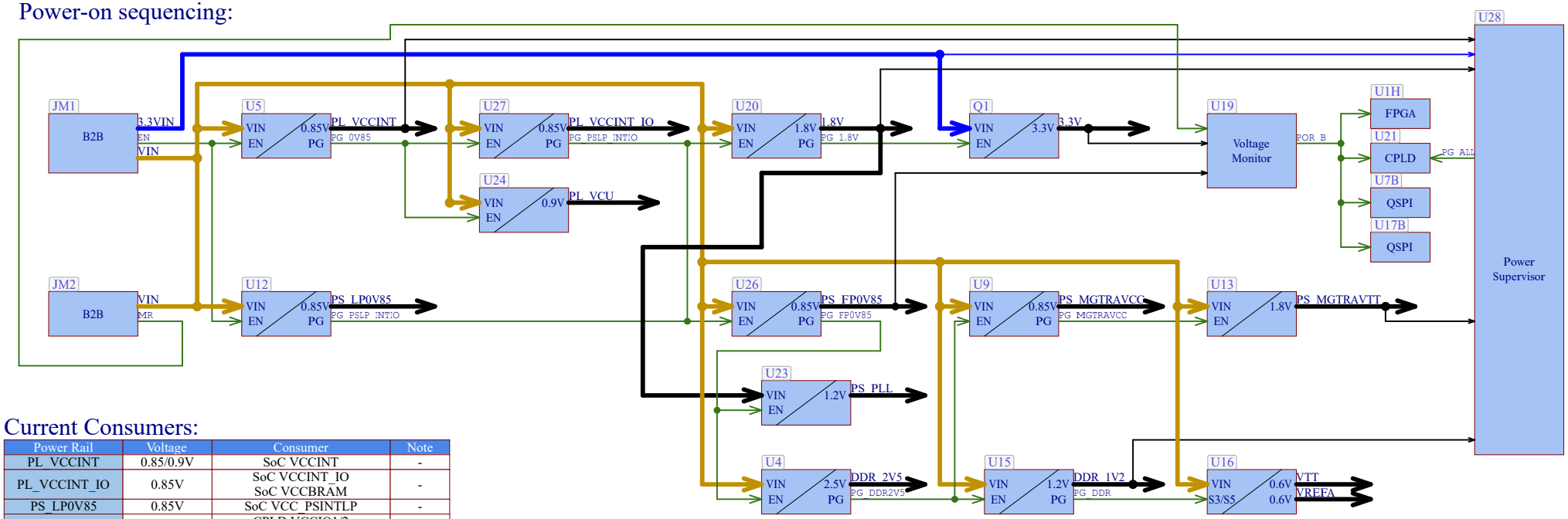
Power-on sequencing:



Current Consumers:

Power Rail	Voltage	Consumer	Note
PL_VCCINT	0.85/0.9V	SoC VCCINT	-
PL_VCCINT_IO	0.85V	SoC VCCINT_IO SoC VCCBRAM	-
PS_LP0V85	0.85V	SoC VCC_PSINTLP	-
1.8V	1.8V	CPLD VCCIO1/2 B2B JM1 SoC VCCO_66 QSPI FLASH QUAD CLK VDDO SoC VCCO_PS_503 eMMC VCCQ ETH PHY VDDO SoC VCCPSDDR_PLL USB PHY VDD18 SoC VCC_AUX SoC VCC_AUX_IO SoC VCC_PS_AUX	-
PL_VCU	0.9V	SoC VCCINT_VCU	-
PS_AVCC	0.85V	SoC PS_MGTRAVCC	-
PS_FP0V85	0.85V	SoC VCC_PS_INTFP_DDR SoC VCC_PS_INTFP	-
PS_PLL	1.2V	SoC VCC_PSPLL	-
DDR_2V5	2.5V	DDR VPP	-
3.3V	3.3V	B2B JM2 SoC VCCO_PSIO1_501 QUAD CLK VDD eMMC VCC EEPROM VCC CLK GEN 25M VDD USB PHY VDD33/VBAT CLK GEN 52M VDD	-
PS_AVTT	1.8V	SoC PS_MGTRAVTT	-
DDR_1V2	1.2V	DDR VDD/VDDQ SoC VCCO_PSDDR_504	-
VREFA	0.6V	DDR VREFCA	-

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V-5.7V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
	OUT			Power for JTAG	
PSBATT	IN	1.2 - 1.5V	+/-3%	SoC Vbatt	-
VCCO_65	IN	1.0 - 1.8V	+/-3%	IO Bank65	-
VCCO_HD25_26	IN	1.2 - 3.3V	+/-3%	IO Banks 25/26	-
VCCO_HD24_44	IN	1.2 - 3.3V	+/-3%	IO Banks 24/44	
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-

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Title: TE0821 - Power Diagram

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Serial

Serial

Serialnumber 6,3 x 6.3mm

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

UKCA

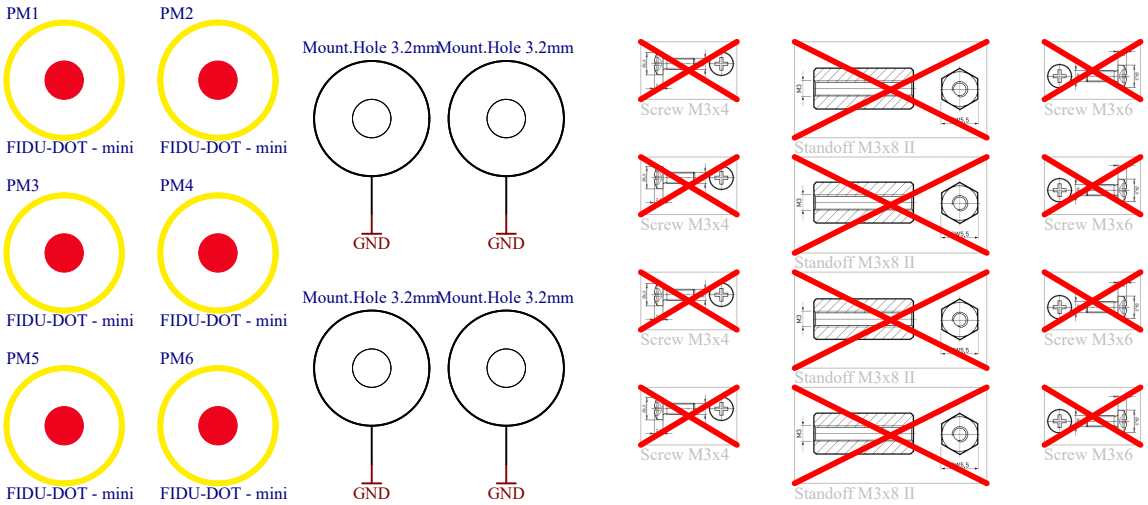
UKCA Logo on Top Overlay

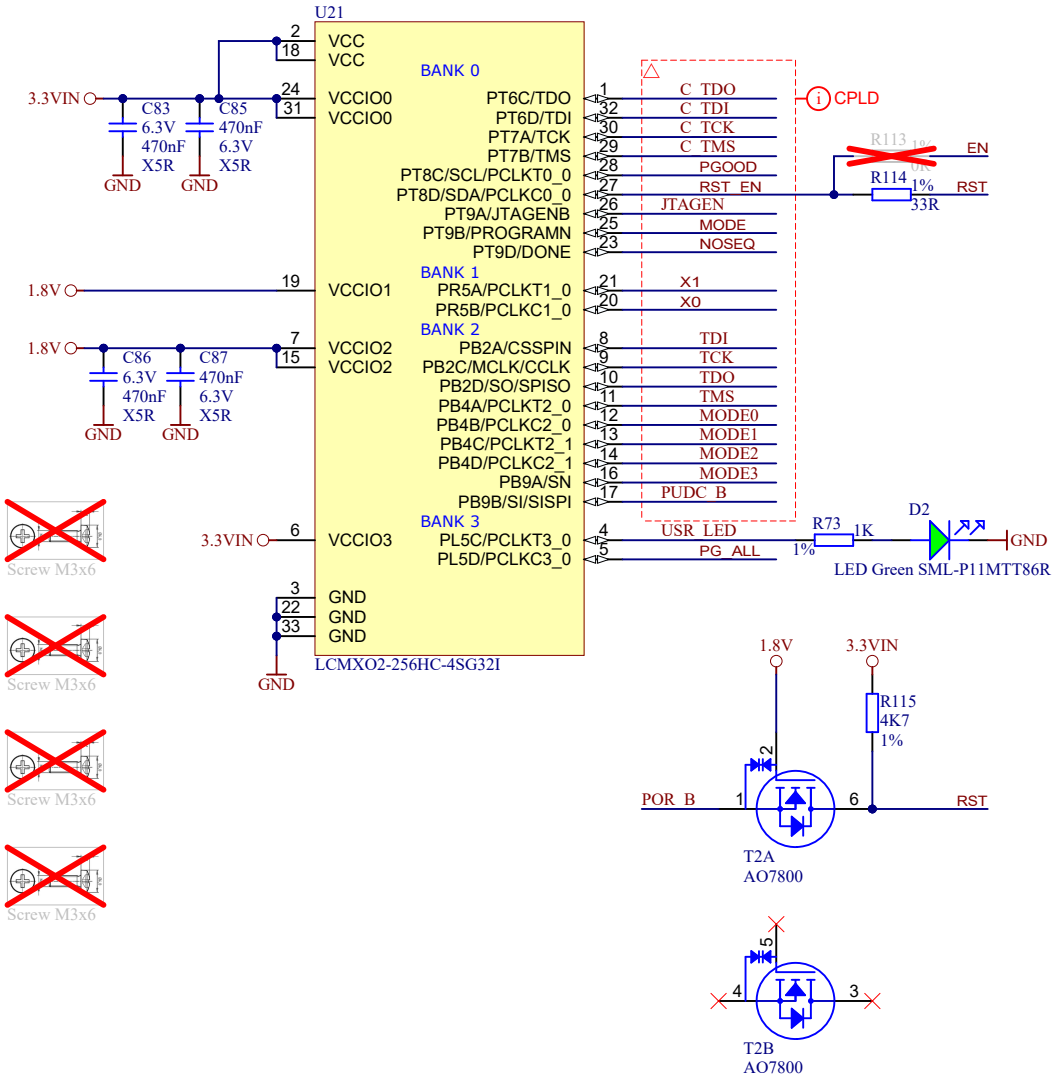
UKCA-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY





Special notes:

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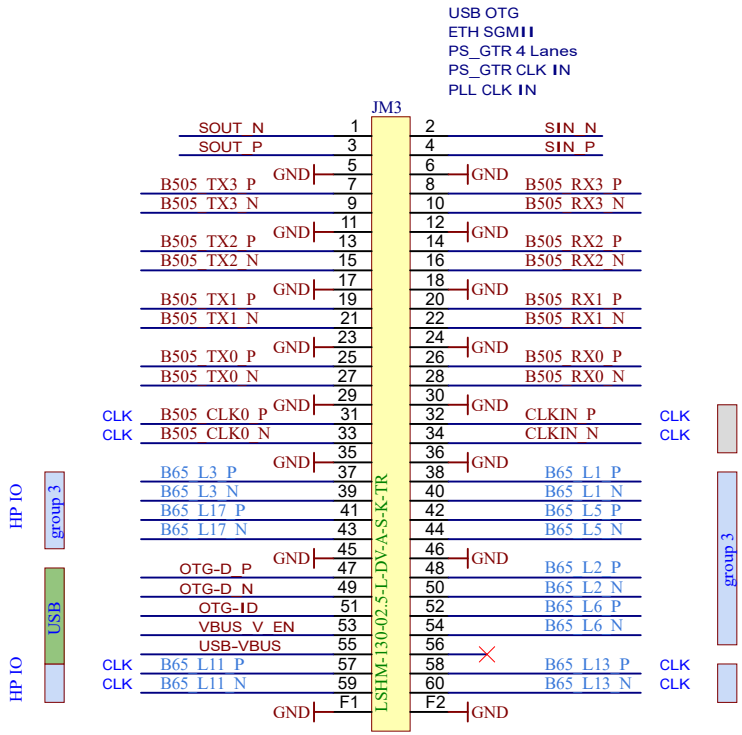
Filename: B2B-Connectors.SchDoc			



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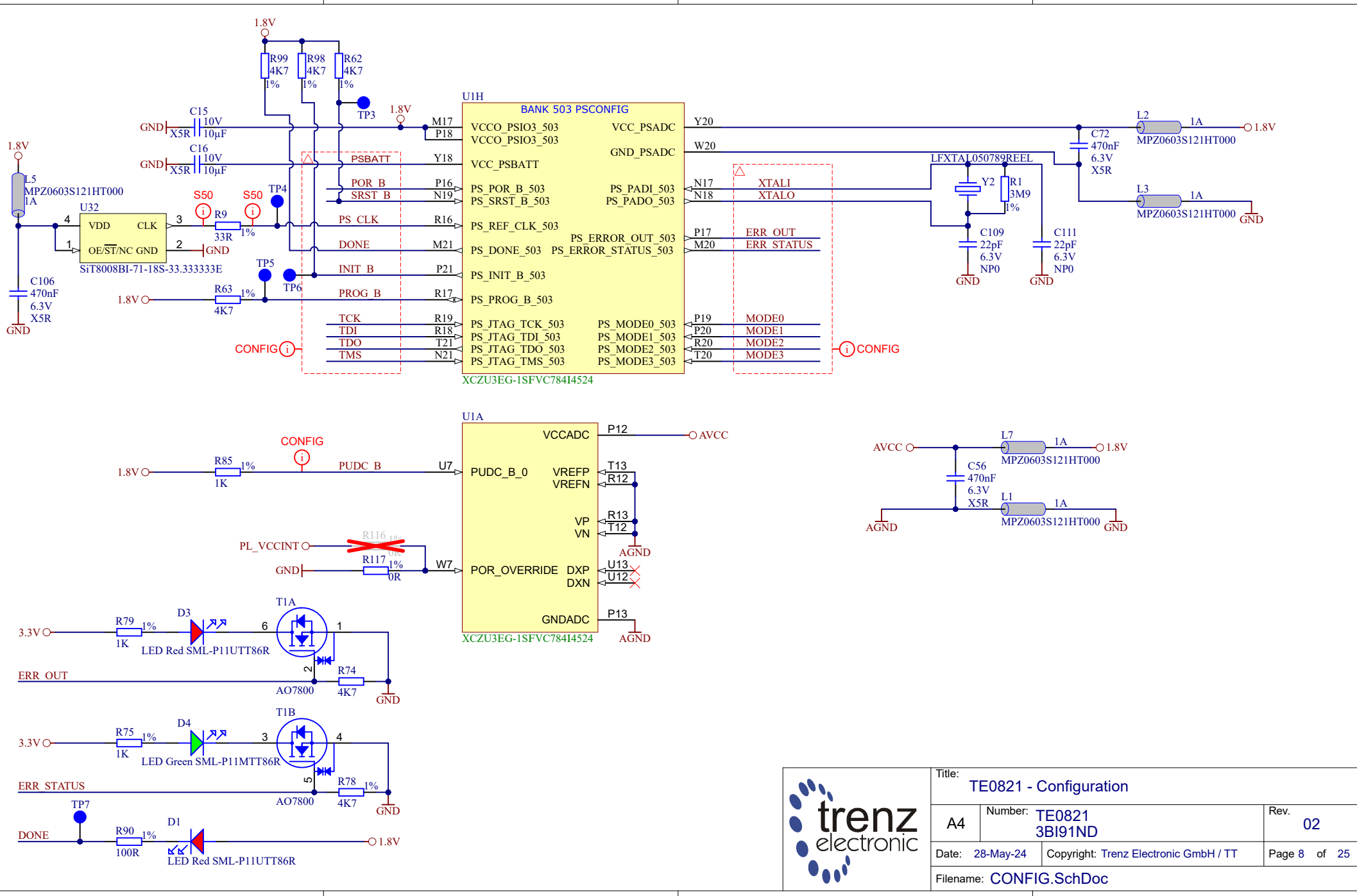
Filename: B2B-Connectors_2.SchDoc			



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Title: TE0821 - Configuration			
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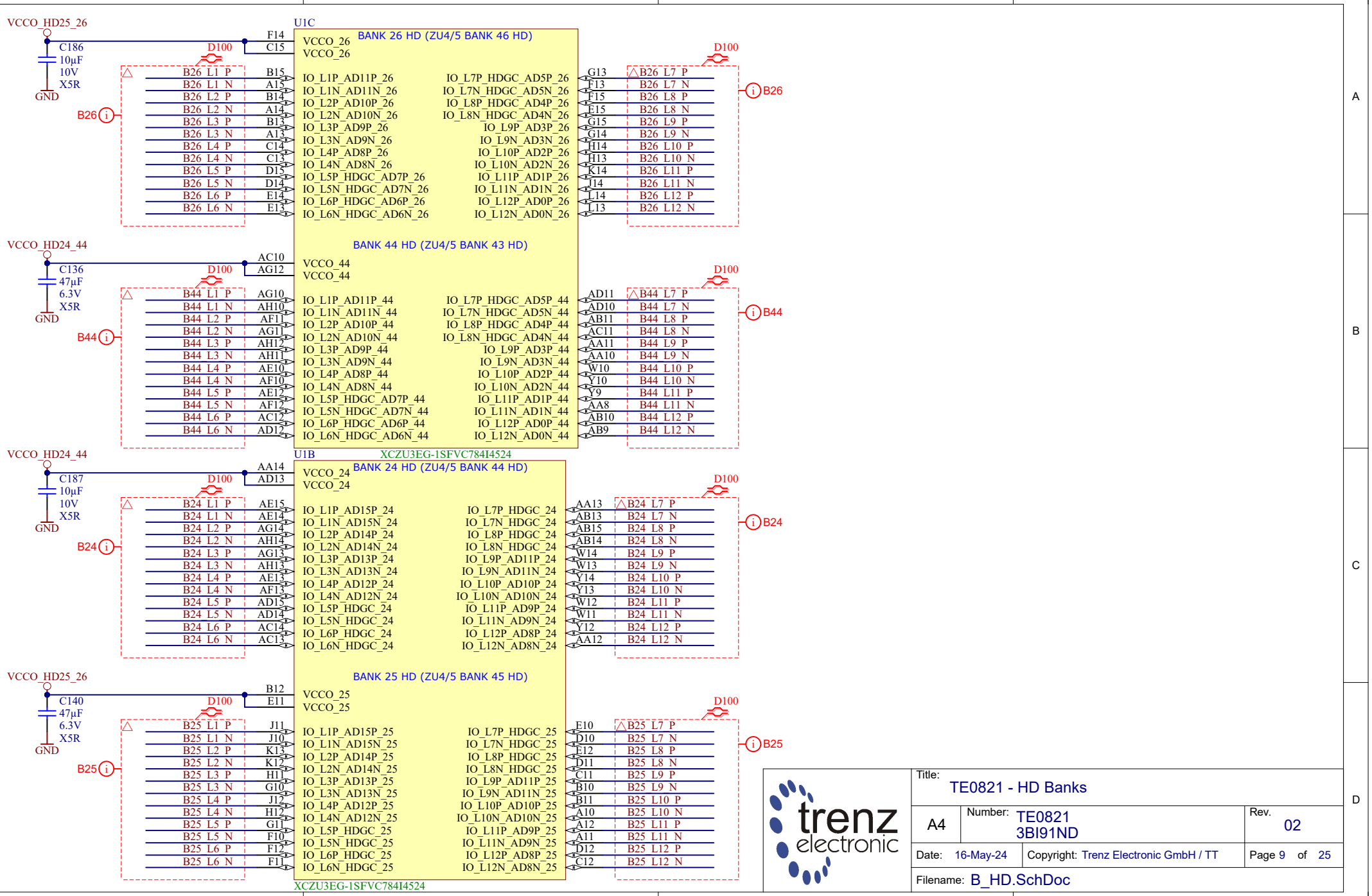
Filename: CONFIG.SchDoc			


U1C
BANK 26 HD (ZU4/5 BANK 46 HD)
VCCO_HD25_26
C186
10µF
10V
X5R
GND
B26
D100
F14
C15
VCCO_26
VCCO_26
IO_L1P_AD11P_26
IO_L1N_AD11N_26
IO_L2P_AD10P_26
IO_L2N_AD10N_26
IO_L3P_AD9P_26
IO_L3N_AD9N_26
IO_L4P_AD8P_26
IO_L4N_AD8N_26
IO_L5P_HDGC_AD7P_26
IO_L5N_HDGC_AD7N_26
IO_L6P_HDGC_AD6P_26
IO_L6N_HDGC_AD6N_26
IO_L7P_HDGC_AD5P_26
IO_L7N_HDGC_AD5N_26
IO_L8P_HDGC_AD4P_26
IO_L8N_HDGC_AD4N_26
IO_L9P_AD3P_26
IO_L9N_AD3N_26
IO_L10P_AD2P_26
IO_L10N_AD2N_26
IO_L11P_AD1P_26
IO_L11N_AD1N_26
IO_L12P_AD0P_26
IO_L12N_AD0N_26
B26_L1_P
B26_L1_N
B26_L2_P
B26_L2_N
B26_L3_P
B26_L3_N
B26_L4_P
B26_L4_N
B26_L5_P
B26_L5_N
B26_L6_P
B26_L6_N
B26_L7_P
B26_L7_N
B26_L8_P
B26_L8_N
B26_L9_P
B26_L9_N
B26_L10_P
B26_L10_N
B26_L11_P
B26_L11_N
B26_L12_P
B26_L12_N
BANK 44 HD (ZU4/5 BANK 43 HD)
VCCO_HD24_44
C136
47µF
6.3V
X5R
GND
B44
AC10
AG12
VCCO_44
VCCO_44
IO_L1P_AD11P_44
IO_L1N_AD11N_44
IO_L2P_AD10P_44
IO_L2N_AD10N_44
IO_L3P_AD9P_44
IO_L3N_AD9N_44
IO_L4P_AD8P_44
IO_L4N_AD8N_44
IO_L5P_HDGC_AD7P_44
IO_L5N_HDGC_AD7N_44
IO_L6P_HDGC_AD6P_44
IO_L6N_HDGC_AD6N_44
IO_L7P_HDGC_AD5P_44
IO_L7N_HDGC_AD5N_44
IO_L8P_HDGC_AD4P_44
IO_L8N_HDGC_AD4N_44
IO_L9P_AD3P_44
IO_L9N_AD3N_44
IO_L10P_AD2P_44
IO_L10N_AD2N_44
IO_L11P_AD1P_44
IO_L11N_AD1N_44
IO_L12P_AD0P_44
IO_L12N_AD0N_44
B44_L1_P
B44_L1_N
B44_L2_P
B44_L2_N
B44_L3_P
B44_L3_N
B44_L4_P
B44_L4_N
B44_L5_P
B44_L5_N
B44_L6_P
B44_L6_N
B44_L7_P
B44_L7_N
B44_L8_P
B44_L8_N
B44_L9_P
B44_L9_N
B44_L10_P
B44_L10_N
B44_L11_P
B44_L11_N
B44_L12_P
B44_L12_N
U1B
XCZU3EG-1SFVC784I4524
BANK 24 HD (ZU4/5 BANK 44 HD)
VCCO_HD24_44
C187
10µF
10V
X5R
GND
B24
AA14
AD13
VCCO_24
VCCO_24
IO_L1P_AD15P_24
IO_L1N_AD15N_24
IO_L2P_AD14P_24
IO_L2N_AD14N_24
IO_L3P_AD13P_24
IO_L3N_AD13N_24
IO_L4P_AD12P_24
IO_L4N_AD12N_24
IO_L5P_HDGC_24
IO_L5N_HDGC_24
IO_L6P_HDGC_24
IO_L6N_HDGC_24
IO_L7P_HDGC_24
IO_L7N_HDGC_24
IO_L8P_HDGC_24
IO_L8N_HDGC_24
IO_L9P_AD11P_24
IO_L9N_AD11N_24
IO_L10P_AD10P_24
IO_L10N_AD10N_24
IO_L11P_AD9P_24
IO_L11N_AD9N_24
IO_L12P_AD8P_24
IO_L12N_AD8N_24
B24_L1_P
B24_L1_N
B24_L2_P
B24_L2_N
B24_L3_P
B24_L3_N
B24_L4_P
B24_L4_N
B24_L5_P
B24_L5_N
B24_L6_P
B24_L6_N
B24_L7_P
B24_L7_N
B24_L8_P
B24_L8_N
B24_L9_P
B24_L9_N
B24_L10_P
B24_L10_N
B24_L11_P
B24_L11_N
B24_L12_P
B24_L12_N
BANK 25 HD (ZU4/5 BANK 45 HD)
VCCO_HD25_26
C140
47µF
6.3V
X5R
GND
B25
B12
E11
VCCO_25
VCCO_25
IO_L1P_AD15P_25
IO_L1N_AD15N_25
IO_L2P_AD14P_25
IO_L2N_AD14N_25
IO_L3P_AD13P_25
IO_L3N_AD13N_25
IO_L4P_AD12P_25
IO_L4N_AD12N_25
IO_L5P_HDGC_25
IO_L5N_HDGC_25
IO_L6P_HDGC_25
IO_L6N_HDGC_25
IO_L7P_HDGC_25
IO_L7N_HDGC_25
IO_L8P_HDGC_25
IO_L8N_HDGC_25
IO_L9P_AD11P_25
IO_L9N_AD11N_25
IO_L10P_AD10P_25
IO_L10N_AD10N_25
IO_L11P_AD9P_25
IO_L11N_AD9N_25
IO_L12P_AD8P_25
IO_L12N_AD8N_25
B25_L1_P
B25_L1_N
B25_L2_P
B25_L2_N
B25_L3_P
B25_L3_N
B25_L4_P
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Title: TE0821 - HD Banks
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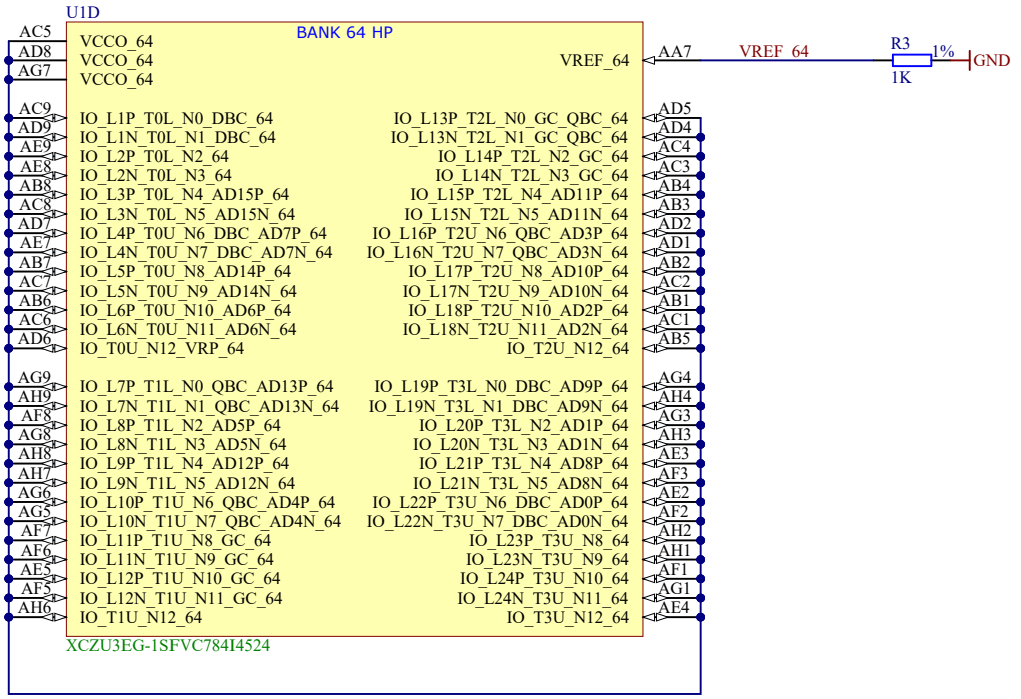
Filename: B_HD.SchDoc



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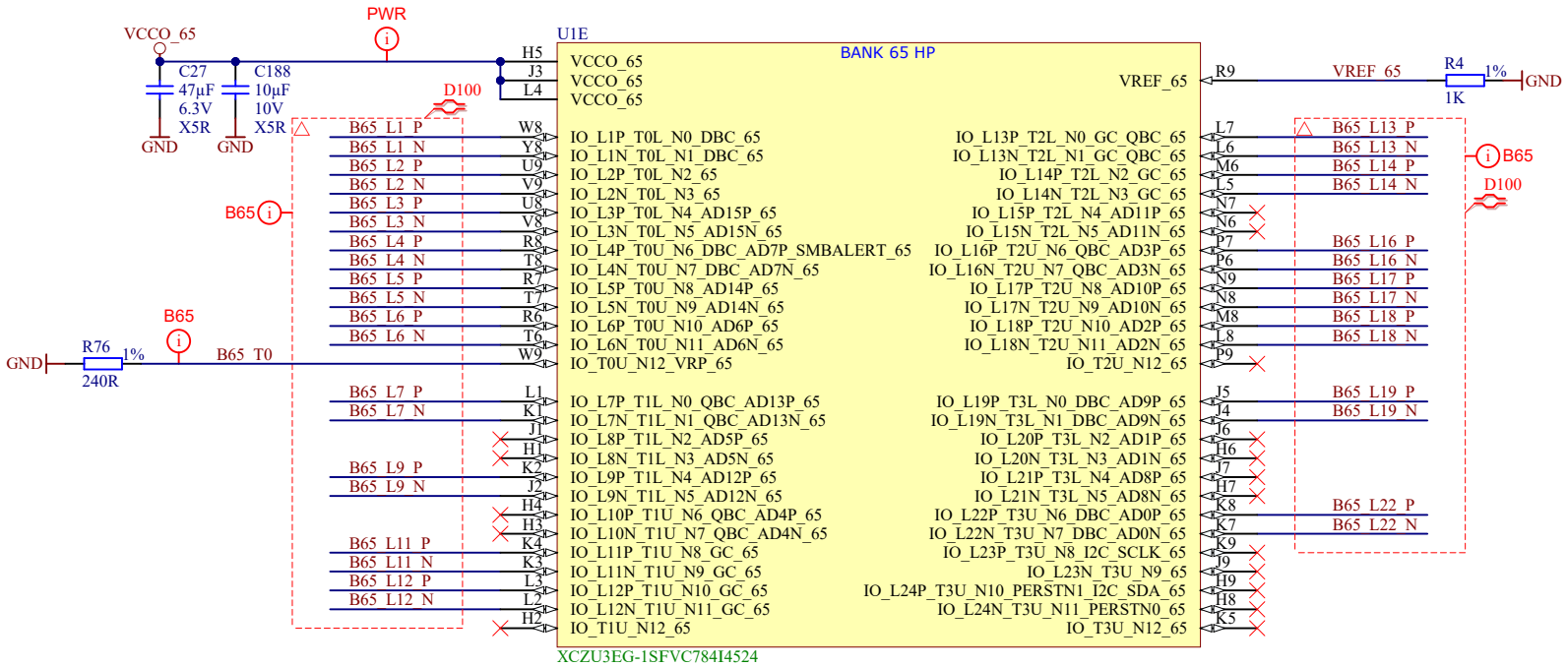

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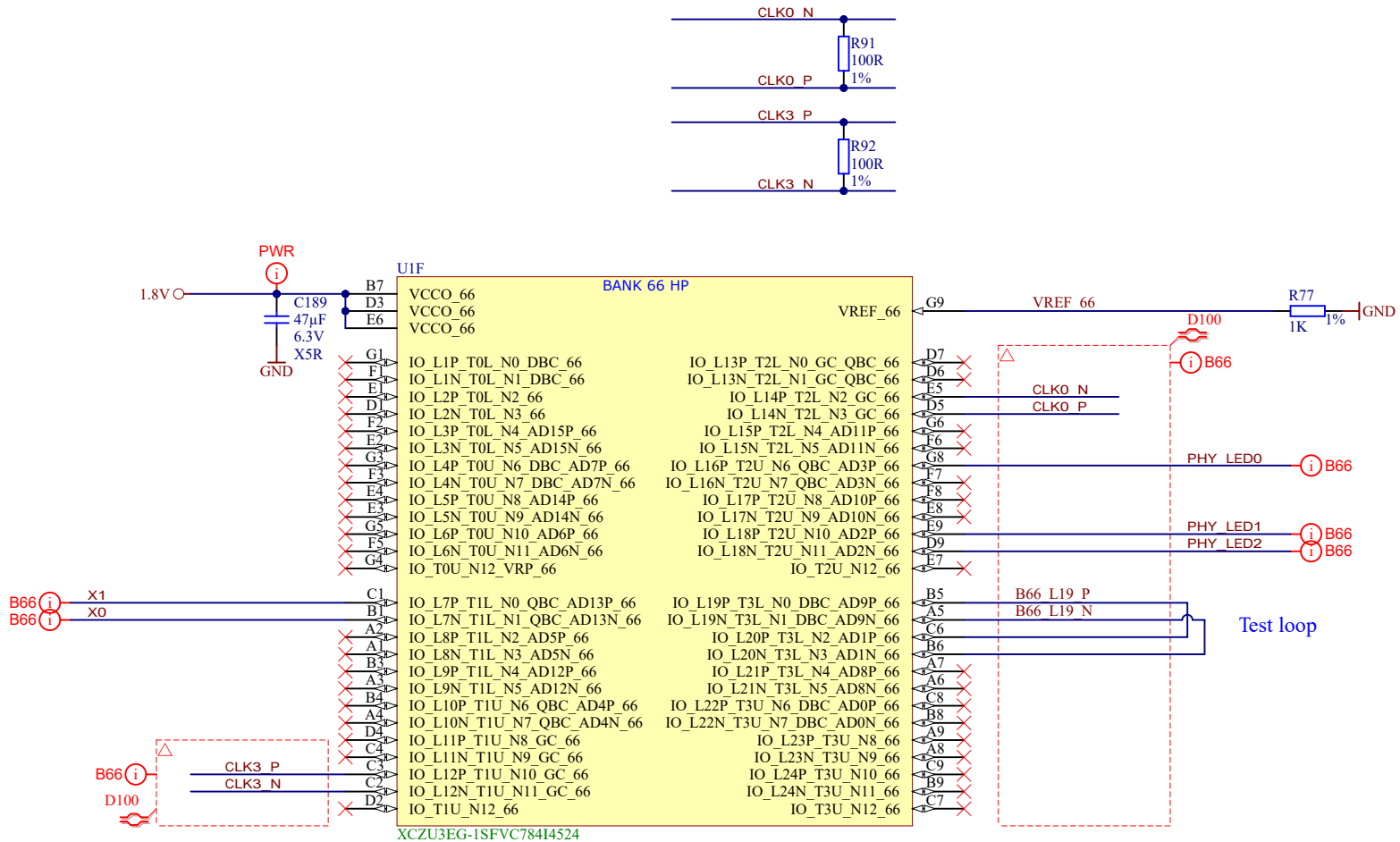
Filename: B65.SchDoc			



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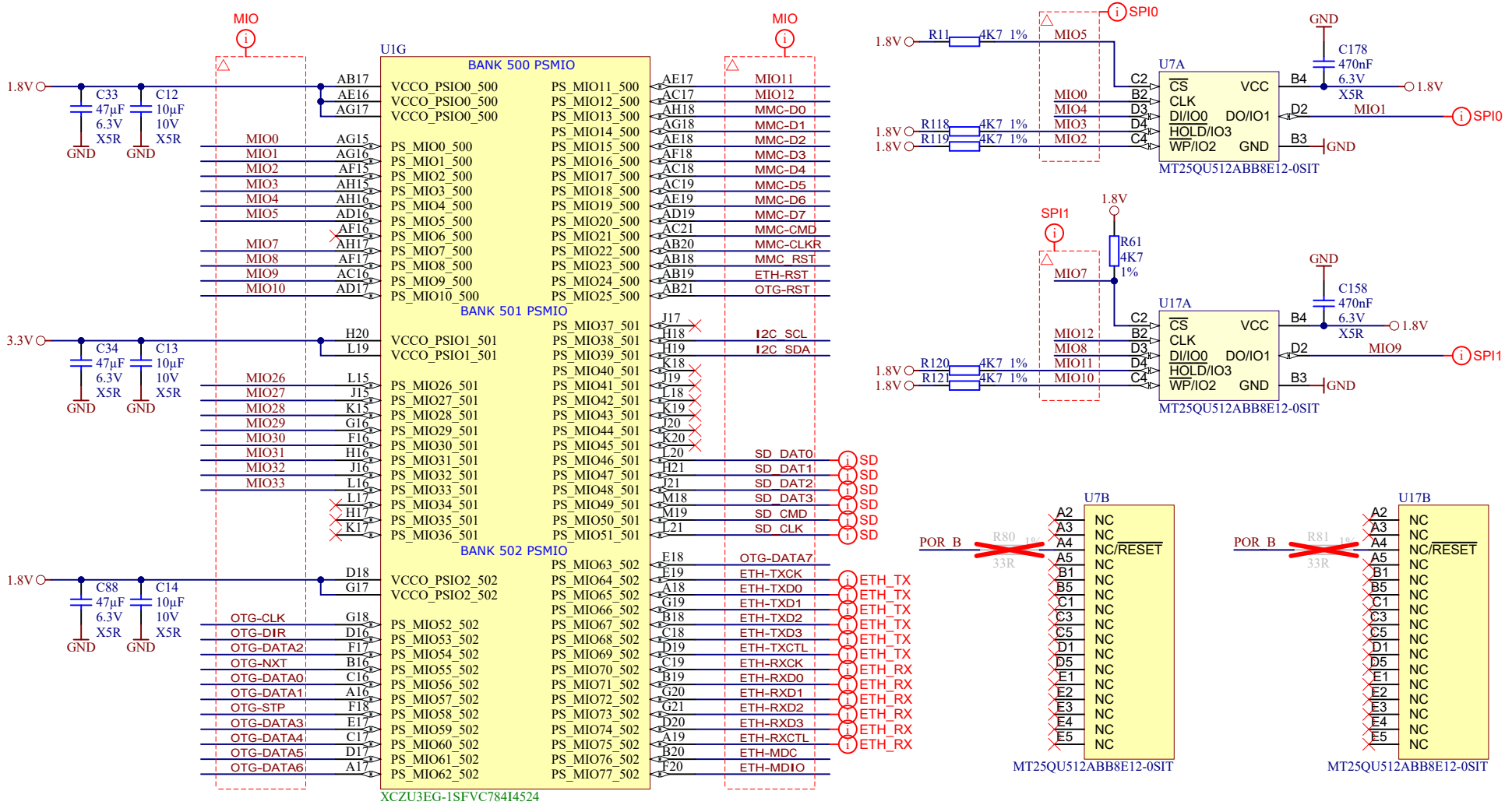

Title: TE0821 - MIO Banks			
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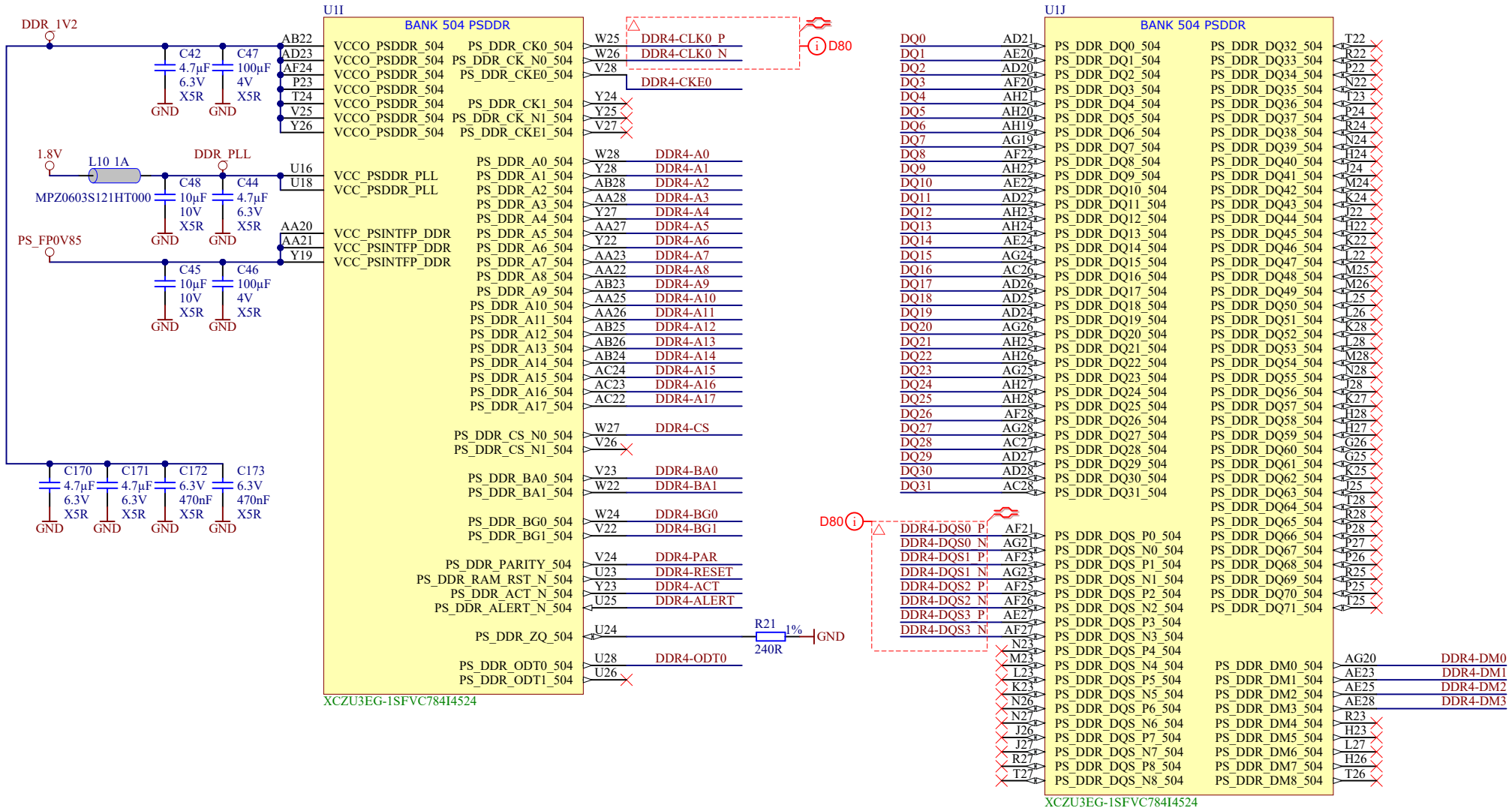
Filename: B_MIO.SchDoc			



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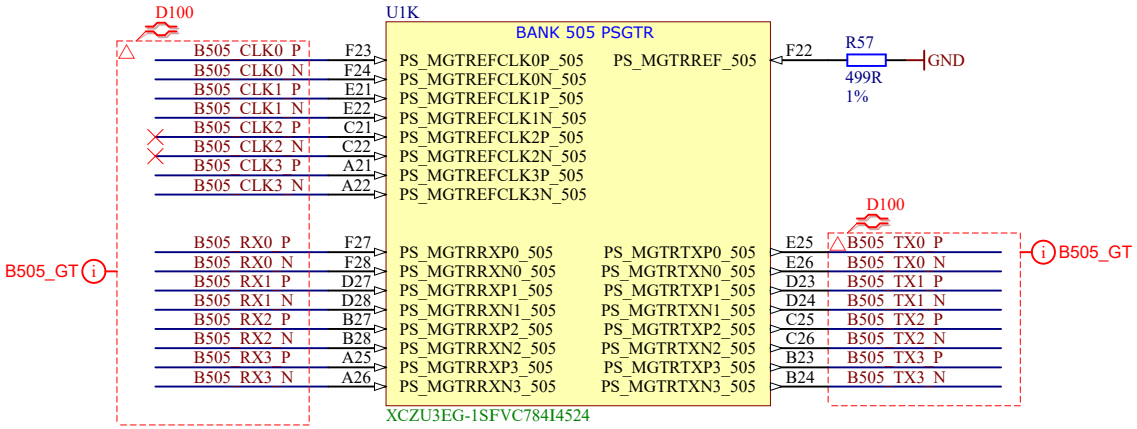
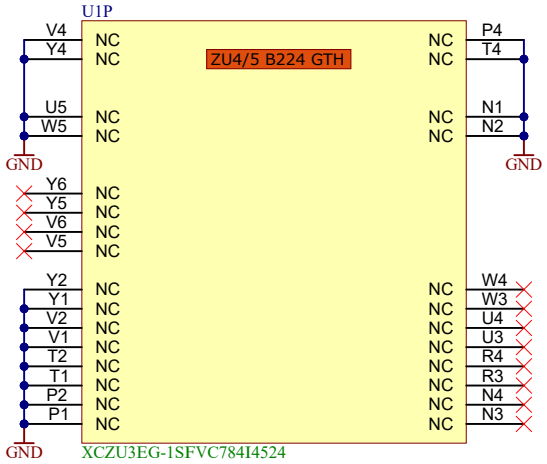
Filename: PS_DDR.SchDoc			





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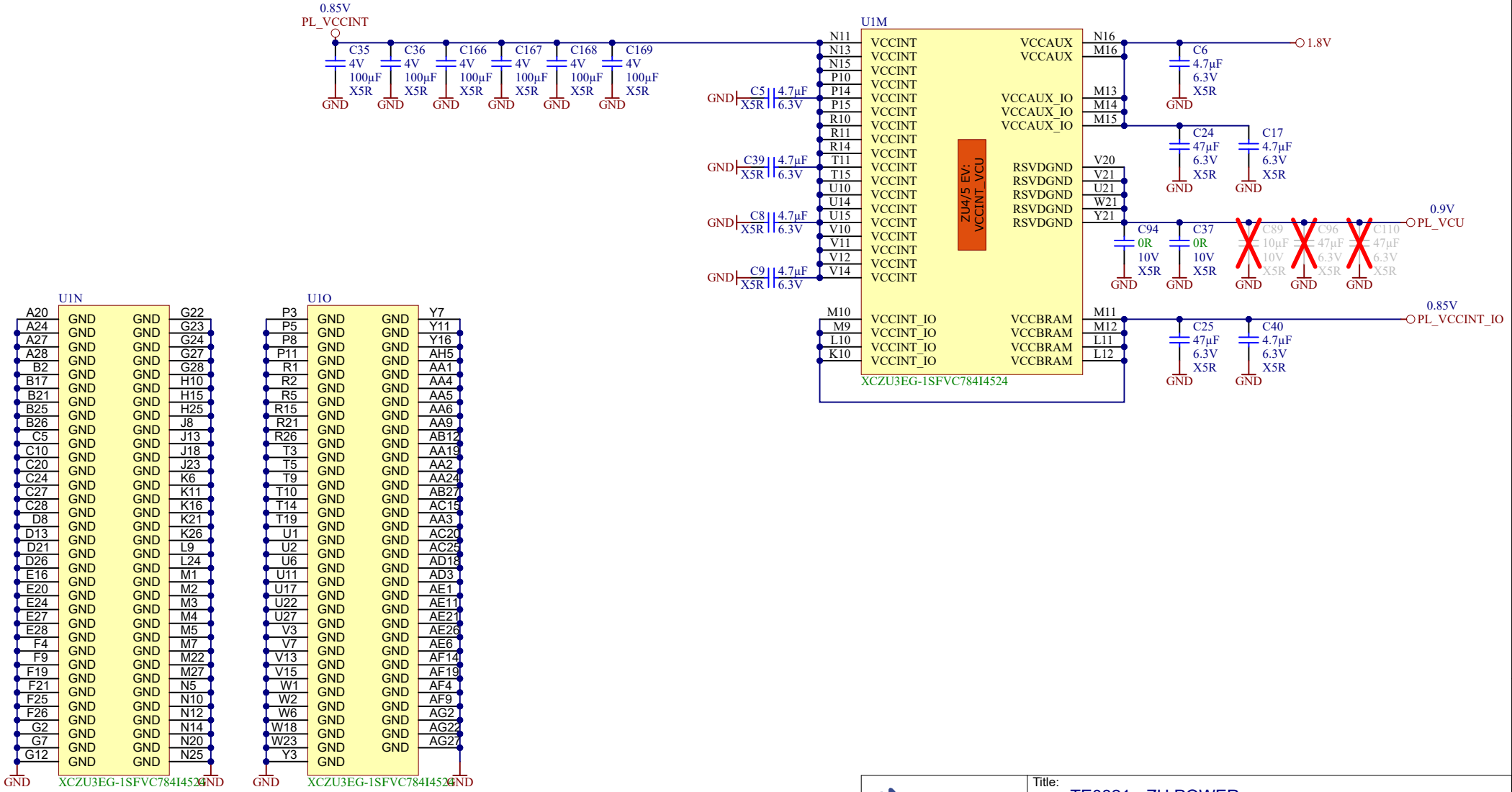

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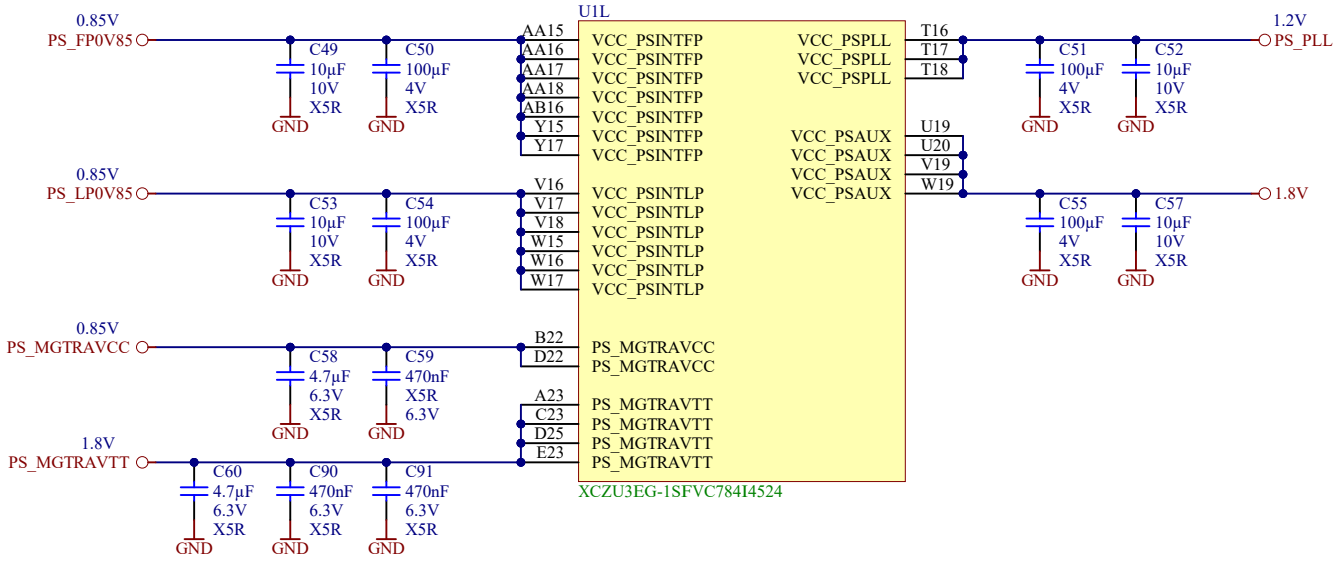
Filename: ZU_POWER.SchDoc		



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Title: TE0821 - ZU PS POWER		
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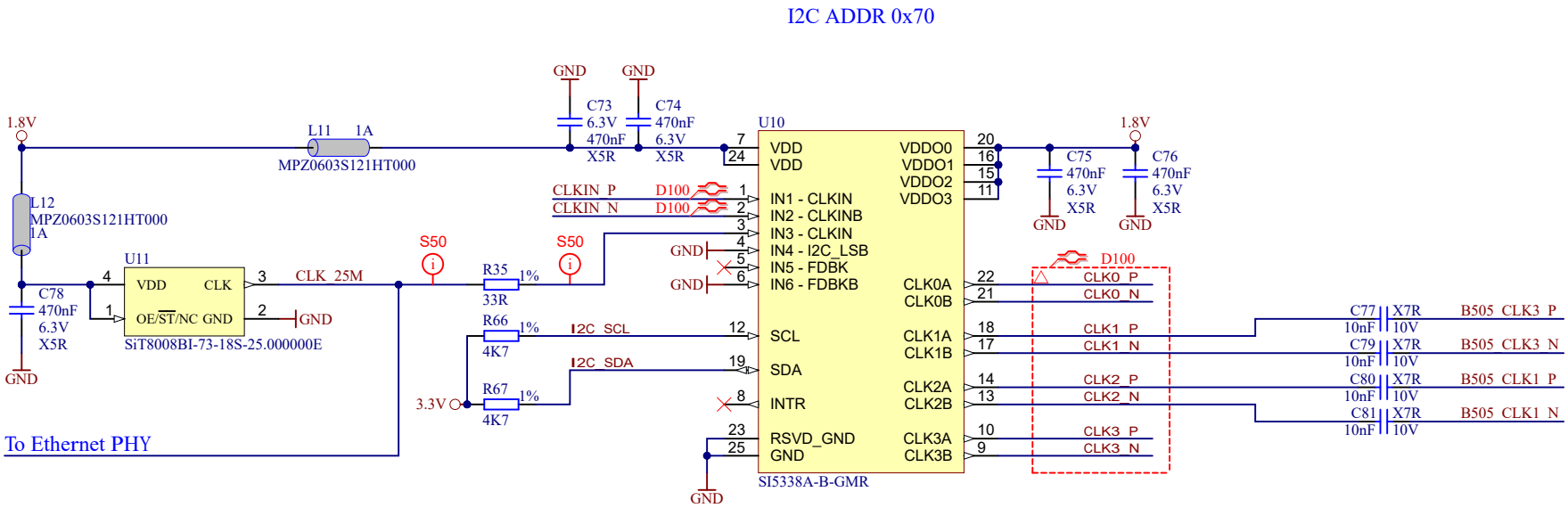

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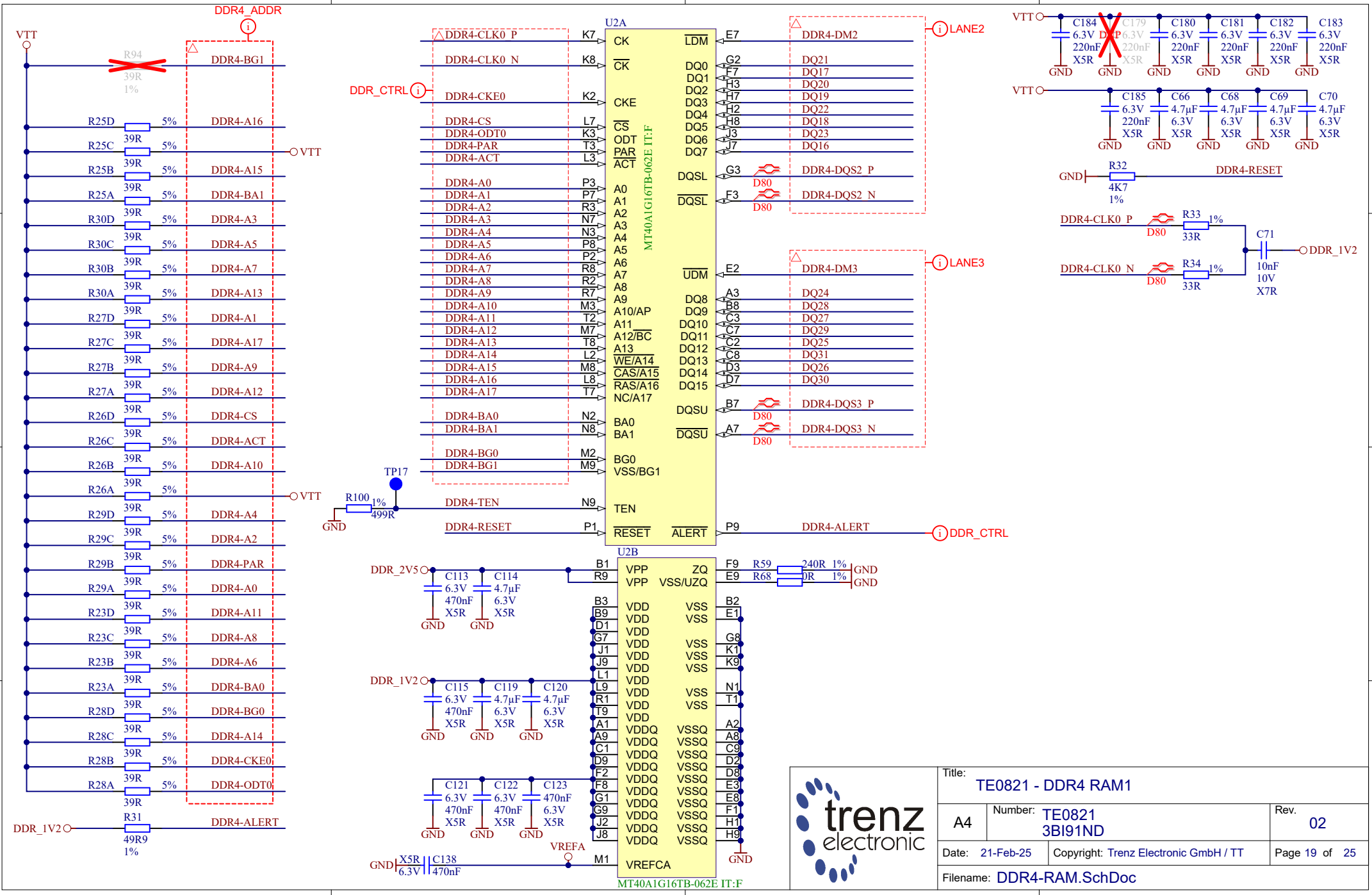
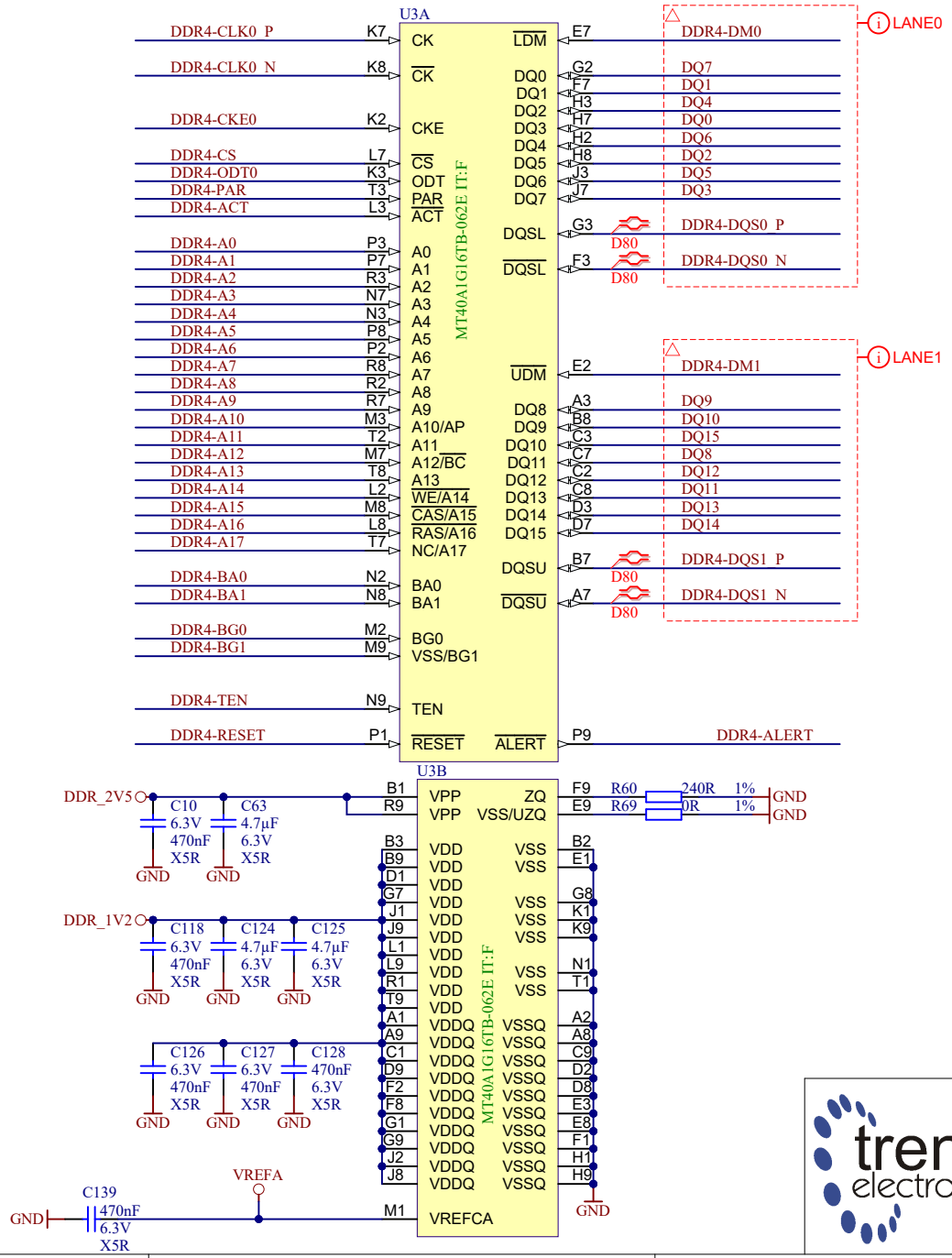
A4	Number: TE0821 3BI91ND		Rev. 02
Date: 30-Sep-24	Copyright: 2015 Trenz Electronic GmbH		Page 18 of 25
Filename: CLK.SchDoc			


DDR4_ADDR
VTT
R94 39R 1%
DDR4-BG1
R25D 39R 5% DDR4-A16
R25C 39R 5% VTT
R25B 39R 5% DDR4-A15
R25A 39R 5% DDR4-BA1
R30D 39R 5% DDR4-A3
R30C 39R 5% DDR4-A5
R30B 39R 5% DDR4-A7
R30A 39R 5% DDR4-A13
R27D 39R 5% DDR4-A1
R27C 39R 5% DDR4-A17
R27B 39R 5% DDR4-A9
R27A 39R 5% DDR4-A12
R26D 39R 5% DDR4-CS
R26C 39R 5% DDR4-ACT
R26B 39R 5% DDR4-A10
R26A 39R 5% VTT
R29D 39R 5% DDR4-A4
R29C 39R 5% DDR4-A2
R29B 39R 5% DDR4-PAR
R29A 39R 5% DDR4-A0
R23D 39R 5% DDR4-A11
R23C 39R 5% DDR4-A8
R23B 39R 5% DDR4-A6
R23A 39R 5% DDR4-BA0
R28D 39R 5% DDR4-BG0
R28C 39R 5% DDR4-A14
R28B 39R 5% DDR4-CKE0
R28A 39R 5% DDR4-ODT0
DDR_1V2
R31 49R9 1%
DDR4-ALERT
U2A
DDR4-CLK0_P
DDR4-CLK0_N
DDR_CTRL
DDR4-CKE0
DDR4-CS
DDR4-ODT0
DDR4-PAR
DDR4-ACT
DDR4-A0
DDR4-A1
DDR4-A2
DDR4-A3
DDR4-A4
DDR4-A5
DDR4-A6
DDR4-A7
DDR4-A8
DDR4-A9
DDR4-A10
DDR4-A11
DDR4-A12
DDR4-A13
DDR4-A14
DDR4-A15
DDR4-A16
DDR4-A17
DDR4-BA0
DDR4-BA1
DDR4-BG0
DDR4-BG1
DDR4-TEN
DDR4-RESET
MT40A1G16TB-062E IT:F
CK
CK
CKE
CS
ODT
PAR
ACT
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
WE/A14
CAS/A15
RAS/A16
NC/A17
BA0
BA1
BG0
VSS/BG1
TEN
RESET
LDM
UDM
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQSL
DQSL
DQSU
DQSU
ALERT
DDR4-DM2
DDR4-DM3
DDR4-DQS2_P
DDR4-DQS2_N
DDR4-DQS3_P
DDR4-DQS3_N
DQ21
DQ17
DQ20
DQ19
DQ22
DQ18
DQ23
DQ16
DQ24
DQ28
DQ27
DQ29
DQ25
DQ31
DQ26
DQ30
D80
LANE2
LANE3
DDR4-ALERT
DDR_CTRL
TP17
R100 1% 499R
GND
U2B
DDR_2V5
DDR_1V2
VPP
VPP
VDD
VDDQ
VSS
VSSQ
ZQ
VSS/UZQ
R59 240R 1%
R68 0R 1%
C113 6.3V 470nF X5R
C114 6.3V 4.7µF X5R
C115 6.3V 470nF X5R
C119 6.3V 4.7µF X5R
C120 6.3V 4.7µF X5R
C121 6.3V 470nF X5R
C122 6.3V 470nF X5R
C123 6.3V 470nF X5R
VREFA
VREFCA
C138 6.3V X5R 470nF
MT40A1G16TB-062E IT:F
VTT
C184 6.3V 220nF X5R DNP
C179 6.3V 220nF X5R
C180 6.3V 220nF X5R
C181 6.3V 220nF X5R
C182 6.3V 220nF X5R
C183 6.3V 220nF X5R
C185 6.3V 220nF X5R
C66 4.7µF 6.3V X5R
C68 4.7µF 6.3V X5R
C69 4.7µF 6.3V X5R
C70 4.7µF 6.3V X5R
R32 4K7 1%
DDR4-RESET
R33 33R 1%
R34 33R 1%
C71 10nF 10V X7R
DDR_1V2
trenz electronic
Title: TE0821 - DDR4 RAM1
A4
Number: TE0821 3BI91ND
Rev. 02
Date: 21-Feb-25
Copyright: Trenz Electronic GmbH / TT
Page 19 of 25
Filename: DDR4-RAM.SchDoc



trenz electronic	Title: TE0821 - DDR4 RAM2		
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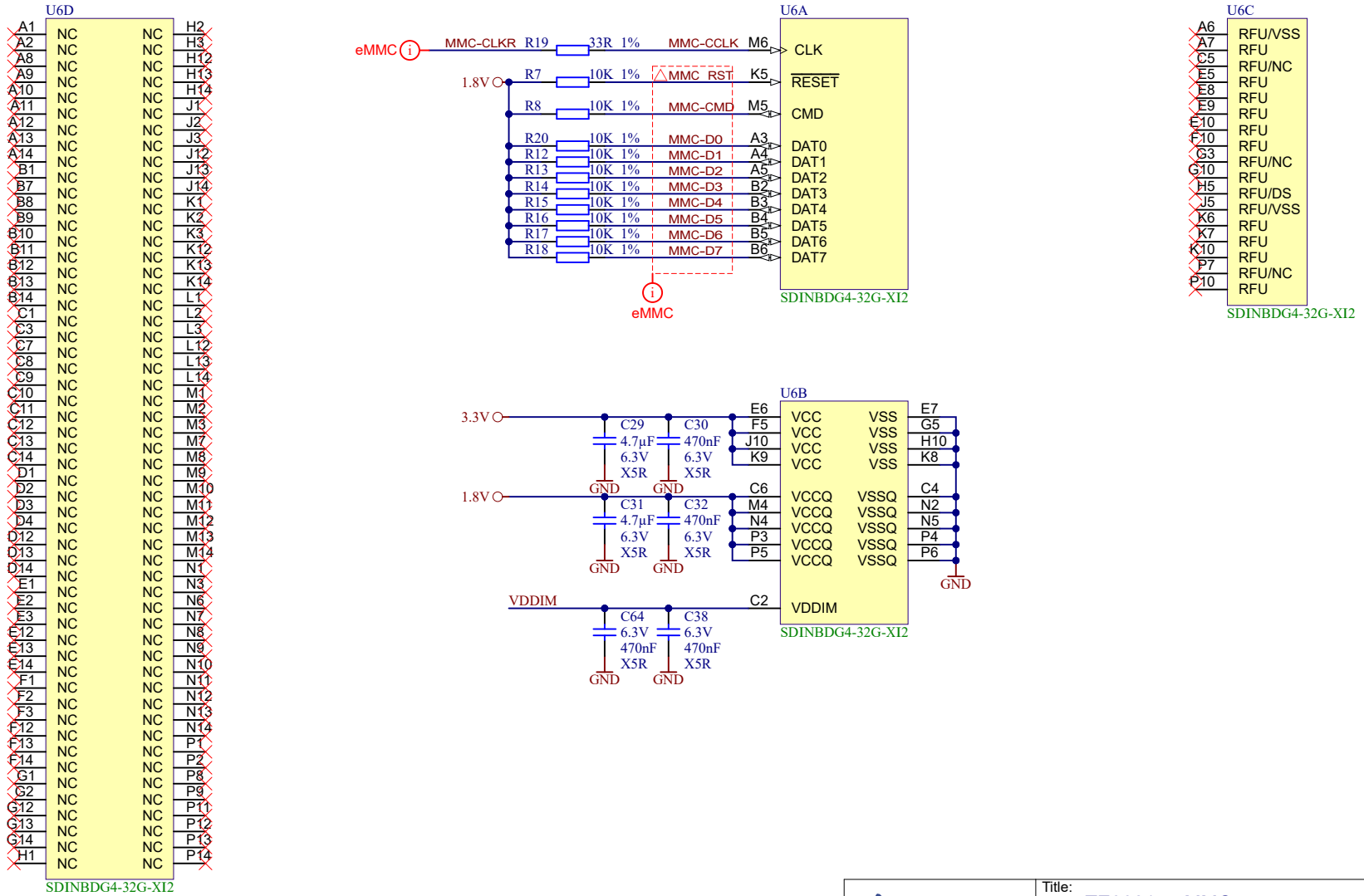
	Date: 29-May-24	Copyright: Trenz Electronic GmbH / TT	Page 20 of 25
	Filename: DDR4-RAM_2.SchDoc		



trenz electronic	Title: TE0821 - eMMC		
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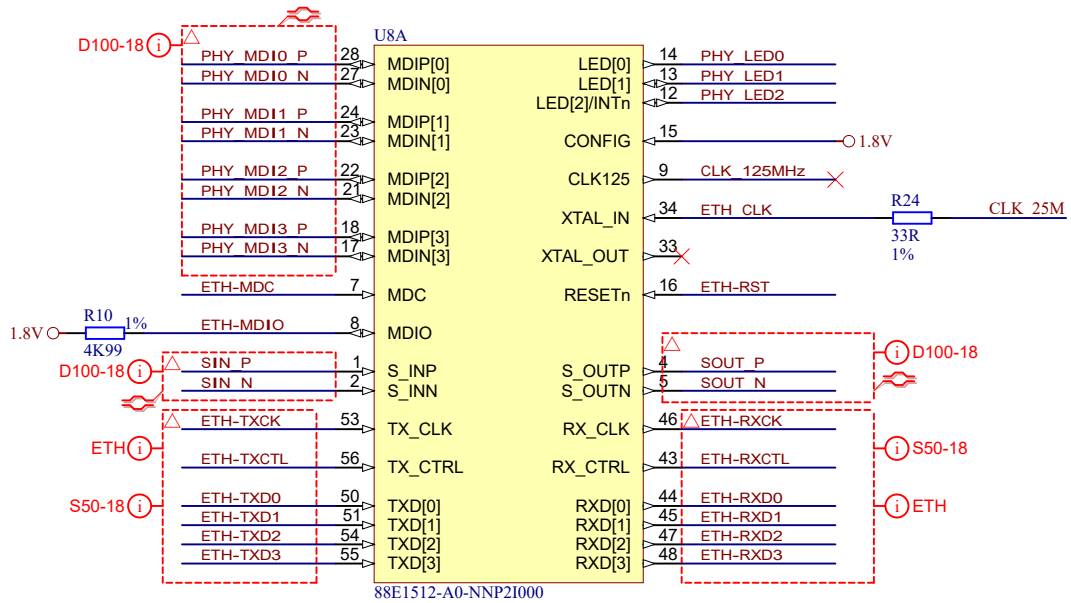
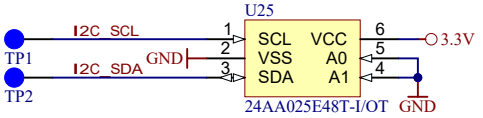
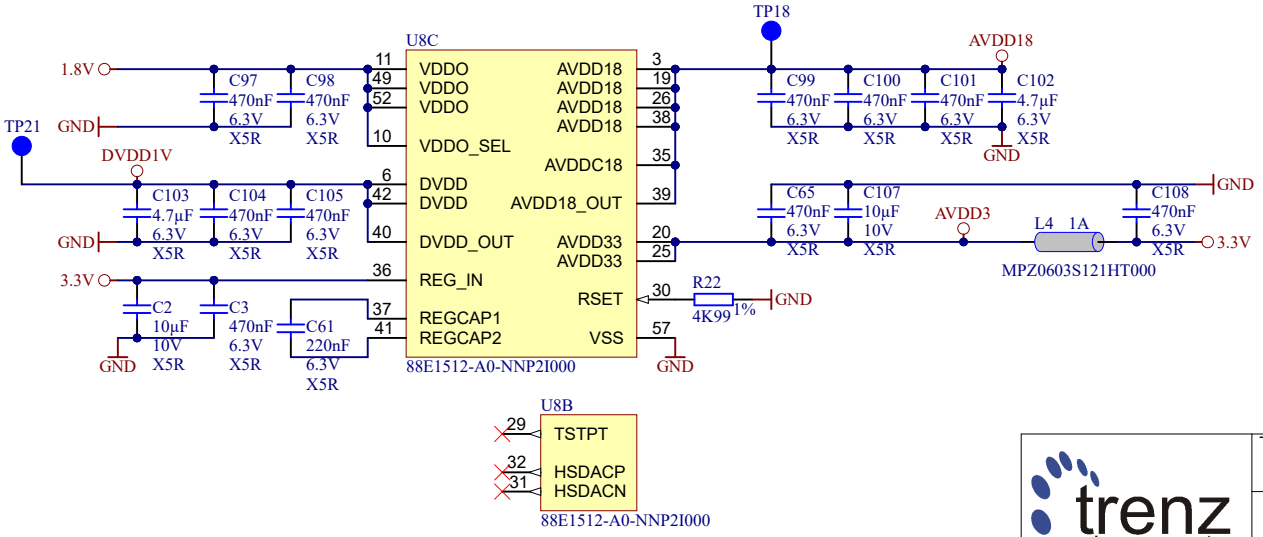
Date: 15-Apr-24	Copyright: Trenz Electronic GmbH / TT		Page 21 of 25
Filename: eMMC.SchDoc			



I2C ADDR 0x50

EEPROM for MAC





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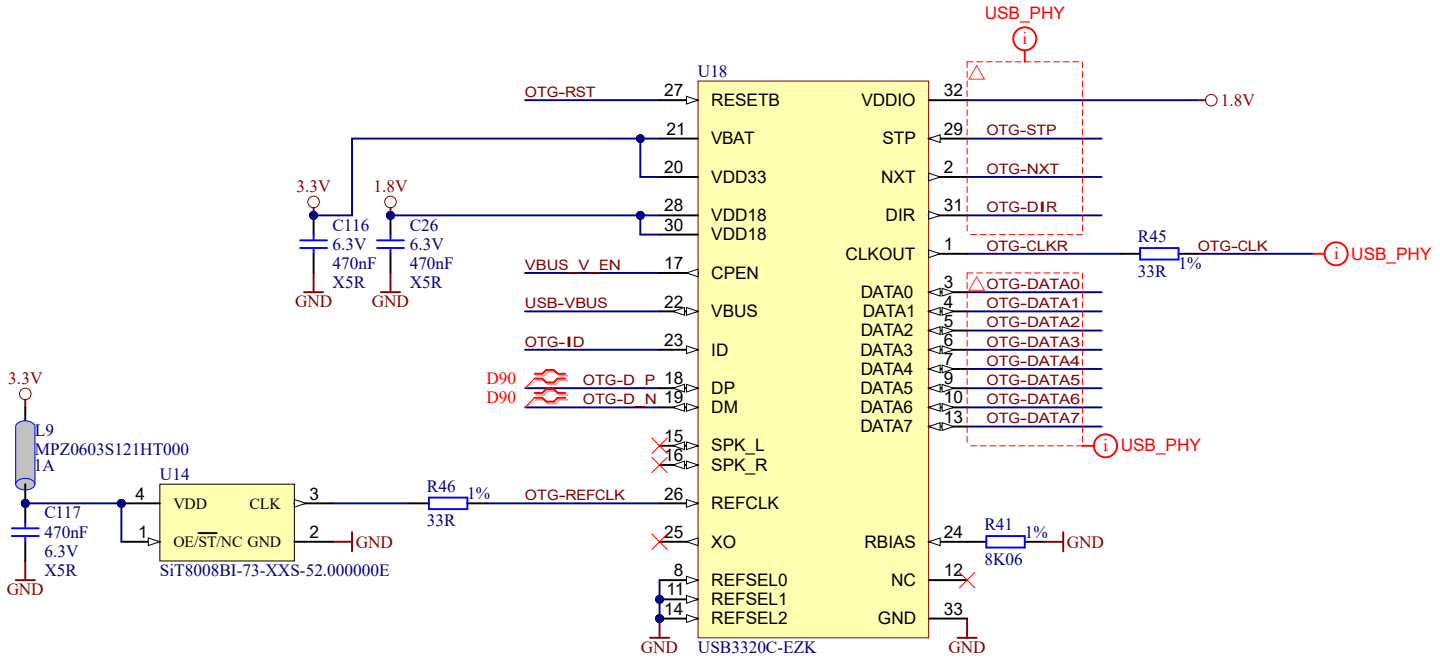
Title: TE0821 - Ethernet PHY			
A4	Number: TE0821 3BI91ND		Rev. 02
Date: 28-May-24	Copyright: 2015 Trenz Electronic GmbH		Page 22 of 25
Filename: ETH-PHY.SchDoc			



trenz electronic	Title: TE0821 - USB PHY		
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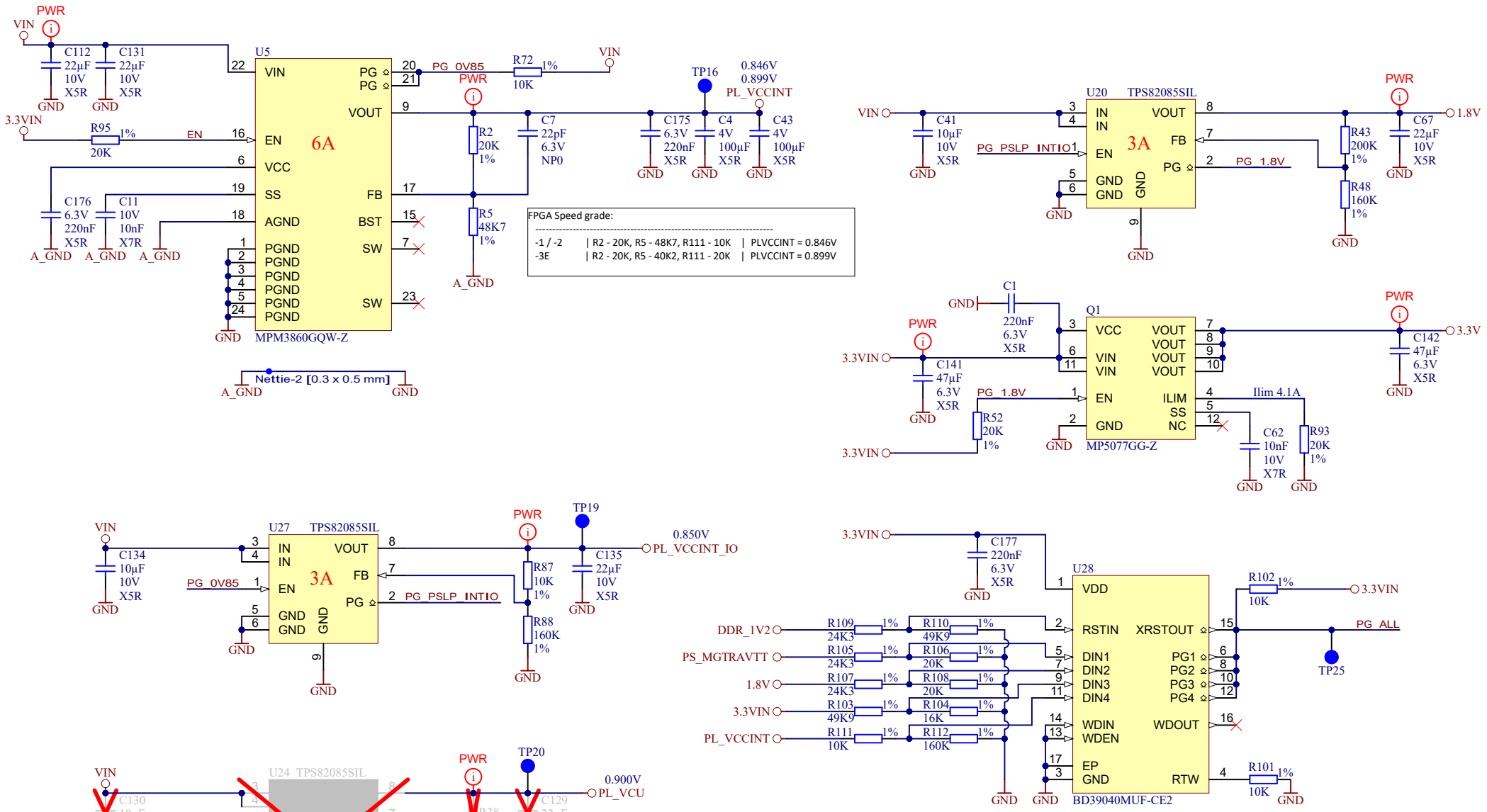
Date: 16-May-24	Copyright: 2015 Trenz Electronic GmbH		Page 23 of 25
Filename: USB-PHY.SchDoc			



trenz electronic	Title: TE0821 - POWER		
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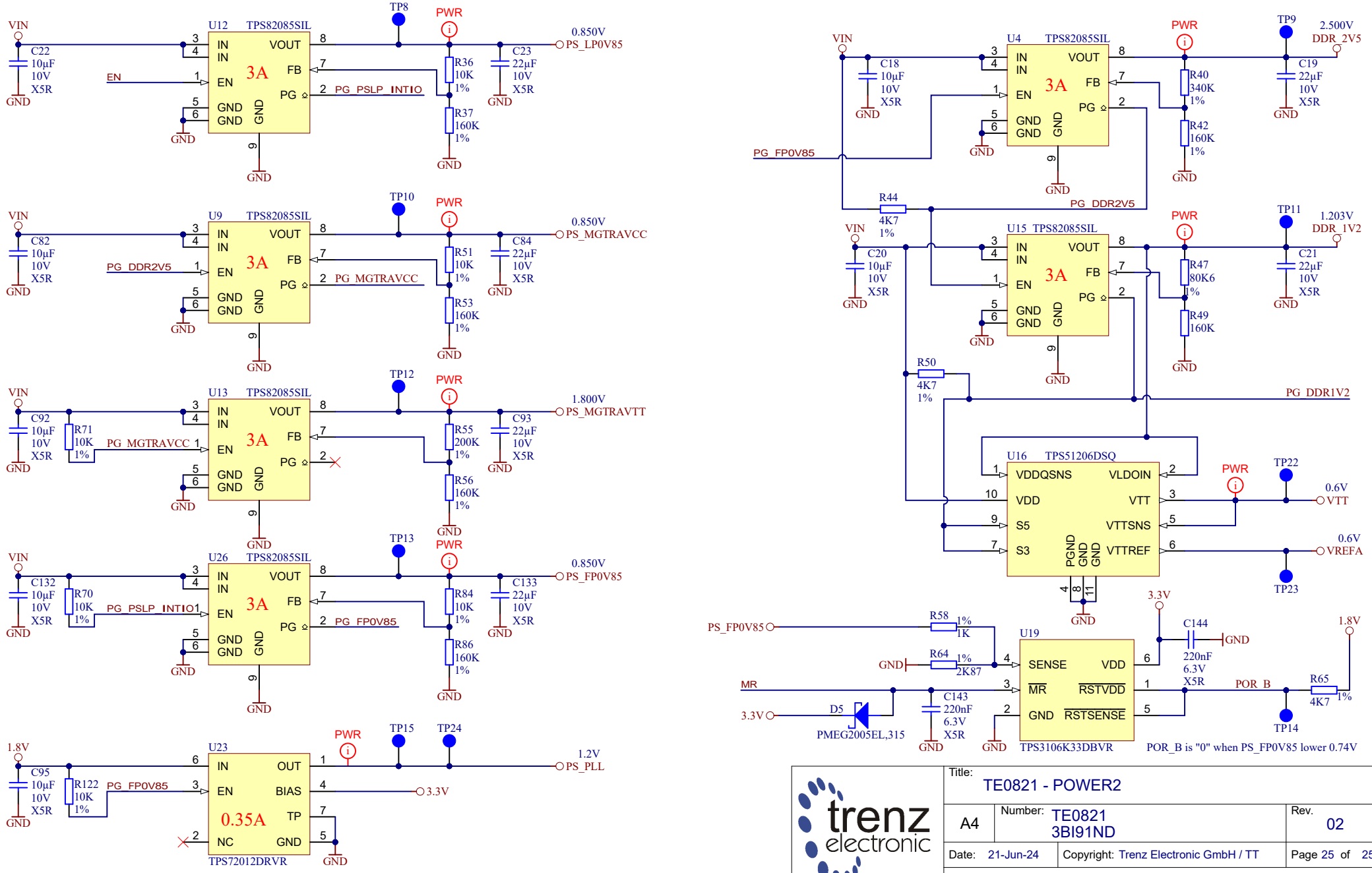
	Date: 28-May-24	Copyright: Trenz Electronic GmbH / TT	Page 24 of 25
	Filename: POWER.SchDoc		



Title: TE0821 - POWER2			
A4	Number: TE0821 3BI91ND		Rev. 02
Date: 21-Jun-24	Copyright: Trenz Electronic GmbH / TT		Page 25 of 25
Filename: POWER_1.SchDoc			