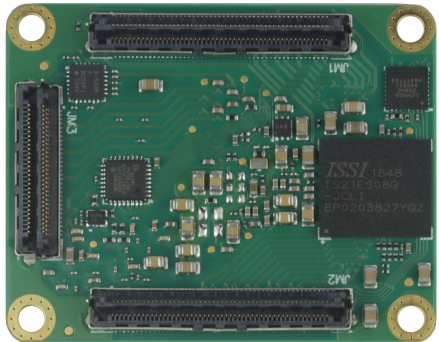
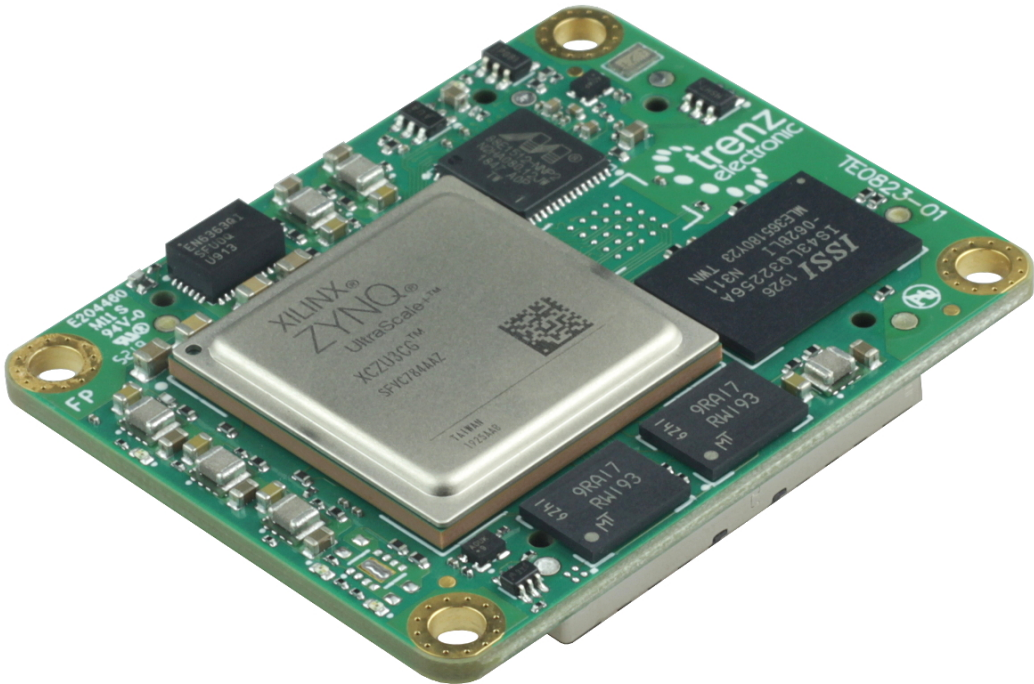




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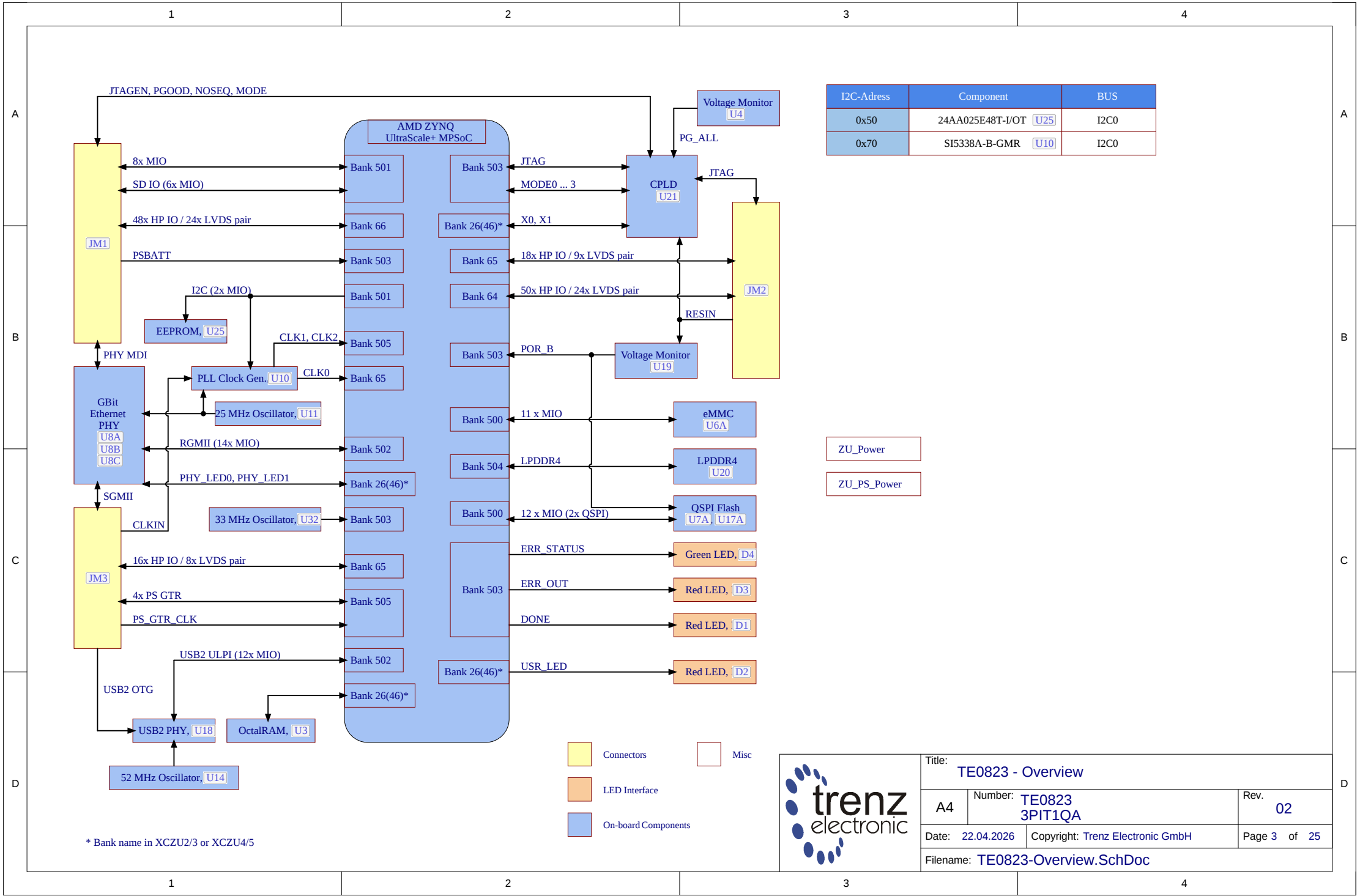
Schematics and other handouts serve for informational purposes only!

Drawn by	LH
Checked by	ED/MR
Assembly variant	3PIT1QA
Created by	LH
Modified by	LH
Modified at	2025-12-15

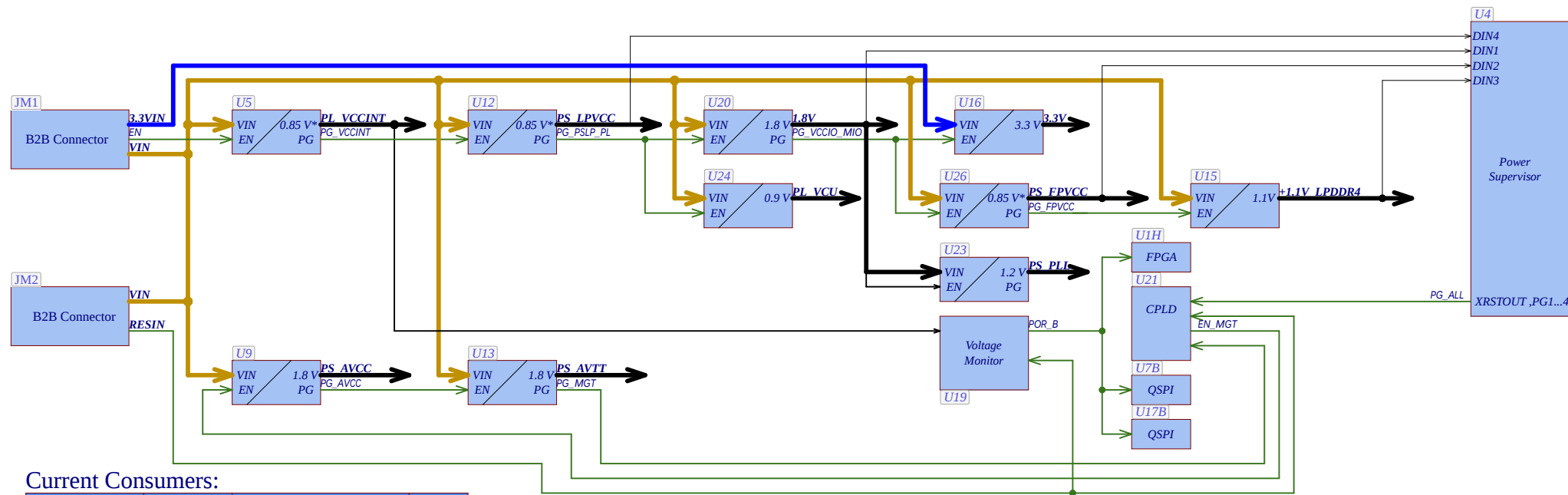


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A4	Number: TE0823 3PIT1QA	Rev. 02
Date: 15.04.2026	Copyright: Trenz Electronic GmbH	Page 1 of 25
Filename: Legal Notices Modules.SchDoc		

1		2		3		4																
A	<table><thead><tr><th>REV</th><th>Description</th><th></th></tr></thead><tbody><tr><td>-01</td><td>Initial revision</td><td>-</td></tr><tr><td>-01a</td><td>1. R38 value was changed to 20K (was: 40K2) to set VCU 0.9V</td><td>VY</td></tr><tr><td>-01b</td><td>1. added block diagram 2. added page "Legal notices" 3. R51 value was changed to 10K (was: 20K) to set PS_VCU 0.85V</td><td>VY</td></tr><tr><td>-02</td><td>1. Replaced EOL buck converter EN6363QI (<u>U5</u>) with MPM3860. 2. Renamed net PS_LP0V85 to PS_LPVCC and net PS_FP0V85 to PS_FPVCC. 3. Added BD39040MUF-C (<u>U4</u>) as an additional power supervisor. 4. Added signal PG_ALL to CPLD. 5. Replaced EOL LPDDR4 RAM IS43LQ32256A-062BLI (<u>U2A</u>) with IS43LQ32K01S2A-046BLI. 6. Replaced TPS27081ADDCR (Q1) with MP5077GG-Z (<u>U16</u>). 7. Replaced EOL SiT8008AI-73-XXS-52.000000E (<u>U14</u>) with SiT8008BI-73-XXS-52.000000E. 8. All LVDS and MGT tracks extended by 1 mm due to PCB changes. 9.Added C144 and C145 and optional 100 ohm termination resistor R106 to CLK0 for AC coupling. 10. Net PG_FPD renamed to PG_ALL. 11. Added MOSFET <u>T2A</u> to ensure correct power good sequence.</td><td>LH</td></tr></tbody></table>						REV	Description		-01	Initial revision	-	-01a	1. R38 value was changed to 20K (was: 40K2) to set VCU 0.9V	VY	-01b	1. added block diagram 2. added page "Legal notices" 3. R51 value was changed to 10K (was: 20K) to set PS_VCU 0.85V	VY	-02	1. Replaced EOL buck converter EN6363QI (<u>U5</u>) with MPM3860. 2. Renamed net PS_LP0V85 to PS_LPVCC and net PS_FP0V85 to PS_FPVCC. 3. Added BD39040MUF-C (<u>U4</u>) as an additional power supervisor. 4. Added signal PG_ALL to CPLD. 5. Replaced EOL LPDDR4 RAM IS43LQ32256A-062BLI (<u>U2A</u>) with IS43LQ32K01S2A-046BLI. 6. Replaced TPS27081ADDCR (Q1) with MP5077GG-Z (<u>U16</u>). 7. Replaced EOL SiT8008AI-73-XXS-52.000000E (<u>U14</u>) with SiT8008BI-73-XXS-52.000000E. 8. All LVDS and MGT tracks extended by 1 mm due to PCB changes. 9.Added C144 and C145 and optional 100 ohm termination resistor R106 to CLK0 for AC coupling. 10. Net PG_FPD renamed to PG_ALL. 11. Added MOSFET <u>T2A</u> to ensure correct power good sequence.	LH	A
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C							C															
D	 <table><tr><td colspan="3">Title: TE0823 - Revision changes</td></tr><tr><td>A4</td><td>Number: TE0823 3PIT1QA</td><td>Rev. 02</td></tr><tr><td>Date: 15.04.2026</td><td>Copyright: Trenz Electronic GmbH</td><td>Page 2 of 25</td></tr><tr><td colspan="3">Filename: Revision Changes.SchDoc</td></tr></table>						Title: TE0823 - Revision changes			A4	Number: TE0823 3PIT1QA	Rev. 02	Date: 15.04.2026	Copyright: Trenz Electronic GmbH	Page 2 of 25	Filename: Revision Changes.SchDoc			D			
Title: TE0823 - Revision changes																						
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Date: 15.04.2026	Copyright: Trenz Electronic GmbH	Page 2 of 25																				
Filename: Revision Changes.SchDoc																						
1		2		3		4																



* Bank name in XCZU2/3 or XCZU4/5



Current Consumers:

Power Rail	Voltage	Consumer	Note
PL_VCCINT	0.72/0.85/0.9 V	SoC VCCINT	-
PS_LPVCC	0.85 V / 0.9 V	SoC VCCINT_IO SoC VCCBRAM SoC VCC_PSINTLP	-
1.8V	1.8 V	CPLD VCCIO1/2 B2B JM1/JM2 SoC VCCO_66/65/64 QSPI FLASH QUAD CLK VDDO eMMC VCCQ ETH PHY VDDO SoC VCCPSDDR_PLL USB PHY VDD18 SoC VCC_AUX SoC VCC_AUX_IO SoC VCC_PS_AUX SoC VCCO_PSIO0/2_500/2 DDR VDD1	-
PL_VCU	0.9 V	SoC VCCINT_VCU	-
PS_AVCC	0.85 V	SoC PS_MGTRAVCC	-
PS_FPVCC	0.85 V / 0.9 V	SoC VCC_PS_INTFP_DDR SoC VCC_PS_INTFP	-
PS_PLL	1.2 V	SoC VCC_PSPLL	-
3.3V	3.3 V	SoC VCCO_PSIO1_501 QUAD CLK VDD eMMC VCC EEPROM VCC CLK GEN 25M VDD USB PHY VDD33/VBAT CLK GEN 52M VDD	-
PS_AVTT	1.8 V	SoC PS_MGTRAVTT	-
LPDDR_+1.1V	1.1 V	DDR VDD2/VDDQ SoC VCCO_PSDDR_504	-

* Voltage depends on assembly variant.

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3 V	+/- 5 %	Carrier Power	Main Power
VIN	IN	3.3 V - 5 V	+/- 5 %	Carrier Power	Main Power
PSBATT	IN	1.2 V - 1.5 V	-	RTC Power	
VCCO_64	IN	1 V - 1.8 V	+/- 3 %	Bank Power	HP IO Bank 64
VCCO_65	IN	1 V - 1.8 V	+/- 3 %	Bank Power	HP IO Bank 65
VCCO_66	IN	1 V - 1.8 V	+/- 3 %	Bank Power	HP IO Bank 66
3.3V	OUT	3.3 V	-	Carrier Power	
1.8V	OUT	+1.8 V	-	Carrier Power	



Title: TE0823 - Power overview		
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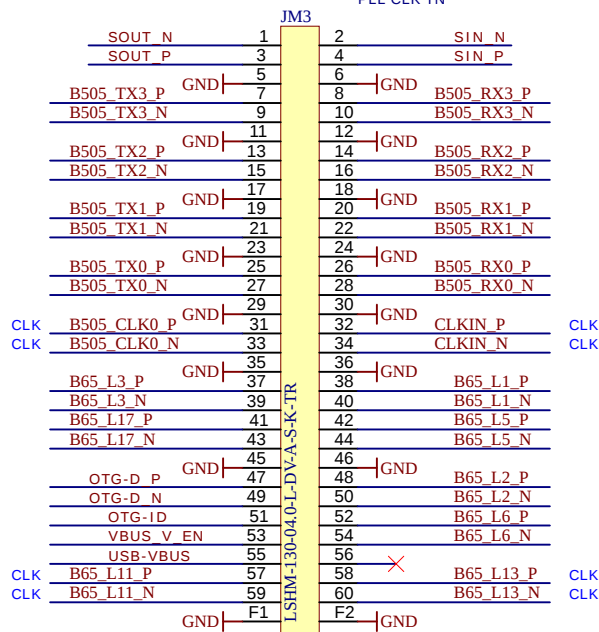
2

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B65(HP) 16 IO, 8 LVDS Pairs
USB OTG
ETH SGMII
PS_GTR 4 Lanes
PS_GTR CLK IN
PLL CLK IN

group 3 0..VCCO_65



AC coupling and 100 Ω termination on carrier board mandatory!

VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)



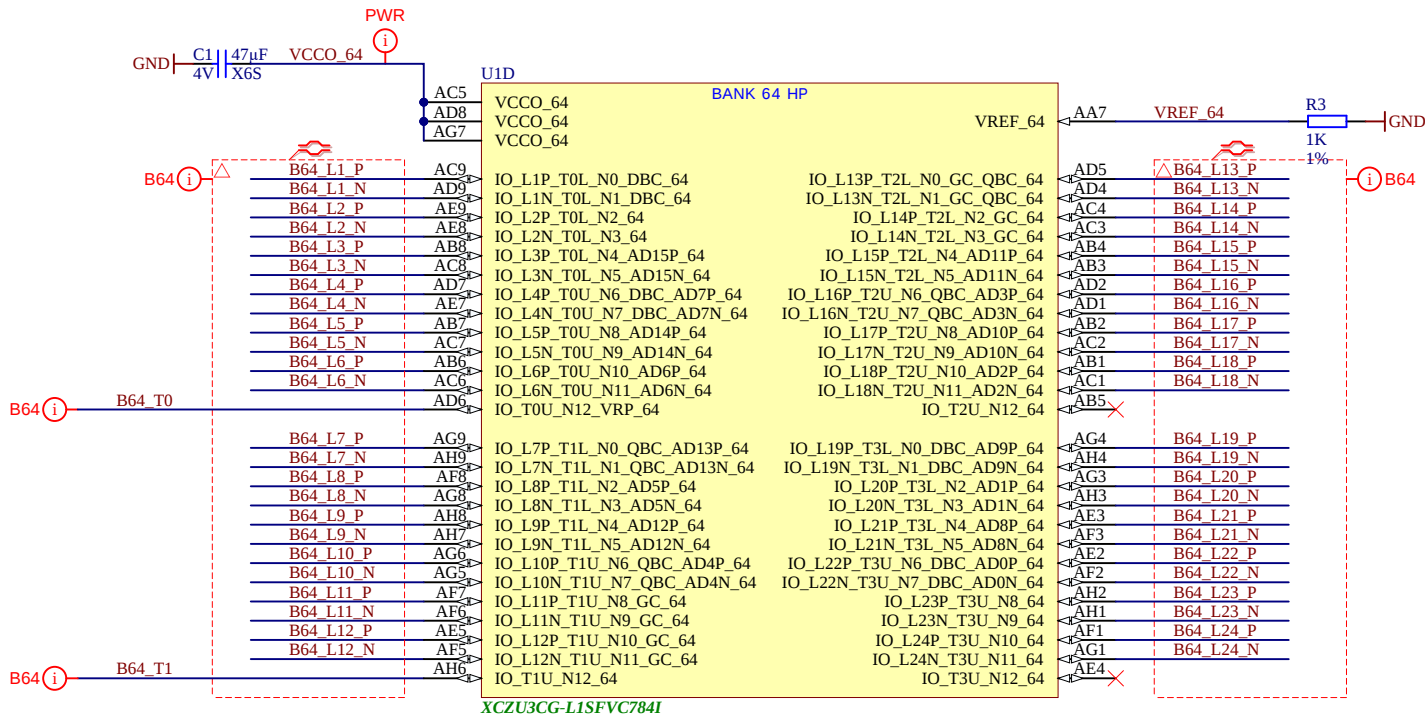
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Date: 15.04.2026	Copyright: Trenz Electronic GmbH	Page 6 of 25
Filename: B2B-Connectors_2.SchDoc		

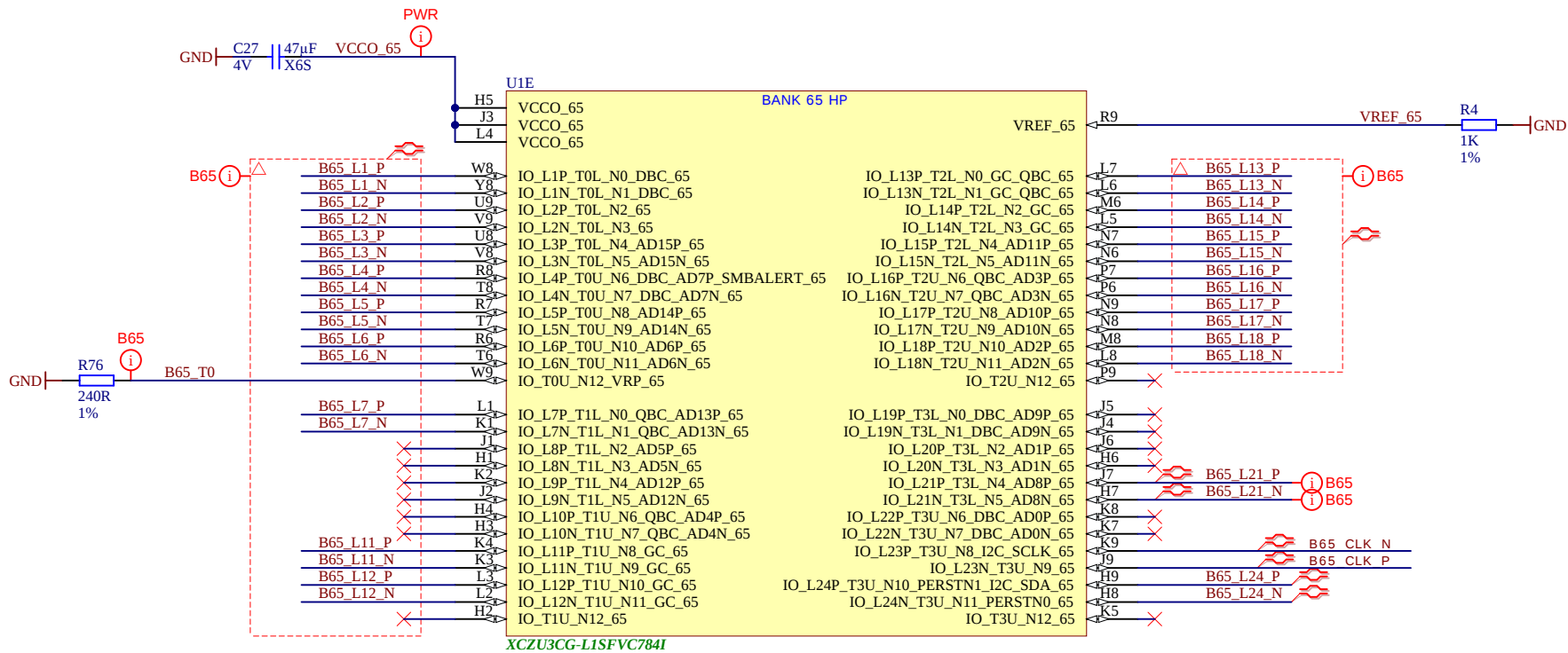
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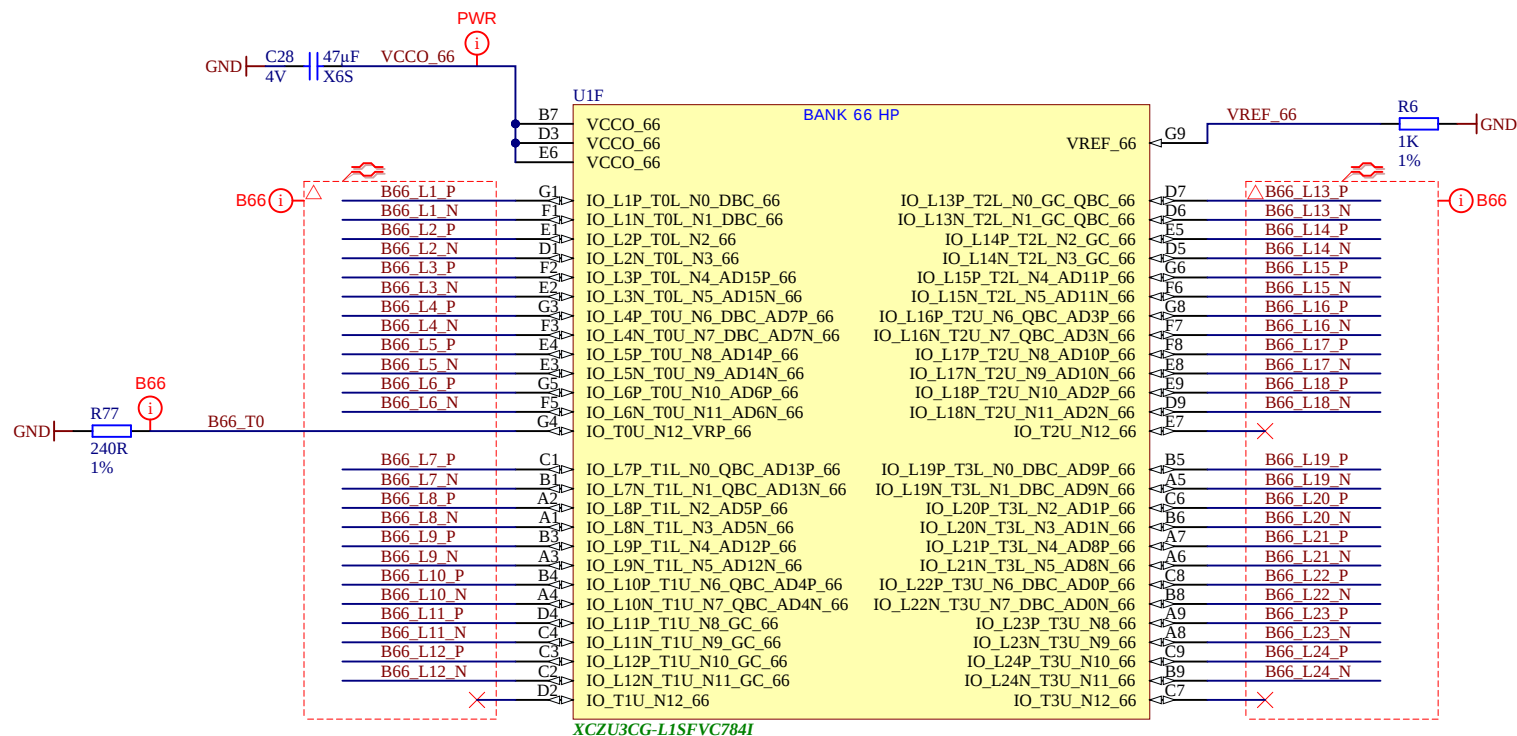
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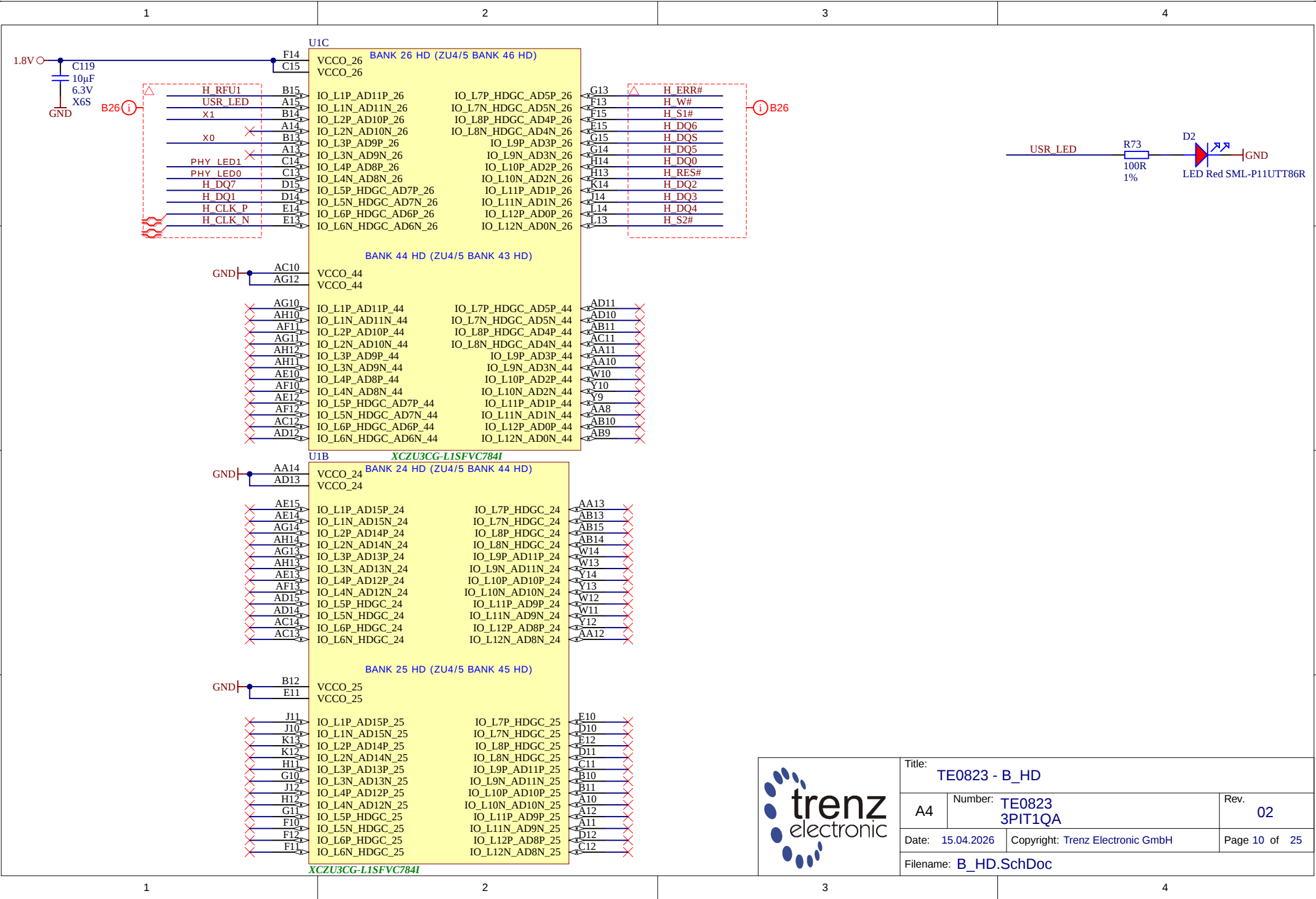


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Filename: B65.SchDoc		Page 8 of 25	

Rev. 02	
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Title: TE0823 - B66		
A4	Number: TE0823 3PIT1QA	Rev. 02
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Title: TE0823 - B_HD		
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A

A

B

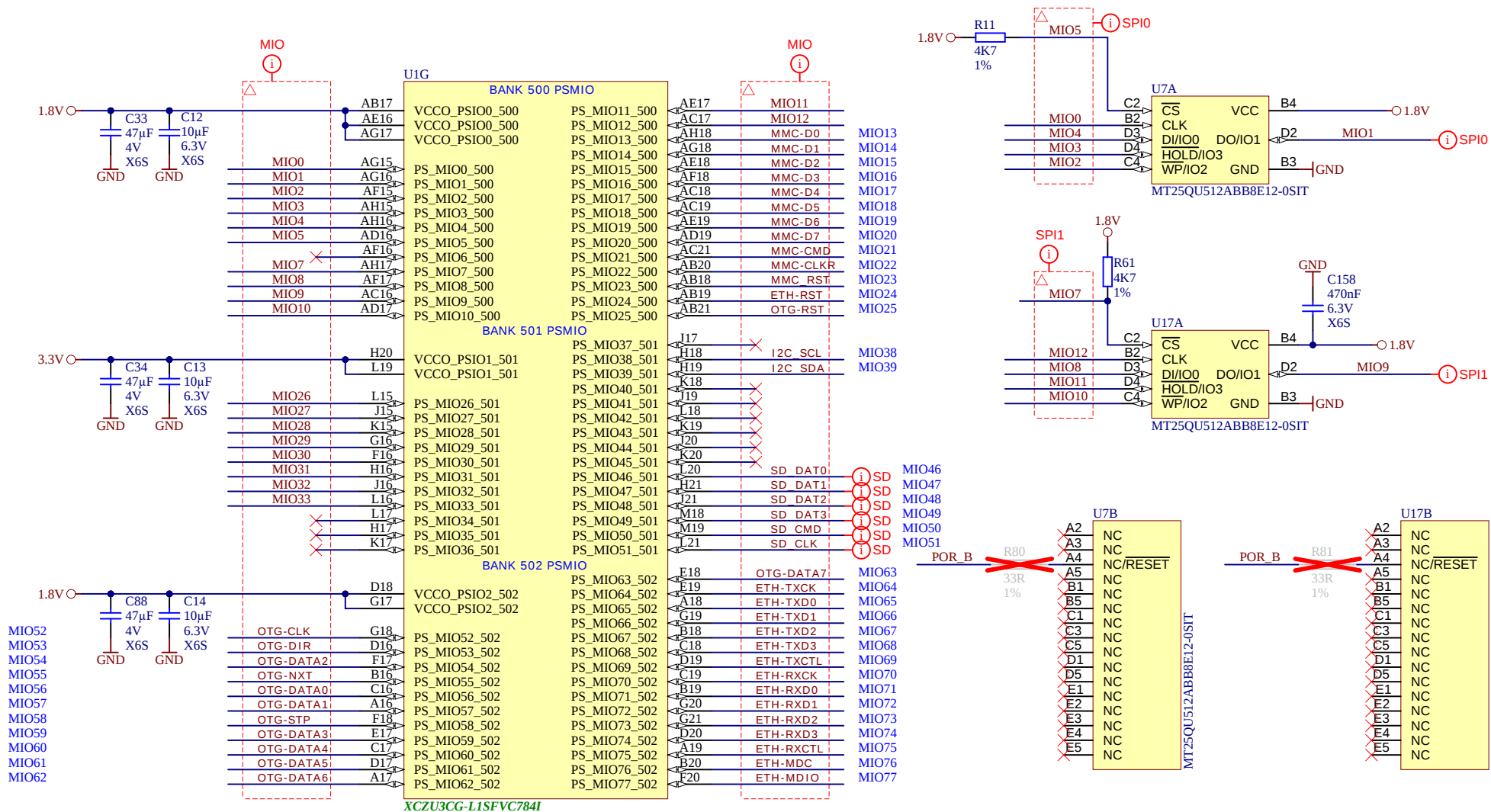
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C

C

D

D



Title: TE0823 - B_MIO		
A4	Number: TE0823 3PIT1QA	Rev. 02
Date: 15.04.2026	Copyright: Trenz Electronic GmbH	
Filename: B_MIO.SchDoc		Page 11 of 25

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A

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B

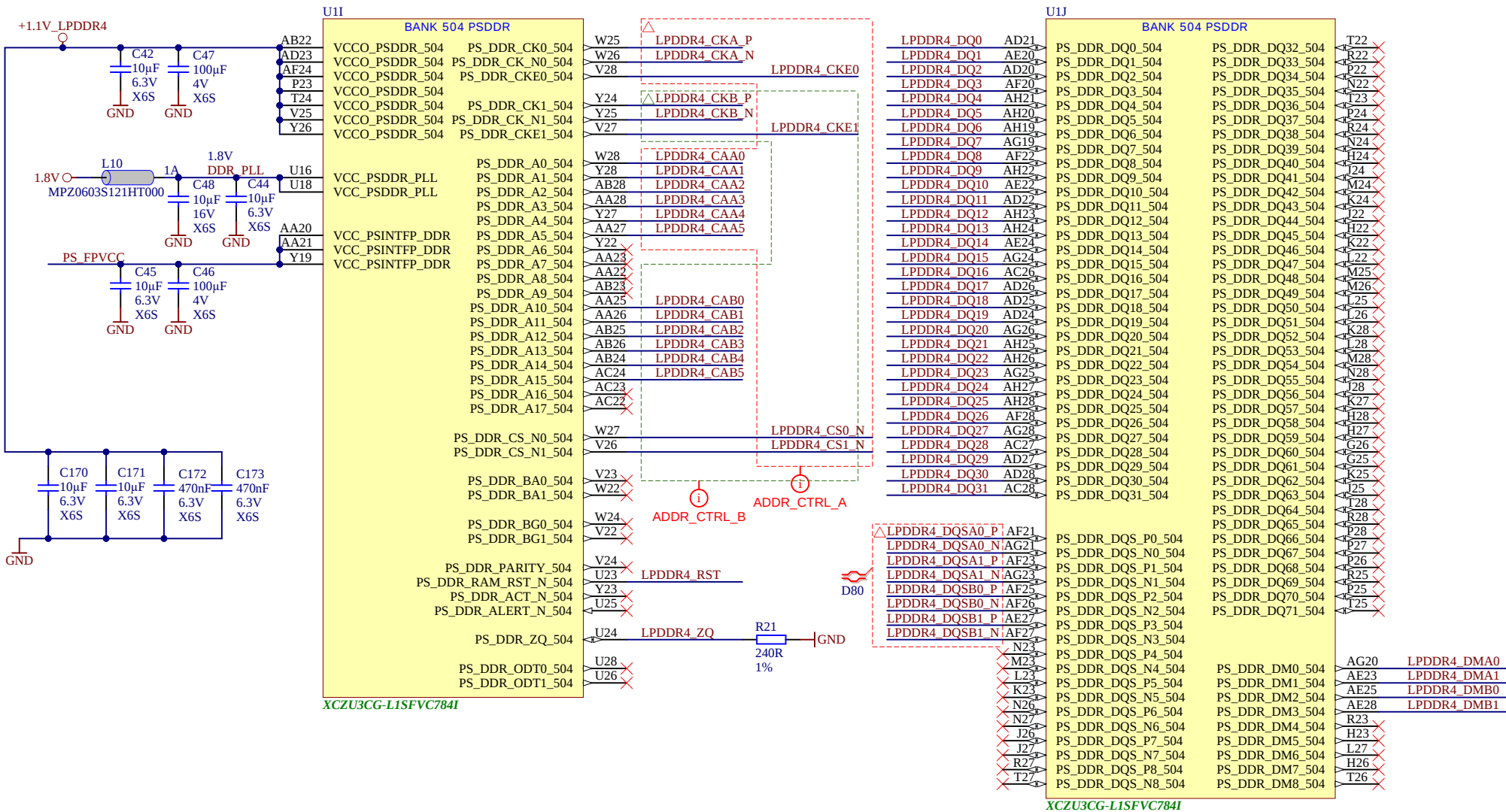
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C

C

D

D



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A

A

B

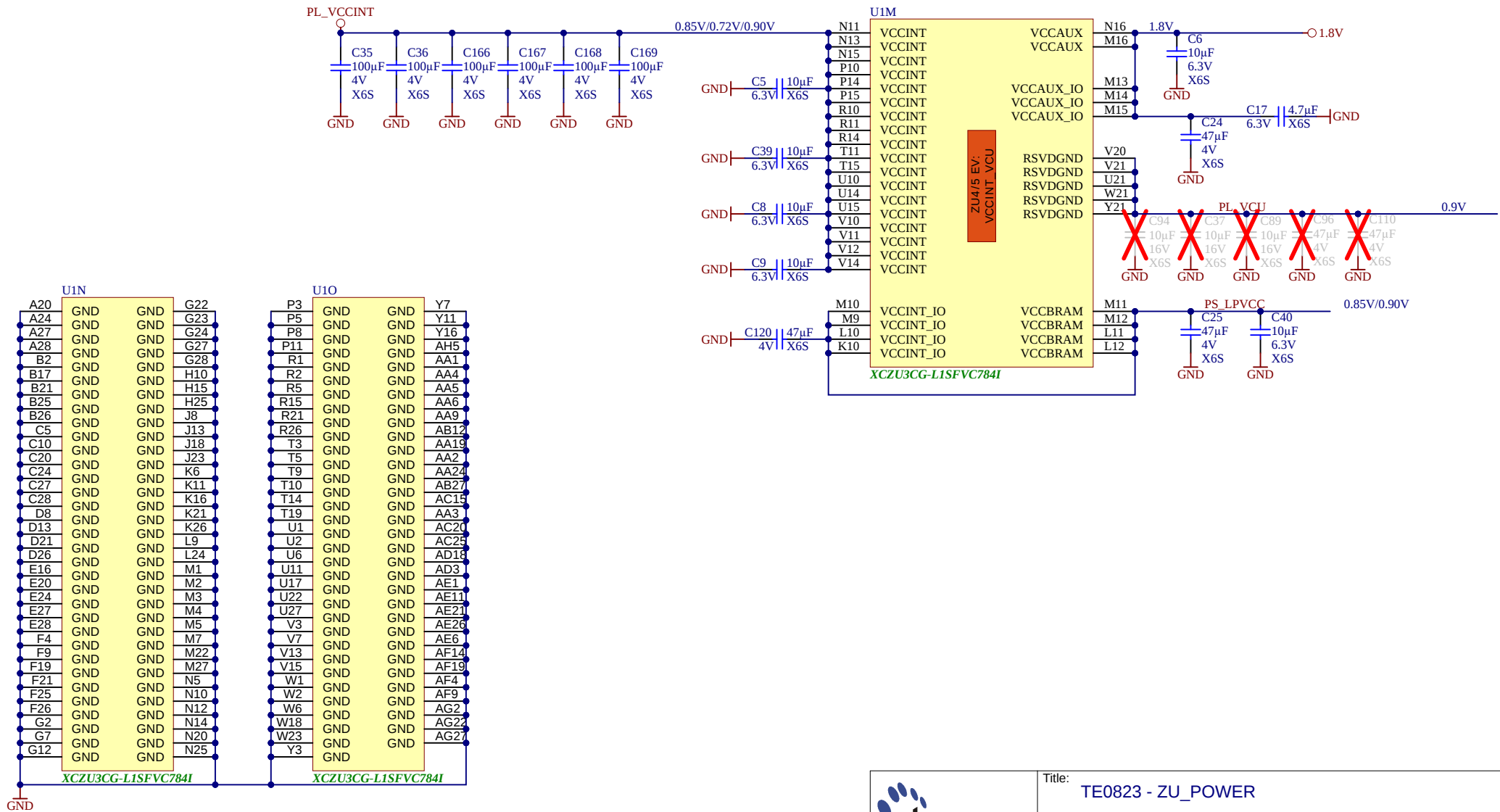
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C

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D



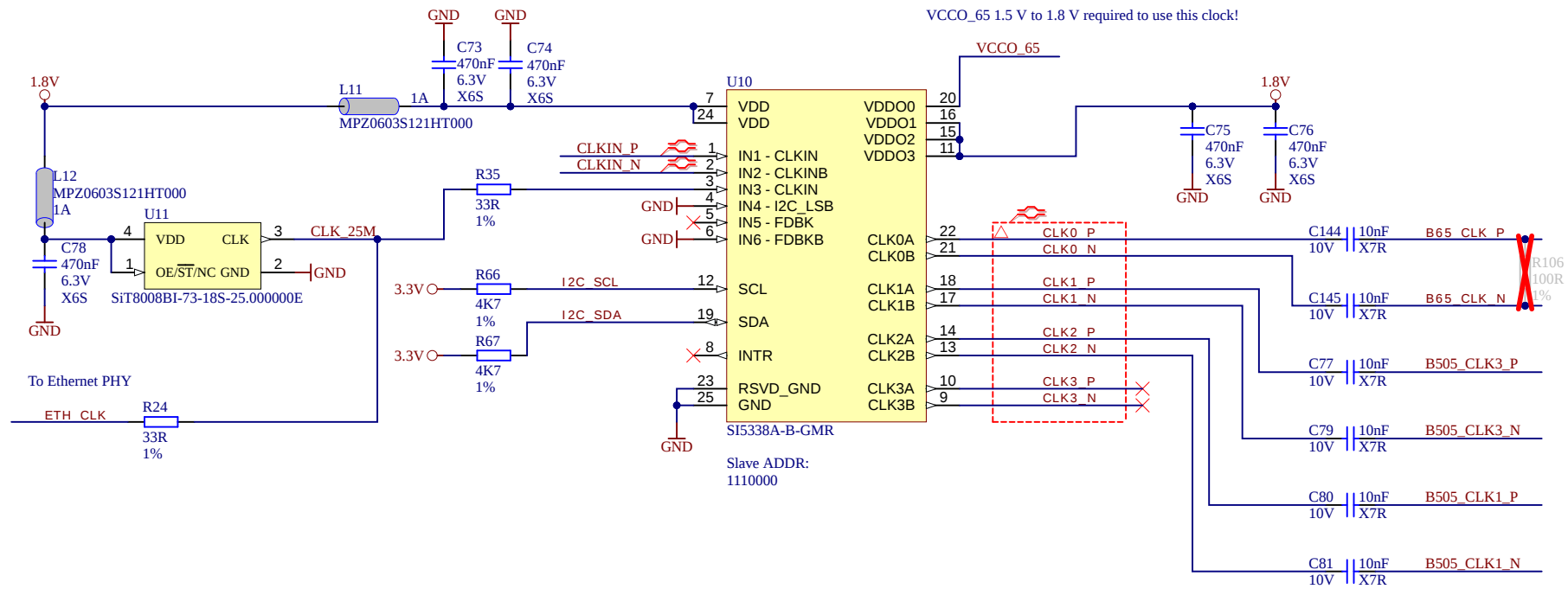
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Filename: ZU_POWER.SchDoc		

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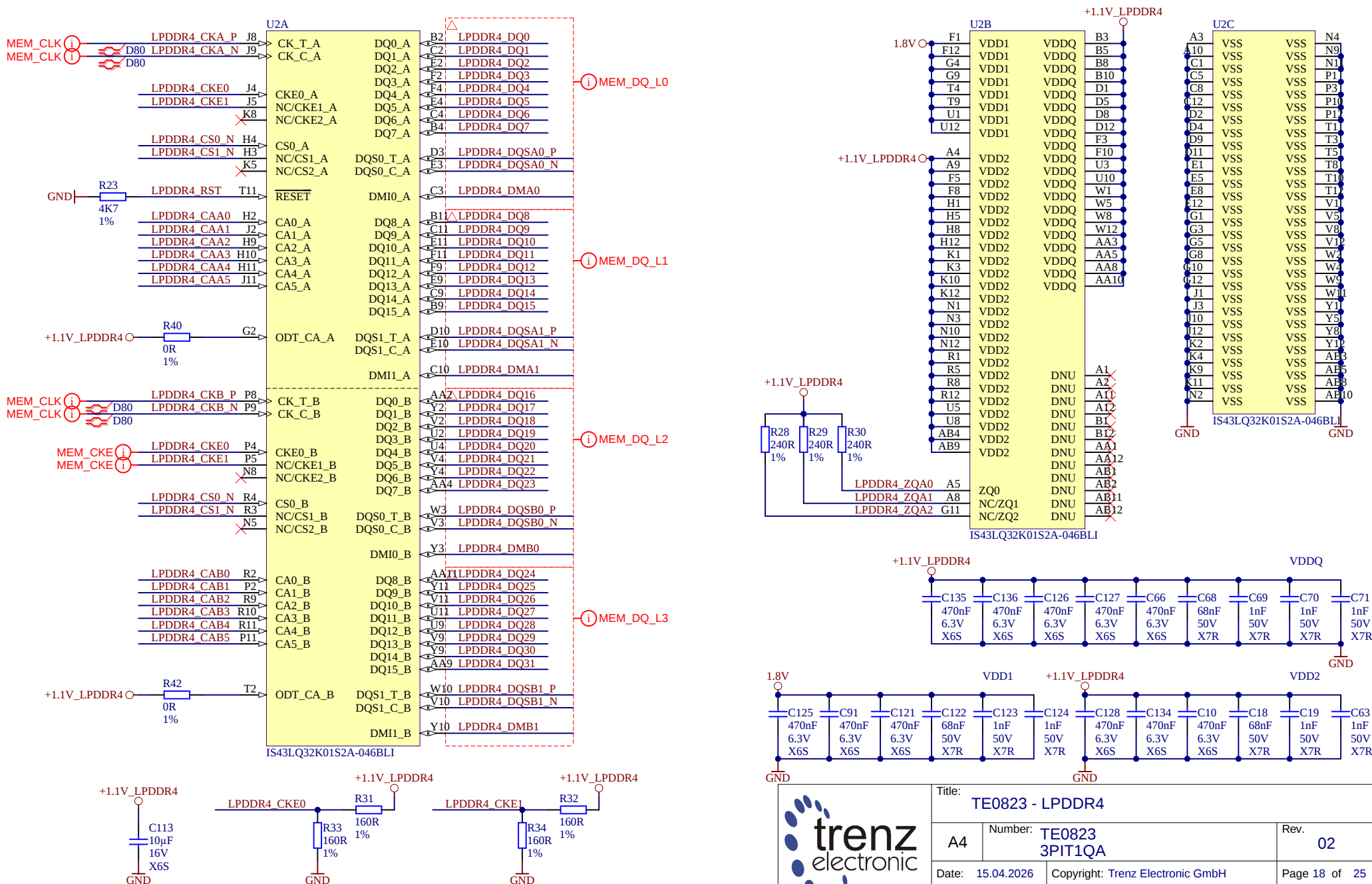
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Filename: CLK.SchDoc		

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Title: TE0823 - LPDDR4		
A4	Number: TE0823 3PIT1QA	Rev. 02
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Filename: LPDDR4.SchDoc		Page 18 of 25

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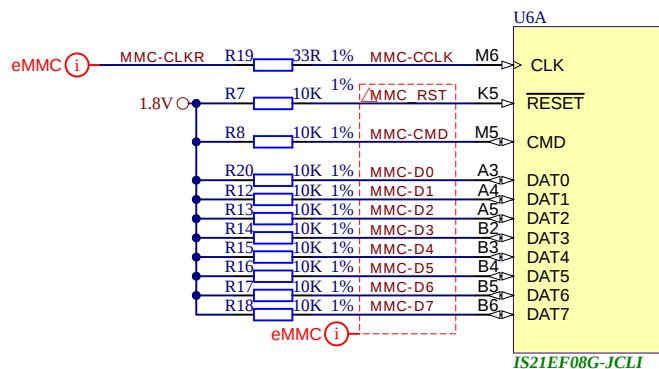
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4

U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M1
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
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F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

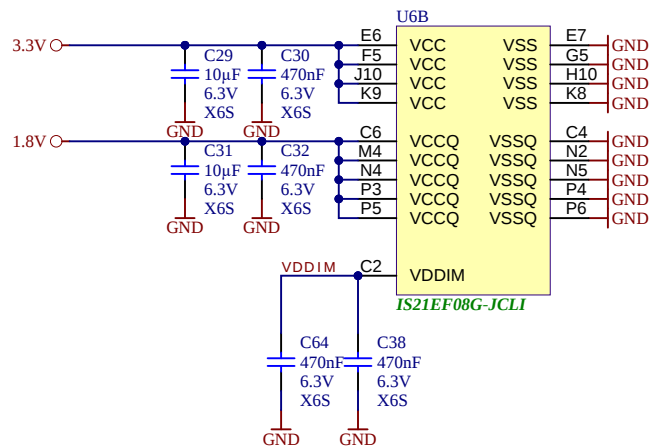
IS21EF08G-JCLI



U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
F10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

IS21EF08G-JCLI



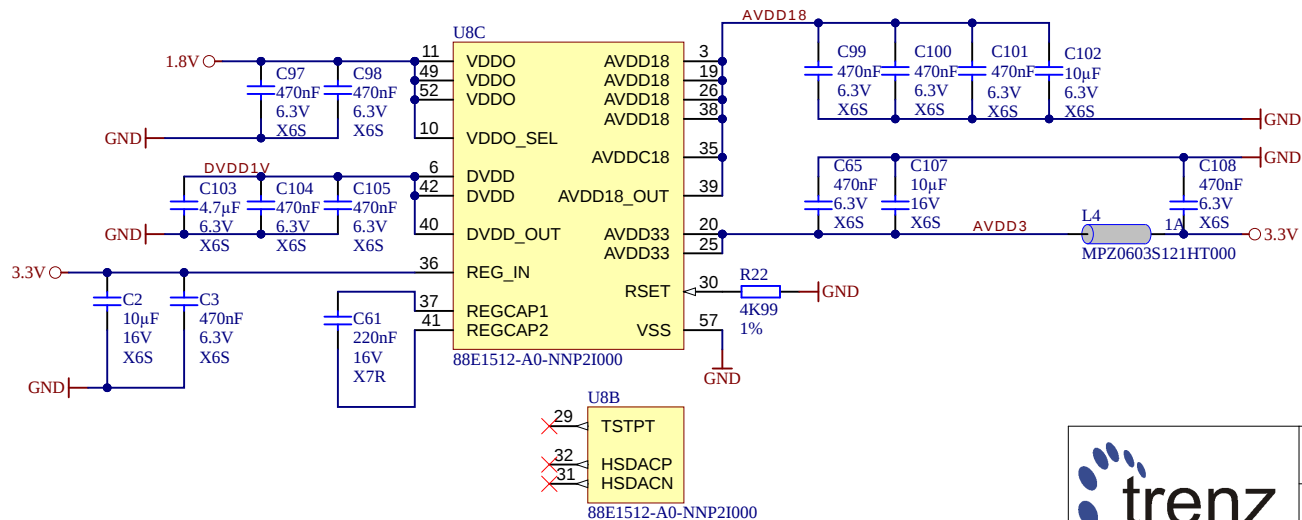
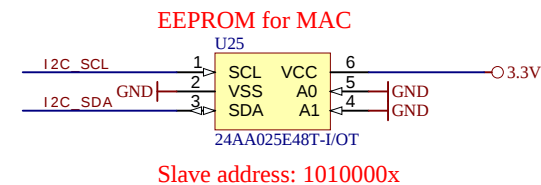
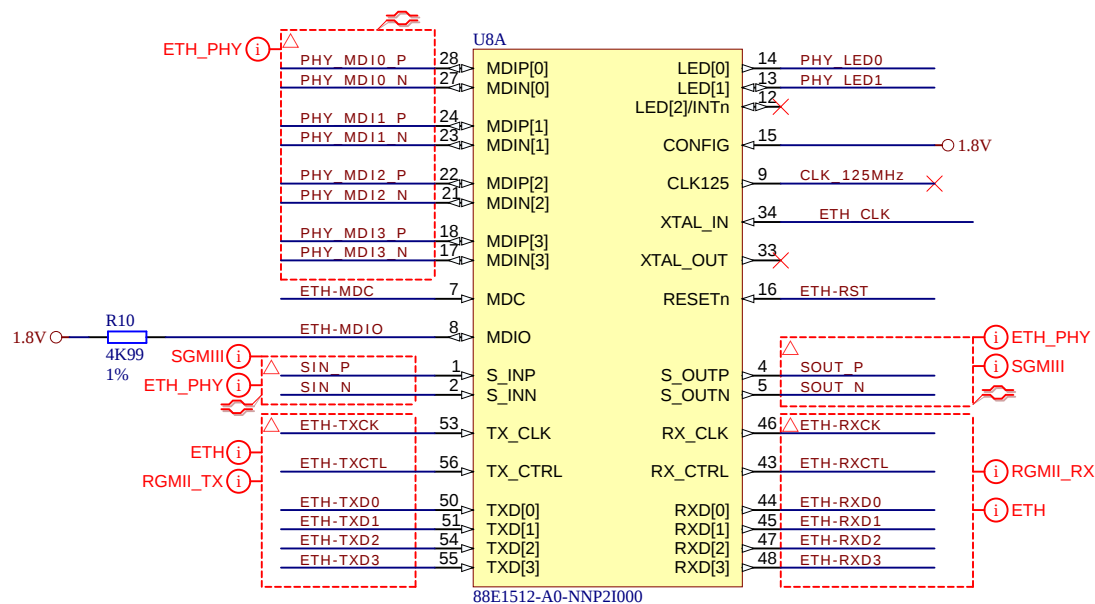
Title: TE0823 - eMMC		
A4	Number: TE0823 3PIT1QA	Rev. 02
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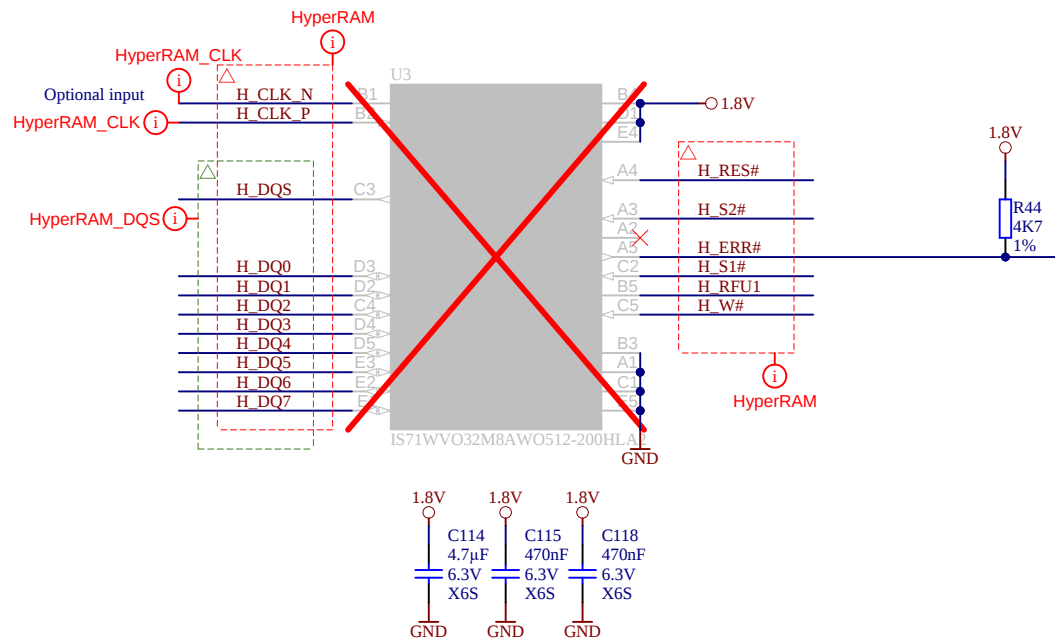
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Title: TE0823 - ETH-PHY		
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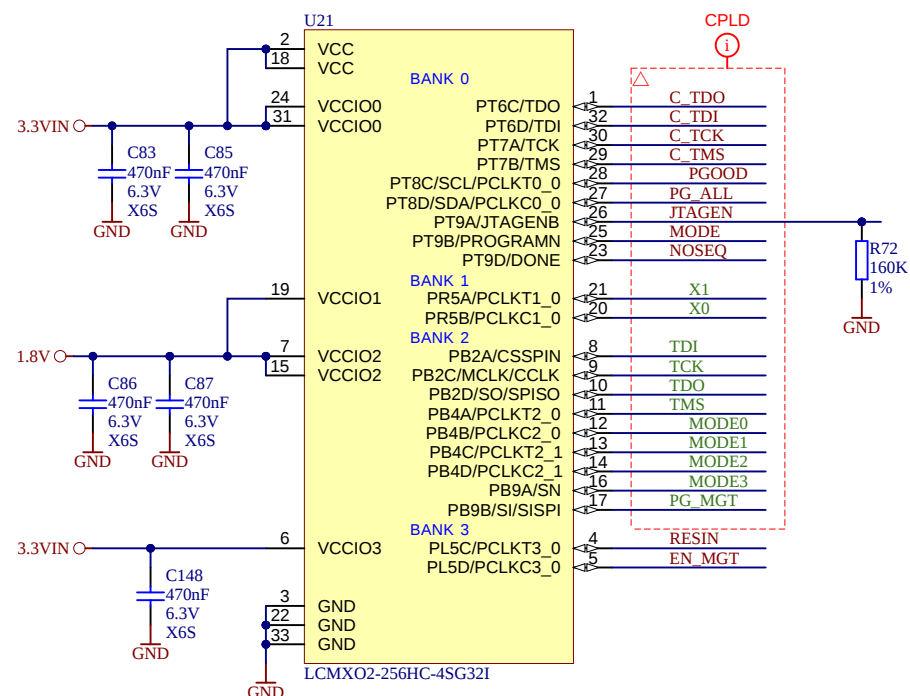
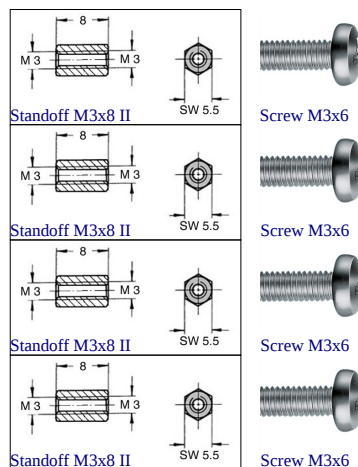
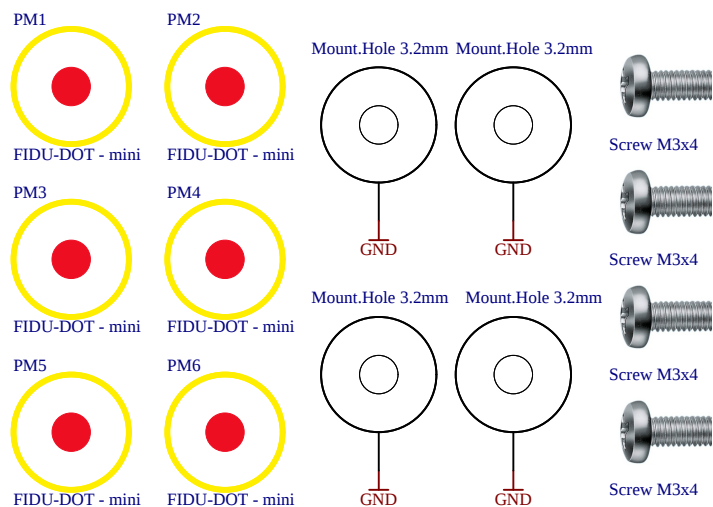
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Title: TE0823 - HyperRAM		
A4	Number: TE0823 3PIT1QA	Rev. 02
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Filename: HyperRAM.SchDoc		

Special notes:

Serial
Serial
Serialnumber 6,3 x 6.3mm



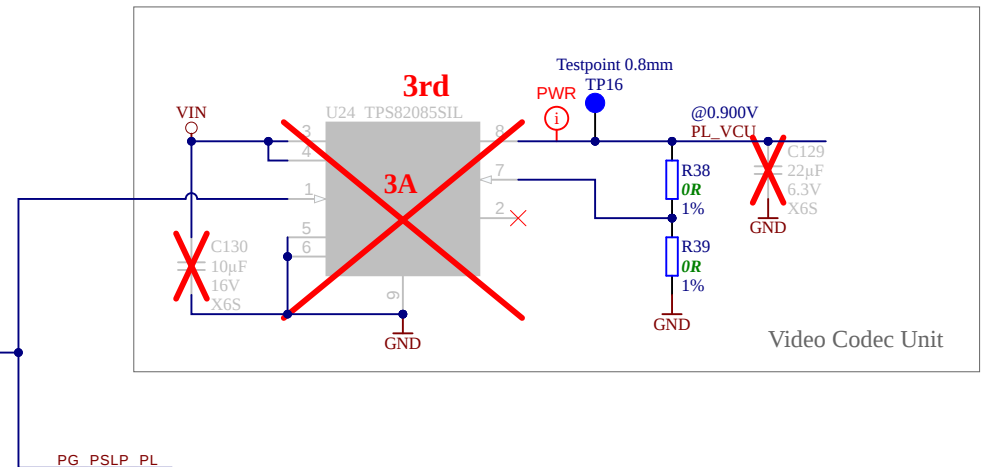
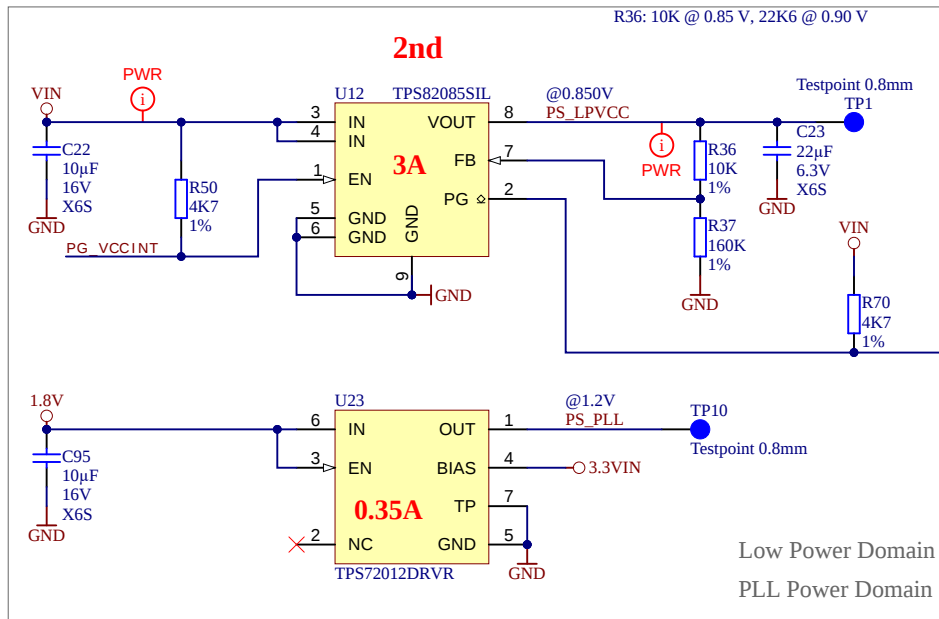
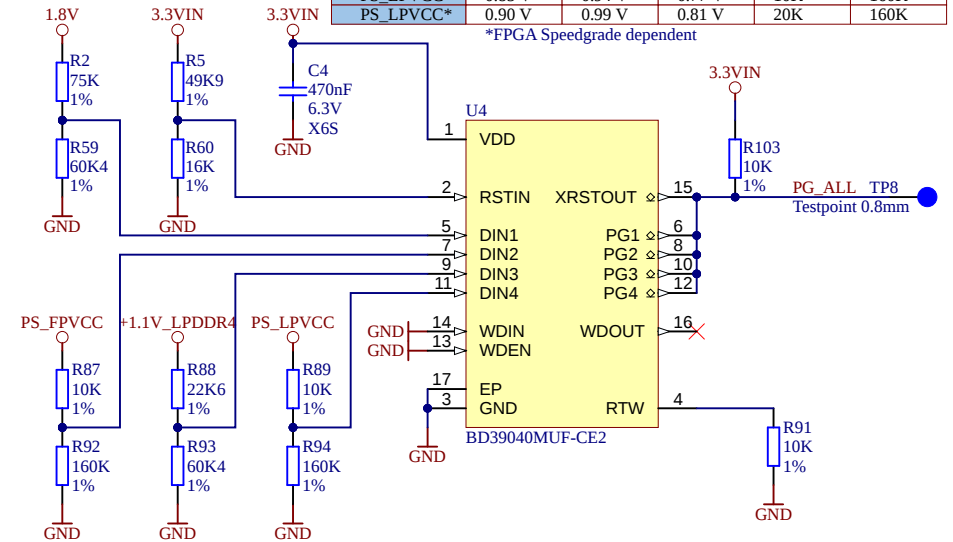
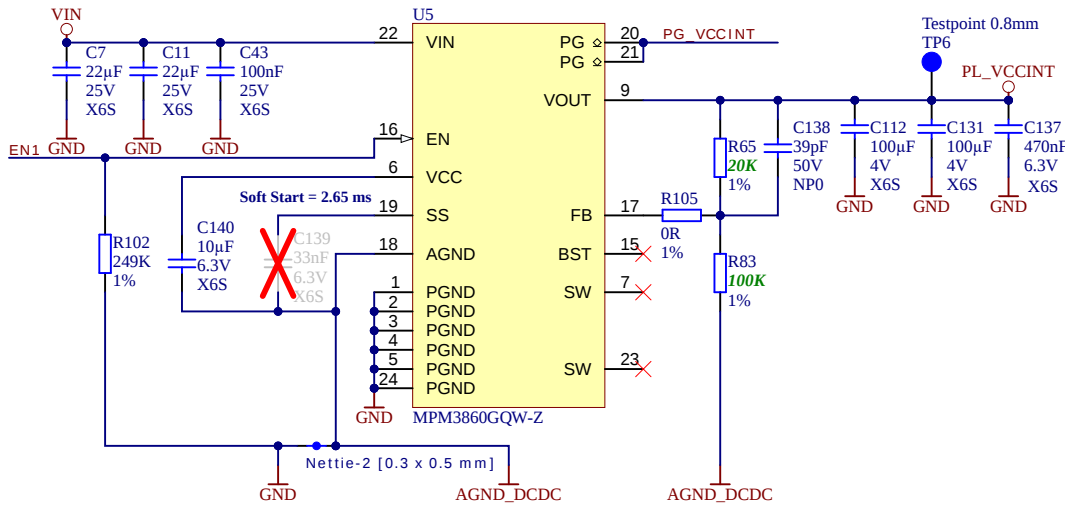
Title: TE0823 - CPLD		
A4	Number: TE0823 3PIT1QA	Rev. 02
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FPGA Speedgrade	Resistor values	Voltage
-1 / -2	R65 - 24K9, R83 - 60K4	PL_VCCINT = 0.847 V
-2E	R65 - 24K9, R83 - 49K9	PL_VCCINT = 0.899 V
-1L1 / 2LE	R65 - 20K, R83 - 100K	PL_VCCINT = 0.720 V

Net	Nominal	OV	UV	R _{ti}	R _{ti}
3.3VIN	3.3 V	3.63 V	2.97 V	49K9	16K
1.8V	1.8 V	1.98 V	1.62 V	75K	60K4
PS_FPVCC*	0.85 V	0.94 V	0.77 V	10K	160K
PS_FPVCC*	0.90 V	0.99 V	0.81 V	20K	160K
+1.1V_LPDDR4	1.1 V	1.21 V	0.99 V	22K6	60K4
PS_LPVCC*	0.85 V	0.94 V	0.77 V	10K	160K
PS_LPVCC*	0.90 V	0.99 V	0.81 V	20K	160K

*FPGA Speedgrade dependent



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