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 Schematics and other handouts serve for informational purposes only!

| | |
|-------------------|------------|
| Design drawn by: | ED |
| Checked by: | MR |
| Assembly variant: | 93E31-A |
| Created by: | MR |
| Modified by: | MR |
| Modified at: | 2021-02-19 |



| | | |
|--|----------------------------------|--------------|
| Title: TE0745 - Legal Notices Modules | | |
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| Filename: Legal Notices Modules.SchDoc | | |

| REV | Description | |
|-----|---|----|
| -01 | Initial revision | |
| -02 | 1. MAC EEPROM Address patch fixed on PCB. 2. Lib components update. | |
| -03 | <p>1. Removed serial number S/N. Connected U2 pin 20 to net "BOOTMODE".</p> <p>2. Changed DCDC (U4) from EN63A0Q1 to MP8869SGL-Z and adapted corresponding circuit. Added assembly option to connect U4 to I2C bus via R91/R101 (I2C address 0x61).</p> <p>3. Increase rated voltage for capacitors C108, C142, C147, C148, and C149 from 6.3 V to 25 V.</p> <p>4. Added diode D3 between signal "RST_IN_N" and "PS_1.8V".</p> <p>5. Added resistor R106 between CPLD U2 pin 25 and signal "RST_IN_N".</p> <p>6. Added option for diode D4 population between signal "PROG_B" and "INIT".</p> <p>7. Changed clock U33 from SiT8008A1-73-XXS-52.000000E to SiT8008BI-73-XXS-52.000000E.</p> <p>8. Added testpoints TP1...43.</p> <p>9. Added voltage monitors U20 and U22 with according circuits.</p> <p>10. Added pull-up resistor R73 for net "PWR_PL_OK".</p> <p>11. Added resistor R103 to optionally connect U31 PG to signal "PWR_PS_OK" or voltage monitor U20.</p> <p>12. Changed supply voltage for VCCPLL from PL_1.8V to PS_1.8V.</p> <p>13. Tied DXP/DXN (U1 pins R14 and R13) directly to GND.</p> <p>14. Added soft start capacitor options C62 for U8 and C78 for U11.</p> <p>15. Added decoupling capacitors</p> <ul style="list-style-type: none"> - C126, C127 for U16, - C129 for U14, - C130 for U19, - C131 for U18, - C144 for U8, - C150 for U11, - C151/C152 for U6, - C153/C154 for U17, - C155/C156 for U32, and - C128 and C157 for U1. <p>16. Changed voltage rating from 6.3 V to 10 V for 100 uF capacitors.</p> <p>17. Changed voltage rating from 6.3 V to 16 V for 10 uF capacitors.</p> <p>18. Changed voltage rating from 6.3 V to 10 V and size from 0402 to 0603 for capacitors C21 and C29.</p> <p>19. Changed size from 0201 to 0402 for 1 kOhm resistors R104 and R105.</p> <p>20. Added 100 Ohm termination resistors R109 and R110 for MGT_REF_CLKs.</p> <p>21. Changed VCCADC_0 supply from VCCIO_0 to PL_1.8V.</p> <p>22. Added UKCA logo.</p> <p>23. Changed voltage divider R21 and R22 to set threshold to 0.936 V.</p> <p>24. Changed DDR clock termination resistor R9 placement position.</p> <p>25. Changed fiducials to standard fiducial type.</p> <p>26. Update revision history.</p> <p>27. Update schematic template.</p> <p>28. Updated power overview.</p> <p>29. Removed page "ZYNQ.SchDoc" and added pages Legal Notices, System Overview.</p> | ED |

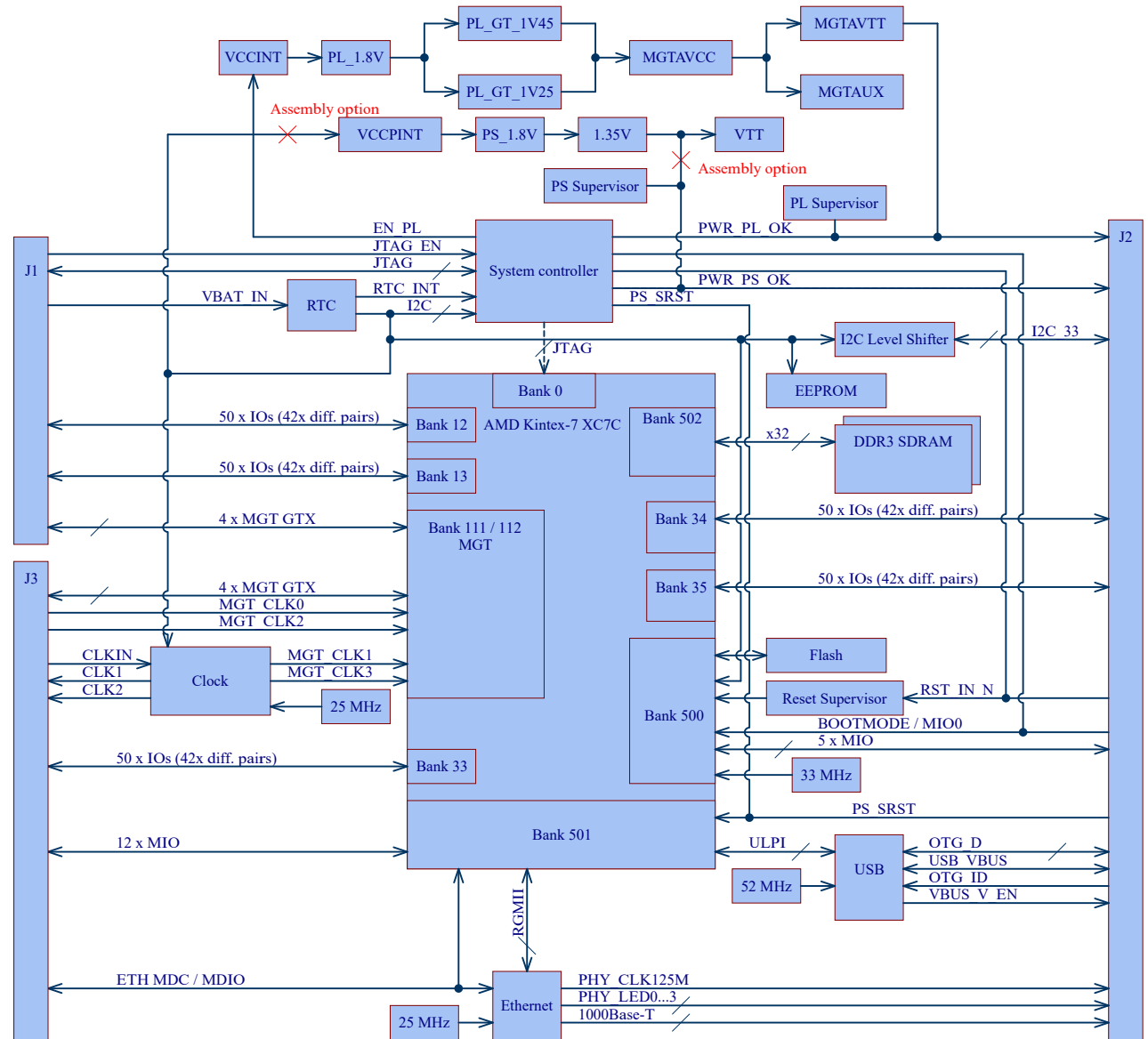
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|  | | Title: TE0745 - Revision Changes | | |
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I2C Address:

| Device | I2C ADDR | Note |
|------------|----------|--------------------|
| SoC U1G | - | I2C Master |
| CPLD U2 | 0x30 | Firmware dependent |
| DCDC U4 | 0x61 | Assembly option |
| PLL U16 | 0x70 | - |
| RTC U24 | 0x6F | RTC register |
| RTC U24 | 0x57 | User SRAM |
| EEPROM U23 | 0x53 | - |

Supported Voltage Ranges:

| Power Rail | Direction | Range | Tolerance | Description | Note |
|------------|-----------|---------------|-----------|-------------------|--------------------|
| PS_3.3V | IN | 3.3 V | +/- 5 % | Micromodule Power | - |
| PS_VIN | IN | 3.3 V | +/- 5 % | Micromodule Power | - |
| PL_VIN | IN | 3.2 V - 4.5 V | - | Micromodule Power | within given range |
| VCCIO_12 | IN | 1.2 V - 3.3 V | +/- 3 % | HR IO Bank 12 | - |
| VCCIO_13 | IN | 1.2 V - 3.3 V | +/- 3 % | HR IO Bank 13 | - |
| VCCIO_33 | IN | 1.2 V - 1.8 V | +/- 3 % | HP IO Bank 33 | - |
| VCCIO_34 | IN | 1.2 V - 1.8 V | +/- 3 % | HP IO Bank 34 | - |
| VCCIO_35 | IN | 1.2 V - 1.8 V | +/- 3 % | HP IO Bank 35 | - |
| VBAT_IN | IN | 1.8 V - 3.3 V | - | RTC | within given range |
| PS_1.8V | OUT | 1.8 V | +/- 3 % | Power for Carrier | - |
| PL_1.8V | OUT | 1.8 V | +/- 3 % | Power for Carrier | - |

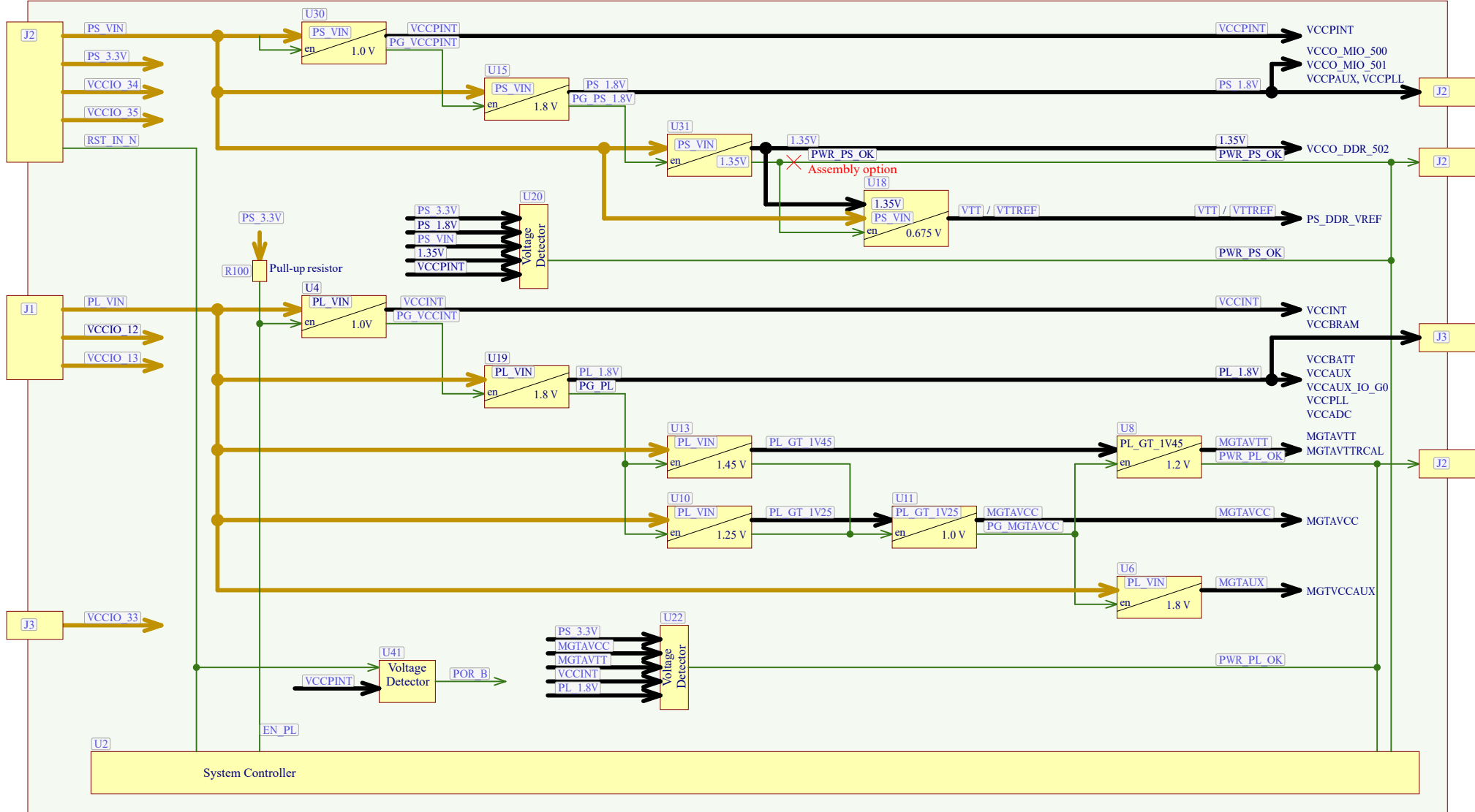


FPGA-PWR



| | | |
|---------------------------------|----------------------------------|--------------|
| Title: TE0745 - System Overview | | |
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Power-on sequencing:



| | | |
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Special notes:

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE

CE Logo on Top Overlay

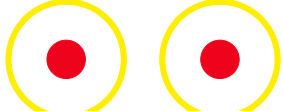
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LOGO1

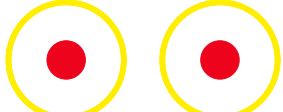
TE Logo PRINT Layer

LOGO PRINT

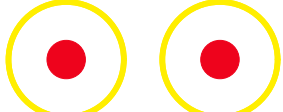
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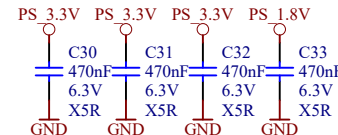
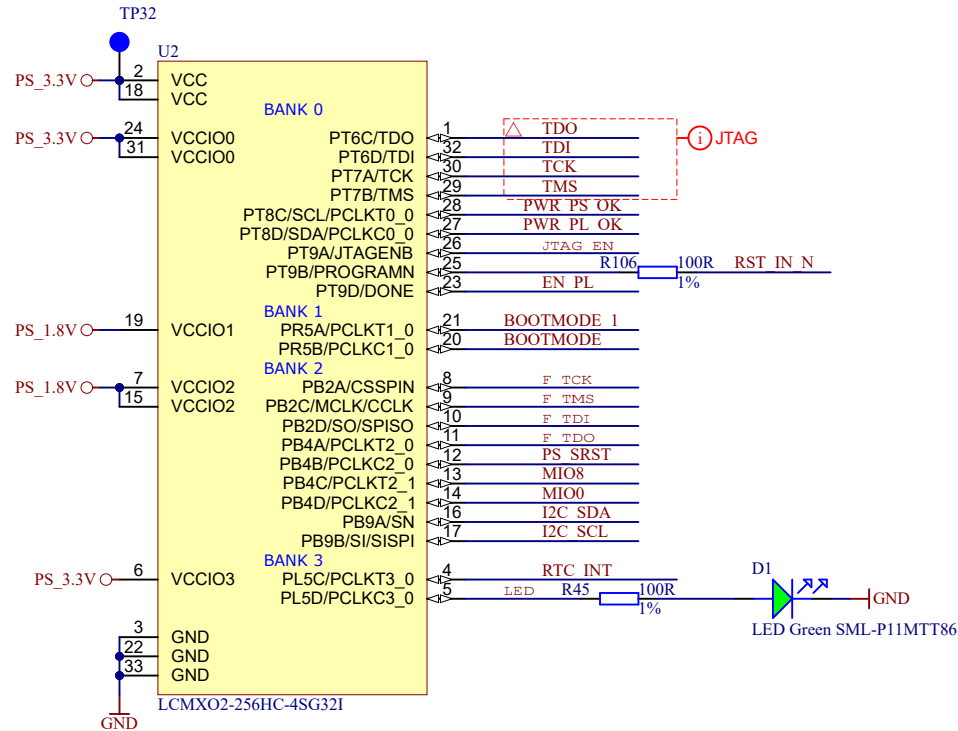
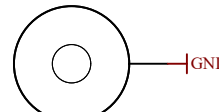
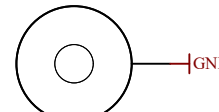
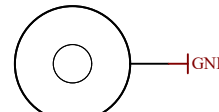
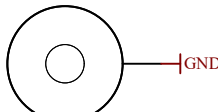
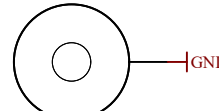
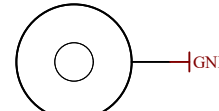
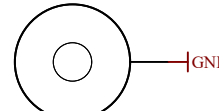
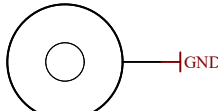
PM1 FIDU-DOT - small PM2 FIDU-DOT - small



PM3 FIDU-DOT - small PM4 FIDU-DOT - small



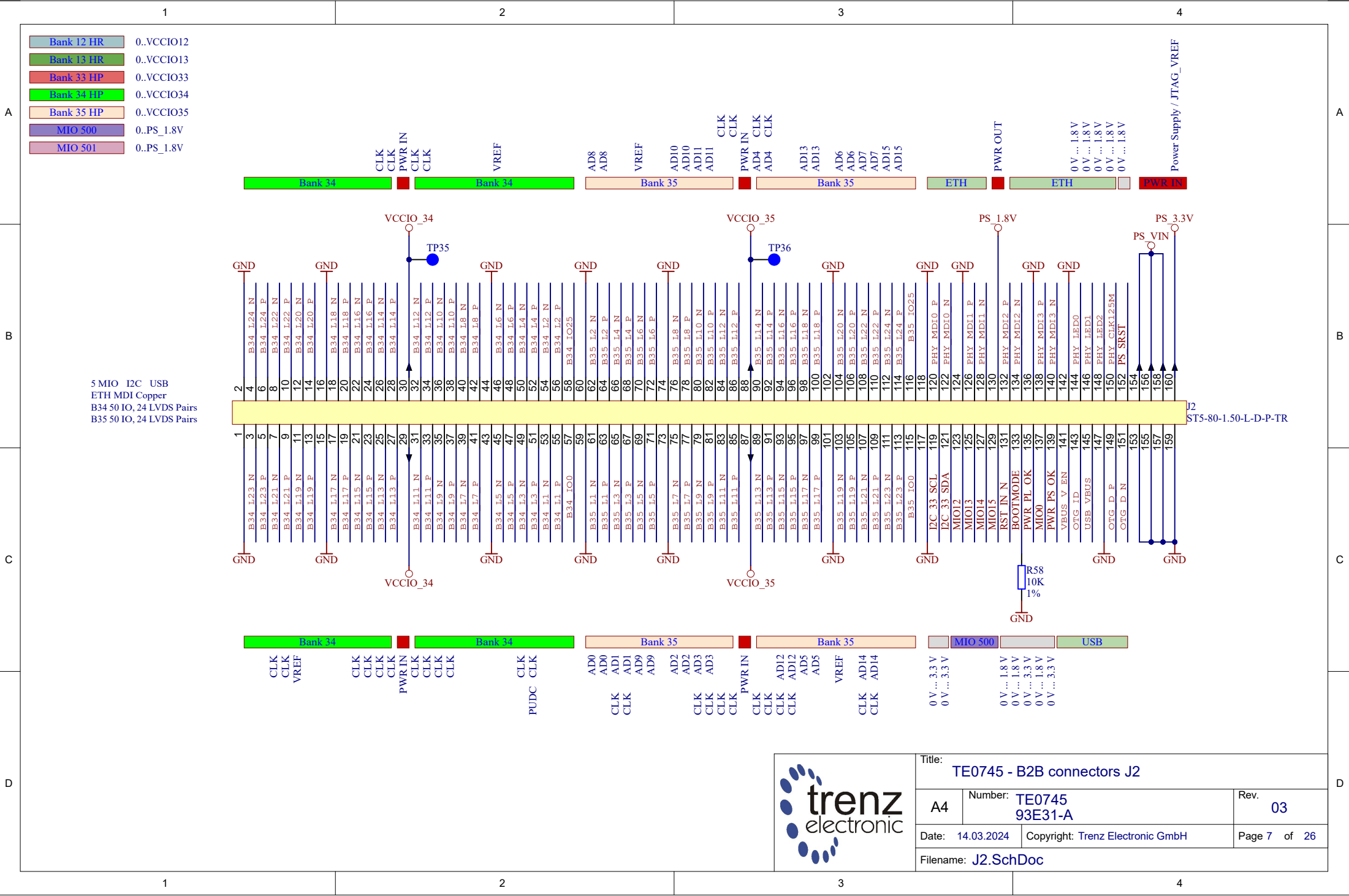
PM5 PM6



Serial
SerialNumber 6,3 x 6.3mm



| | | |
|-----------------------------------|----------------------------------|--------------|
| Title: TE0745 - System Controller | | |
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| Filename: TE0745.SchDoc | | |

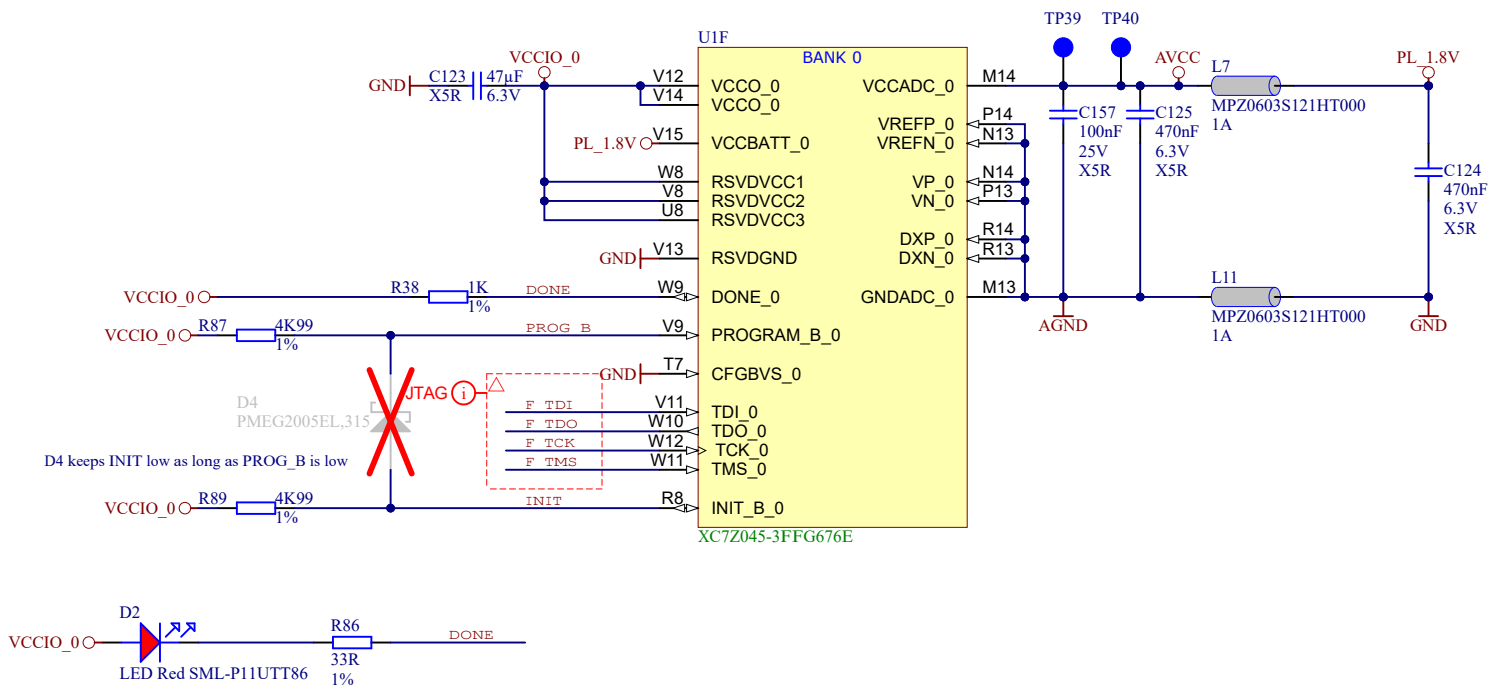
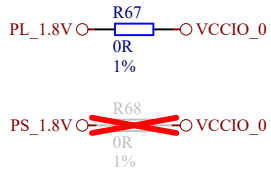


5 MIO I2C USB
 ETH MDI Copper
 B34 50 IO, 24 LVDS Pairs
 B35 50 IO, 24 LVDS Pairs

J2
 ST5-80-1.50-L-D-P-TR

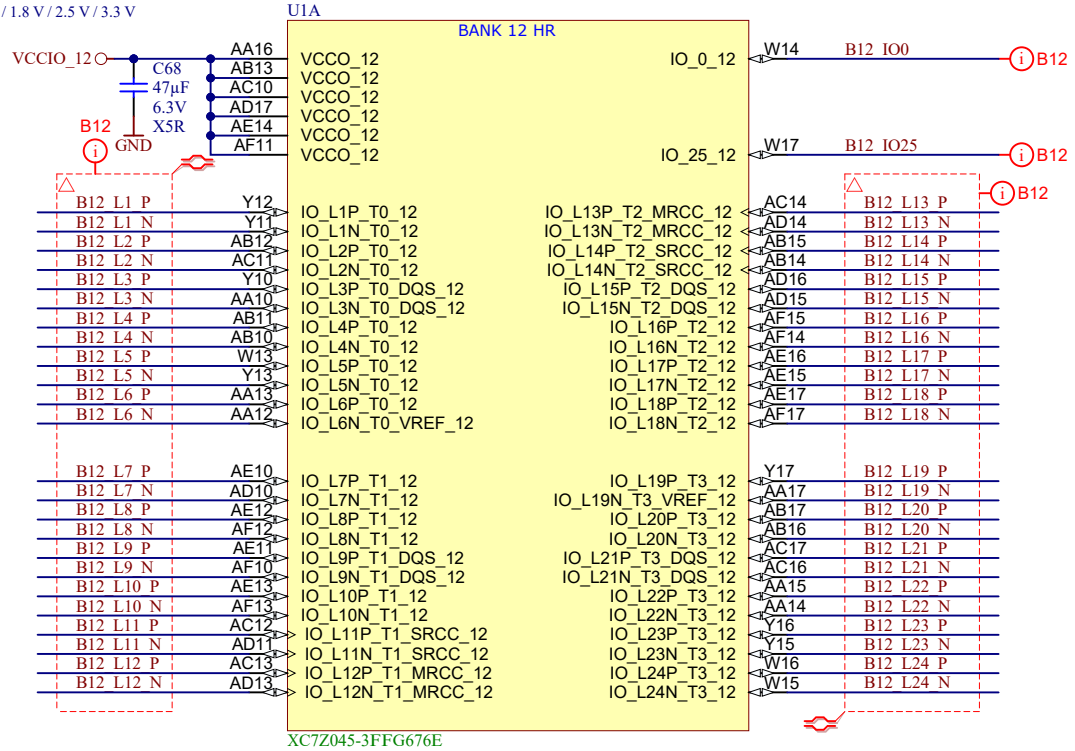


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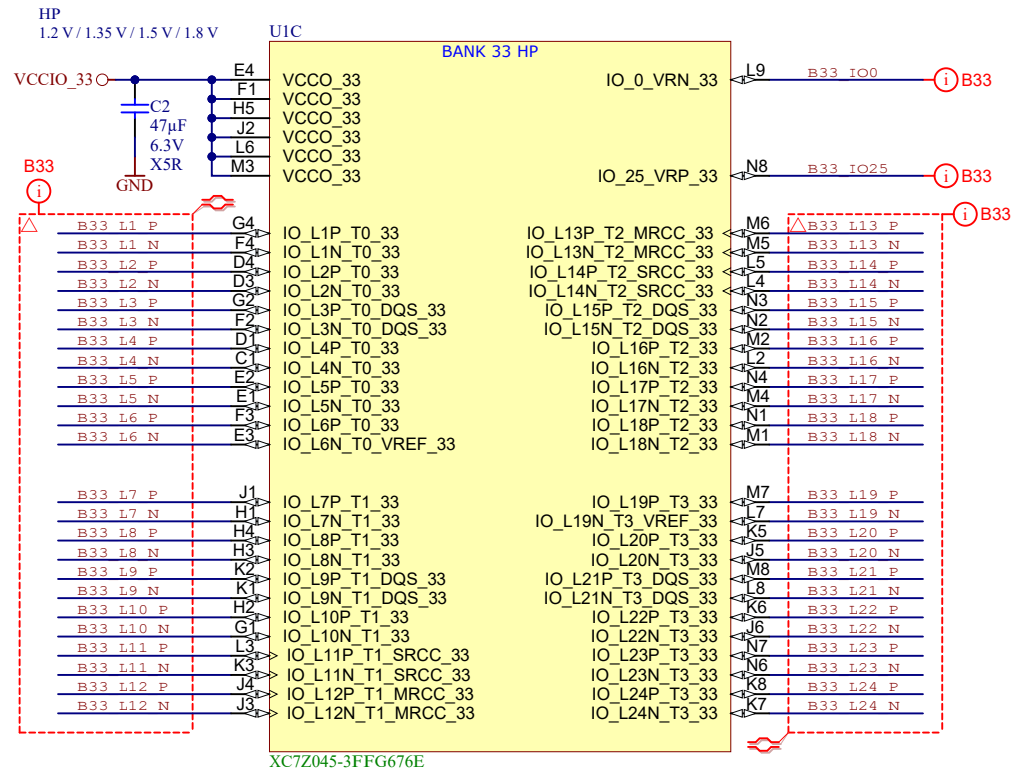


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| | Title: TE0745 - Zynq_MISC | |
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| Filename: ZYNQ_MISC.SchDoc | | |

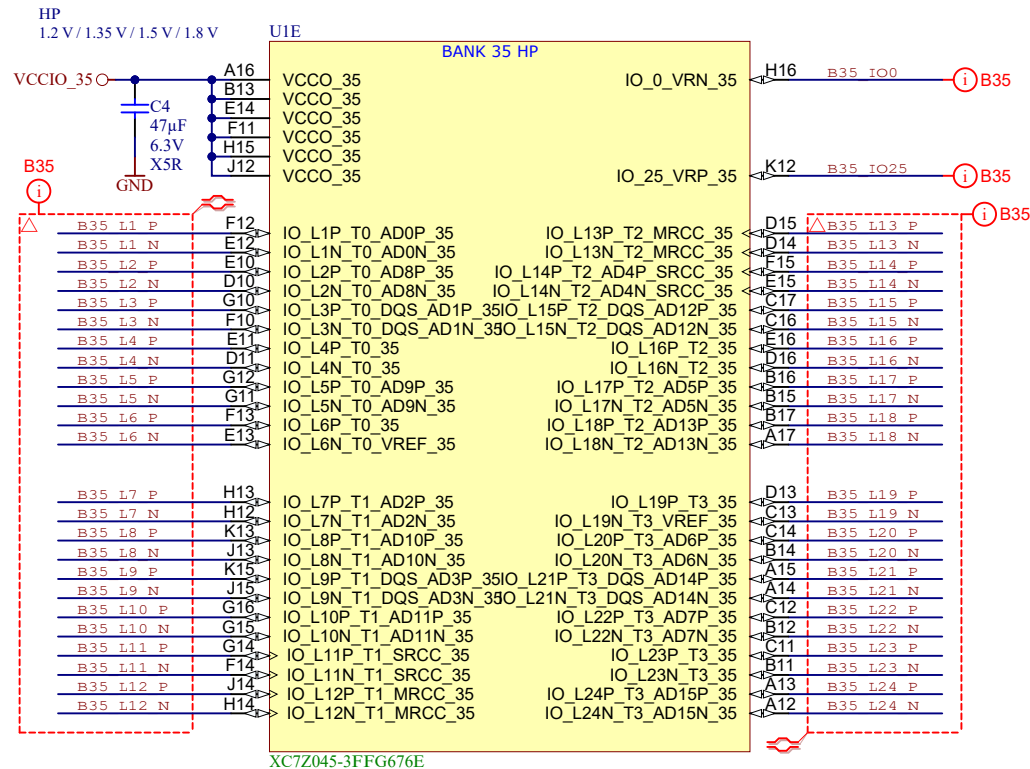
HR
1.2 V/1.35 V/1.5 V/1.8 V/2.5 V/3.3 V




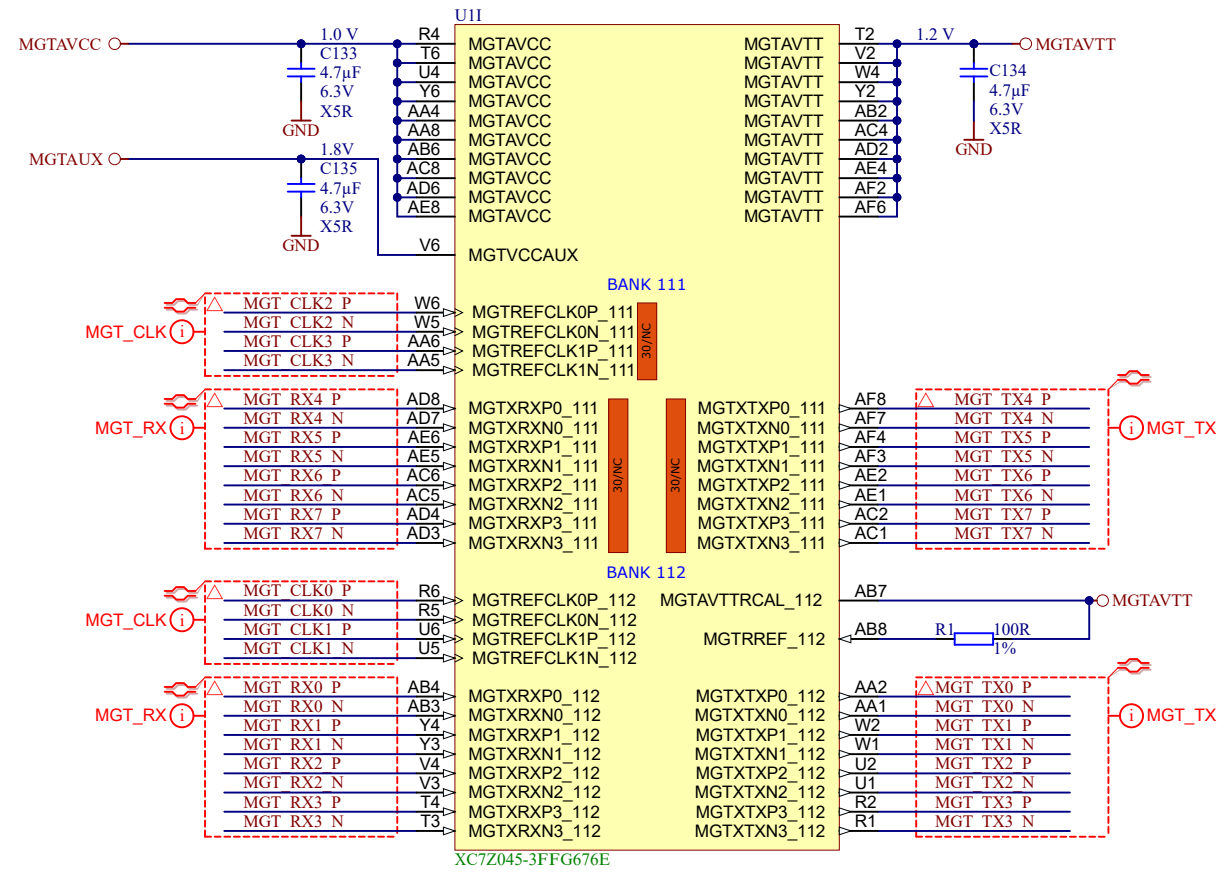
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| Title: TE0745 - Zynq_B12 | | |
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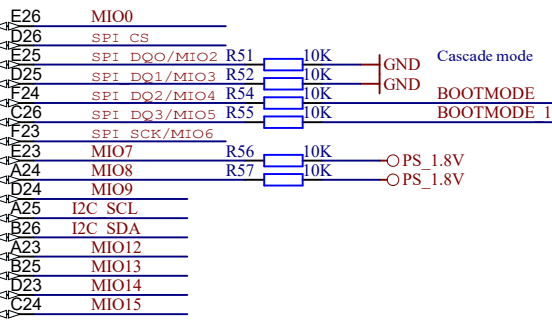
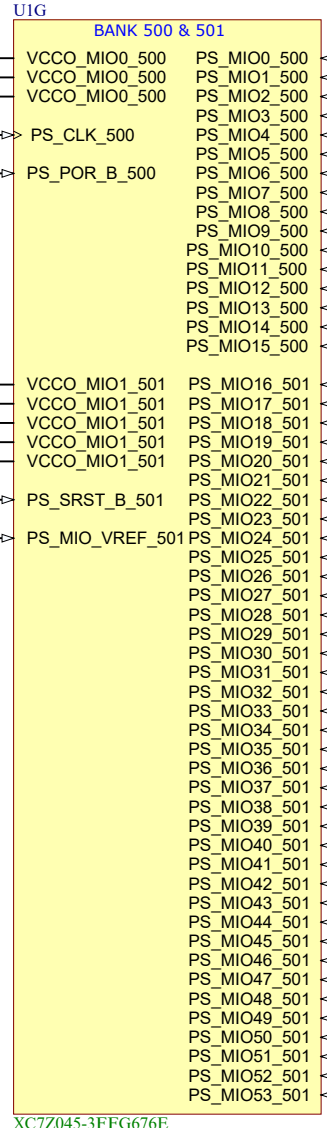
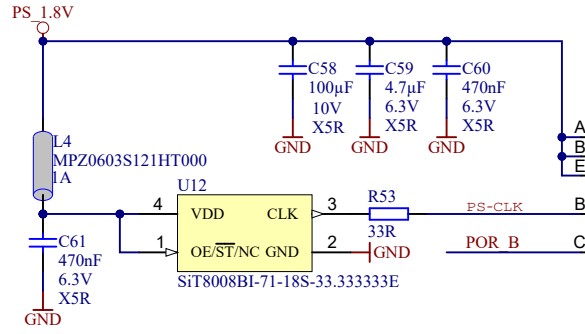
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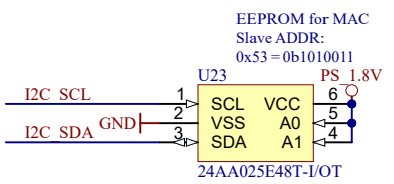
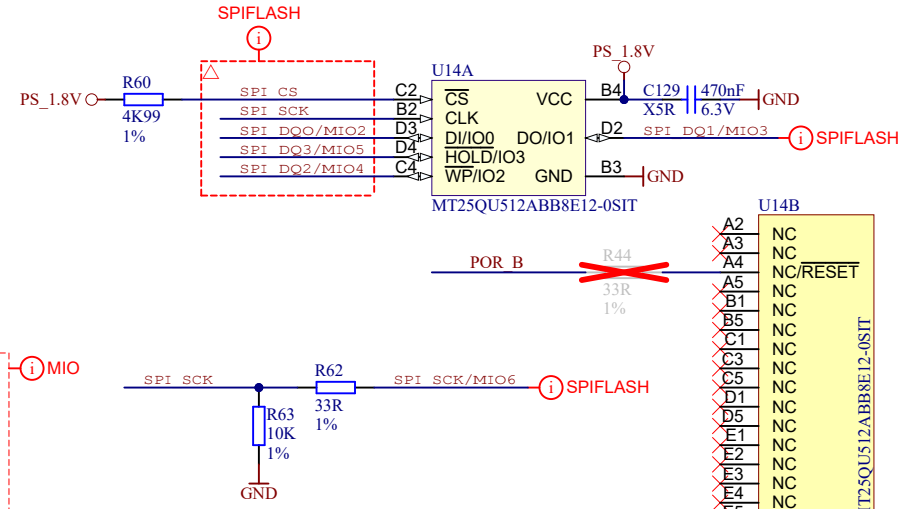
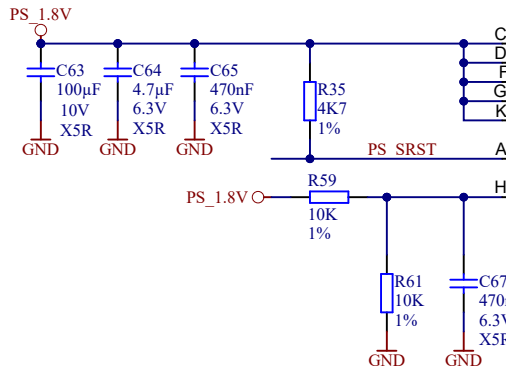


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| Title: TE0745 - Zynq_MGT | | |
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| MIO Bank Voltage | MIO7 Bank0 | MIO8 Bank1 |
|------------------|------------|------------|
| 2.5 V, 3.3 V | 0 | 0 |
| 1.8 V | 1 | 1 |

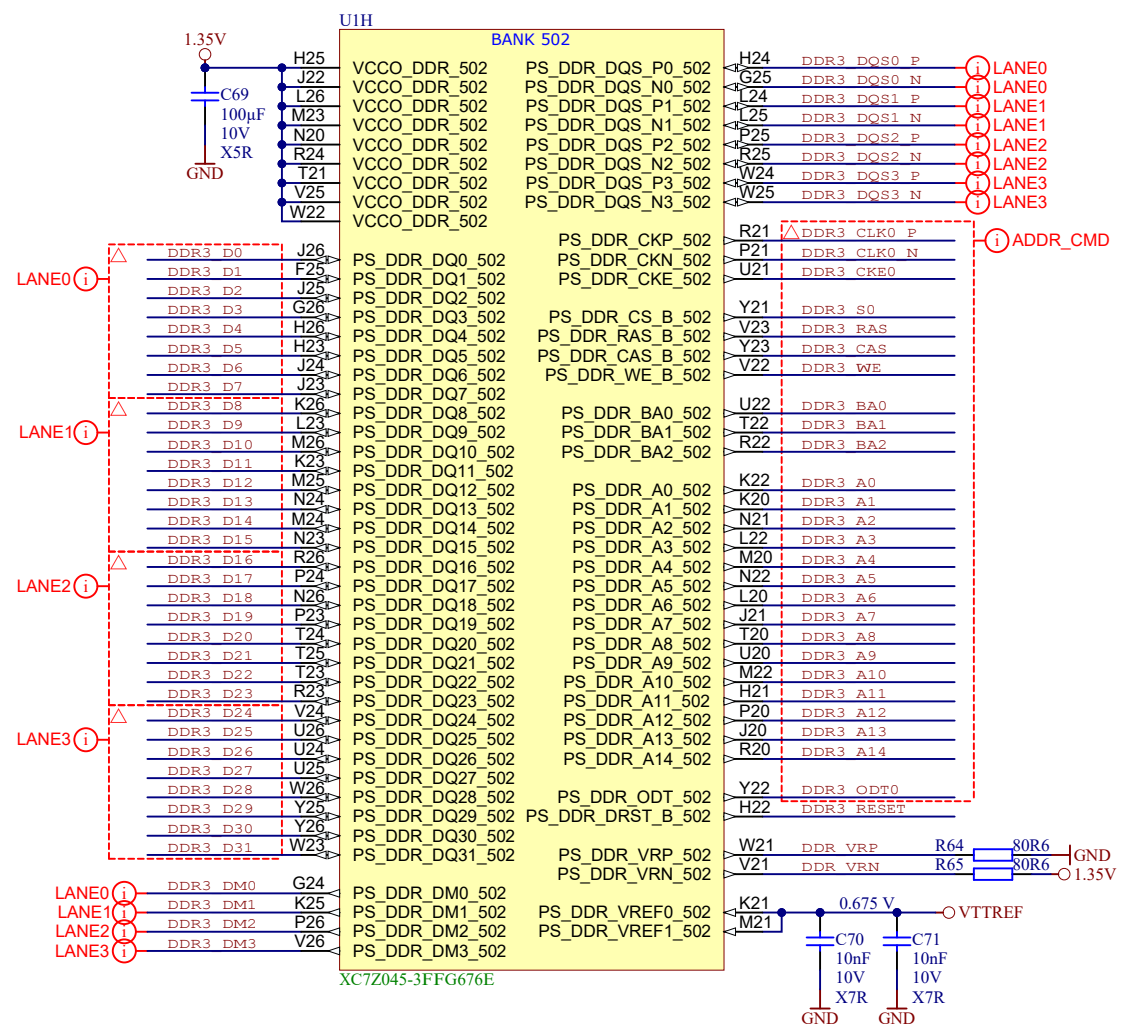
| BOOT MODE | MIO5 | MIO4 | MIO3 |
|----------------|------|------|------|
| JTAG Boot Mode | 0 | 0 | 0 |
| NOR Boot | 0 | 0 | 1 |
| NAND | 0 | 1 | 0 |
| Quad-SPI | 1 | 0 | 0 |
| SD Card | 1 | 1 | 0 |



Title: **TE0745 - Zynq_MIO_Banks**

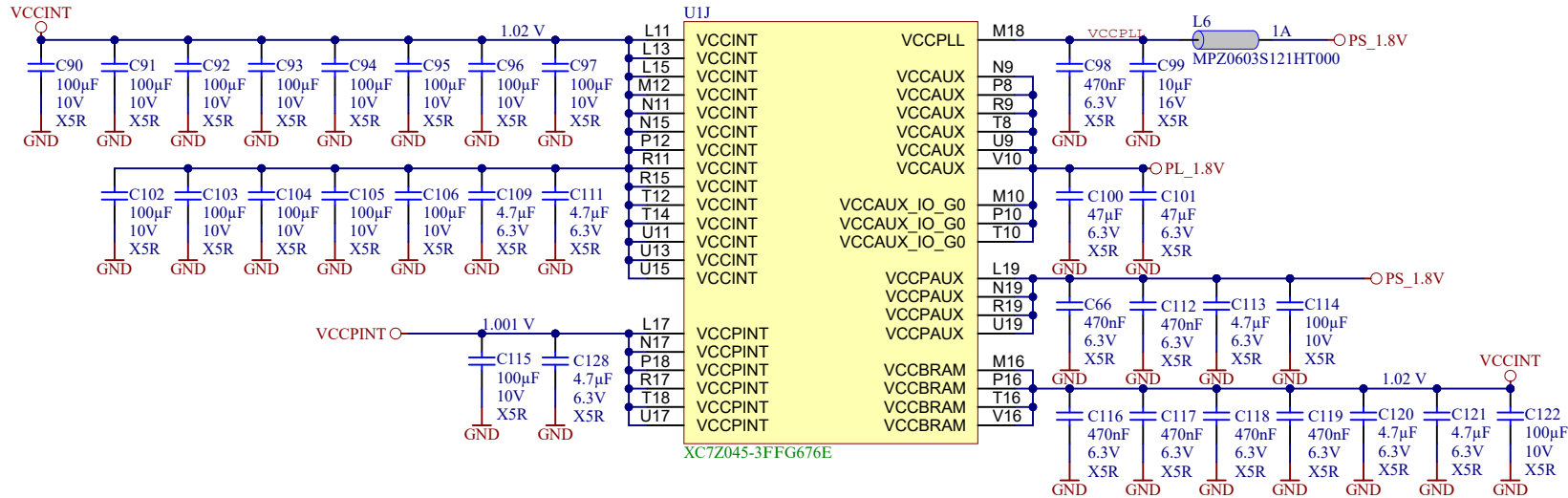
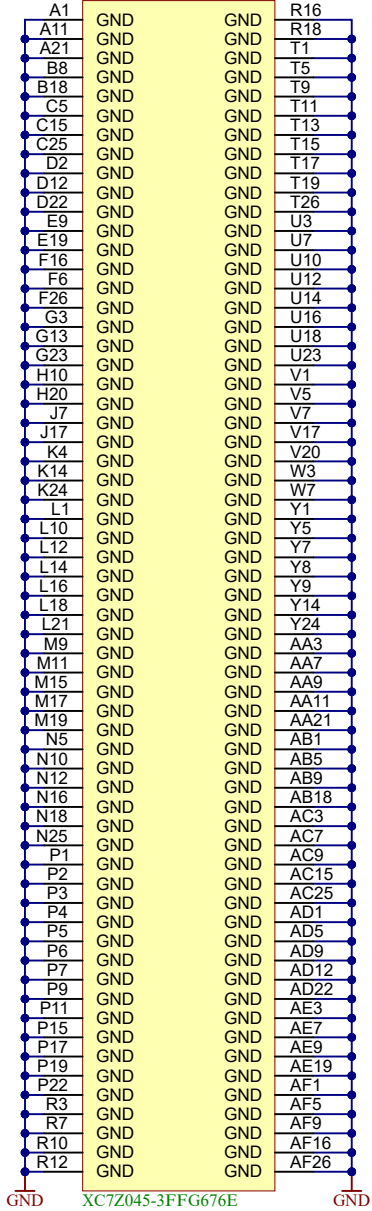
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Filename: **MIO_B500.SchDoc**



| | | |
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| Filename: PS-DDR.SchDoc | | |

UIK



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| Filename: ZYNC_POWER.SchDoc | | |

A

A

B

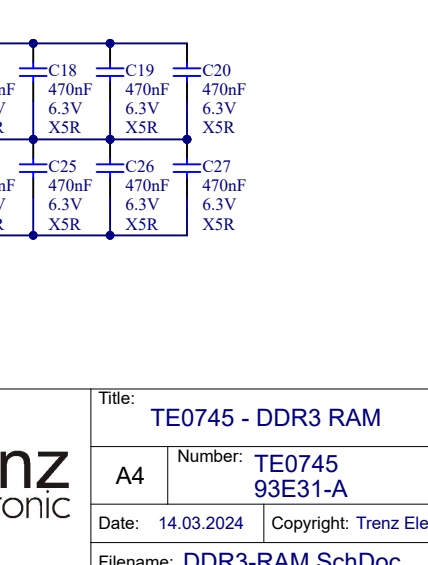
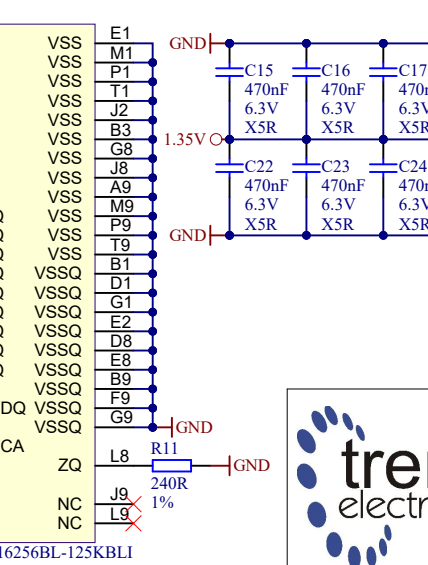
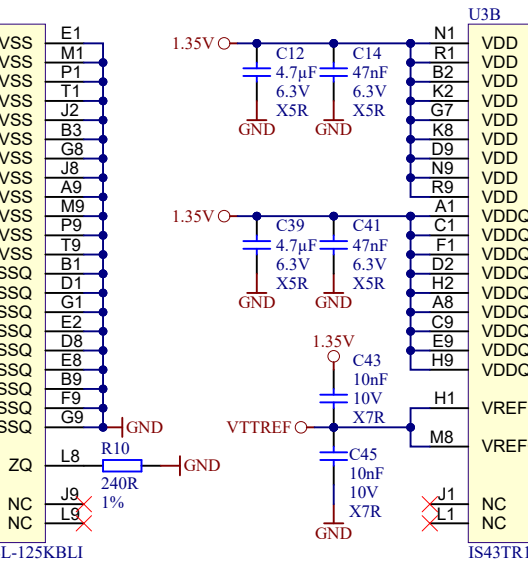
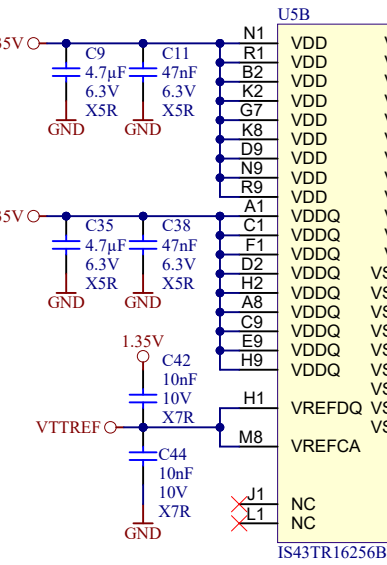
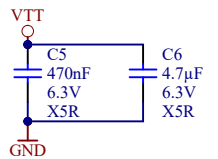
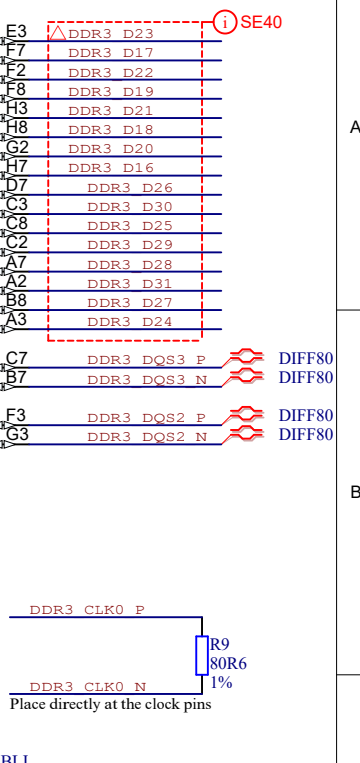
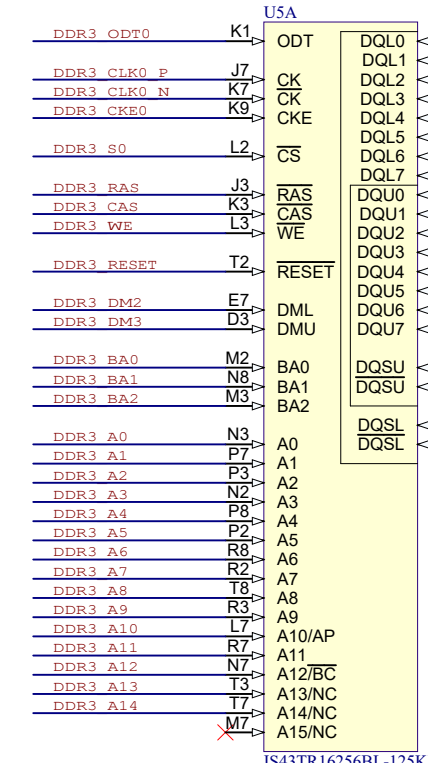
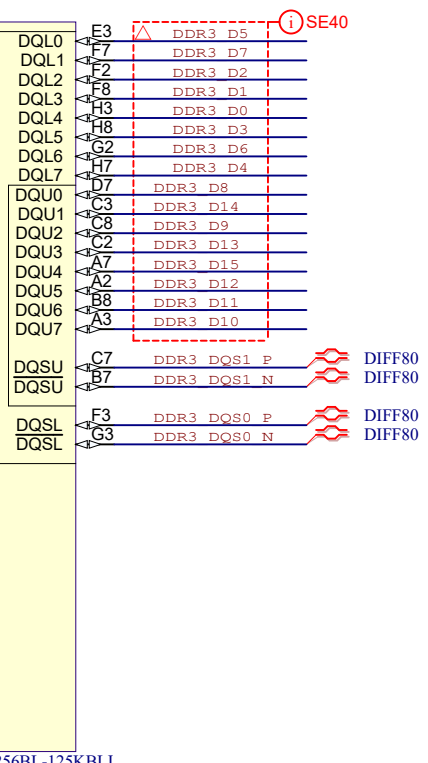
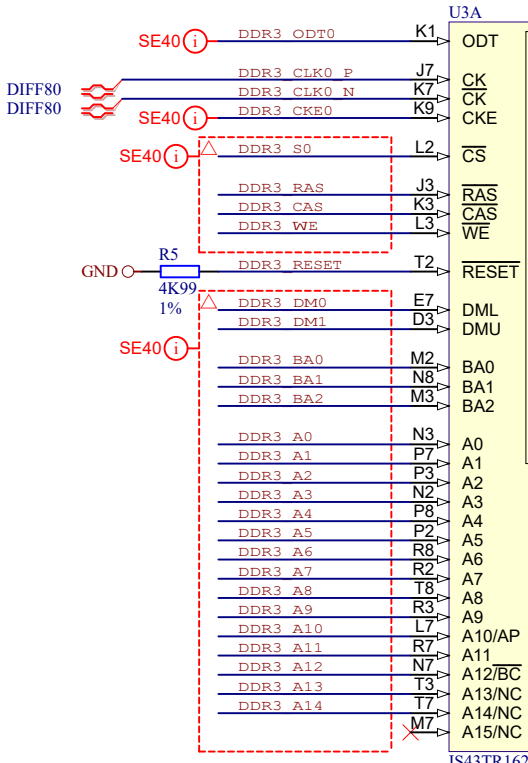
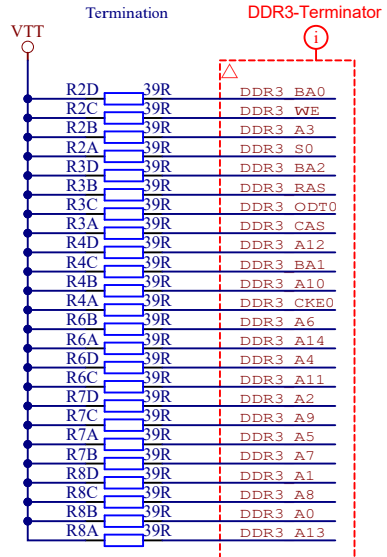
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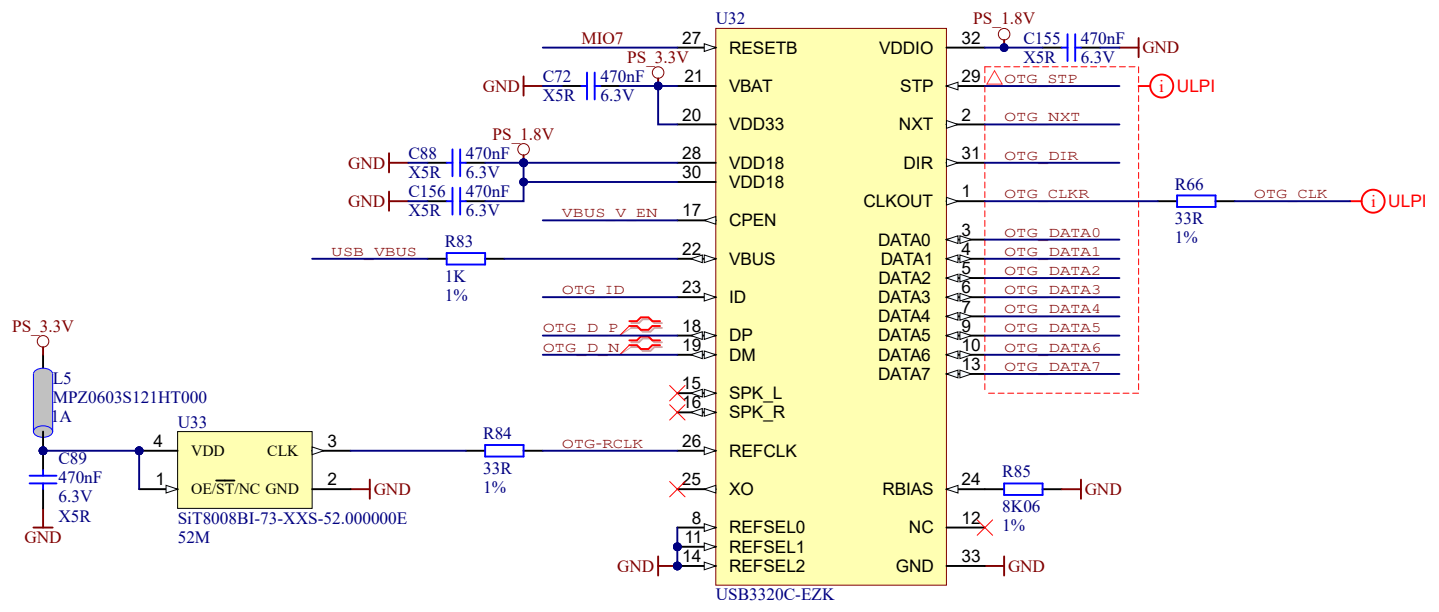
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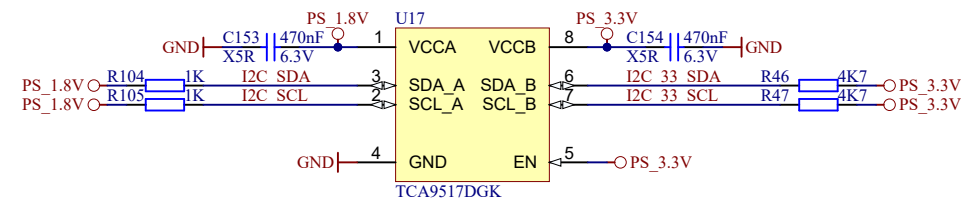
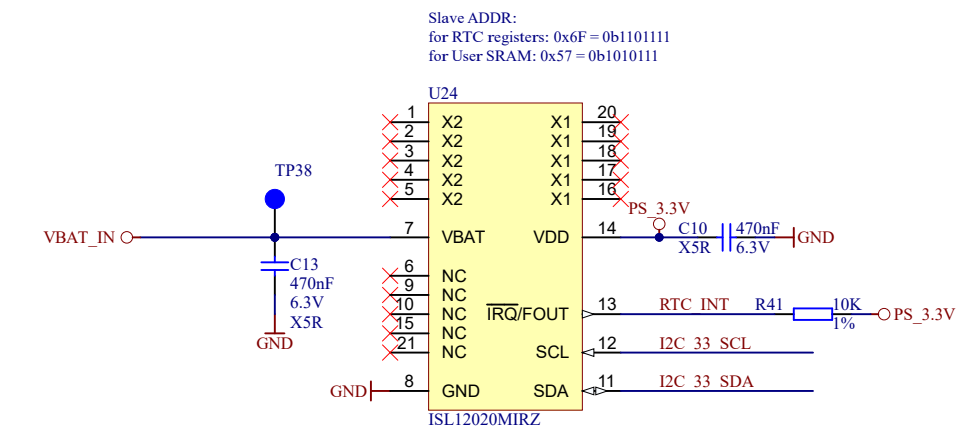

D



| | | |
|---------------------------|----------------------------------|---------------|
| Title: TE0745 - DDR3 RAM | | |
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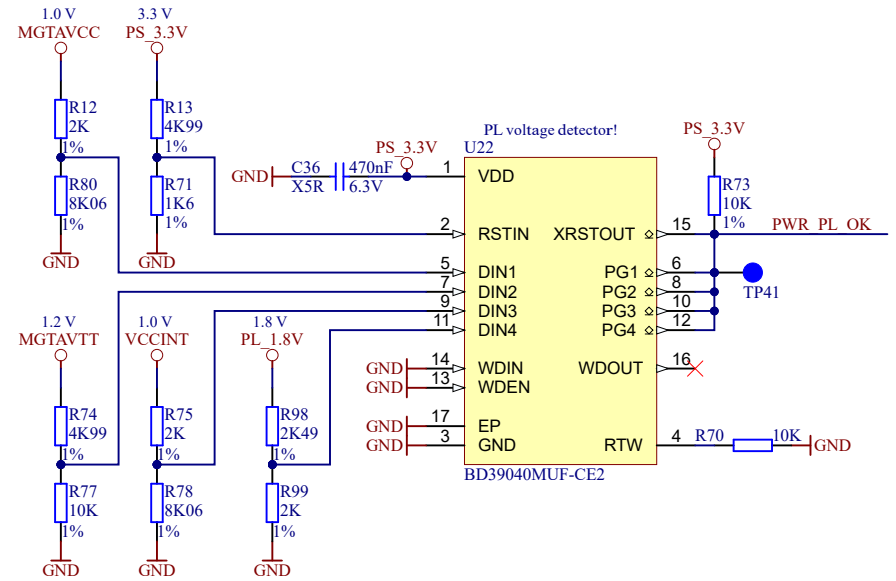
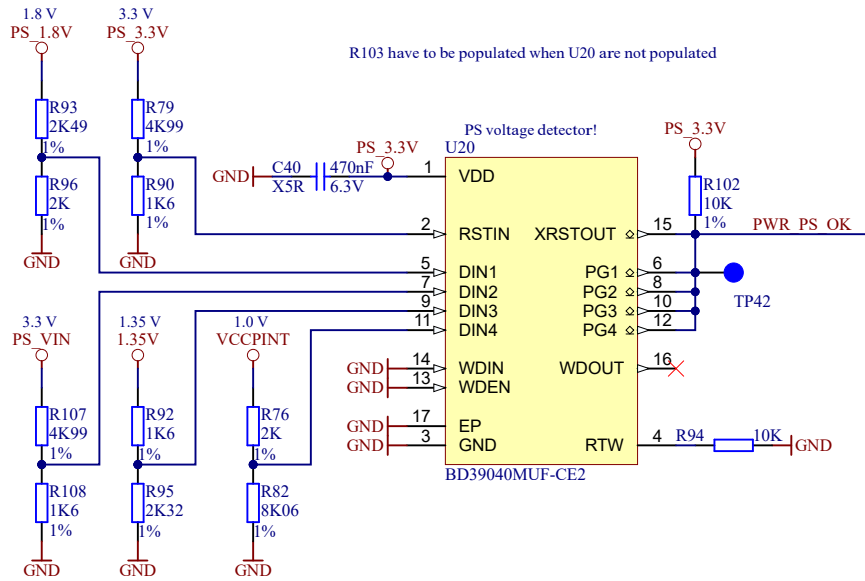
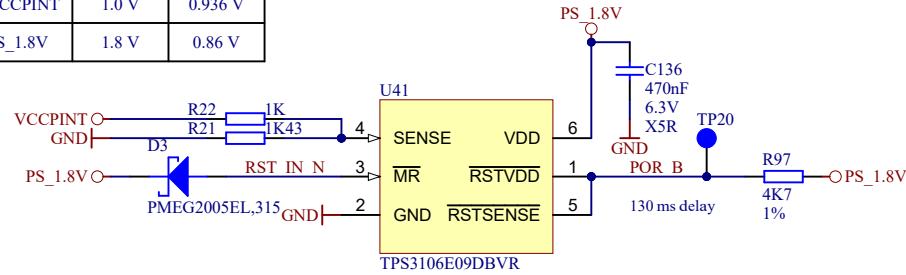


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|--|--------------------------|----------------------------------|---------------|
| | Title: TE0745 - USB_PHY | | |
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| | | |
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| Filename: SENSOR-RTC.SchDoc | | |

| Net Name | Voltage Rail | Low Detect |
|----------|--------------|------------|
| VCCPINT | 1.0 V | 0.936 V |
| PS_1.8V | 1.8 V | 0.86 V |



R103 have to be populated when U20 are not populated

PS voltage detector!

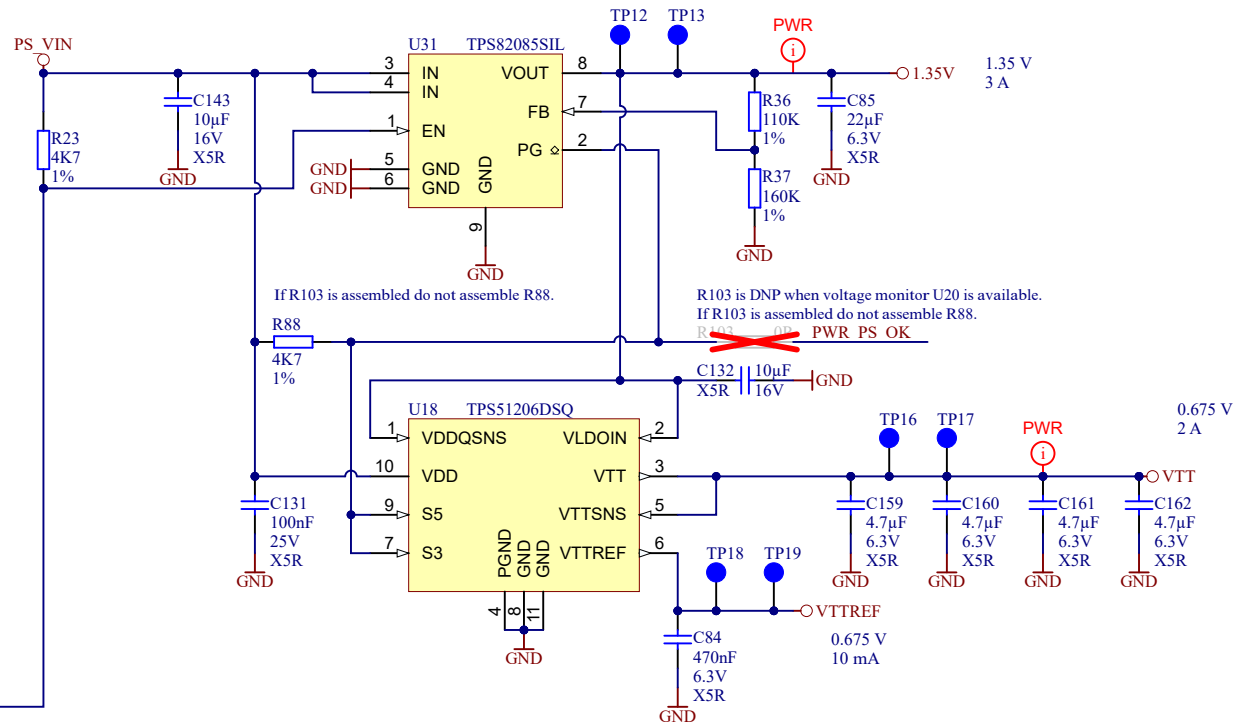
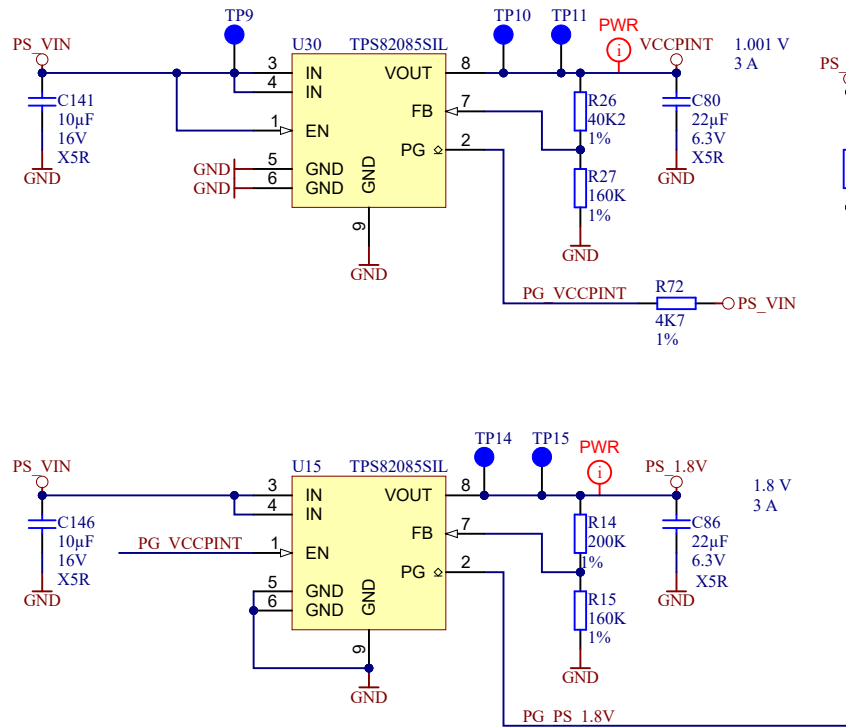
PL voltage detector!


| Net Name | Voltage Rail | Low Detect | High Detect |
|----------|--------------|------------|-------------|
| PS_3.3V | 3.3 V | 2.97 V | 3.62 V |
| PS_1.8V | 1.8 V | 1.62 V | 1.98 V |
| PS_VIN | 3.3 V | 2.97 V | 3.62 V |
| 1.35V | 1.35 V | 1.22 V | 1.49 V |
| VCCPINT | 1.0 V | 0.90 V | 1.10 V |

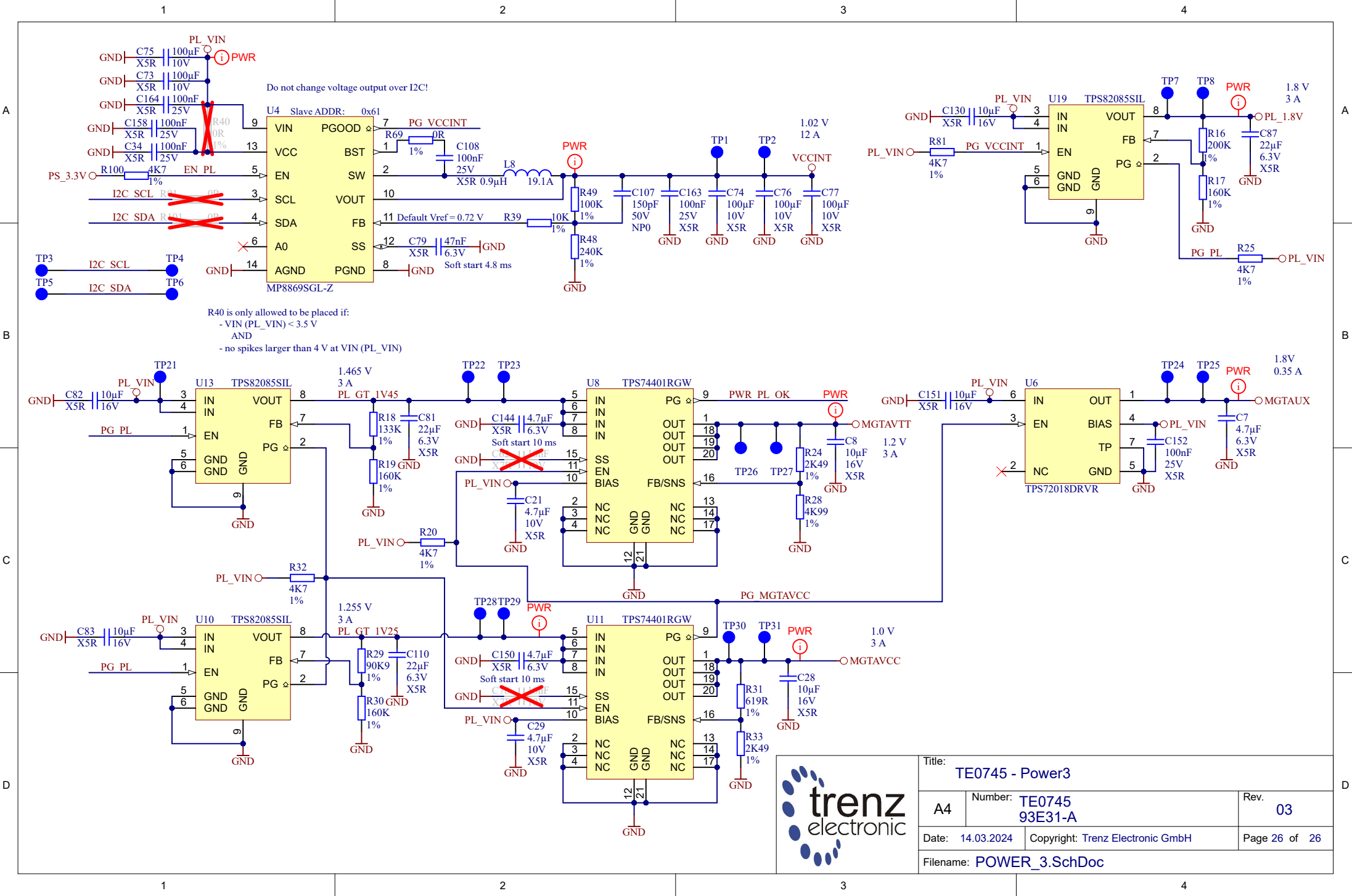
| Net Name | Voltage Rail | Low Detect | High Detect |
|----------|--------------|------------|-------------|
| PS_3.3V | 3.3 V | 2.97 V | 3.62 V |
| MGTAVCC | 1.0 V | 0.90 V | 1.10 V |
| MGTAVTT | 1.2 V | 1.08 V | 1.32 V |
| VCCINT | 1.0 V | 0.90 V | 1.10 V |
| PL_1.8V | 1.8 V | 1.62 V | 1.98 V |



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