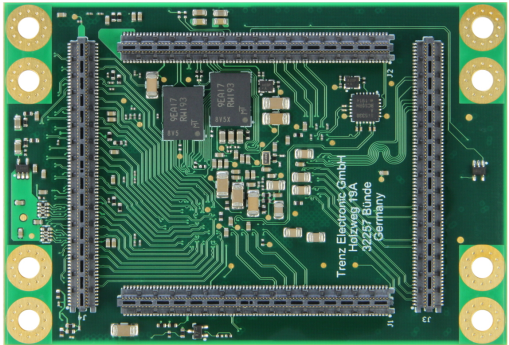
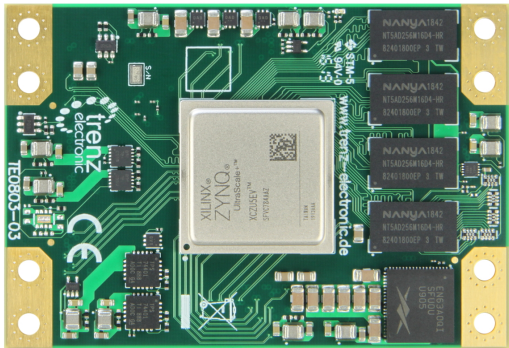


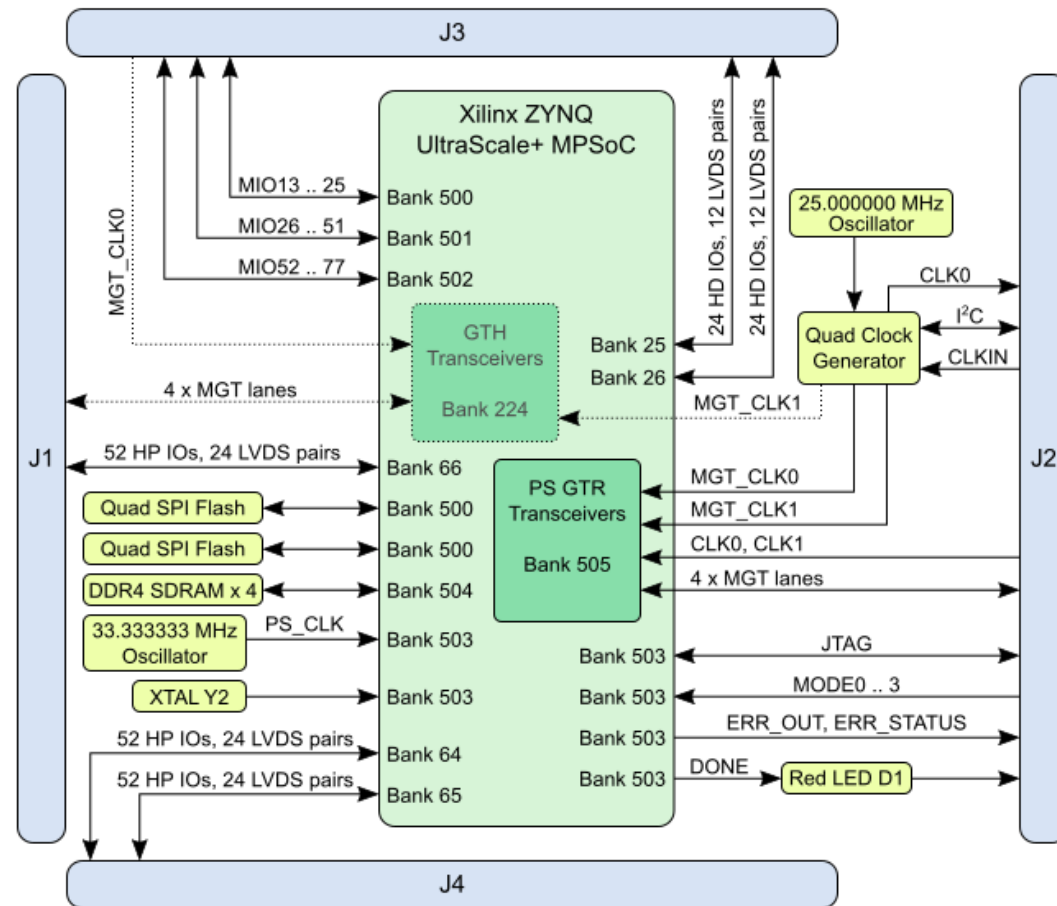


Regarding the usage of our schematics and alike documentation for Trenz module TE0803.

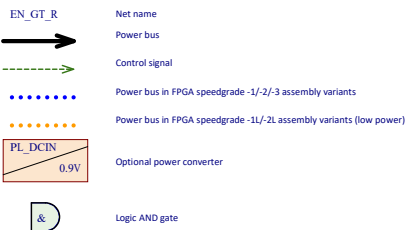
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0803is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0803		
	A4	Number: TE0803 3BE21-L	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 1 of 30
	Filename: Legal Notices Modules.SchDoc		



	Title: TE0803 - System Overview		
	A4	Number: TE0803 3BE21-L	Rev. 04
	Date: 2021-01-19	Copyright: 2015 Trenz Electronic GmbH	Page 2 of 30
	Filename: TE0803-Overview.SchDoc		

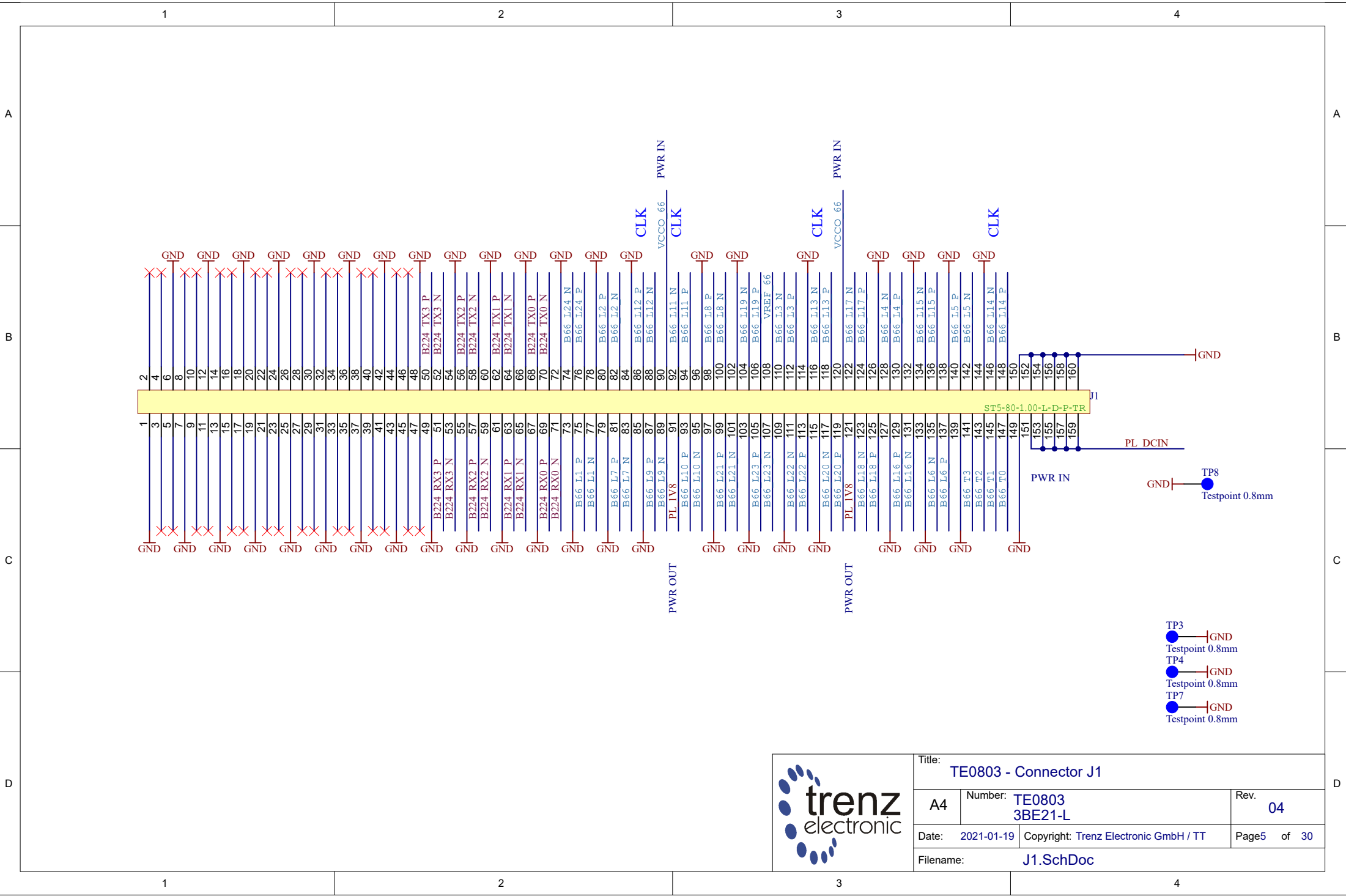


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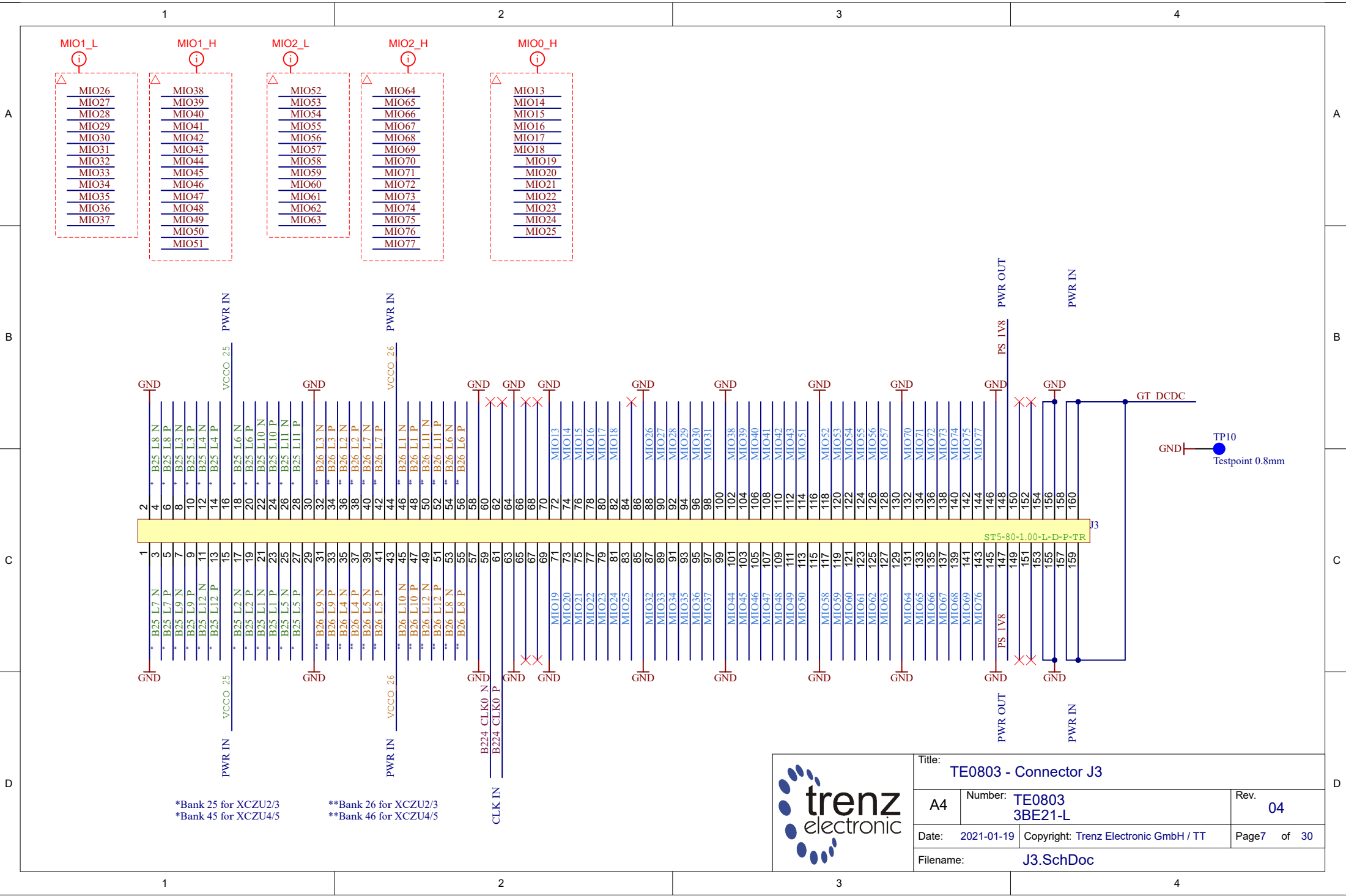
The diagram illustrates the proposed architecture. It consists of a Low-power domain (yellow box) on the left, which is connected to two Full-power domains (yellow boxes) in the center. The Low-power domain has an 'Enable' input and outputs 'PG' signals to both Full-power domains. The top Full-power domain has an 'Enable' input and outputs 'PG' signals to the GTR Transceivers (yellow box) and the Programmable Logic (yellow box). The Programmable Logic has an 'Enable' input and outputs 'PG' signals to the GTH/GTY Transceivers (yellow box). The GTR Transceivers have an 'Enable' input and output 'PG' signals to the GTH/GTY Transceivers. The GTH/GTY Transceivers have an 'Enable' input.



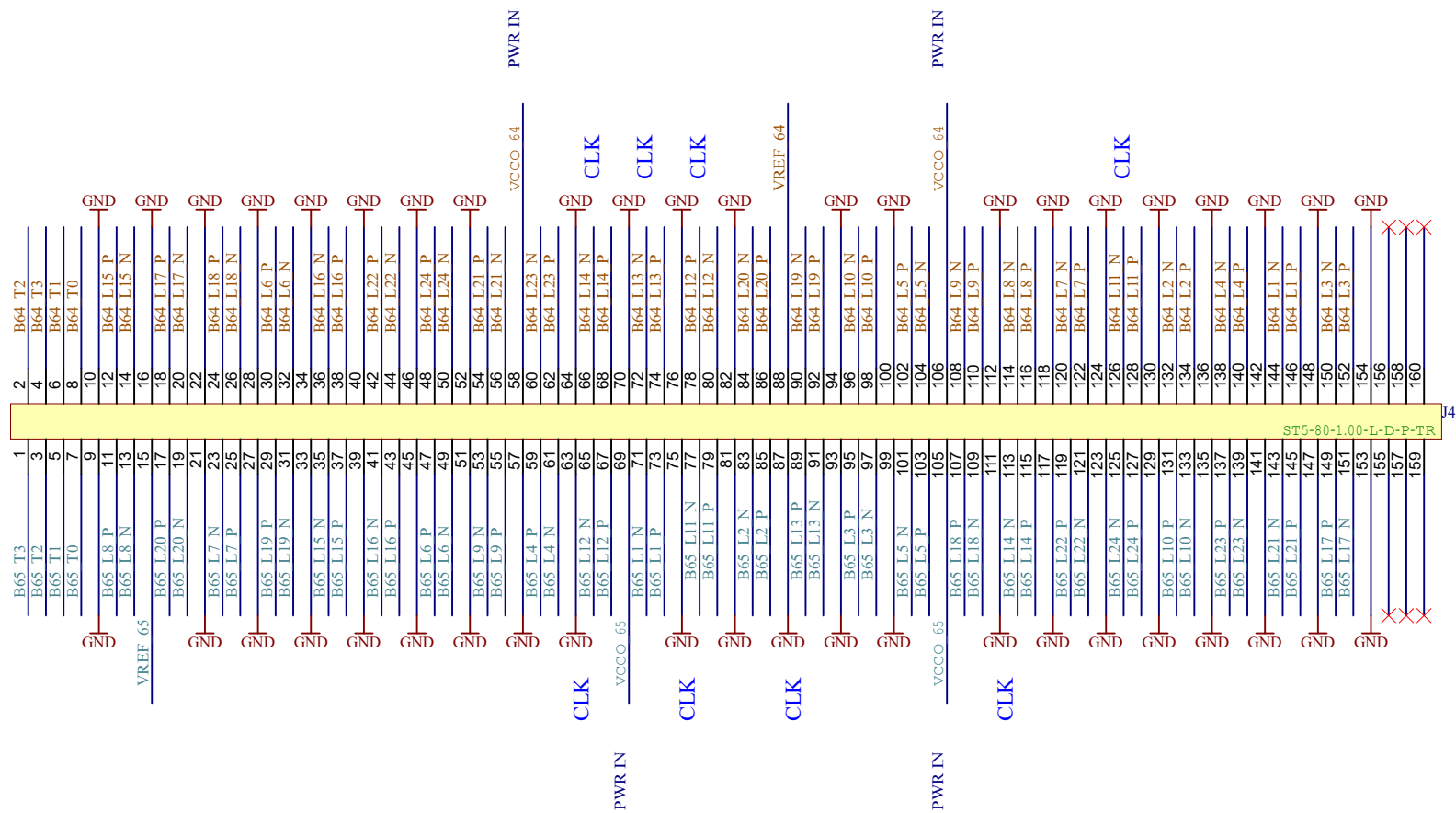
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A3	Number: TE0803 3BE21-L	Rev. 04	
Datum: 2021-01-19		Copyright: Trenz Electronic GmbH / TT	
Filename: Power Diagram.SchDoc		Page 3 of 30	



Title: TE0803 - Connector J1		
A4	Number: TE0803 3BE21-L	Rev. 04
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Filename: J1.SchDoc		



Title: TE0803 - Connector J3		
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Filename: J3.SchDoc		



Title:	TE0803 - Connector J4
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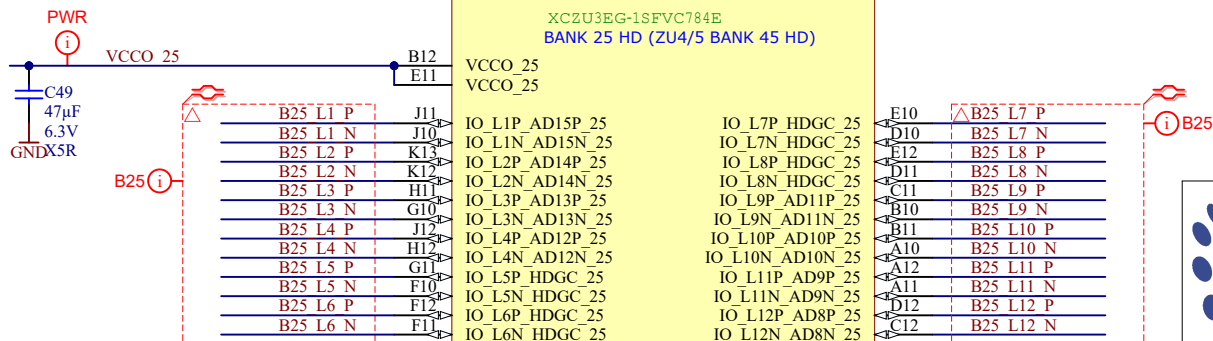
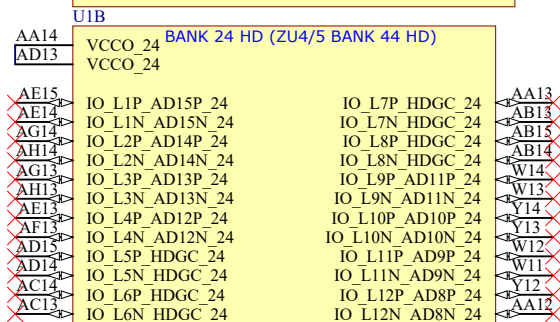
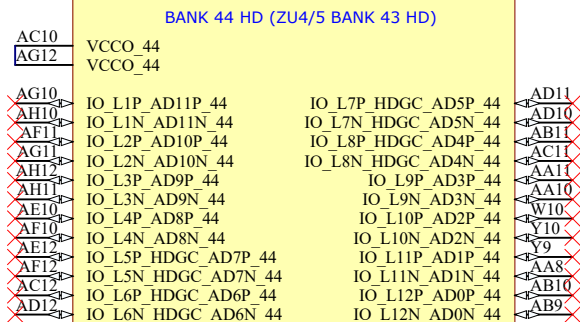
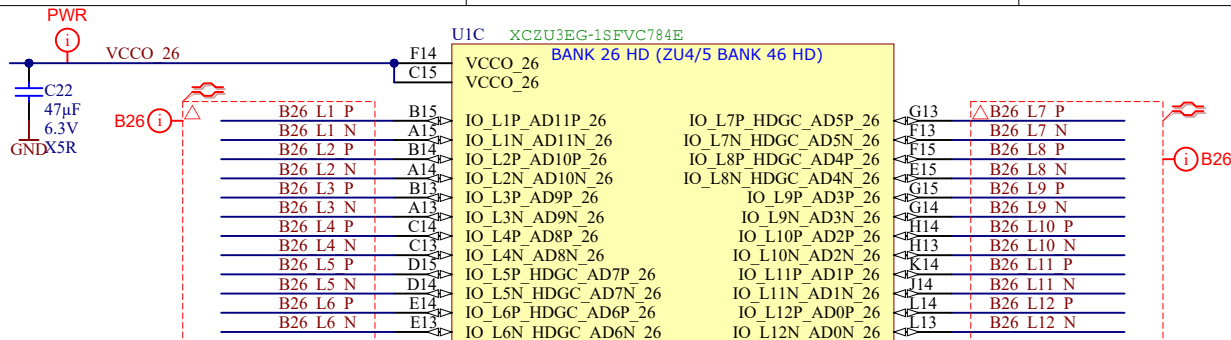
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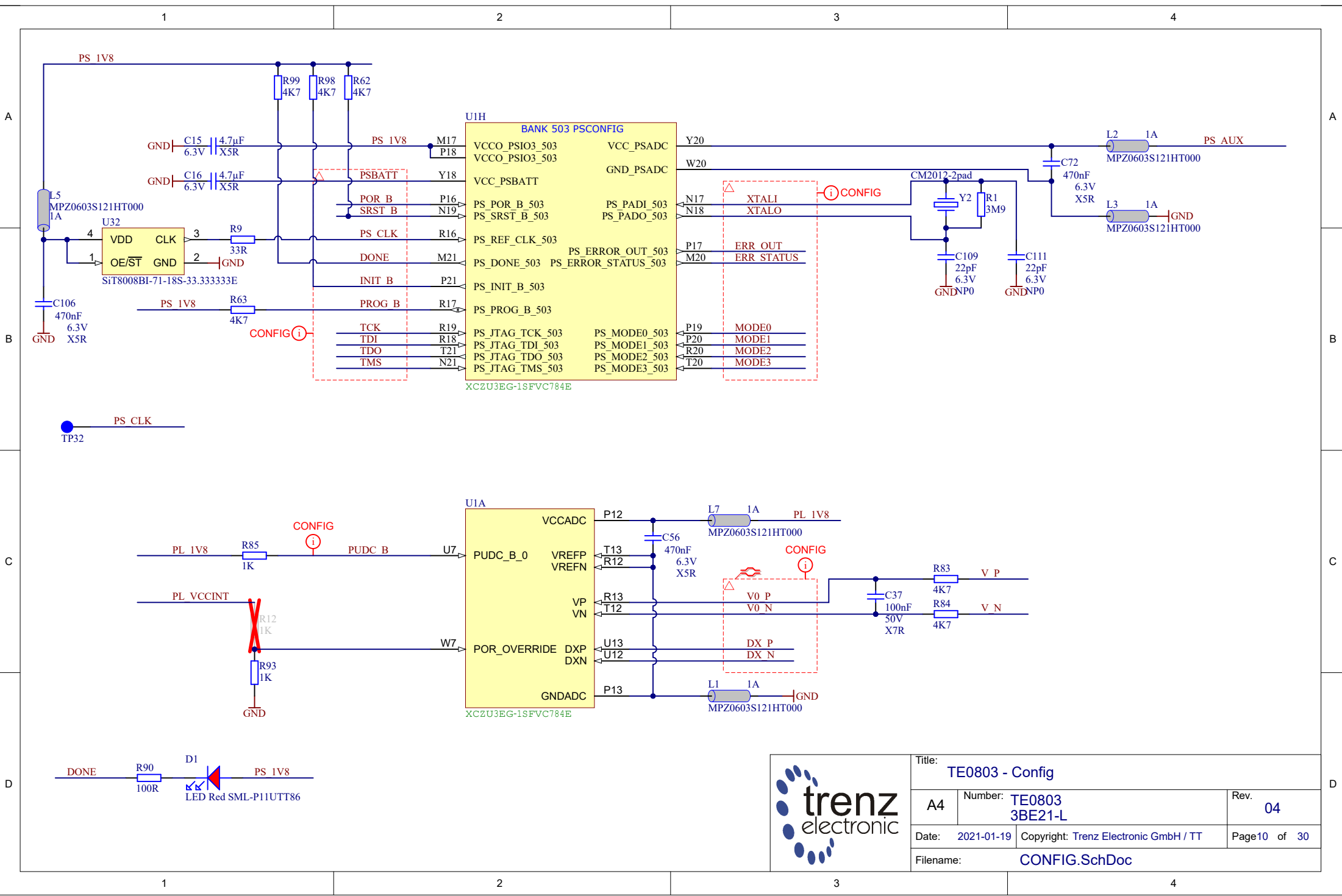
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page9 of 30
Filename: B HD.SchDoc			

1

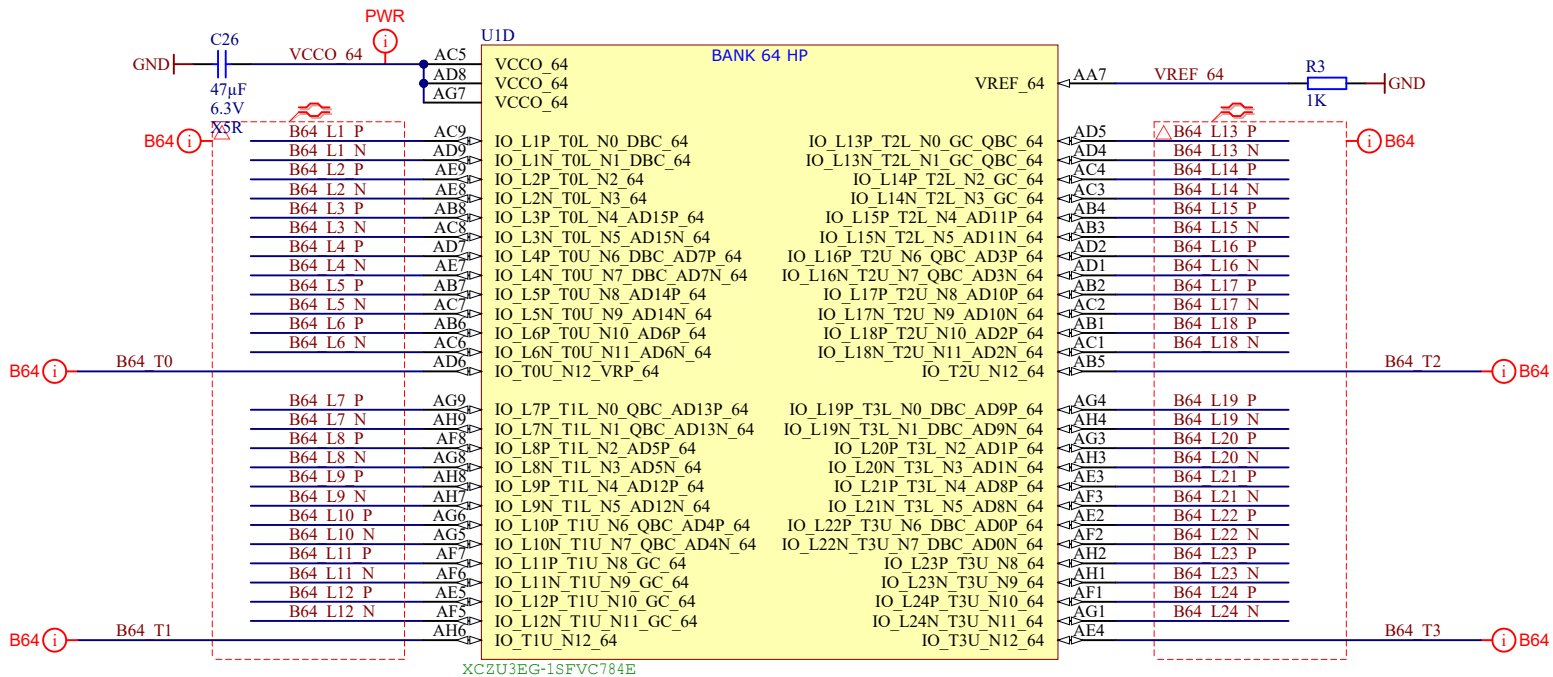
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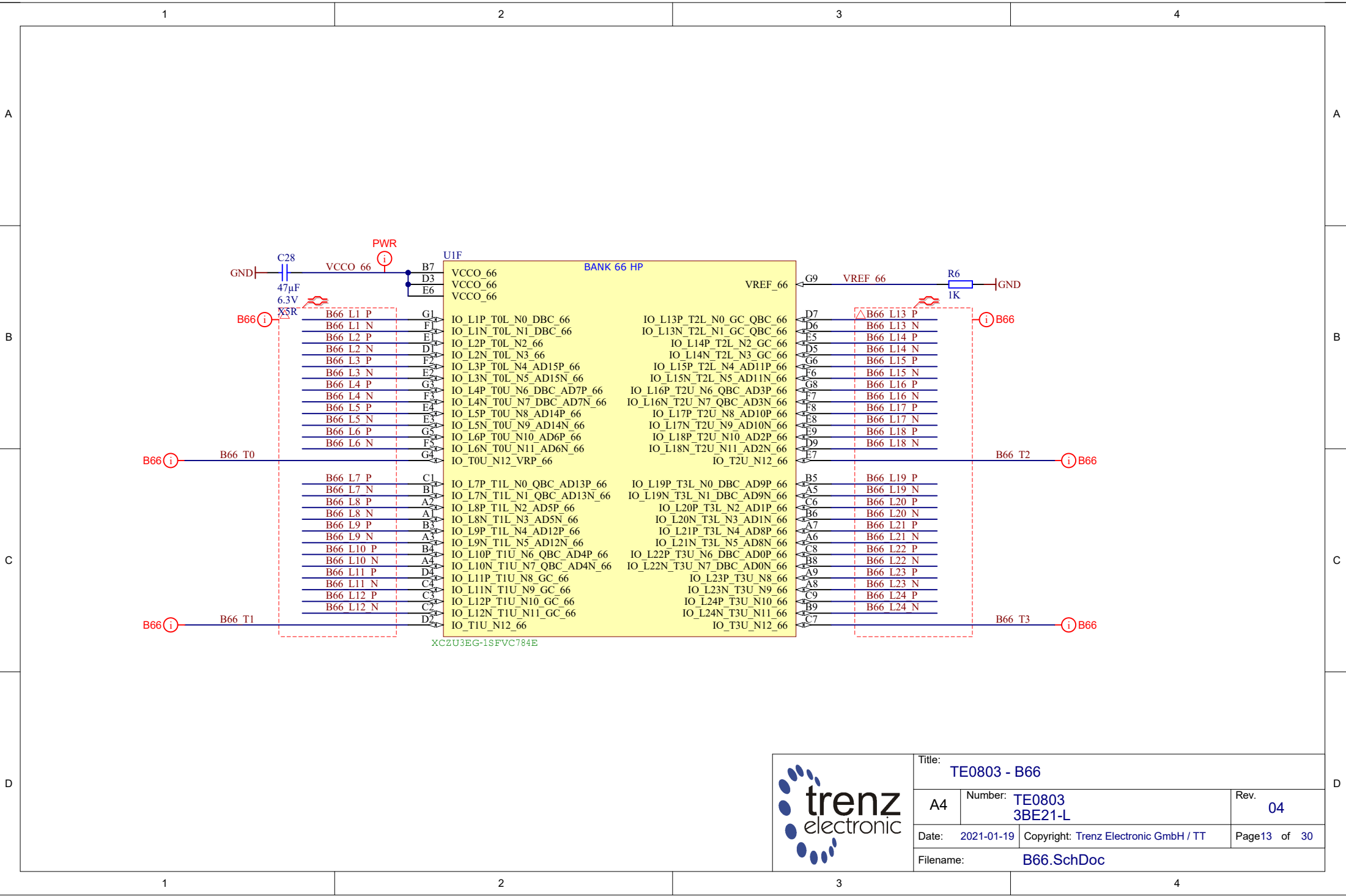


Title: TE0803 - Config			
A4	Number: TE0803 3BE21-L	Rev. 04	
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page10 of 30	
Filename: CONFIG.SchDoc			



Title: TE0803 - B64			
A4	Number: TE0803 3BE21-L	Rev. 04	
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Filename: B64.SchDoc			







Title:TE0803 - B66

A4

Number:TE08033BE21-L

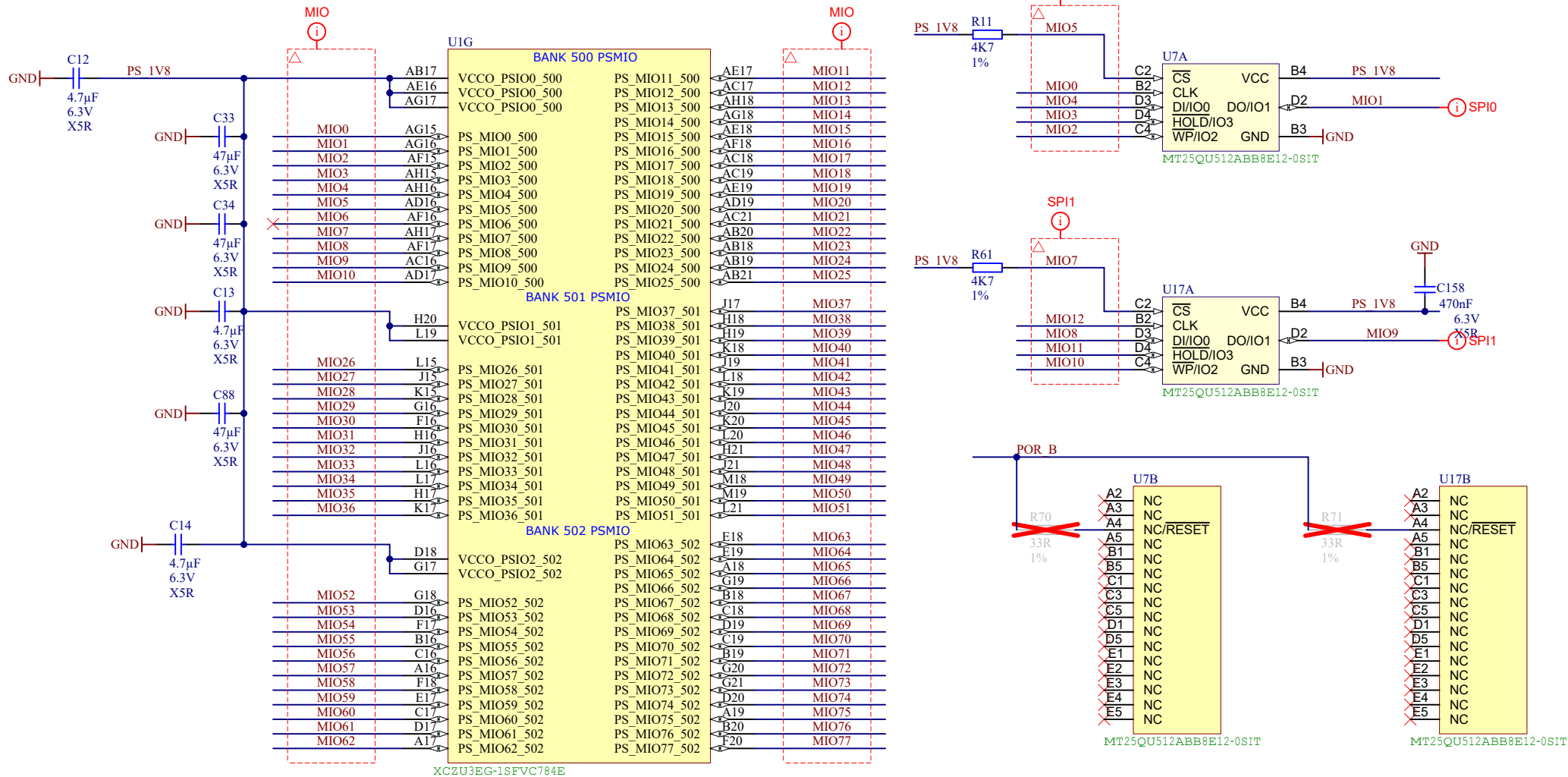
Rev.04

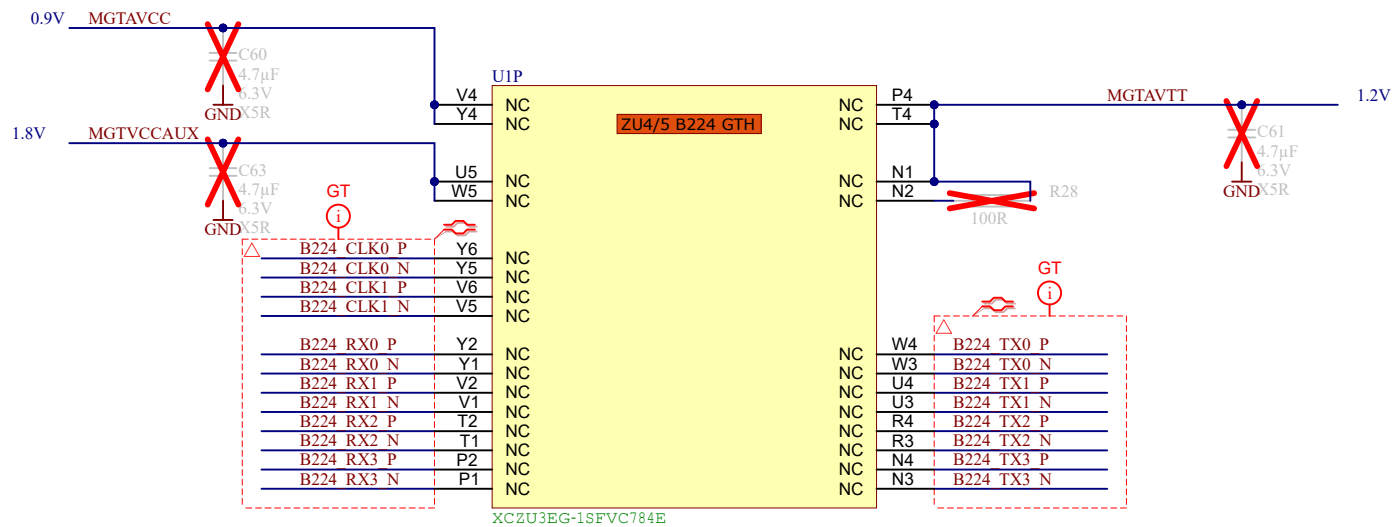
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Copyright: Trenz Electronic GmbH / TT

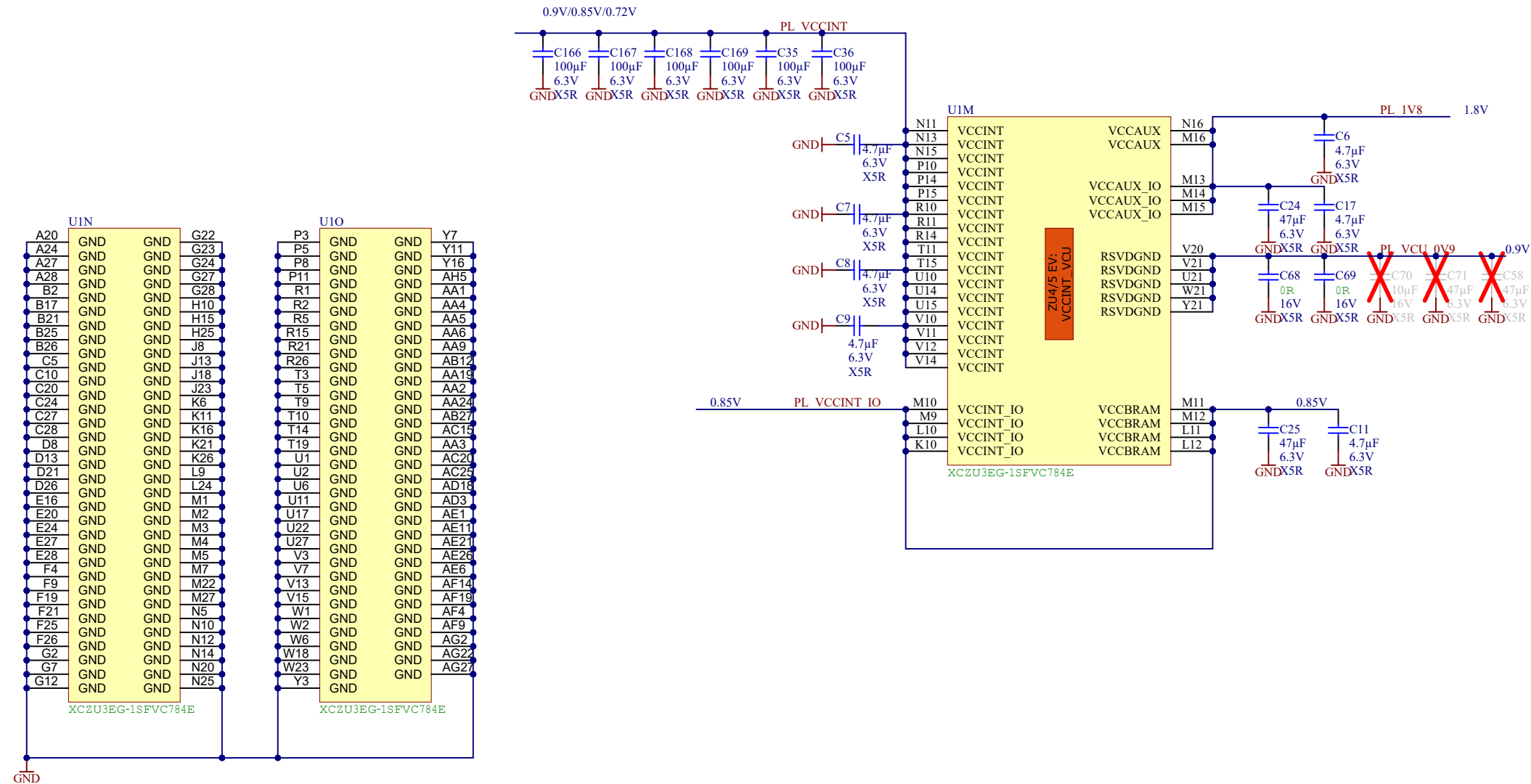
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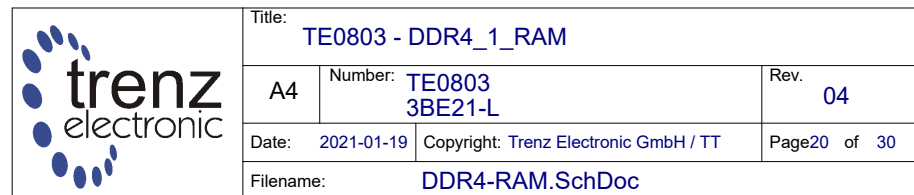


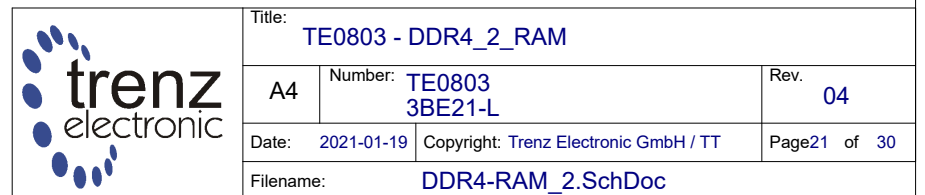


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	Filename: B_GT.SchDoc		



		Title: TE0803 - ZU_POWER	
		A4	Number: TE0803 3BE21-L
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Filename: ZU_POWER.SchDoc		Page 19 of 30	





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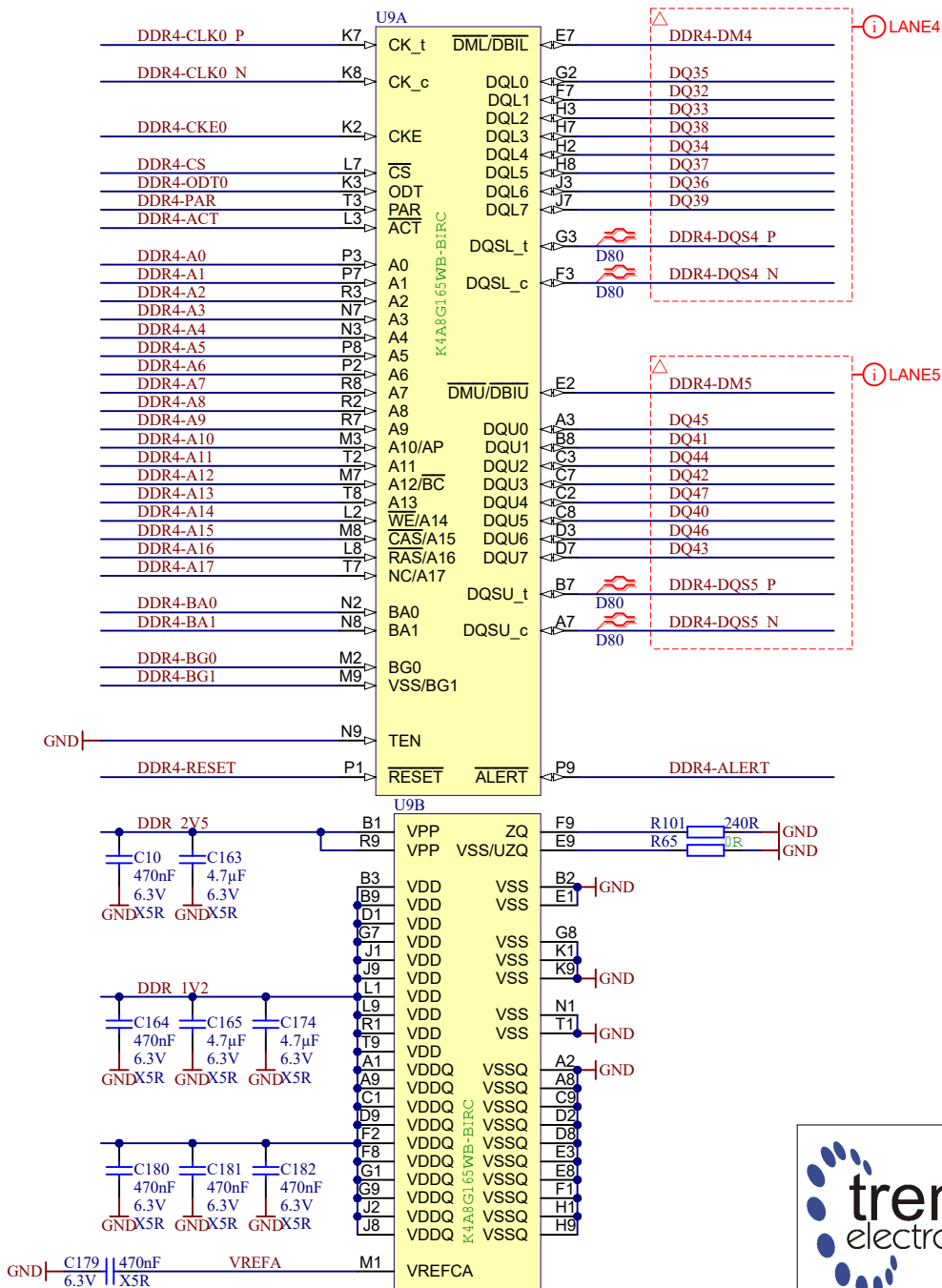
B

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Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 3BE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page22 of 30
Filename: DDR4-RAM_3.SchDoc		

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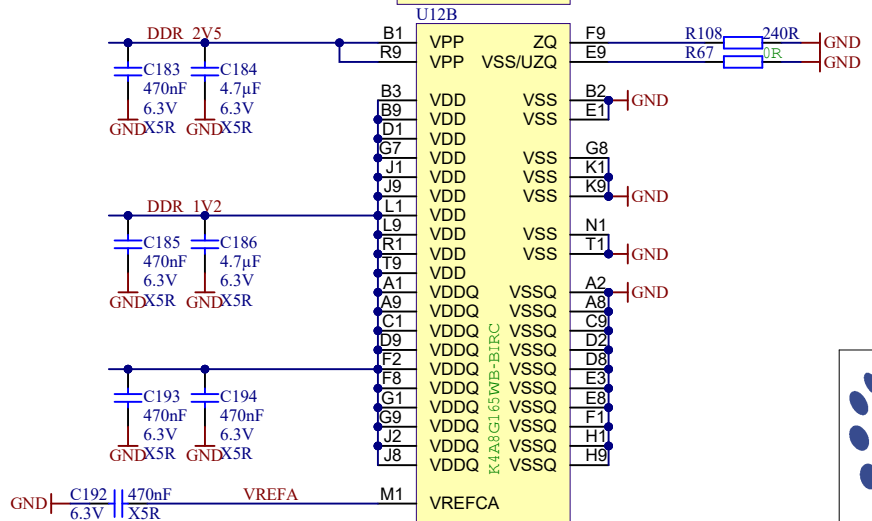
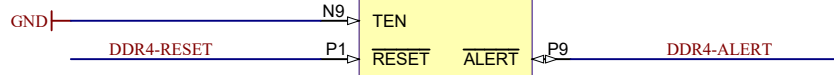
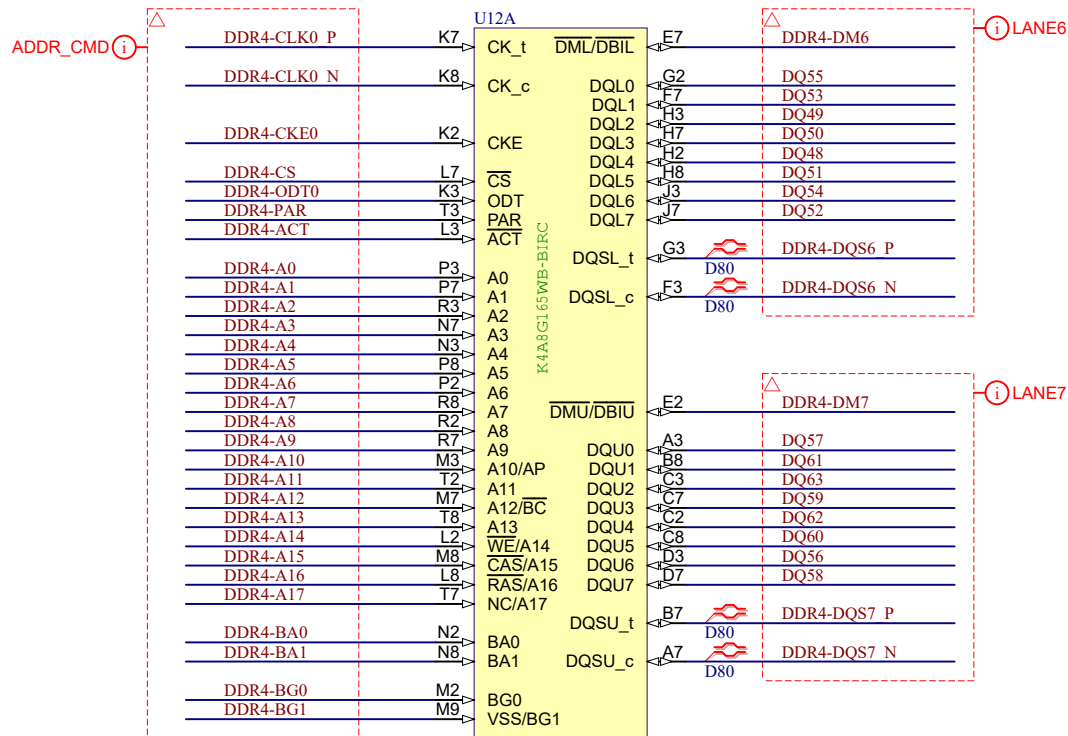
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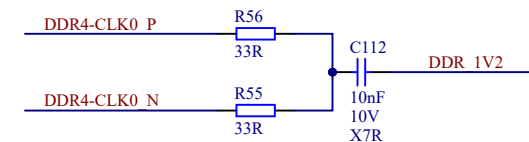
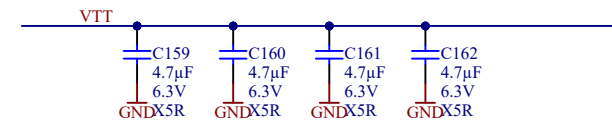
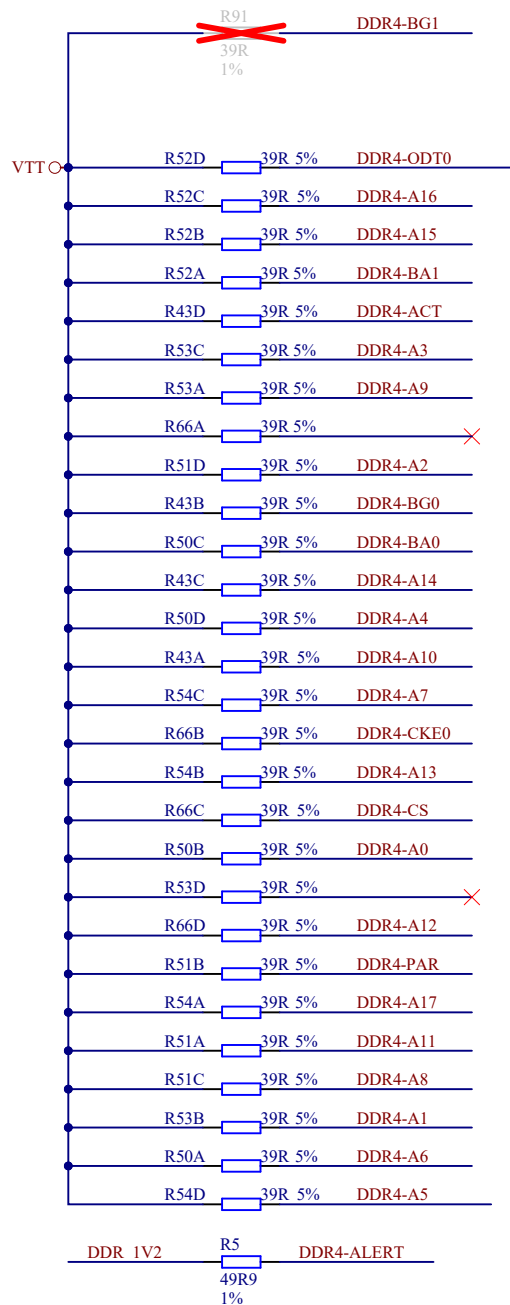
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A4	Number: TE0803 3BE21-L	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page23 of 30
Filename: DDR4-RAM_4.SchDoc		

1

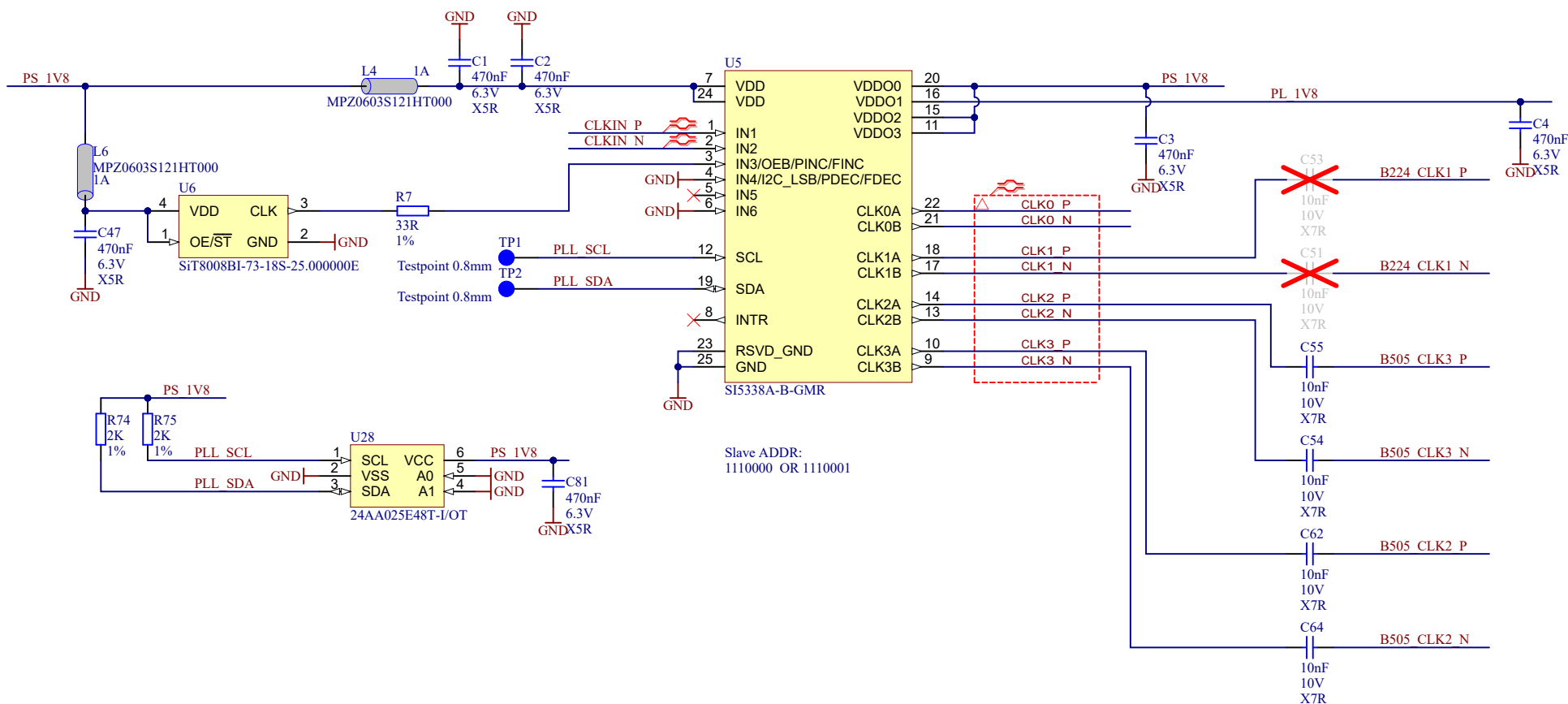
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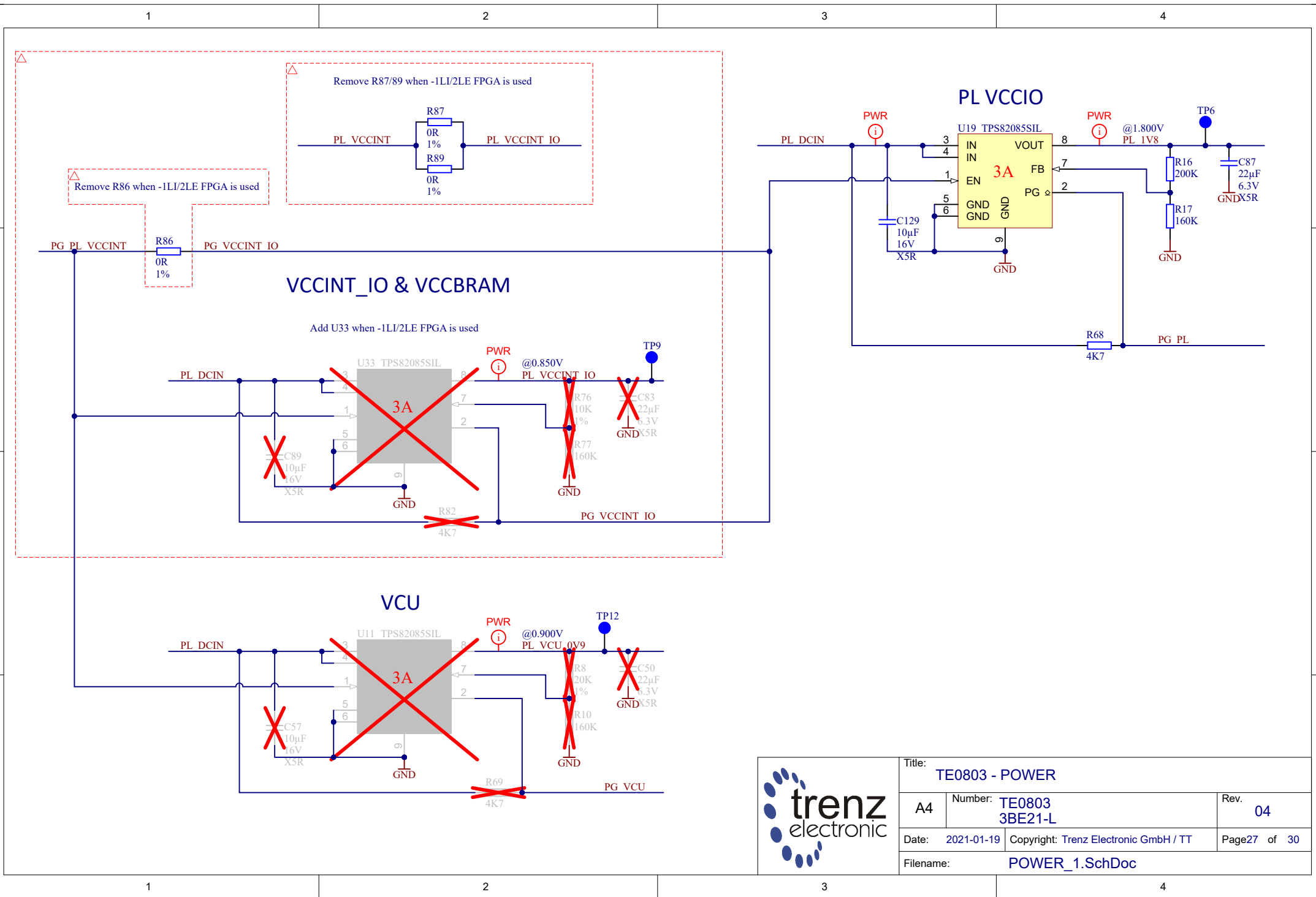
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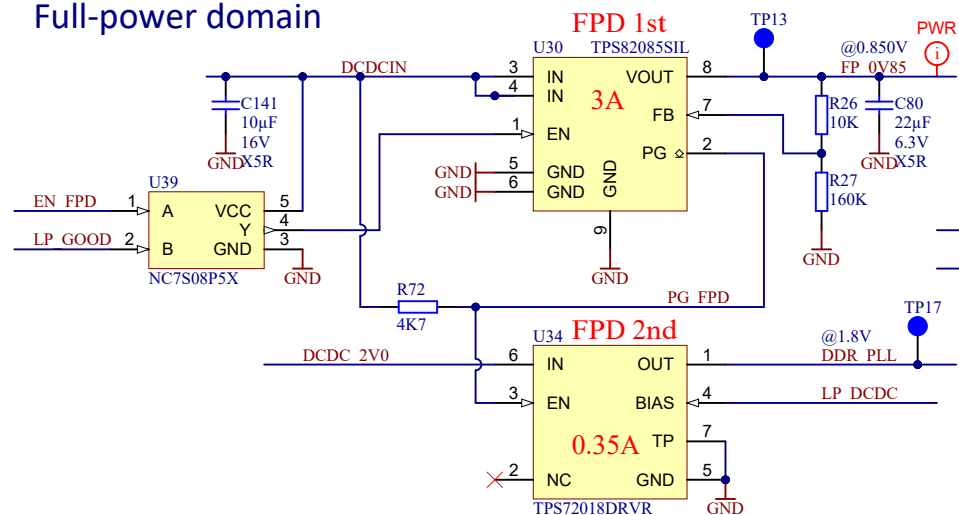
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT			Page 24 of 30
Filename: DDR4-TERM.SchDoc				



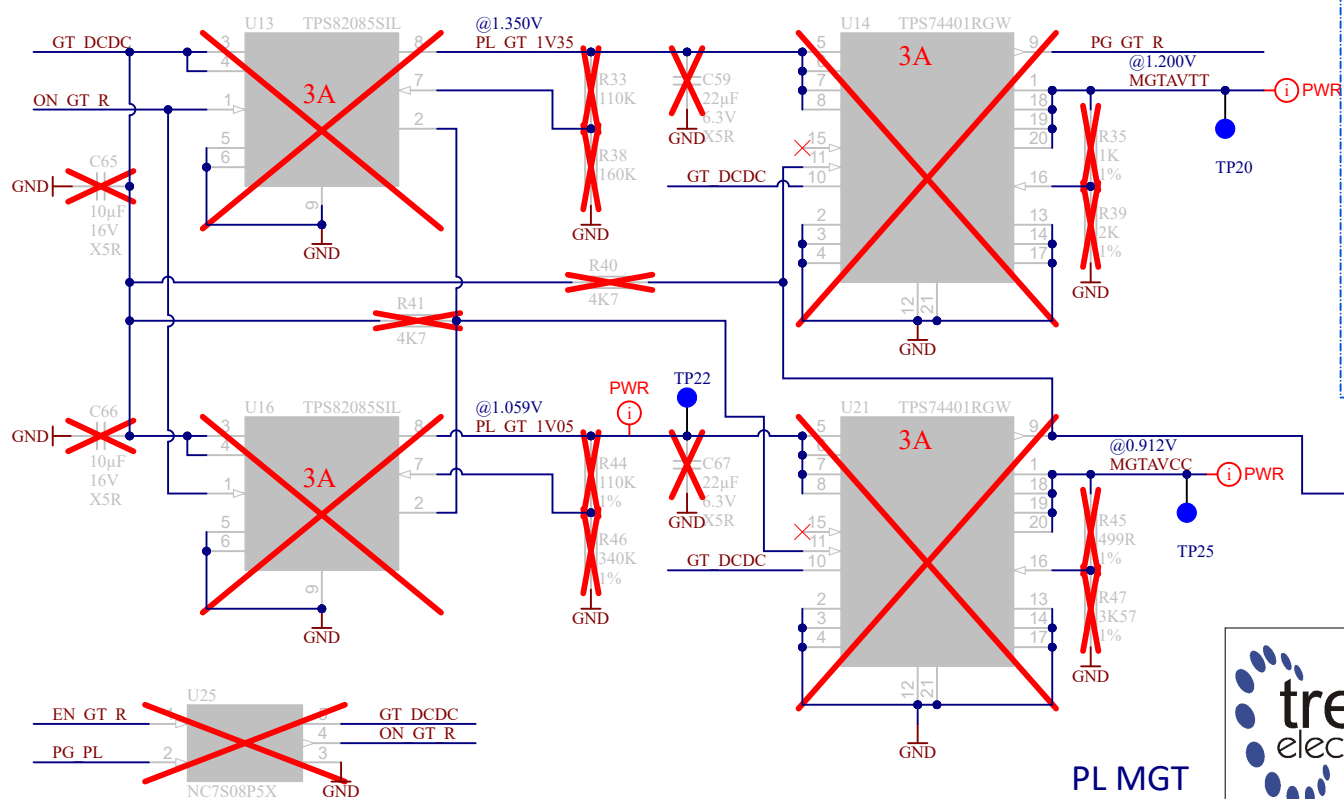
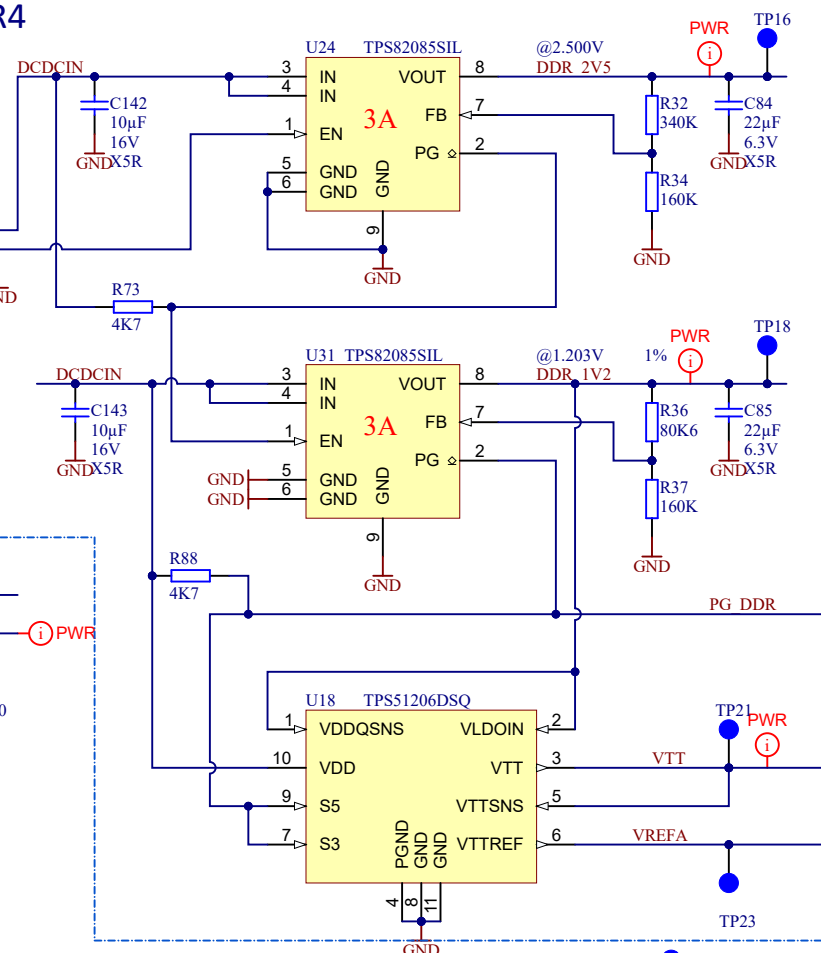
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	A4	Number: TE0803 3BE21-L	Rev. 04
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	Filename: Clock.SchDoc		



Full-power domain



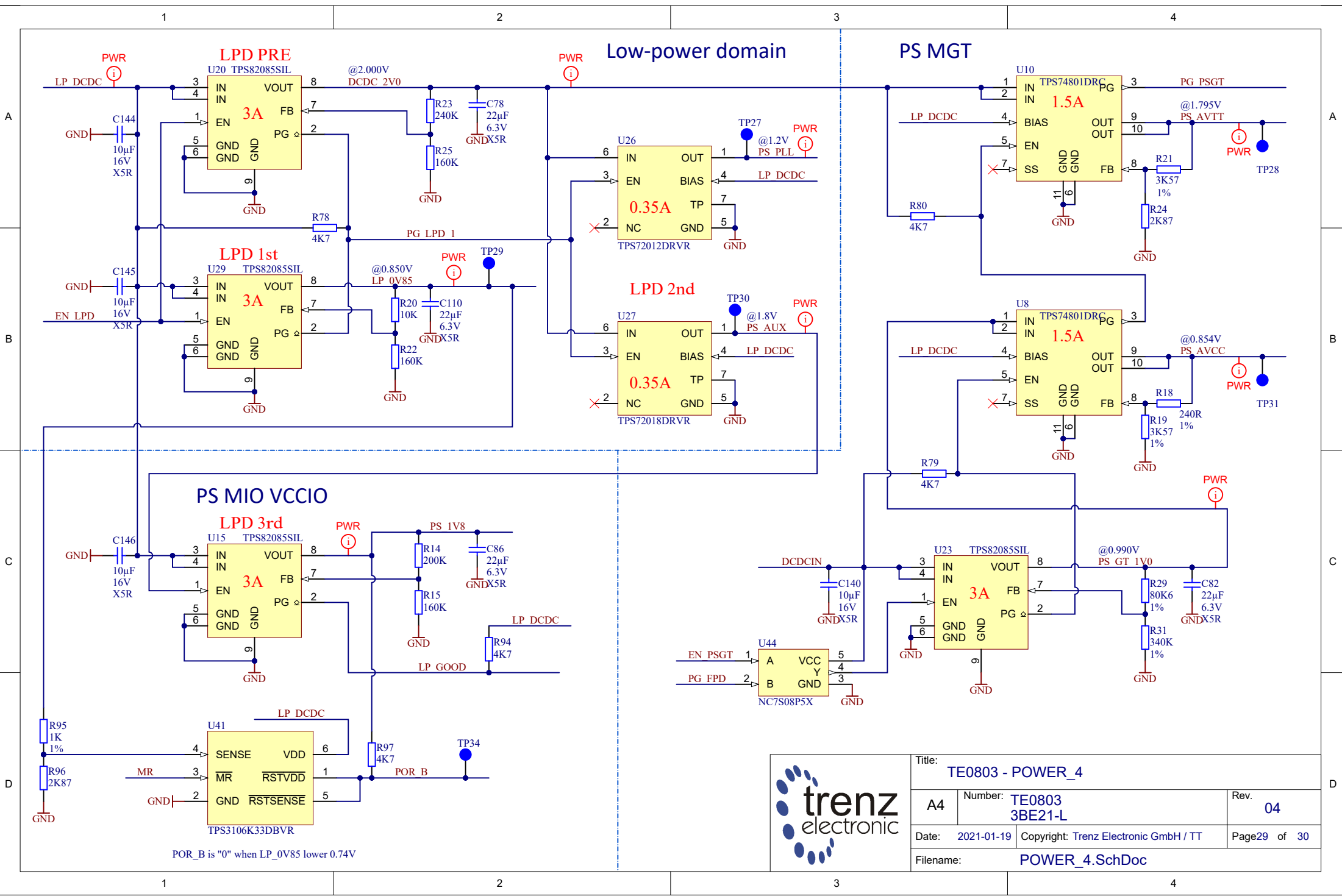
DDR4



PL MGT



Title: TE0803 - POWER_2		
A4	Number: TE0803 3BE21-L	Rev. 04
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Filename: POWER_2.SchDoc		



POR_B is "0" when LP_0V85 lower 0.74V



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Filename: POWER_4.SchDoc			

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A

REV	DATE	Description	
-01		Initial revision	VT
-01a	20.11.2017	1. VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.	VT
-02	20.06.2018	1. Added LDO to DDR_PLL 2. All differential pairs wath length matched with tollerance 0.1mm (excluding package delays) 3. Added MAC EEPROM U28 4. VPS_MGTRAVCC set to 0.85V 5. Added pull-up resistors R68,R69	VT
-03	21.02.2019	1. Added support of DDP DDR4 2. Added support of Low power FPGA (-L1/L2). 3. Revised testpoints 4. Revised J1-J4 connectors net label style	VY
-04	15.12.2020	1. Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; 2. Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; 3. Added option to select POR_OVERRIDE level (R12 and R93) 4. VCCO pins if unused Bank 44 connected together. Same for unused Bank 24 (UG583 recomendation) 5. PCB: updated signal trace lengths. 6. PCB: updated silckscreen. Added company address, CE and WEEE symbols; 7. PCB: added module orientation rectangle painer 8. Changed resistors value of R29, R31, R35, R39, R44-R47 (BOM optimization) 9. Removed traceability part (Obsolete component)	VY
-04	23.02.2022	10. Changed capacitor C92 for all variants from 100 nF to 1 nF.	ED
-04	08.06.2023	11. U4 can be either TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.	VY
-04	23.05.2025	12. L1 - L7 ferrit beads BKP0603HS121-T (EOL) replaced by MPZ0603S121HT000 for all variants.	VG

B

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Title:TE0803 - Revision History

A4

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Rev.04

Date:2021-01-19

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4



Title: TE0803 - Revision History

A4

Number: **TE0803**
3BE21-L

Rev. **04**

Date: 2021-01-19

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Drawn by: VY

Filename: Revision Changes.SchDoc