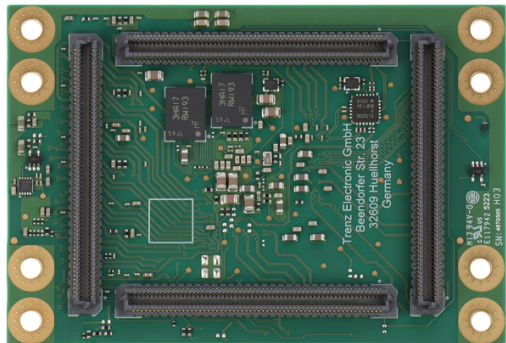
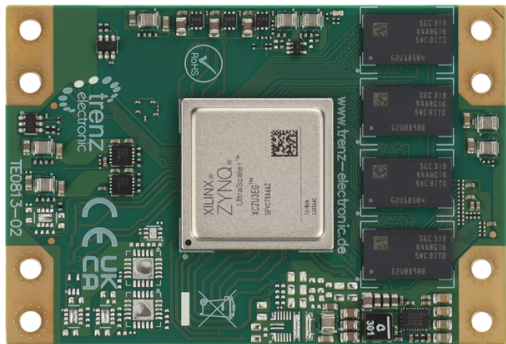
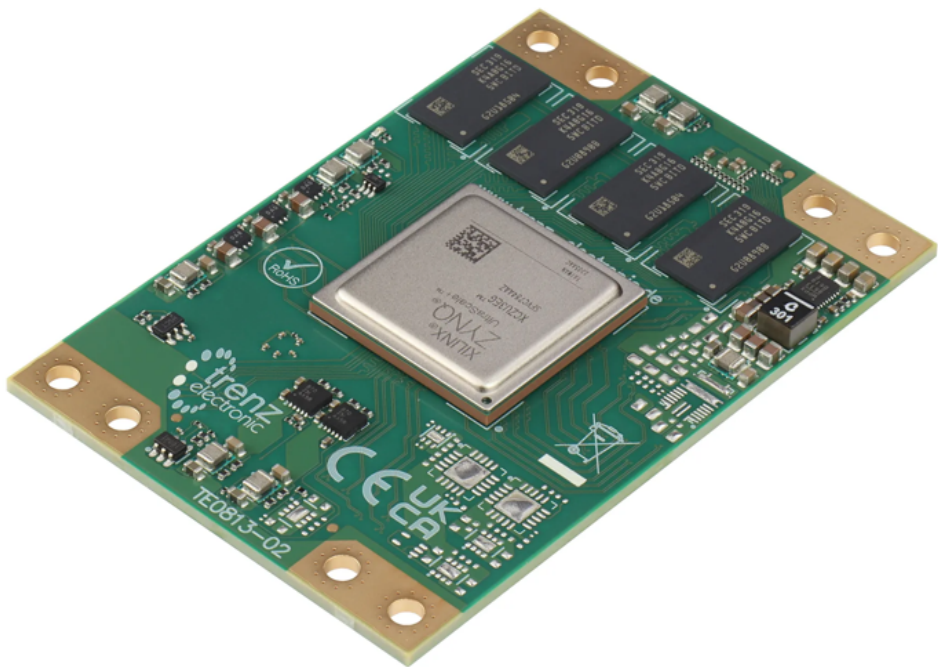




Regarding the usage of our schematics and alike documentation for Trenz module TE0813.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.

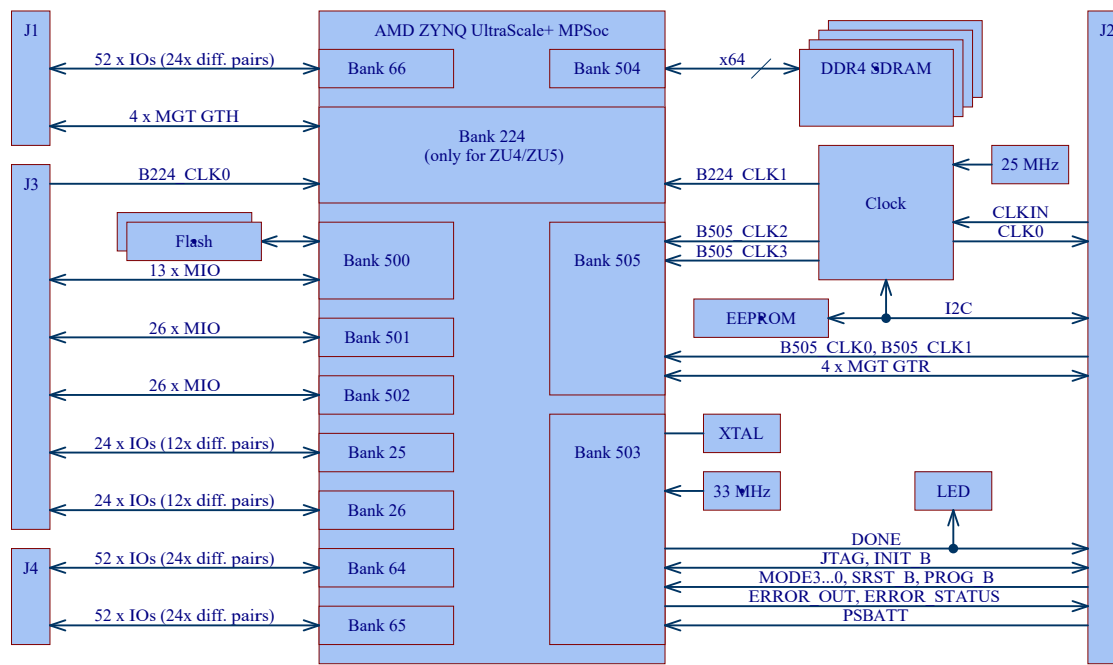
TE0813 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

Drawn by	ED
Checked by	MR
Assembly variant	3AE71-A
Created by	ED
Modified by	ED
Modified at	2023-05-17



Title: TE0813 - Legal Notices		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 04.05.2026	Copyright: Trenz Electronic GmbH	Page 1 of 30
Filename: Legal Notices Modules.SchDoc		



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/- 5 %	Micromodule Power	Management voltage rail, supplied by power rail
PL_DCIN	IN	3.3V	+/- 5 %	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	GTH Transceiver, supplied by power rail
DCDCIN	IN	3.3V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	Supplied by external power rail via B2B connector
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	Supplied by external power rail via B2B connector
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	Supplied by external power rail via B2B connector
VCCO_25	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 25	Supplied by external power rail via B2B connector
VCCO_26	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 26	Supplied by external power rail via B2B connector
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	Supplied by external power rail via B2B connector
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	Micromodule: PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x70	-
EEPROM U28	0x50	-

TE0813

DDR4•TERM

ZU PS POWER

ZU POWER

POWER

POWER 1

POWER 2

POWER 3



Title:	TE0813 - System Overview
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A4

Number:	TE0813 3AE71-A
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Rev. 02

Date: 06.01.2026	Copyright: Trenz Electronic GmbH
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Filename: TE0813-Overview.SchDoc

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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-03	Added Table with Supported Voltage Ranges	
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C92 100nF to 1nF	
	2022-11	Added additional Info about Voltage Range	
-02	2023-07	1. Change DCDC U11 from EN6347Q1 to MPM3860GQW-Z and adapted according circuits. 2. Connected DDR4-TEN signals together for U2, U3, U9, and U12 and pulled them low via 499 Ohm resistor R131. Added a testpoint TP3 for DDR4-TEN. 3. Changed voltage rail from 1.35 V to 1.45 V via adapting voltage divider resistors R33 and R38 and changed according voltage rail name PL_GT_1V35 to PL_GT_1V45. 4. Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R44 and R46 and changed according rail name PL_GT_1V05 to PL_GT_1V15. 5. Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN. 6. Connected enable signal for U11 and U33 from "3.3VIN" to "PG_PL_VCCINT". 7. Added capacitors C137, C147, and C148 for VTT voltage rail. 8. Added resistors R132 (default: not fitted) and R133 to supply U4 VCC either from "PL_DCIN" or from "3.3VIN". 9. Change resistor R92 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.5 A for U4. 10. Added remote sense option: 10.1 R134 for U30 10.2 R135 for U29 10.3 R136 for U31 11. Added decoupling capacitors: 11.1 C210 and C211 for U5. 11.2 C190 for U7. 11.3 C198, C199, and C213 for U8. 11.4 C153, C170...172 for U9 11.5 C196 C197, and C212 for U10. 11.6 C156 and C157 for U12 11.7 C207 and C208 for U14. 11.8 C189 for U17. 11.9 C149...152, C205, and C206 for U18 11.10 C209 and C217 for U21. 11.11 C214...216 for U22. 11.12 C154 and C155 for U24 11.13 C188 and C191 for U26. 11.14 C187 and C195 for U27. 11.15 C203 and C204 for U34. 11.16 C201 for U39. 11.17 C202 for U40. 11.18 C178 for U41. 11.19 C200 for U44. 12. Added testpoints TP4, TP19, TP26. 13. Added UKCA logo. 14. Change 100 nF capacitors C135 and C136 from 6.3 V to 25 V for BOM optimization.	ED

trenz

electronic

Title: TE0813 - Revision History

A4

Number: TE0813
3AE71-A

Rev. 02

Date: 06.01.2026

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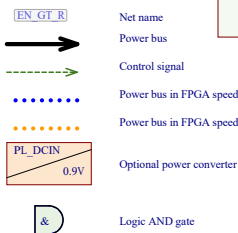
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Power-on sequencing:

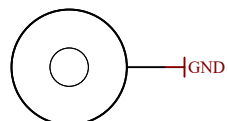
```
graph LR; LP_Enable[Enable] --> LPD[Low-power domain]; PL_Enable[Enable] --> PL[Programmable Logic]; LPD --> FPD[Full-power domain]; PL -- "DCDC 2V0" --> AND1[&]; FPD --> AND1; AND1 --> GTH[GTH Transceivers]; GTH --> GTR[GTR Transceivers]; LP_Enable --> FPD; PL_Enable --> GTH; GTH --> GTR; GTR --> GTR;
```

The diagram illustrates the power-on sequencing logic. It shows five main components: Low-power domain, Programmable Logic, Full-power domain, GTH Transceivers, and GTR Transceivers. The sequencing is controlled by enable signals. The Low-power domain and Programmable Logic both receive an 'Enable' signal. The Low-power domain's output enables the Full-power domain. The Programmable Logic outputs a 'DCDC 2V0' signal, which is ANDed with the output from the Full-power domain to enable the GTH Transceivers. The GTH Transceivers then enable the GTR Transceivers. Additionally, there are direct enable paths from the Low-power domain to the Full-power domain and from the Programmable Logic to the GTH Transceivers.

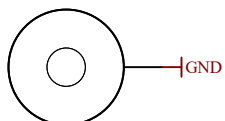


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Datum:	2021-01-19	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: Power Diagram.SchDoc			

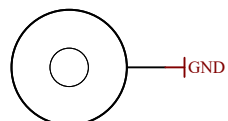
Special notes:



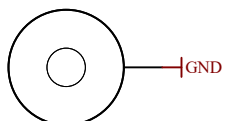
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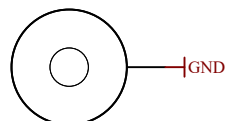
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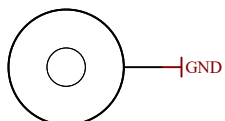
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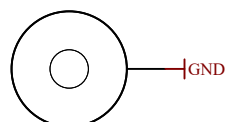
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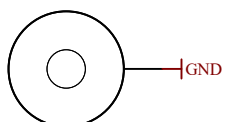
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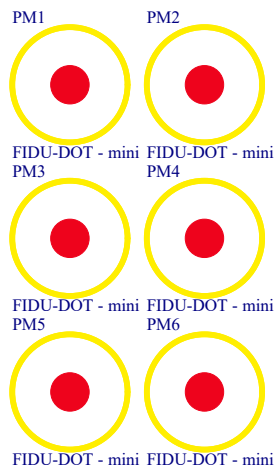
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



UKCA1

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE1

CE Logo on Top Overlay

CE-TOPOVERLAY

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

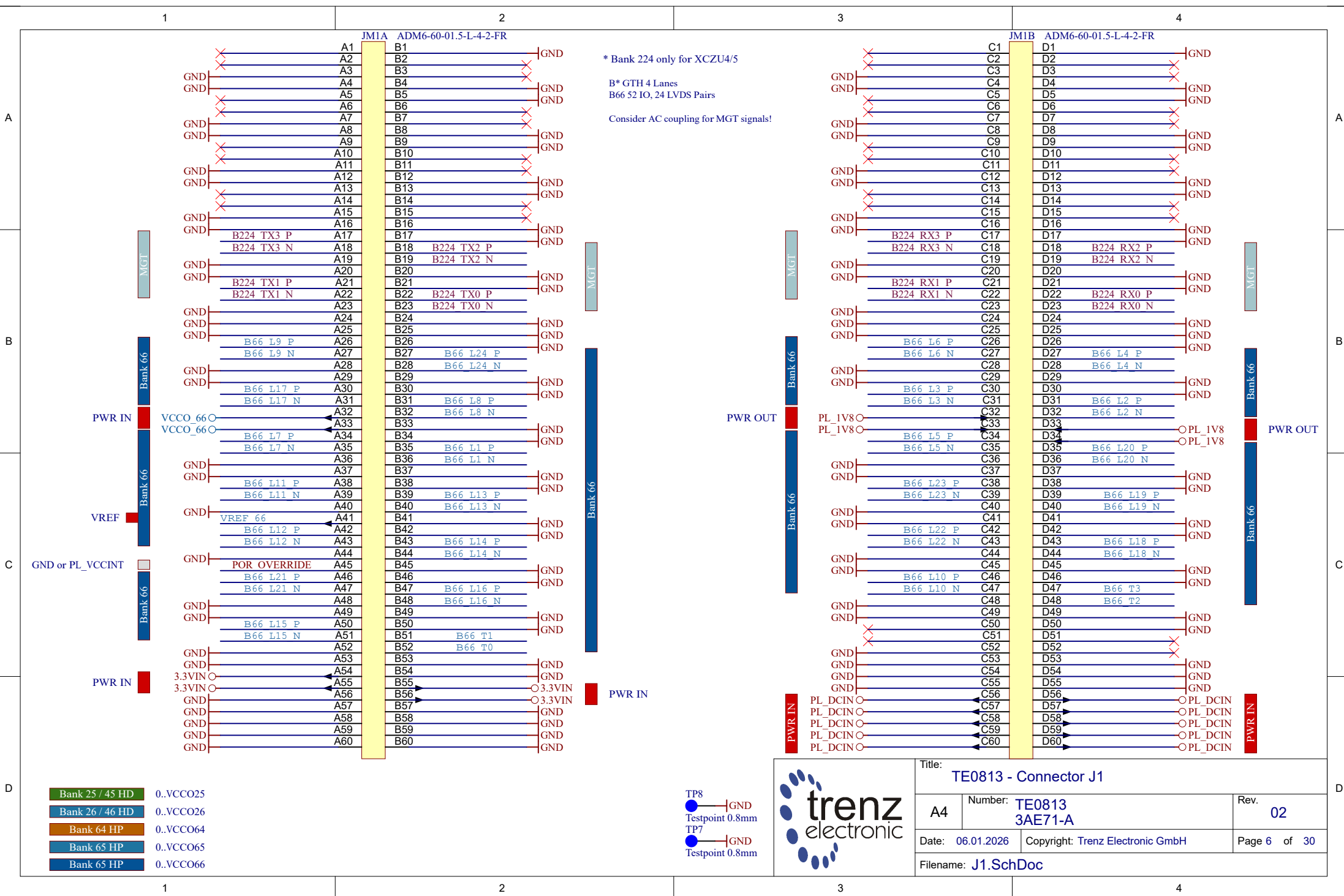
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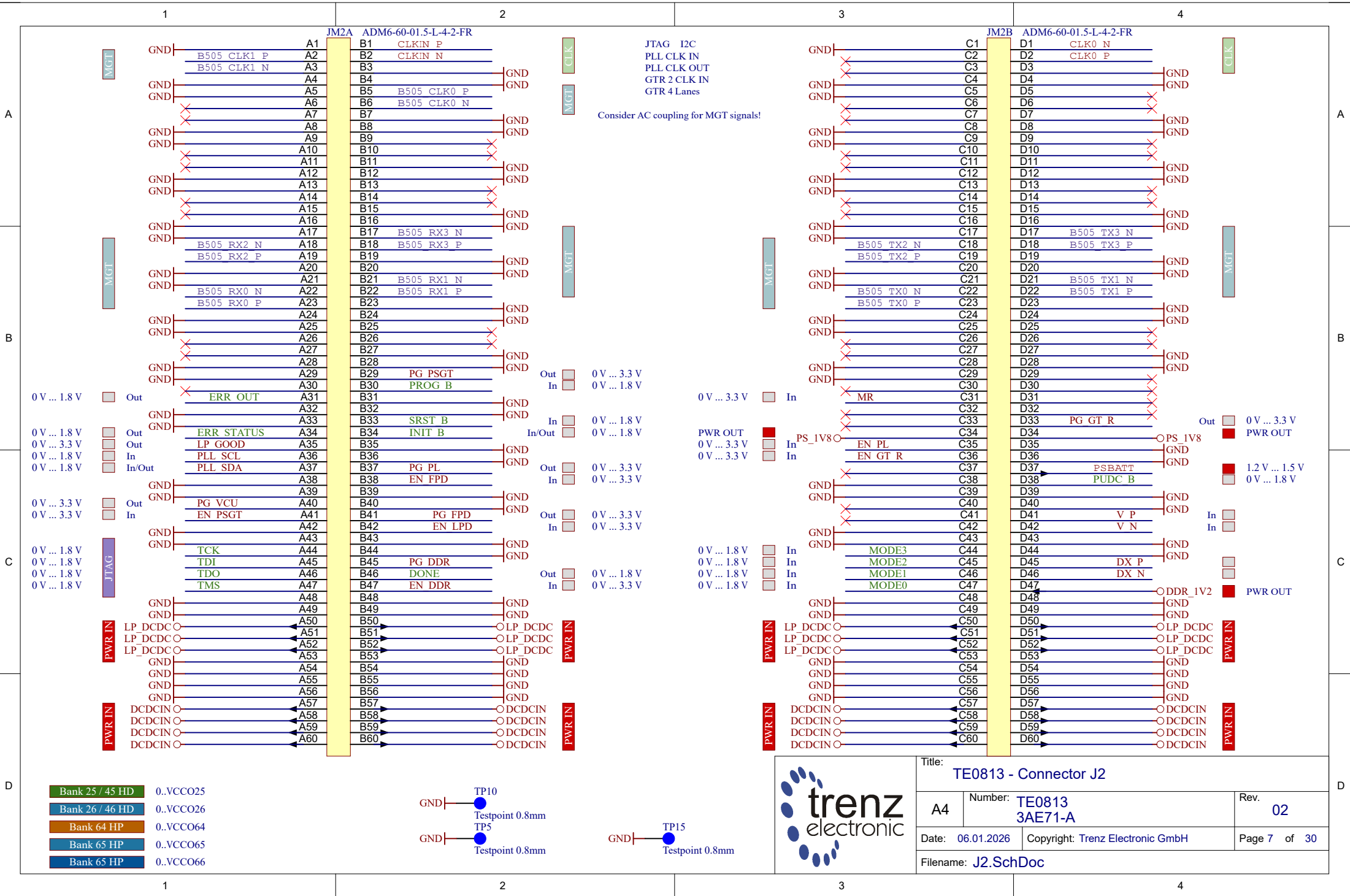
LOGO PRINT

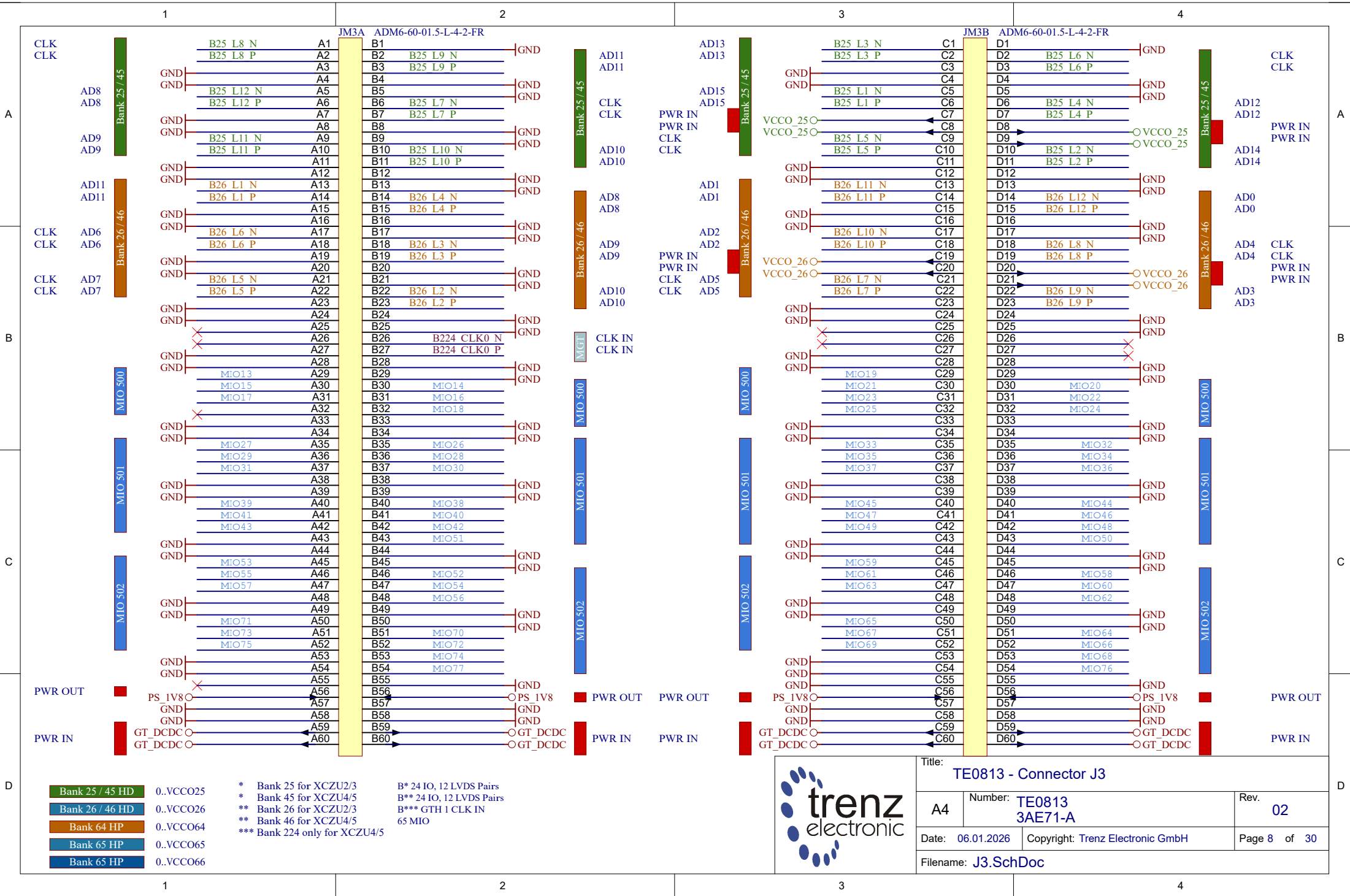
Serial
Serial
Serialnumber 6,3 x 6.3mm



Title: TE0813		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 5 of 30
Filename: TE0813.SchDoc		







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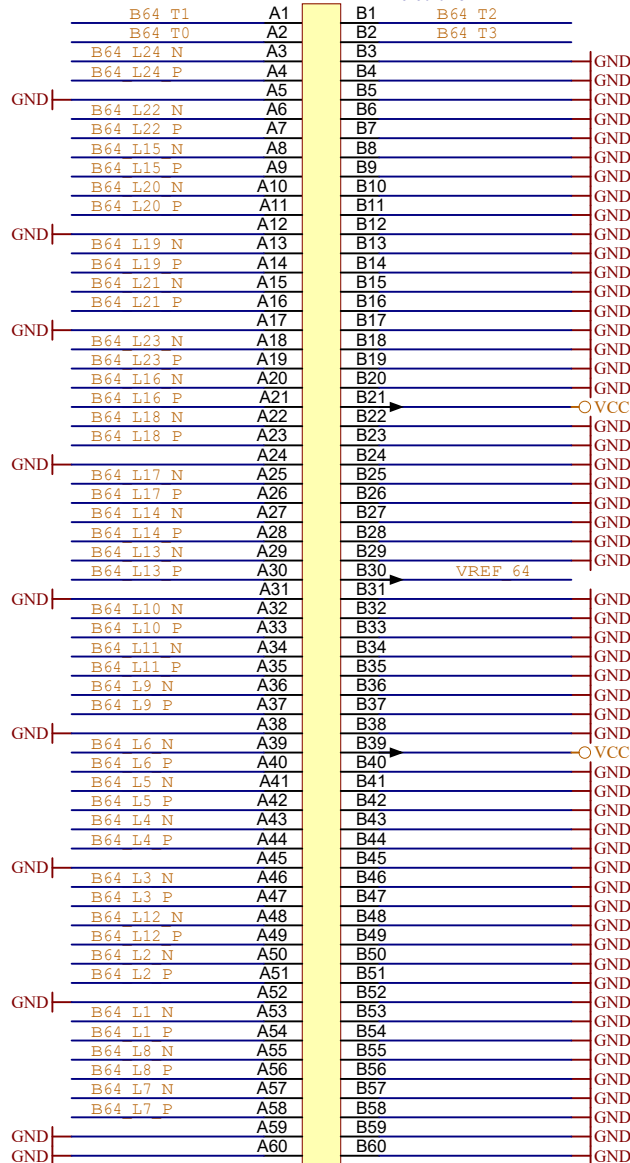
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JM4A ADM6-60-01.5-L-4-2-FR

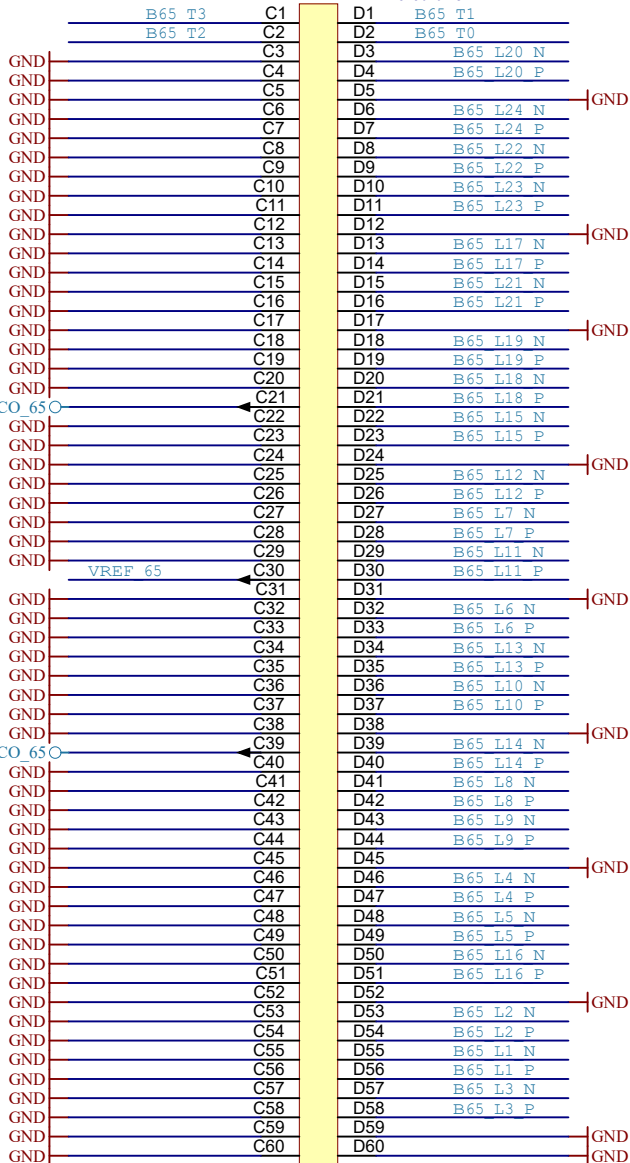


Bank 64

B64 52 IO, 24 LVDS Pairs
B64 52 IO, 24 LVDS Pairs

Bank 65

JM4B ADM6-60-01.5-L-4-2-FR



Bank 65

AD1
AD1
PERSTN0
PERSTN1, I2C_SDA
CLK
CLK
I2C_SCLK
AD10
AD10
AD8
AD8
AD9
CLK
AD9
CLK
AD2
AD2
AD11
AD11
CLK
CLK
CLK
CLK
CLK
CLK
AD6
AD6
CLK
CLK
AD4
CLK
AD4
CLK
CLK
CLK
AD5
AD5
AD12
AD12
AD7
SMBALERT
AD7
CLK
AD14
CLK
AD3
CLK
AD3
CLK
CLK
CLK
AD15
AD15

Bank 25 / 45 HD 0..VCCO25
Bank 26 / 46 HD 0..VCCO26
Bank 64 HP 0..VCCO64
Bank 65 HP 0..VCCO65
Bank 65 HP 0..VCCO66



Title: TE0813 - Connector J4

A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: J4.SchDoc		

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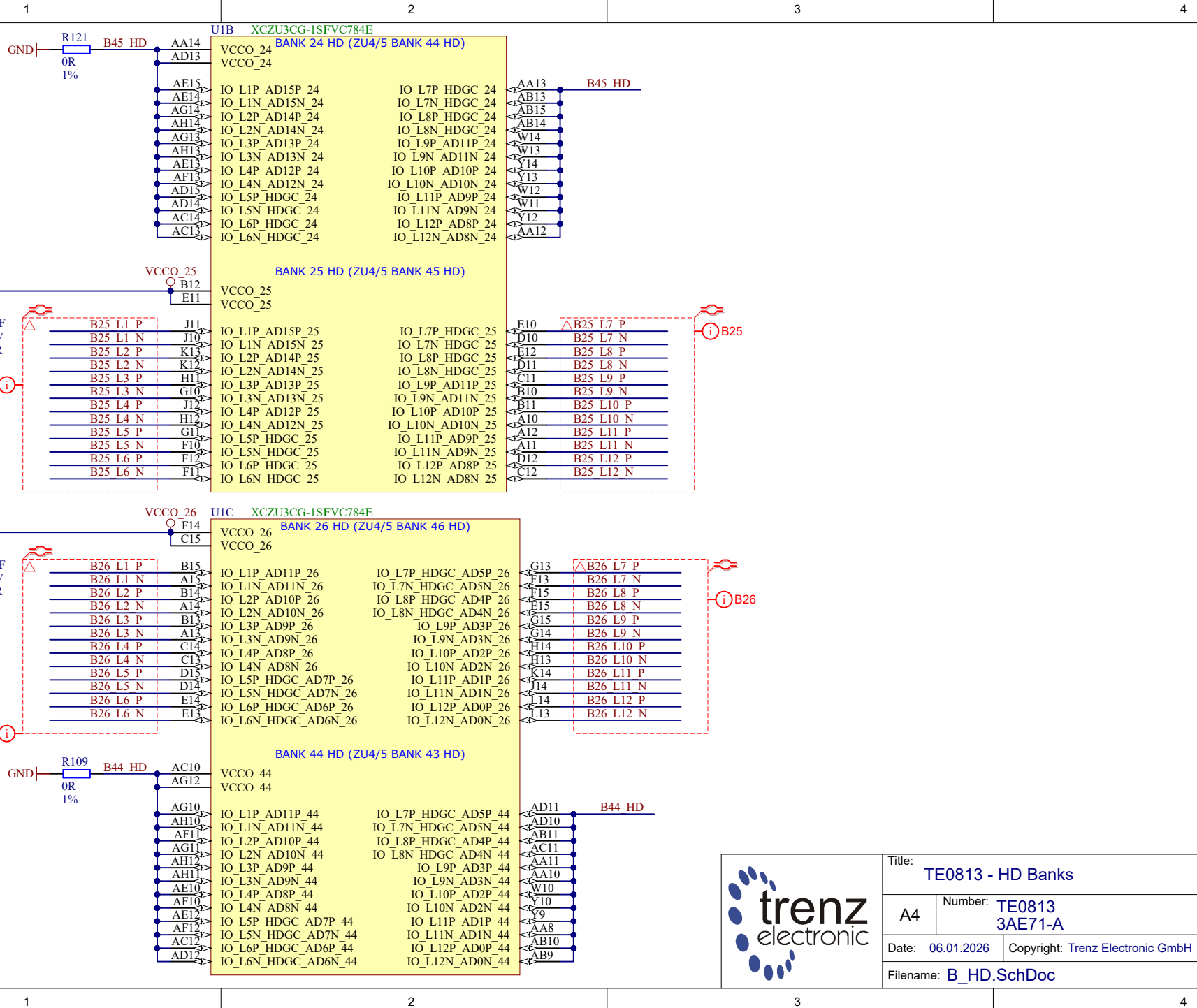
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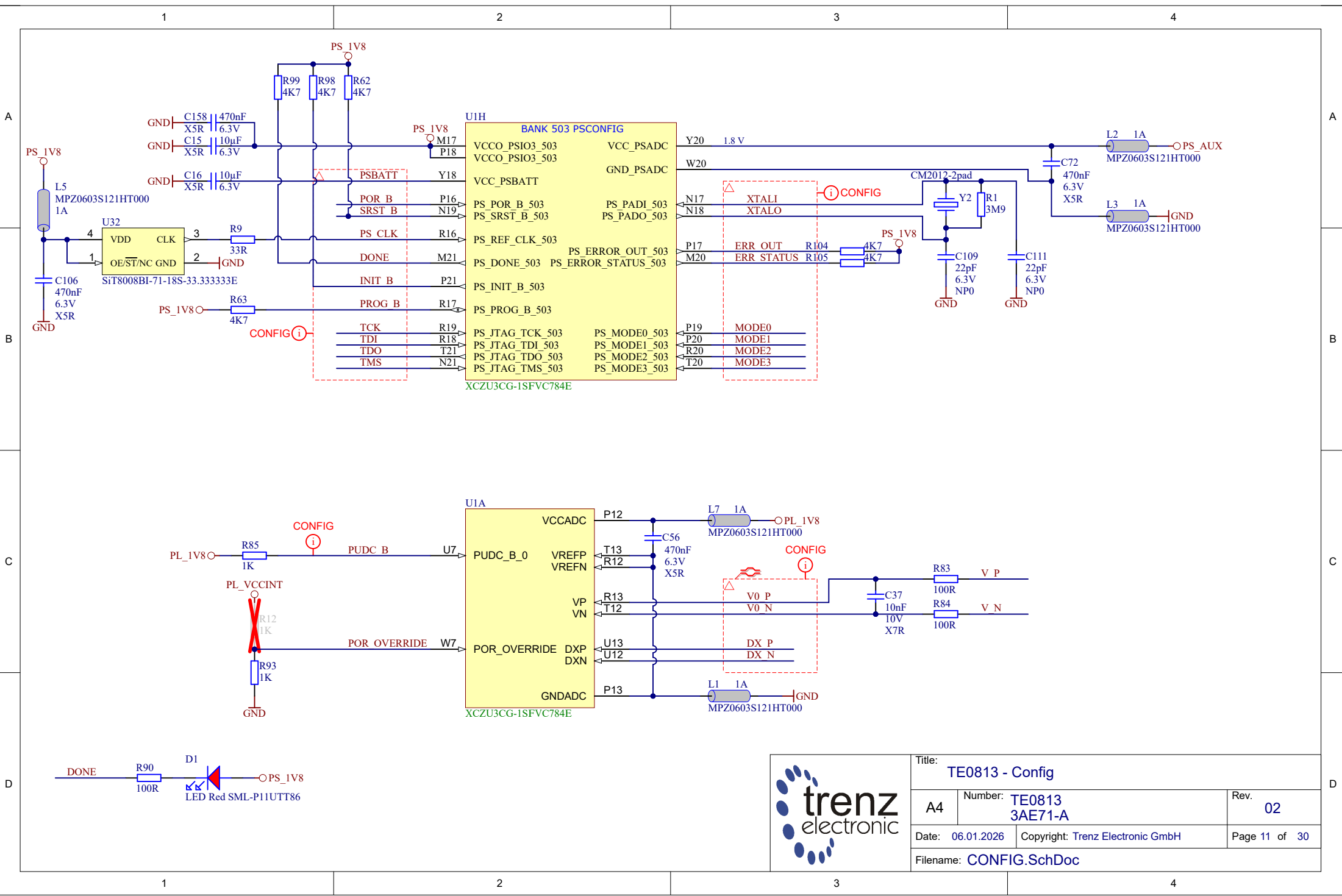
A

B

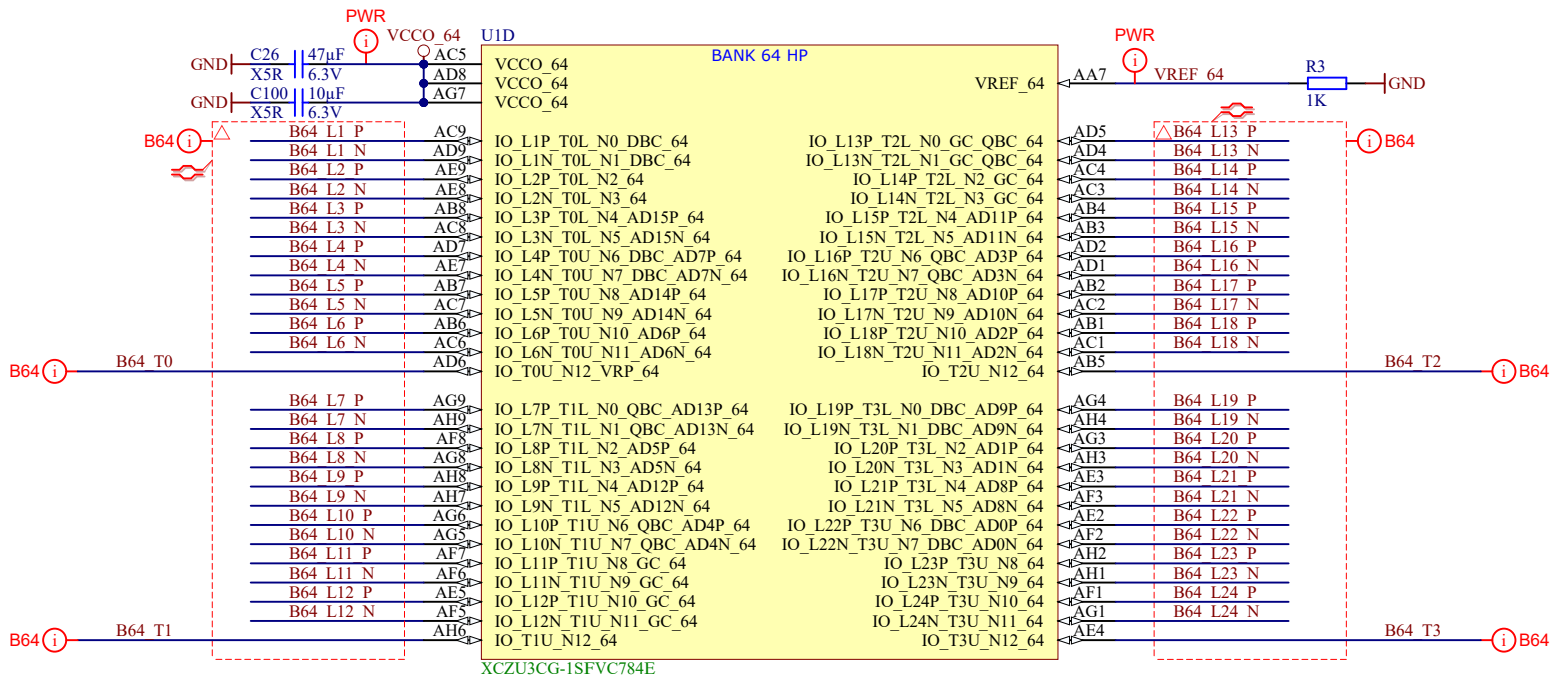
C

D





Title: TE0813 - Config		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 11 of 30
Filename: CONFIG.SchDoc		



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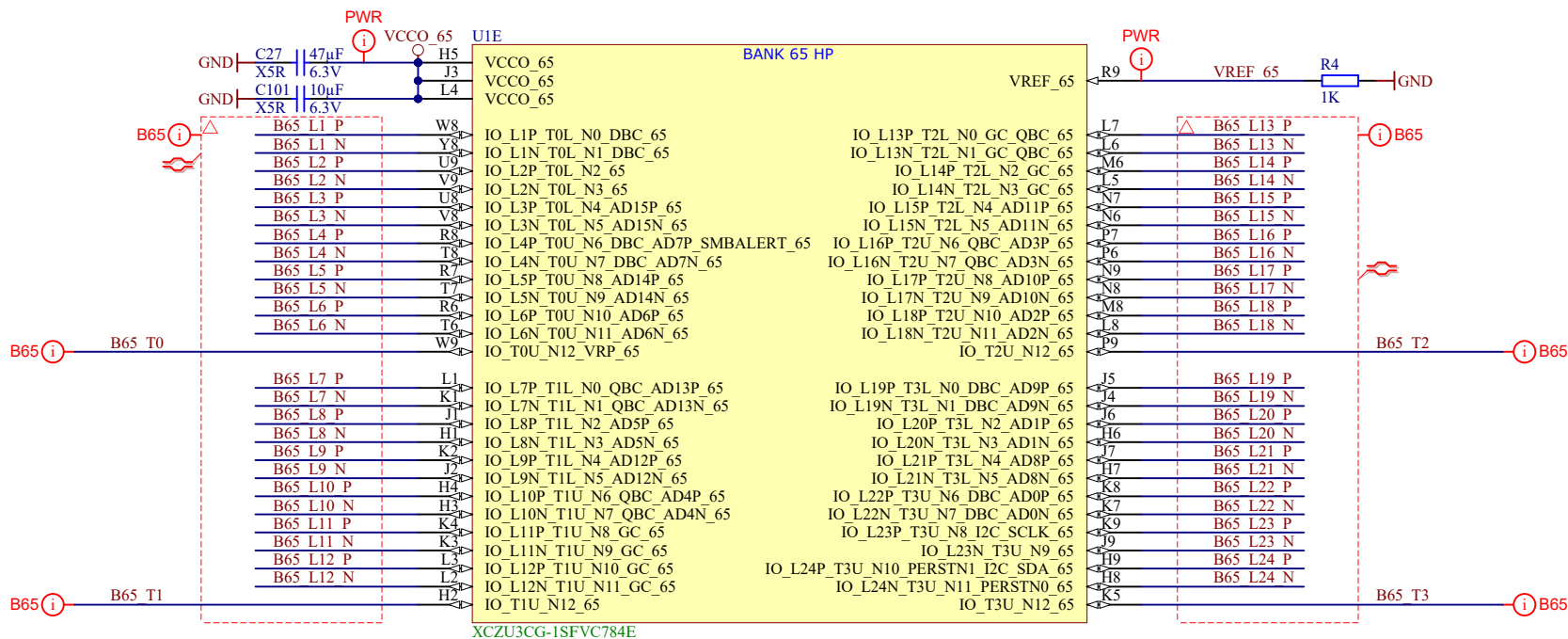
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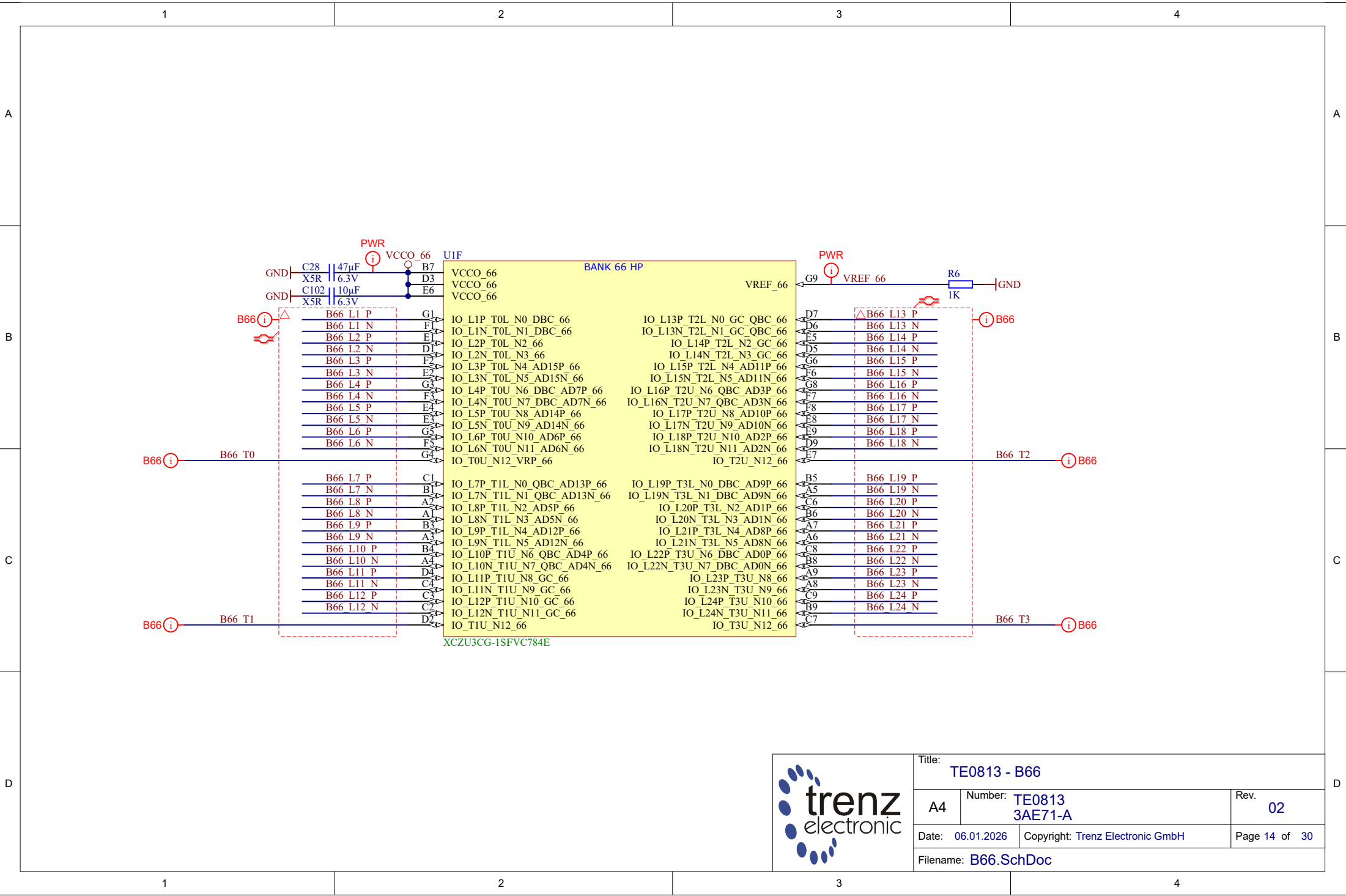
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 13 of 30
Filename: B65.SchDoc		

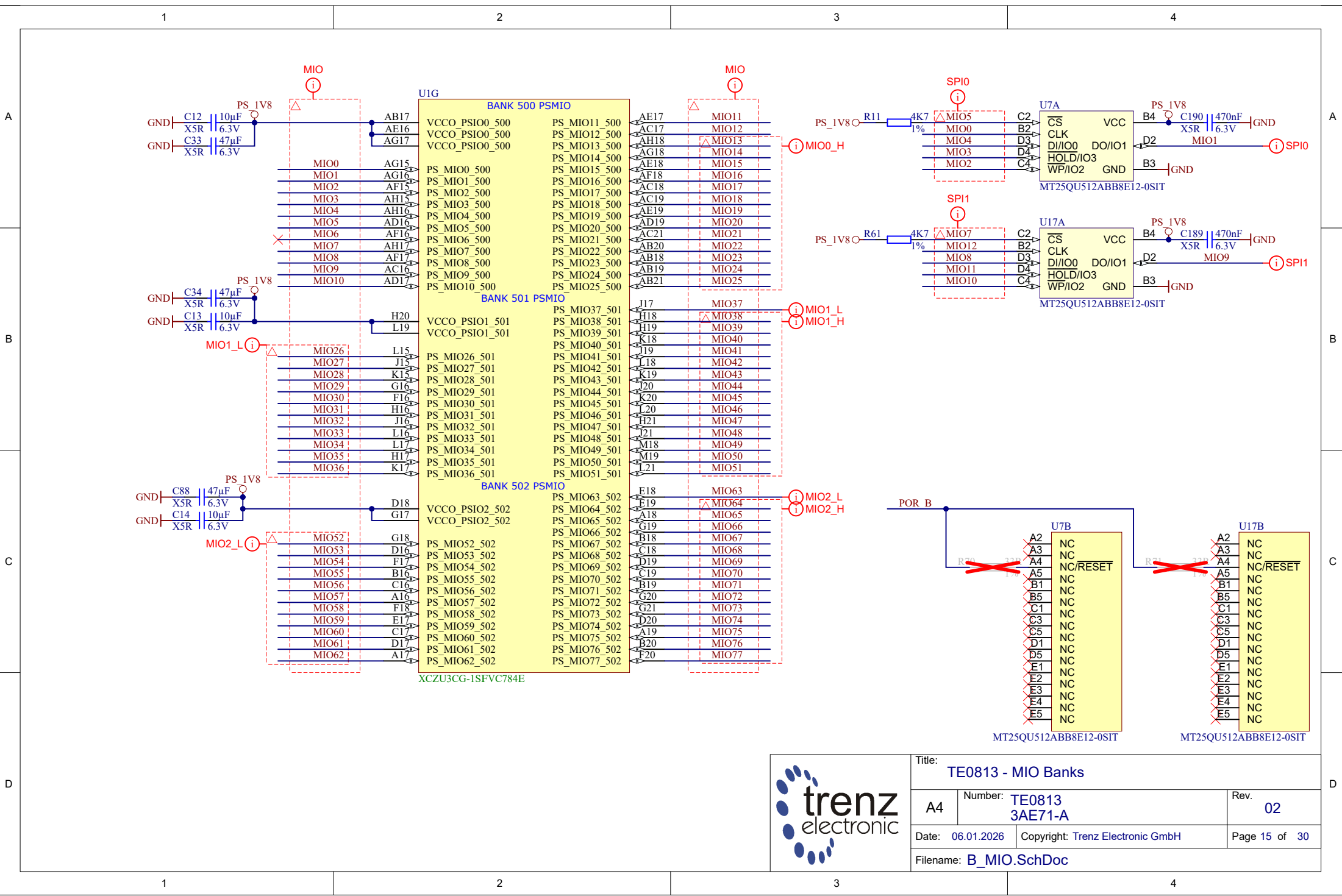
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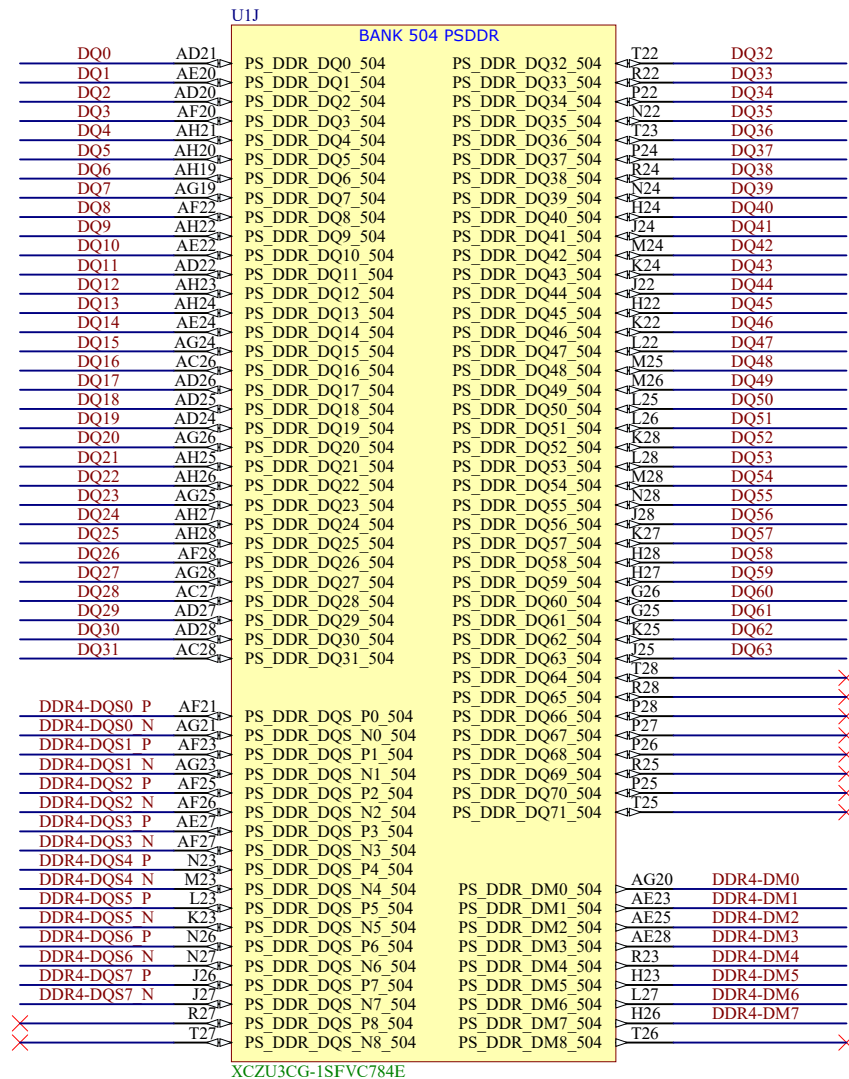
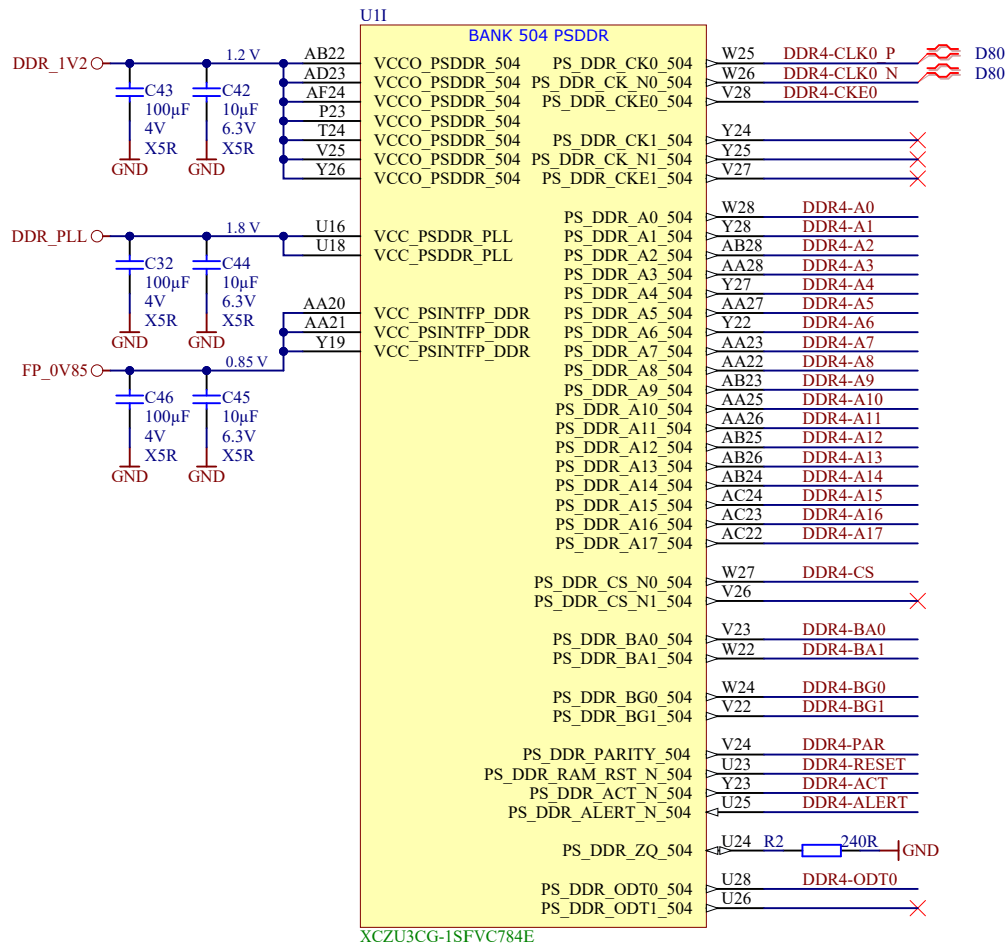
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D



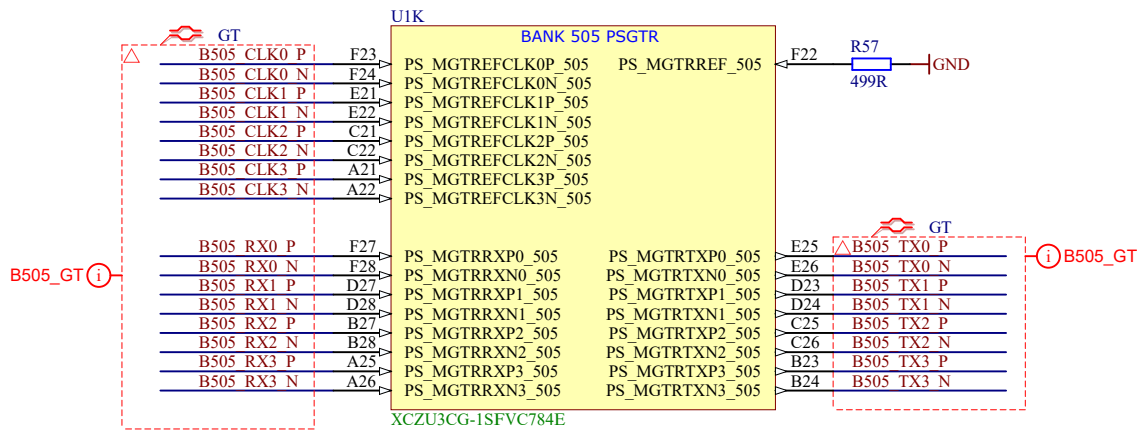
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 16 of 30
Filename: PS_DDR.SchDoc		

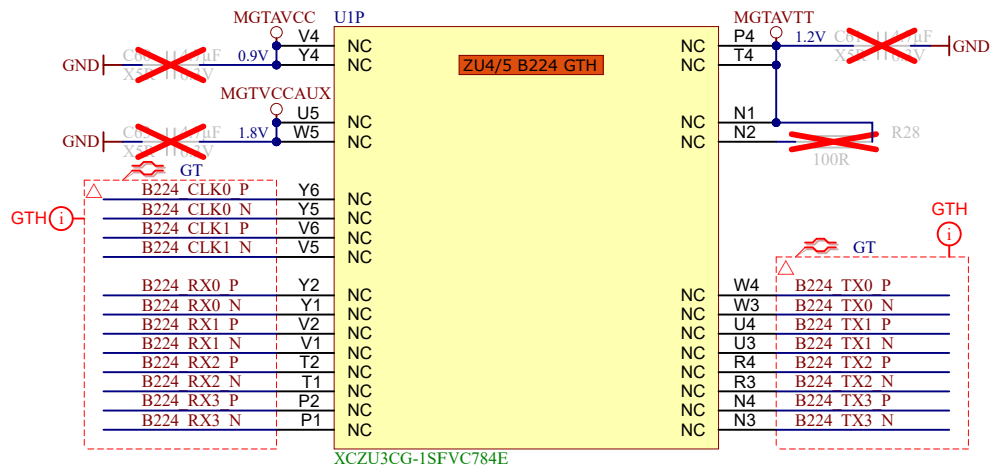
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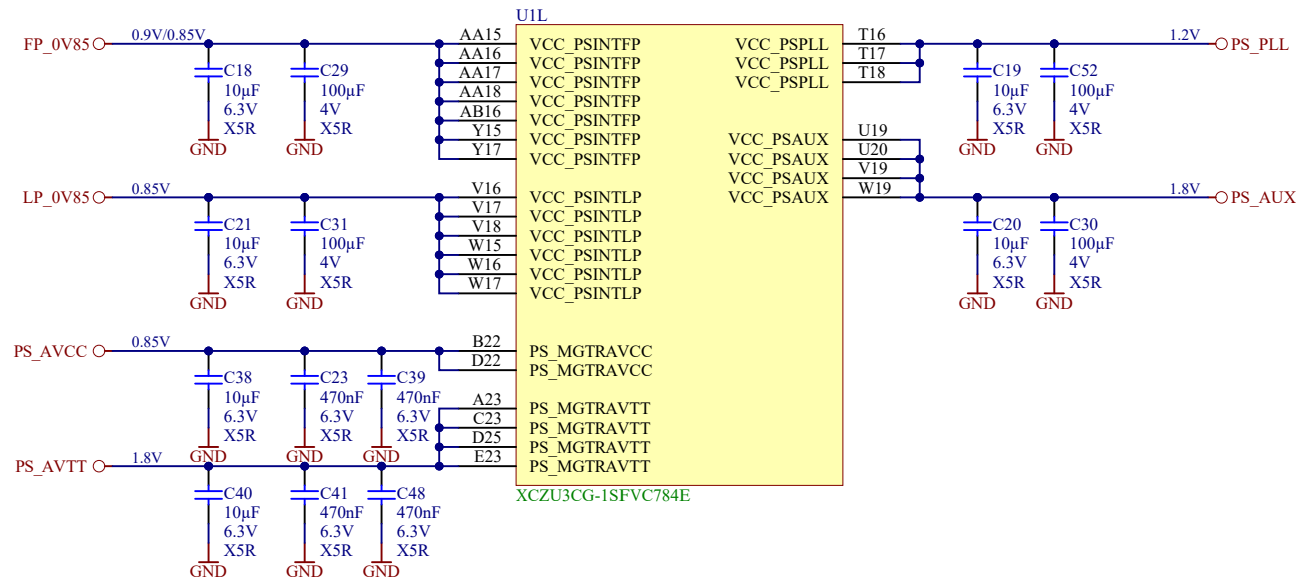
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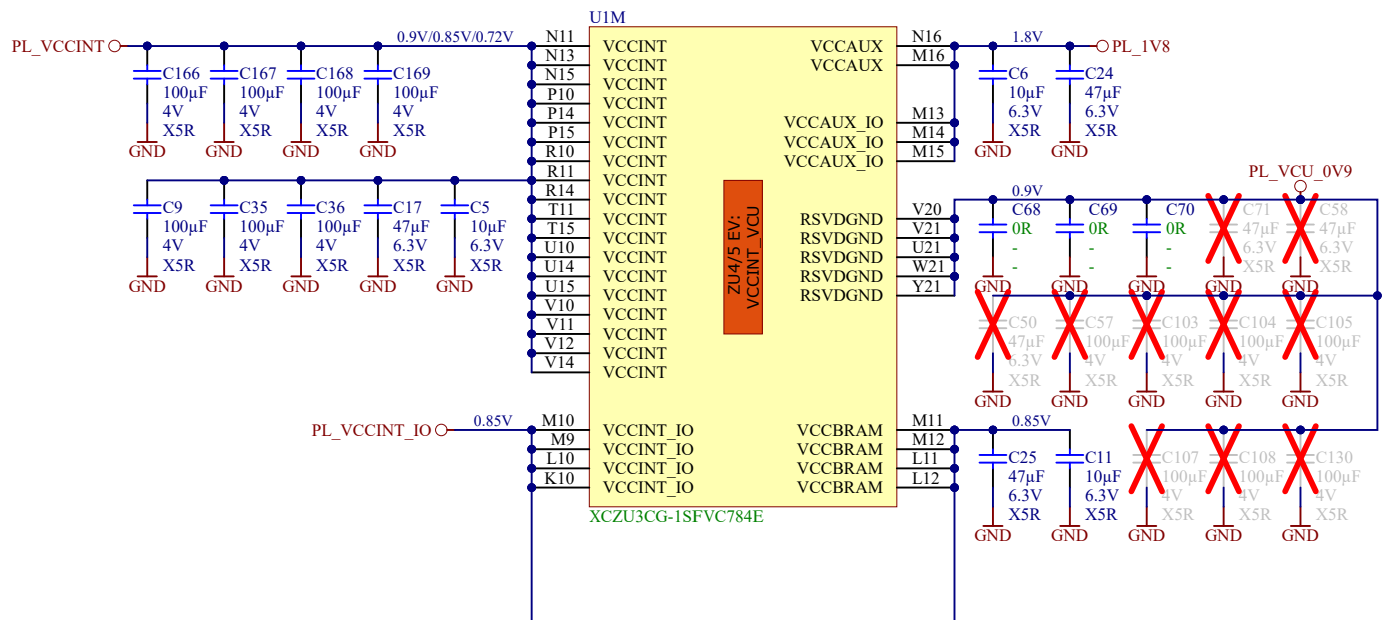


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		A4	Number: TE0813 3AE71-A
Date: 06.01.2026		Copyright: Trenz Electronic GmbH	
Filename: B_GT.SchDoc		Page 18 of 30	





Title: TE0813 - ZU_PS_POWER		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	
Page 19 of 30		
Filename: ZU_PS_POWER.SchDoc		

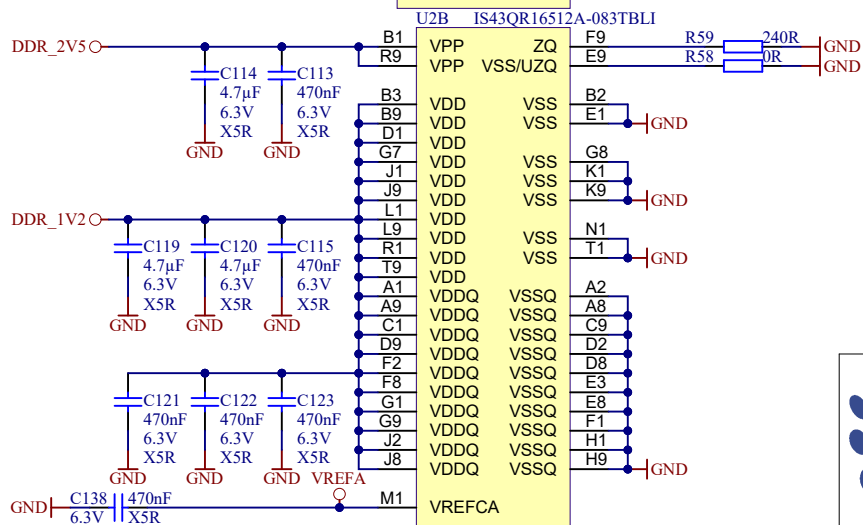
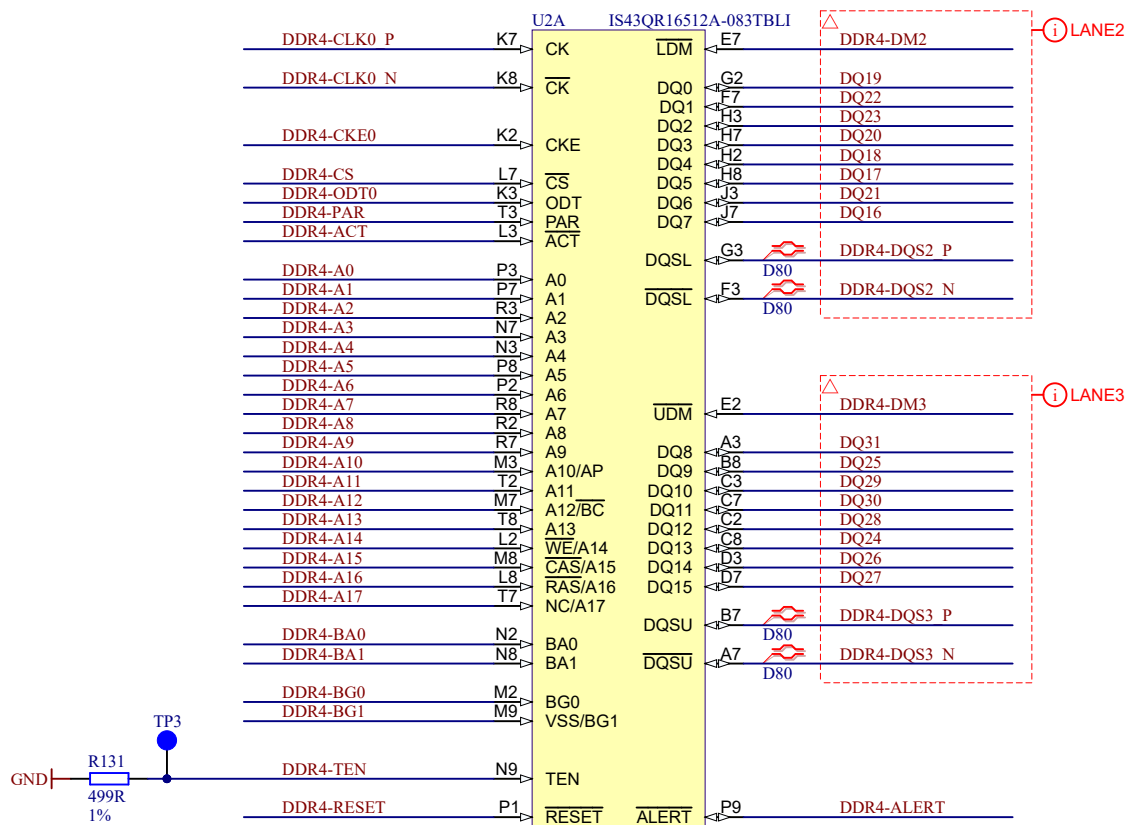


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Title: TE0813 - DDR4_1_RAM		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 21 of 30
Filename: DDR4-RAM.SchDoc		

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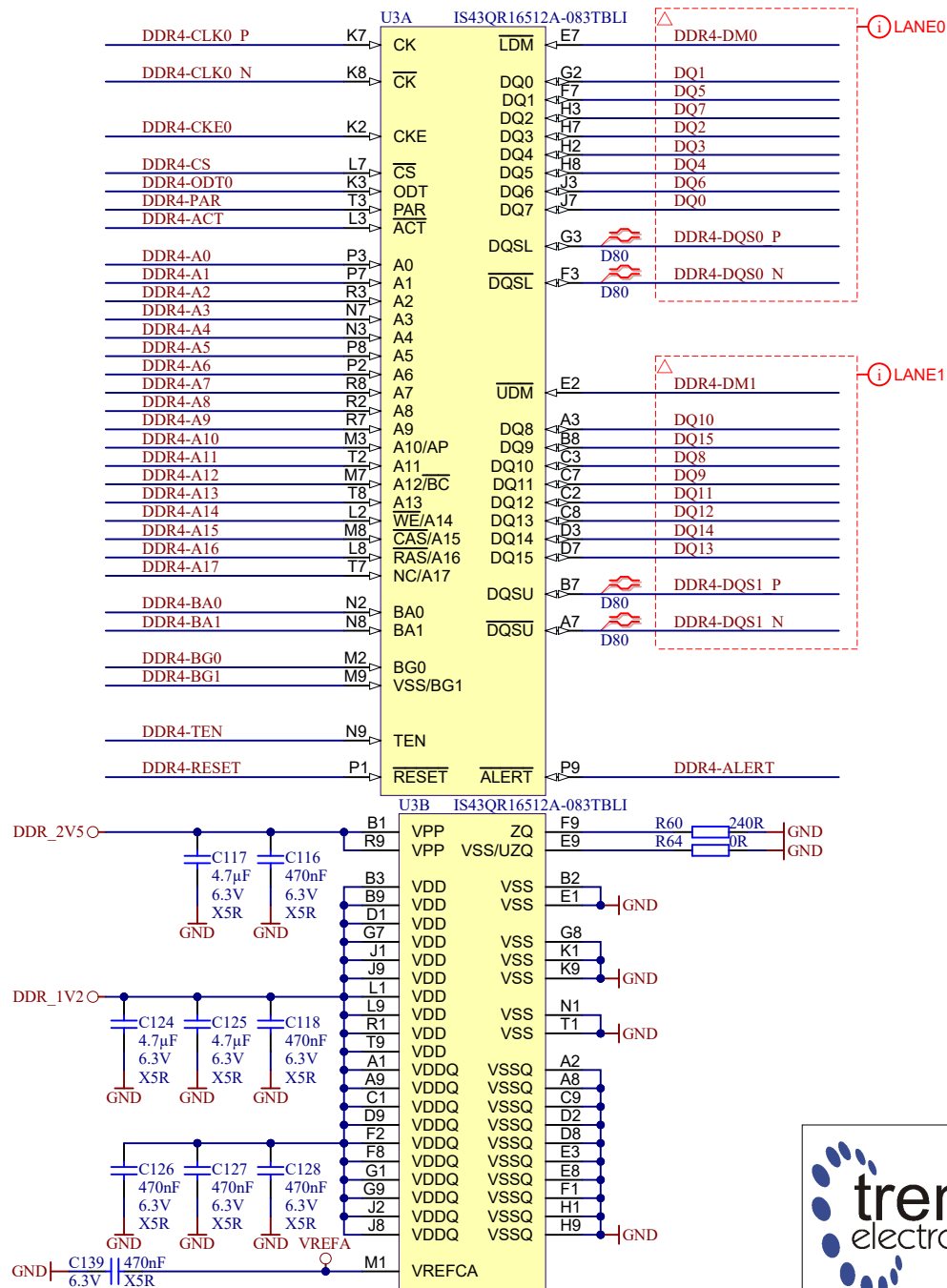
B

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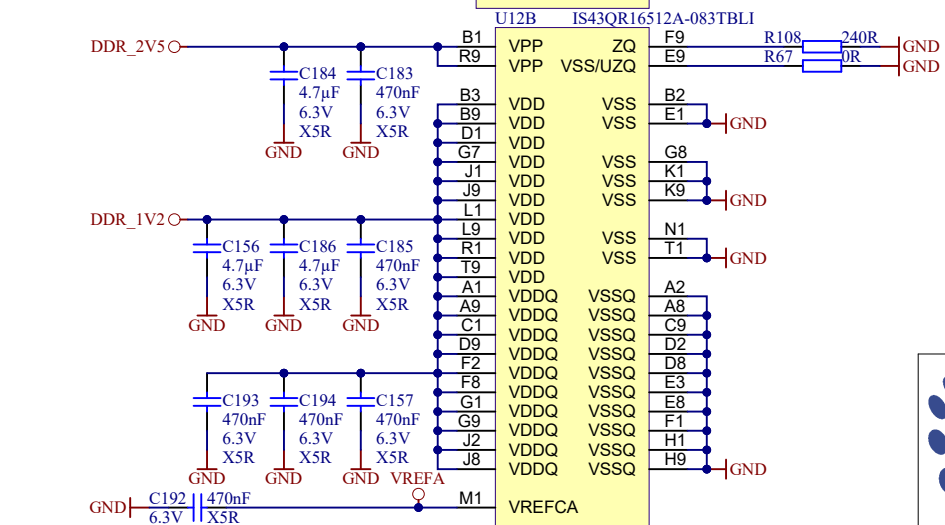
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A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 22 of 30
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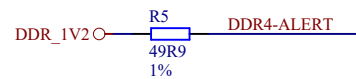
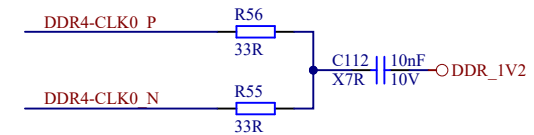
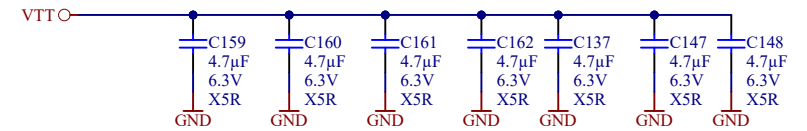
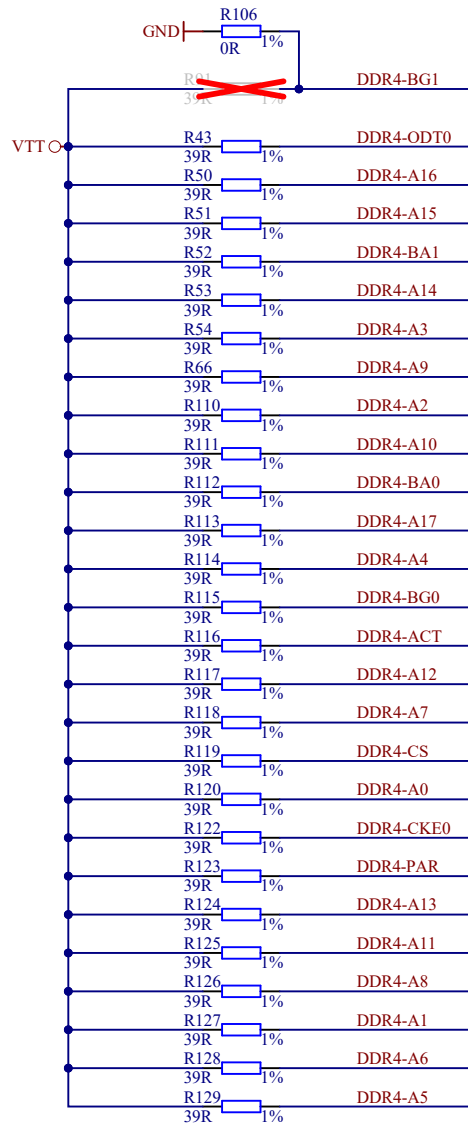
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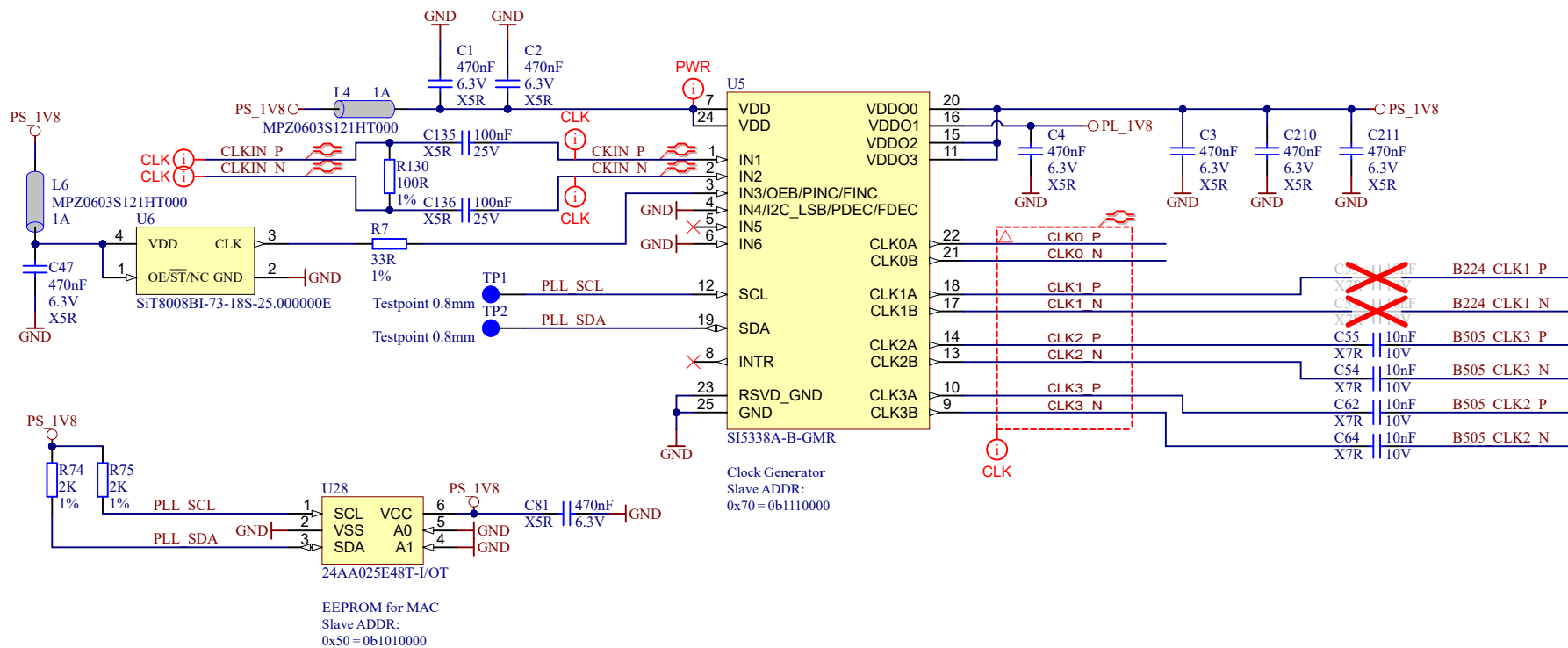
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Filename: **DDR4-RAM 4.SchDoc**



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			A4 Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026			Copyright: Trenz Electronic GmbH	
Filename: DDR4-TERM.SchDoc			Page 25 of 30	

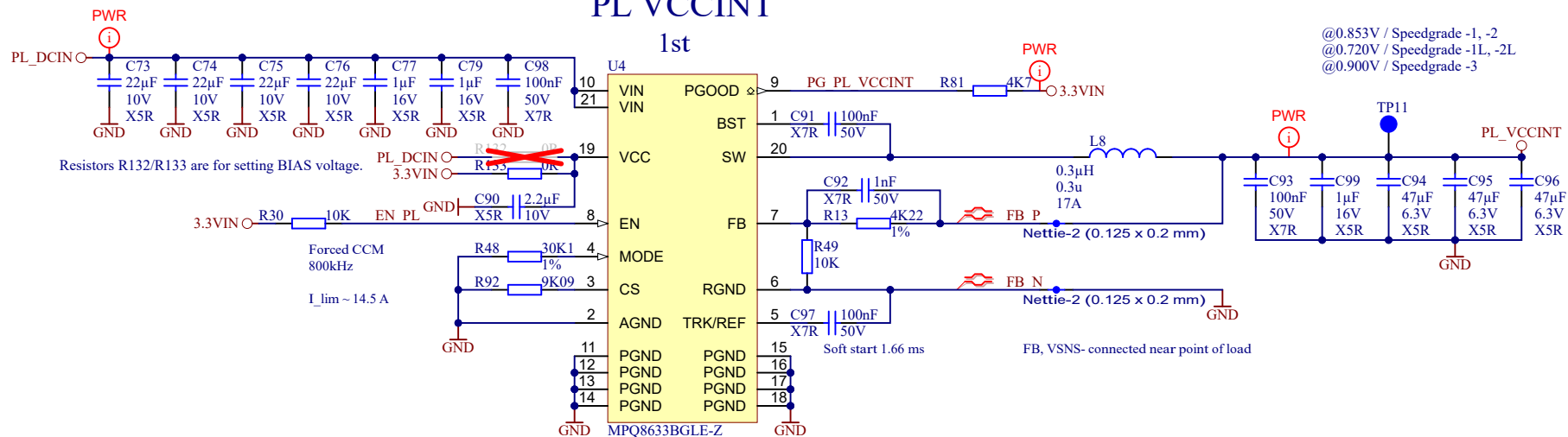


Title: TE0813 - CLOCK		
A4	Number: TE0813 3AE71-A	Rev. 02
Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 26 of 30
Filename: Clock.SchDoc		

U4 can be TPS548A28RWW or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

PL VCCINT

1st



FPGA Speedgrade	R13	R49	PL_VCCINT
-1LI	2 kOhm	10 kOhm	0.720 V
-2LE	2 kOhm	10 kOhm	0.720 V
-1	4.22 kOhm	10 kOhm	0.853 V
-2	4.22 kOhm	10 kOhm	0.853 V
-3E	10 kOhm	20 kOhm	0.900 V

U4 pin compatible with

- TPS548B28 (20A)
- TPS548A28 (15A)
- TPS54JA20 (12A)



Title:	TE0813 - POWER_1
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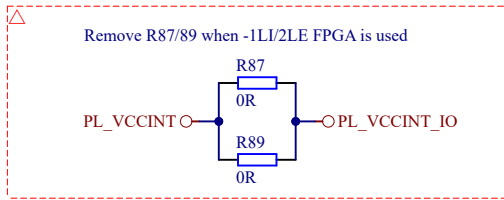
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Date: 06.01.2026 Copyright: Trenz Electronic GmbH

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Rev.	02
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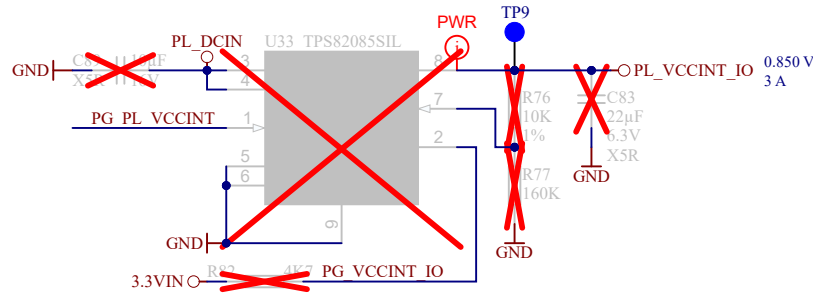


Remove R86 when -1L1/2LE FPGA is used

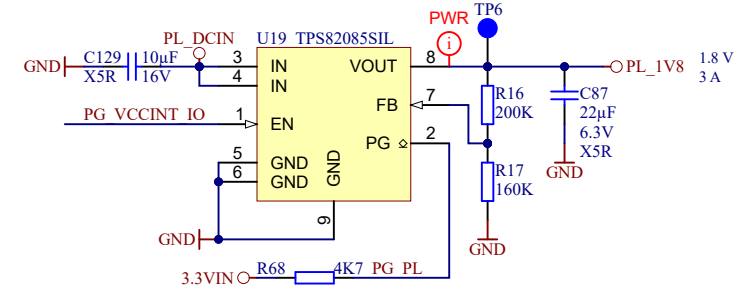


VCCINT_IO & VCCBRAM

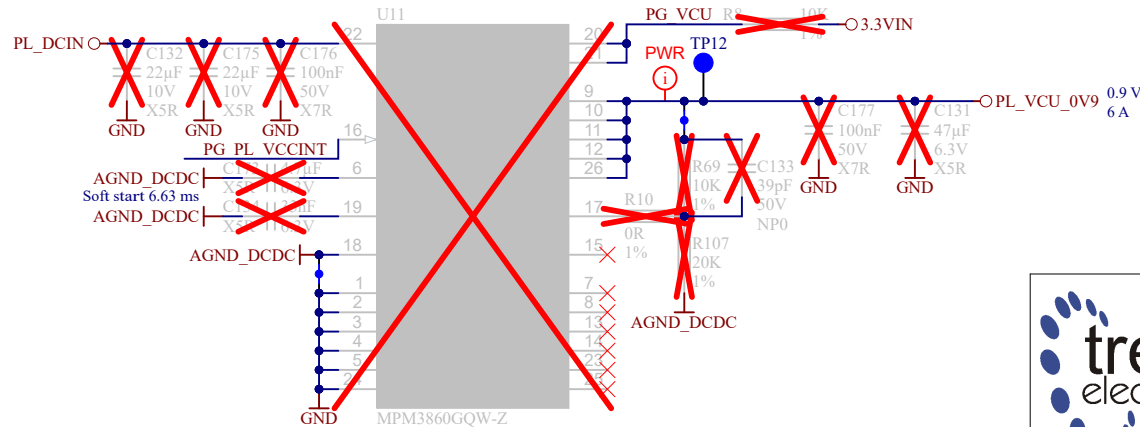
Add U33 when -1L1/2LE FPGA is used



PL VCCIO

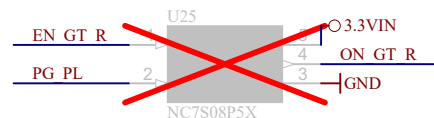
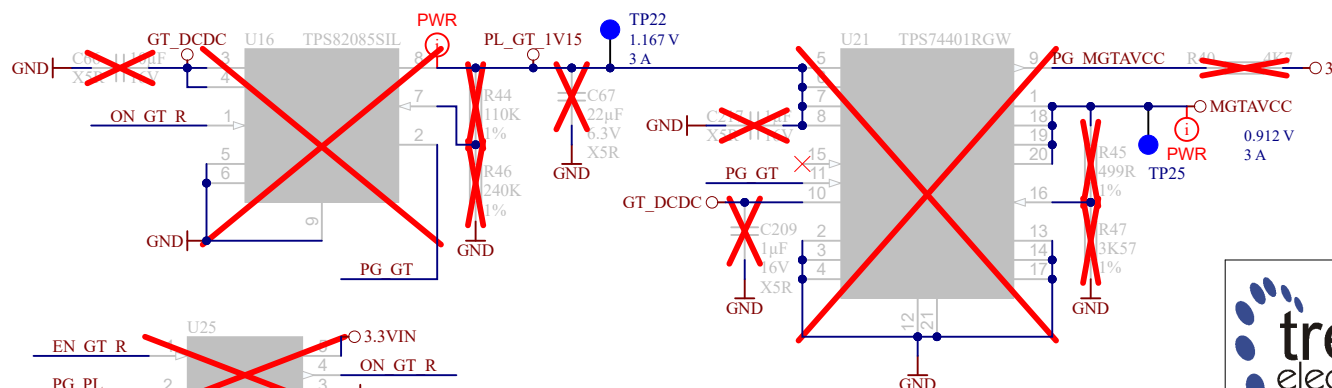
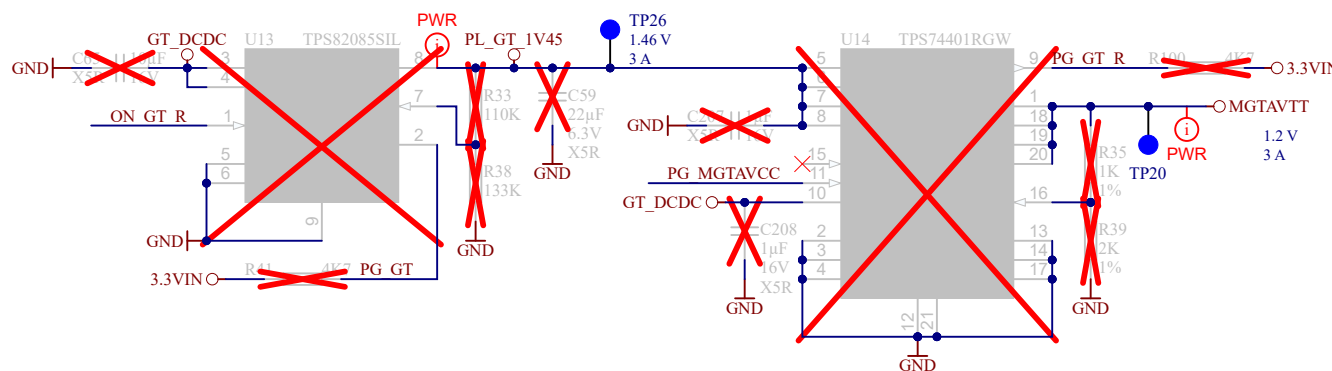
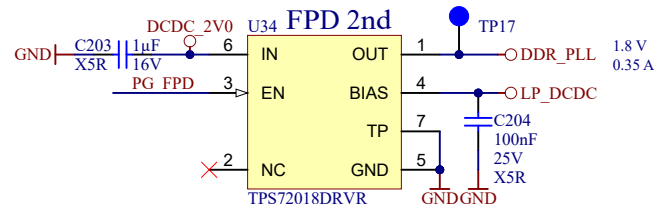
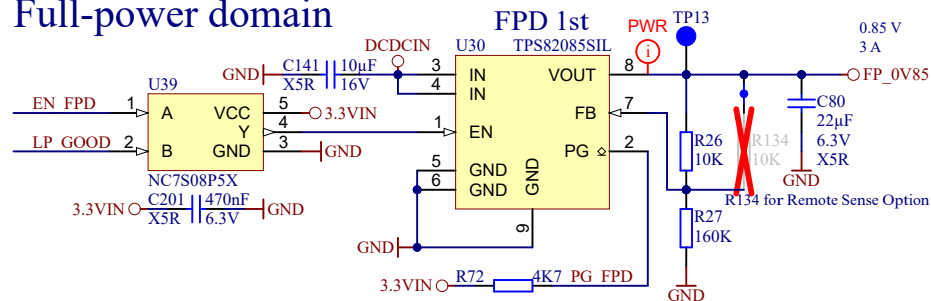


VCU

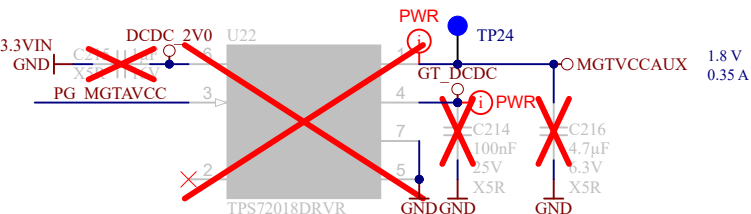
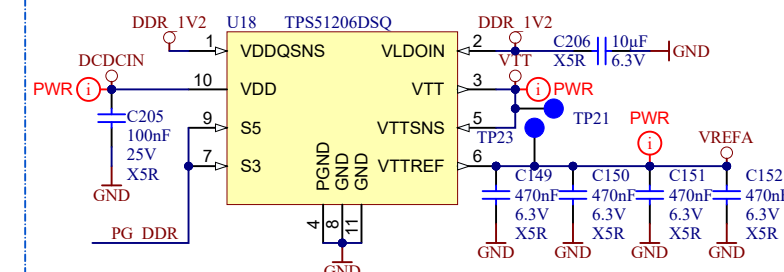
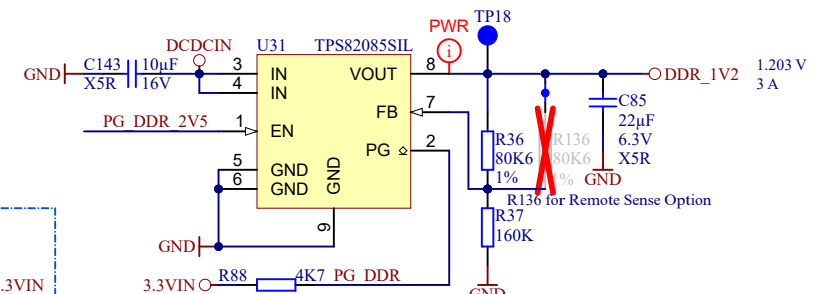
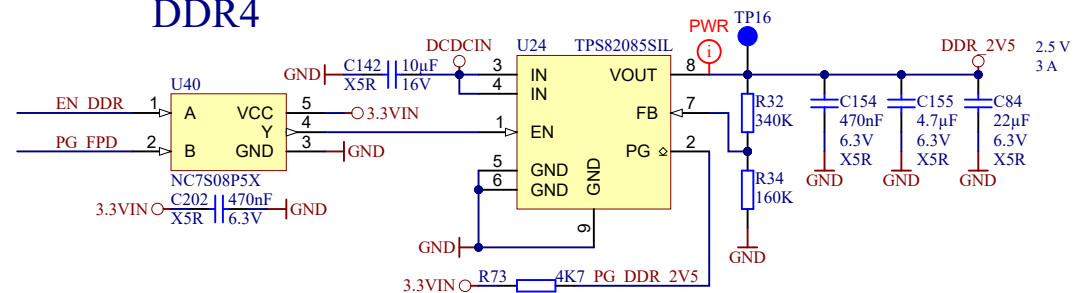


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Full-power domain



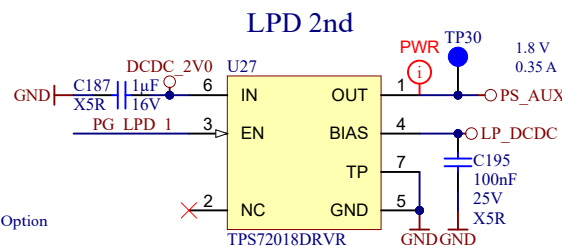
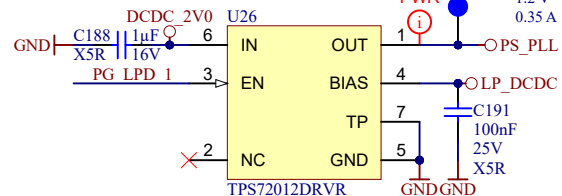
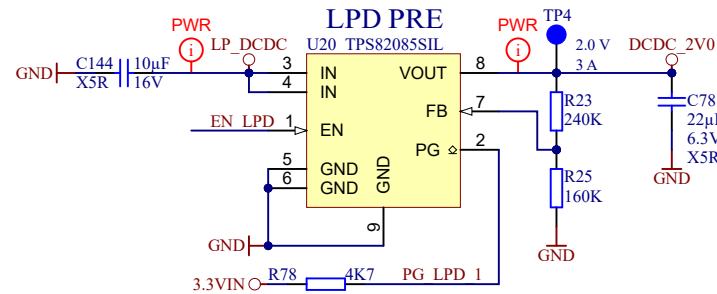
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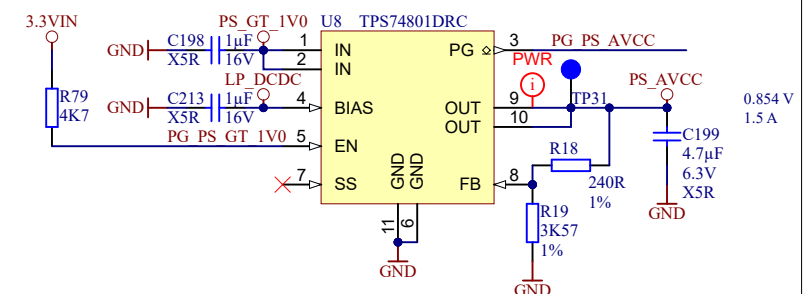
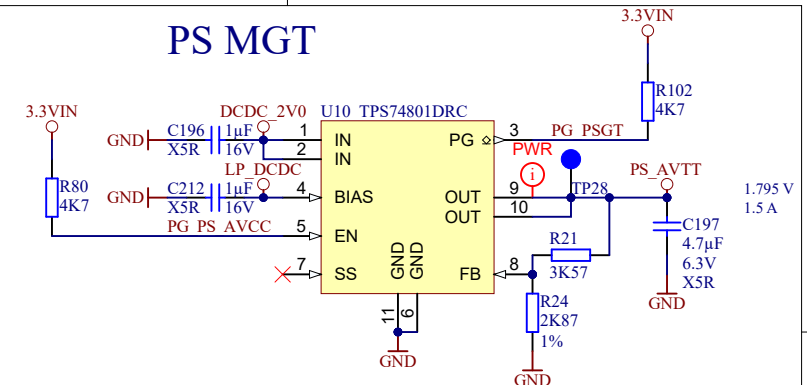
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Filename: POWER_2.SchDoc		Page 29 of 30

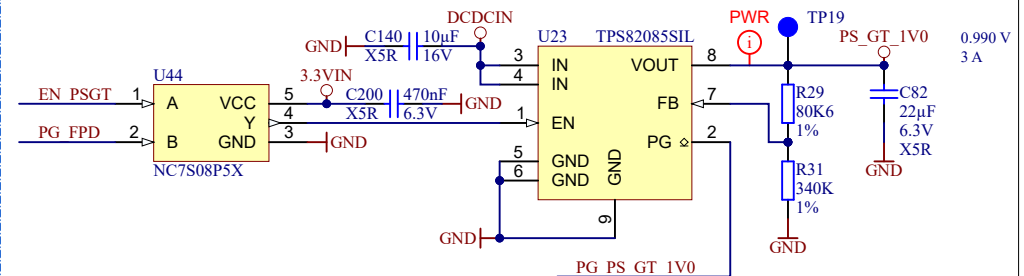
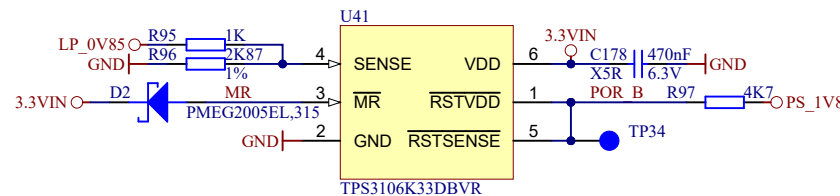
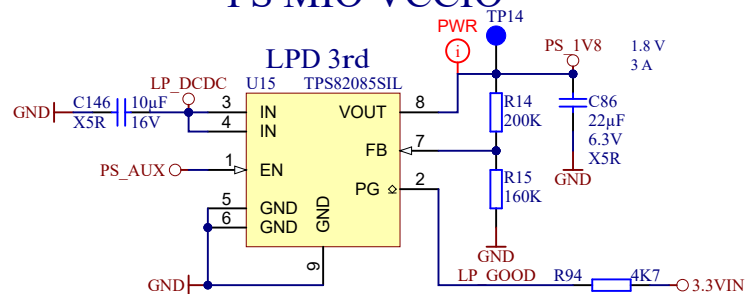
Low-power domain



PS MGT



PS MIO VCCIO



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Net Name	Voltage Rail	Low Detect
LP_0V85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V