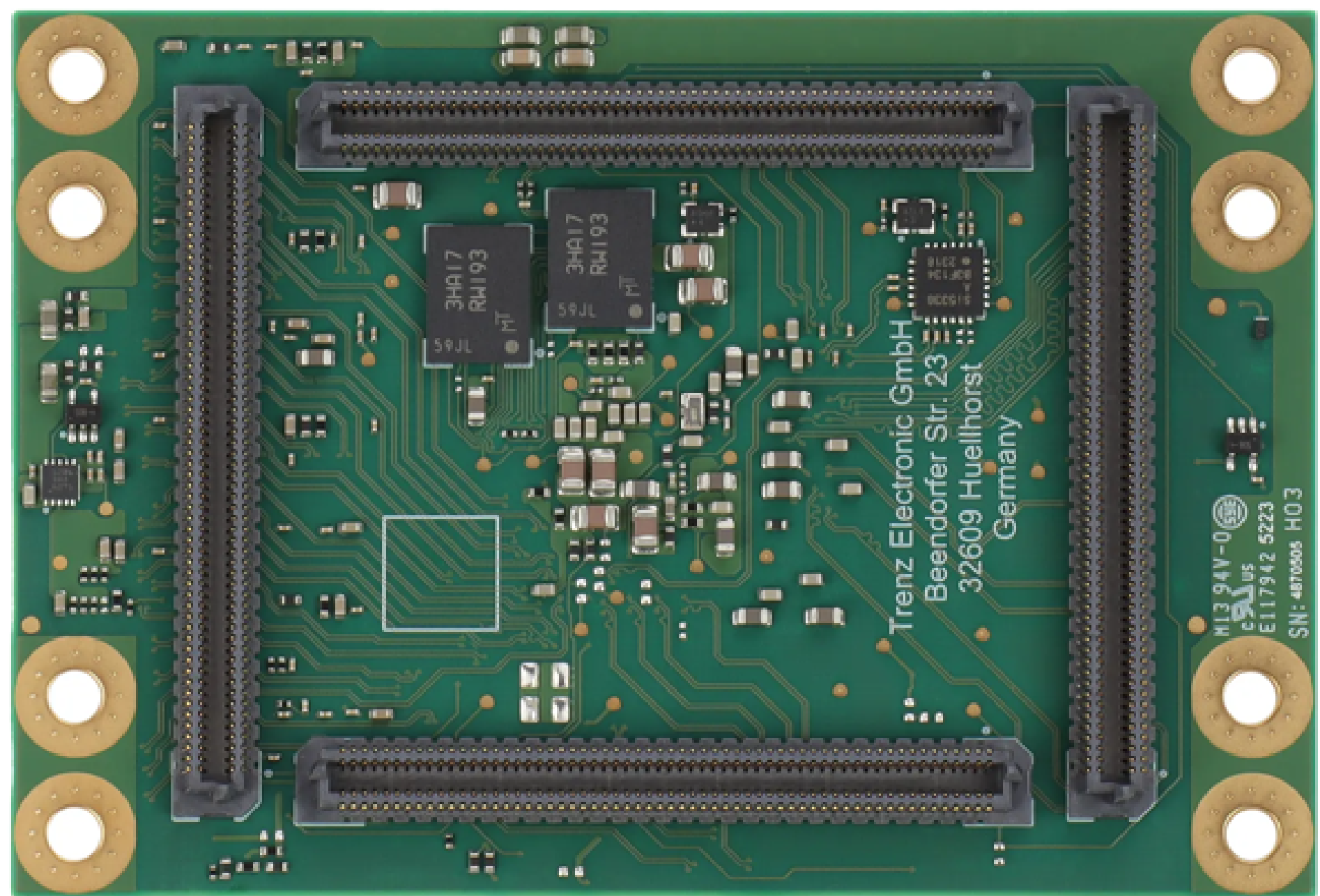
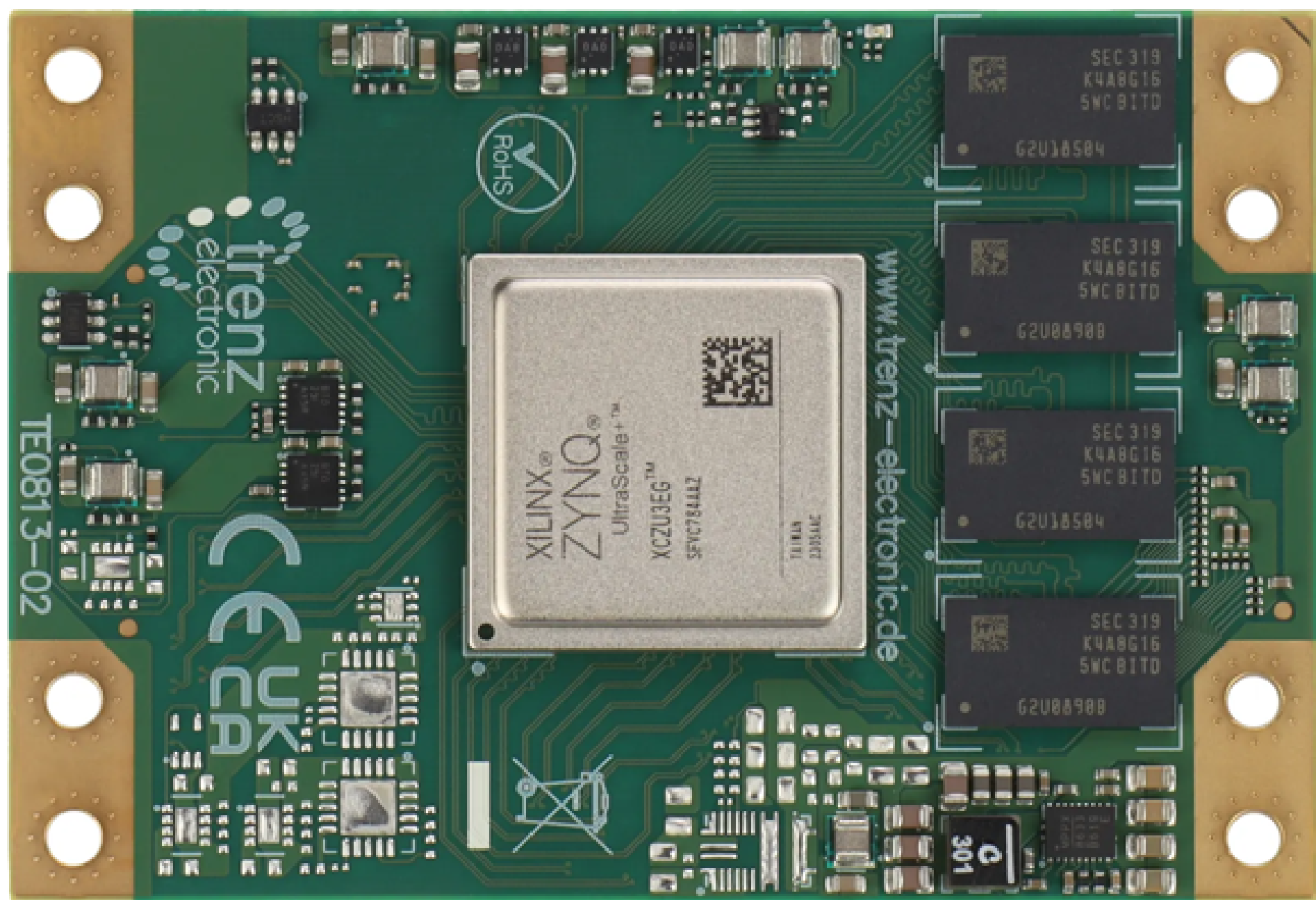
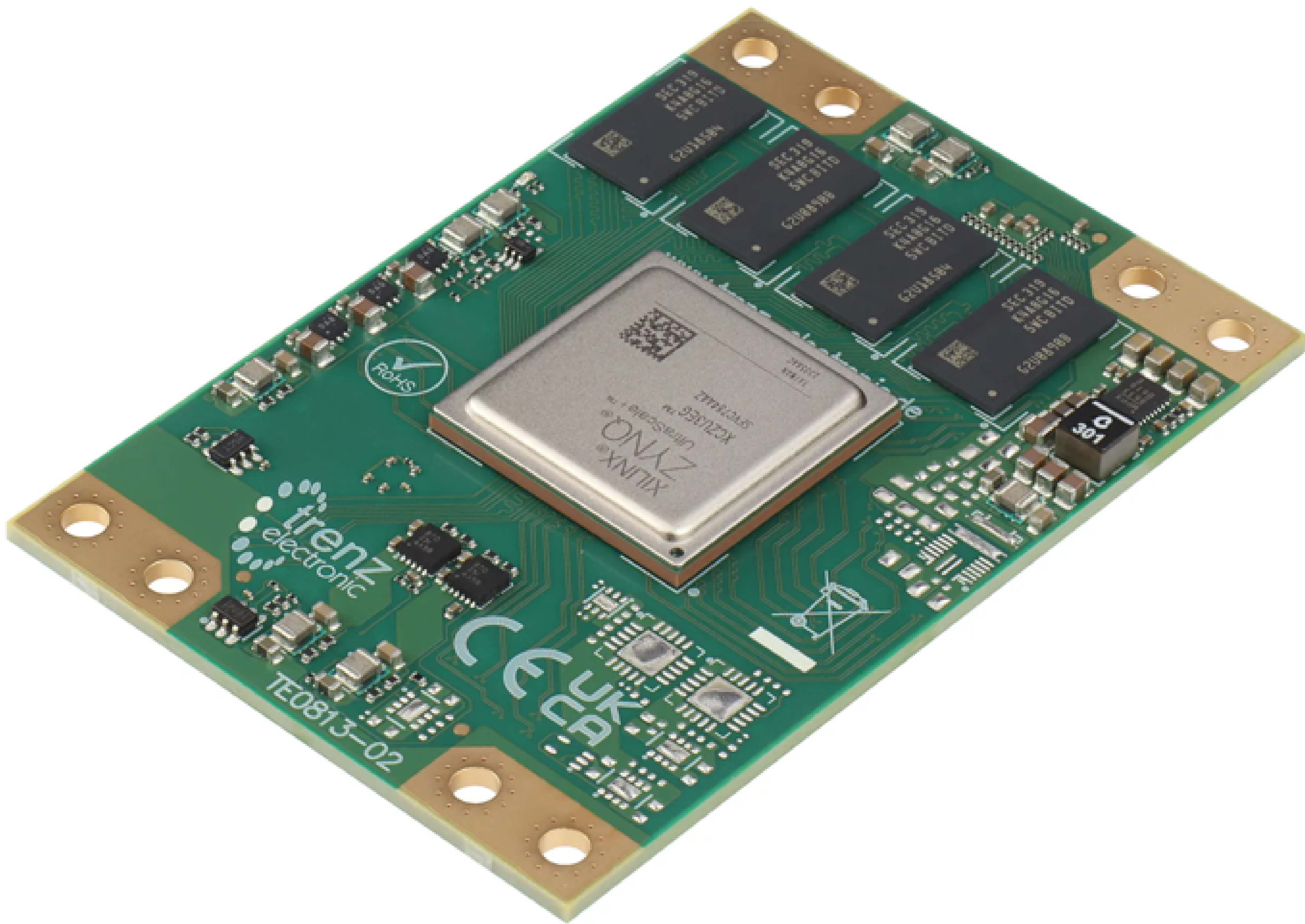


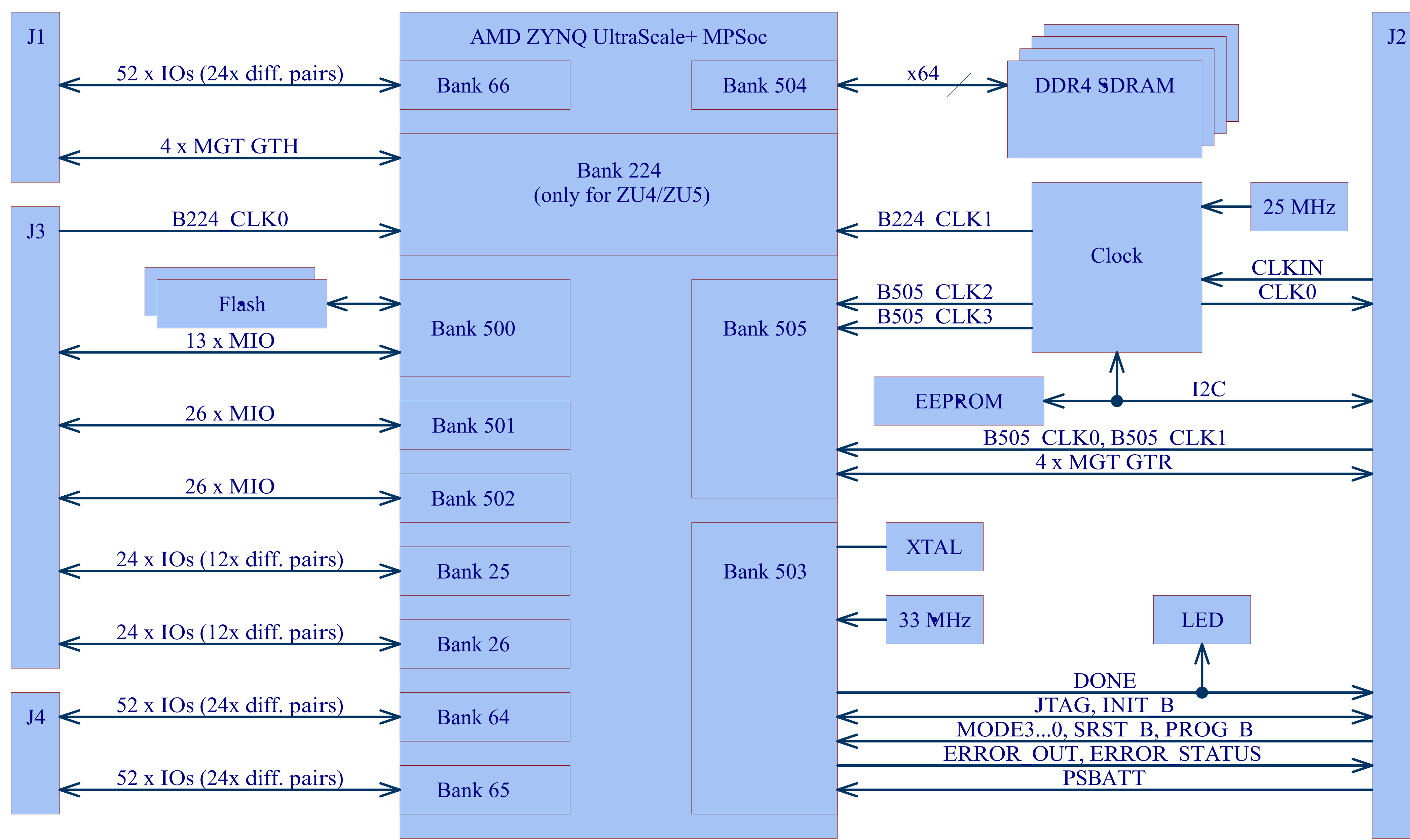


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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation,
even if the design is just adapted or modified.
TE0813 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.
Schematics and other handouts serve for informational purposes only!

Drawn by	ED
Checked by	MR
Assembly variant	3AI81-A
Created by	VG
Modified by	VG
Modified at	2026-02-16



Title: TE0813 - Legal Notices		
A4	Number: TE0813 3AI81-A	Rev. 02
Date: 04.05.2026	Copyright: Trenz Electronic GmbH	Page 1 of 30
Filename: Legal Notices Modules.SchDoc		



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3V	+/- 5 %	Micromodule Power	Management voltage rail, supplied by power rail
PL_DCIN	IN	3.3V	+/- 5 %	Micromodule Power	Programmable Logic, supplied by power rail
LP_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	Low-Power Domain, supplied by power rail
GT_DCDC	IN	3.3V	+/- 3 %	Micromodule Power	GTH Transceiver, supplied by power rail
DCDCIN	IN	3.3V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR, supplied by power rail
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	Supplied by external power rail via B2B connector
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	Supplied by external power rail via B2B connector
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	Supplied by external power rail via B2B connector
VCCO_25	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 25	Supplied by external power rail via B2B connector
VCCO_26	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 26	Supplied by external power rail via B2B connector
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	Supplied by external power rail via B2B connector
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Micromodule: Processing System
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	Micromodule: PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x70	-
EEPROM U28	0x50	-

TE0813

DDR4-TERM

ZU PS POWER

ZU POWER

POWER

POWER_1

POWER_2

POWER_3



Title:	TE0813 - System Overview
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A4

Number:	TE0813 3AI81-A
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Rev. 02

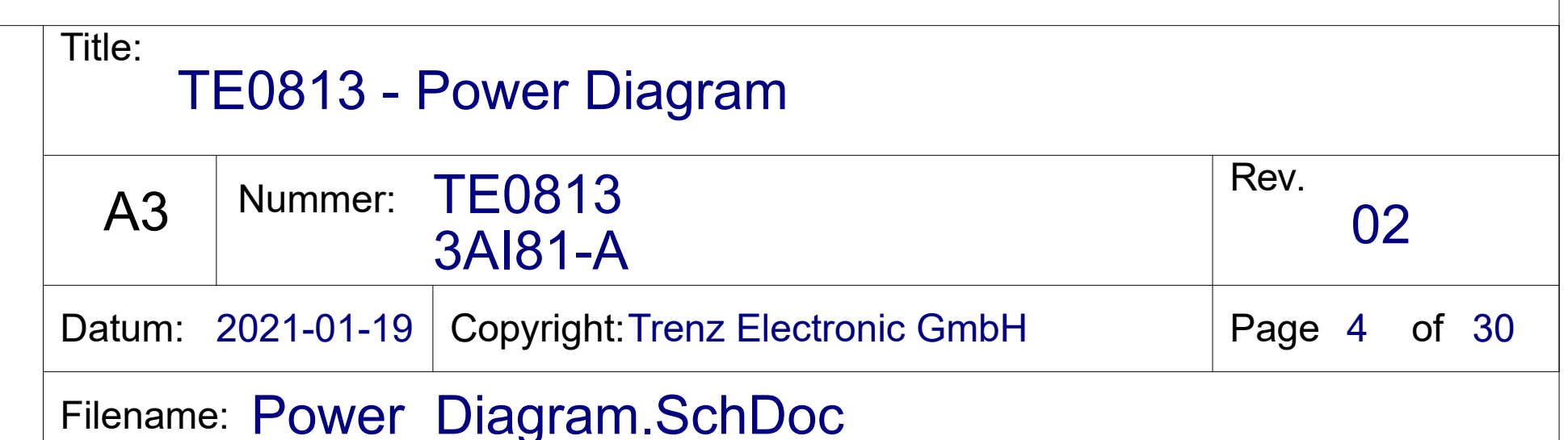
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Page 2 of 30

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B							B																		
C							C																		
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 3 of 30																							
Filename: Revision Changes.SchDoc																									
1		2		3		4																			



1

2

3

4

Special notes:

A

B

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

PM1

PM2

FIDU-DOT - mini

FIDU-DOT - mini

PM3

PM4

FIDU-DOT - mini

FIDU-DOT - mini

PM5

PM6

FIDU-DOT - mini

FIDU-DOT - mini

UKCA1

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE1

CE Logo on Top Overlay

CE-TOPOVERLAY

MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial

Serial

Serialnumber 6,3 x 6.3mm

trenz

electronic

Title: TE0813

A4

Number: TE0813
3AI81-A

Rev. 02

Date: 06.01.2026

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Filename: TE0813.SchDoc

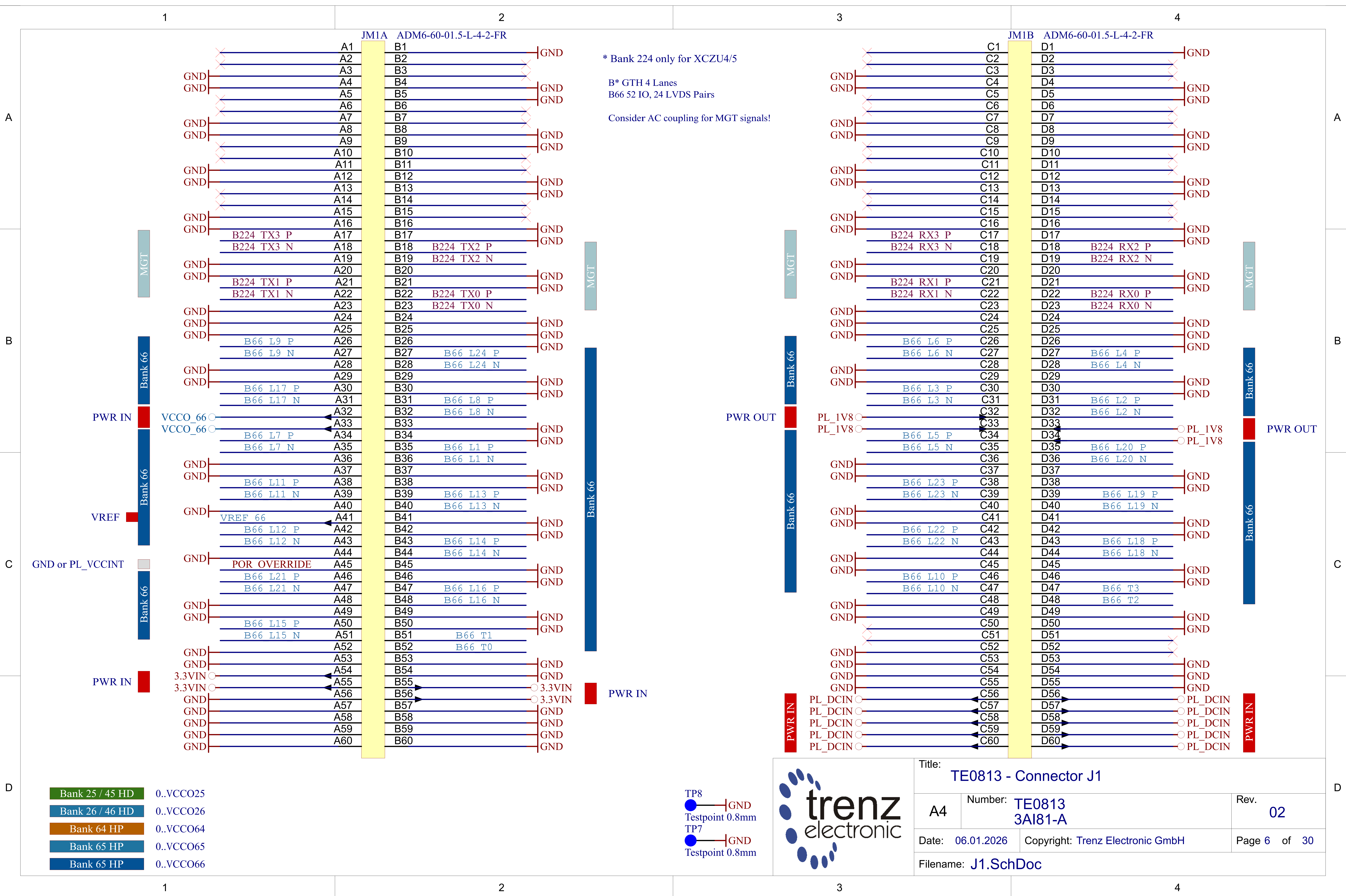
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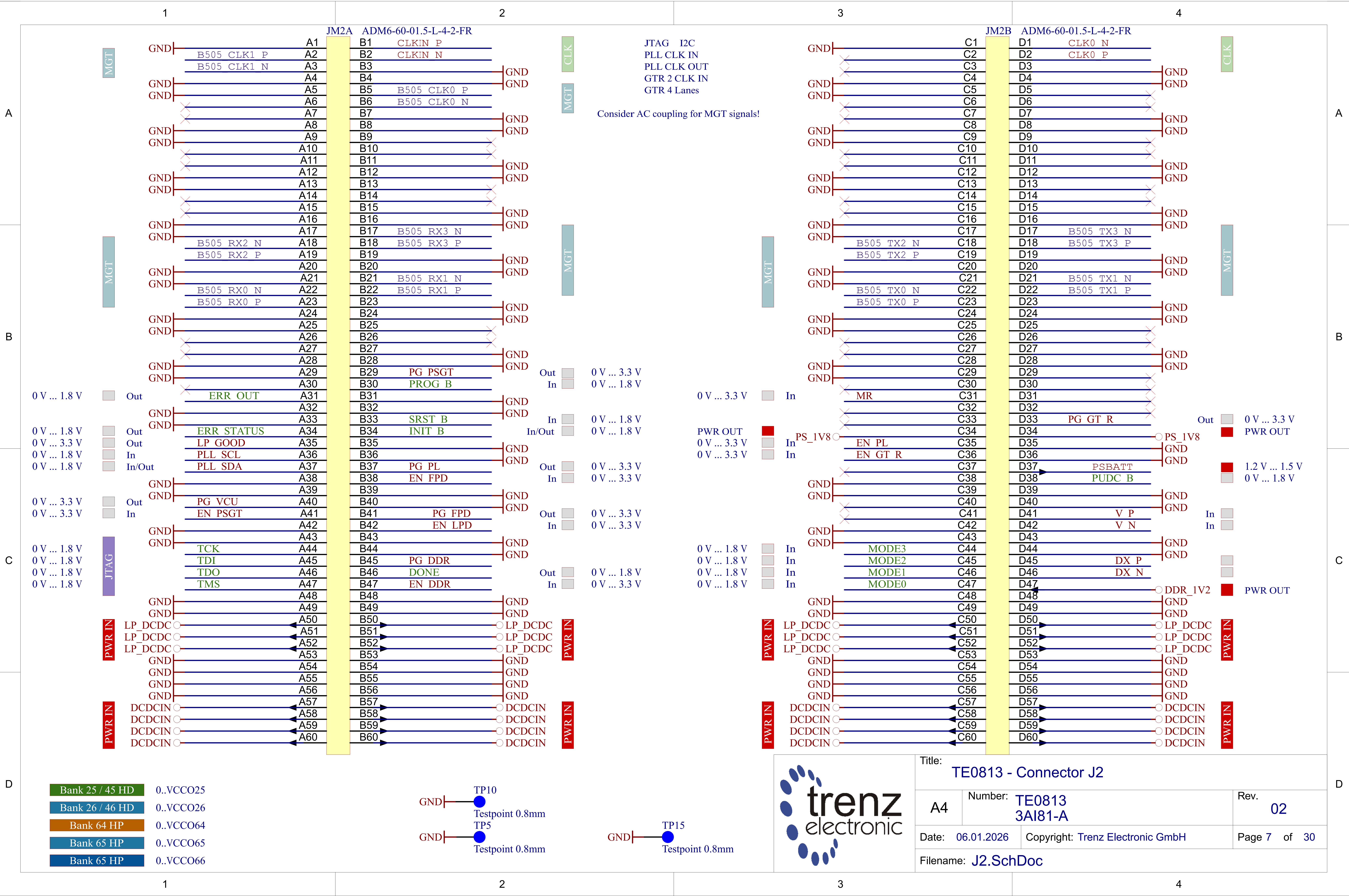
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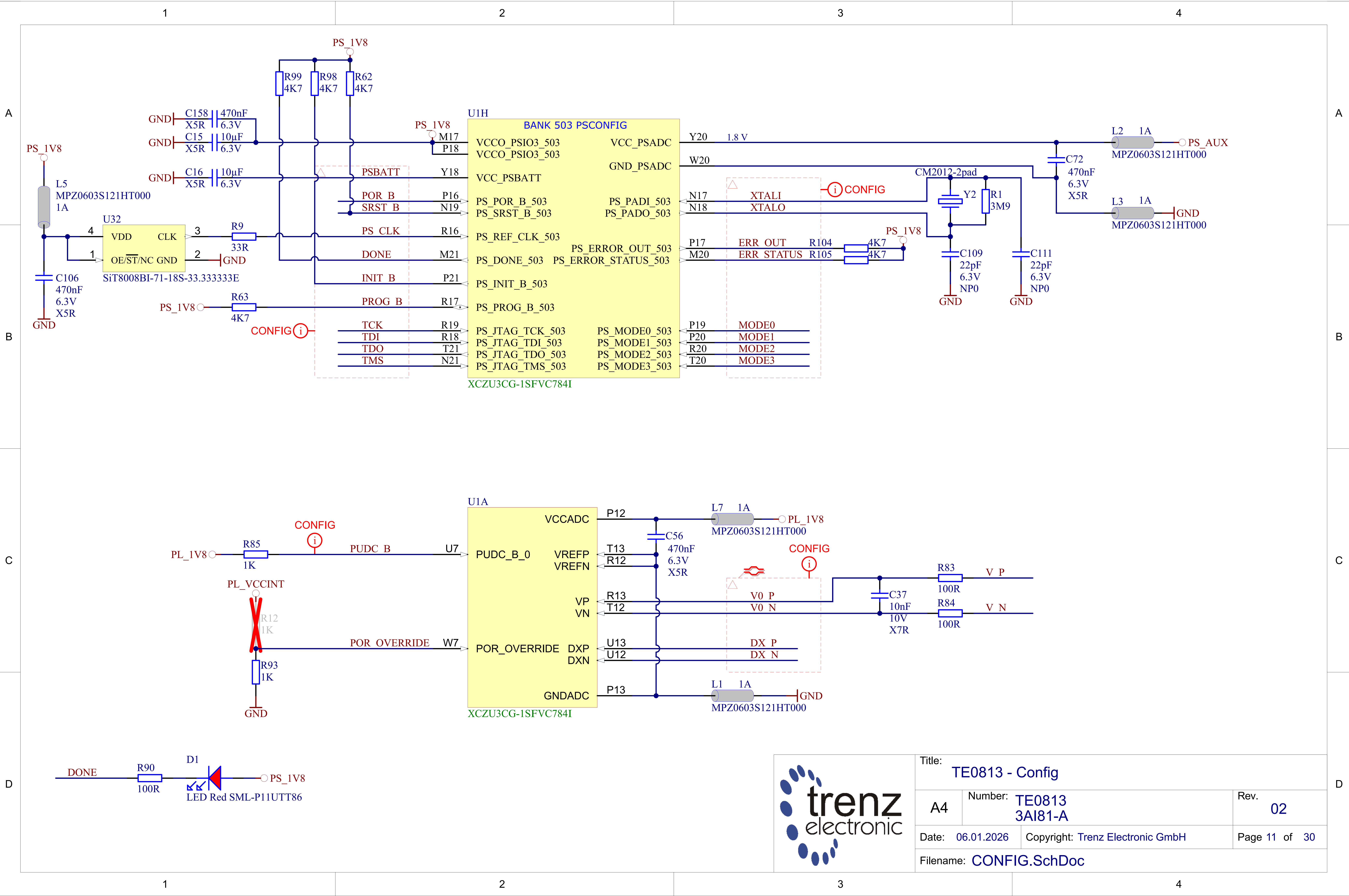
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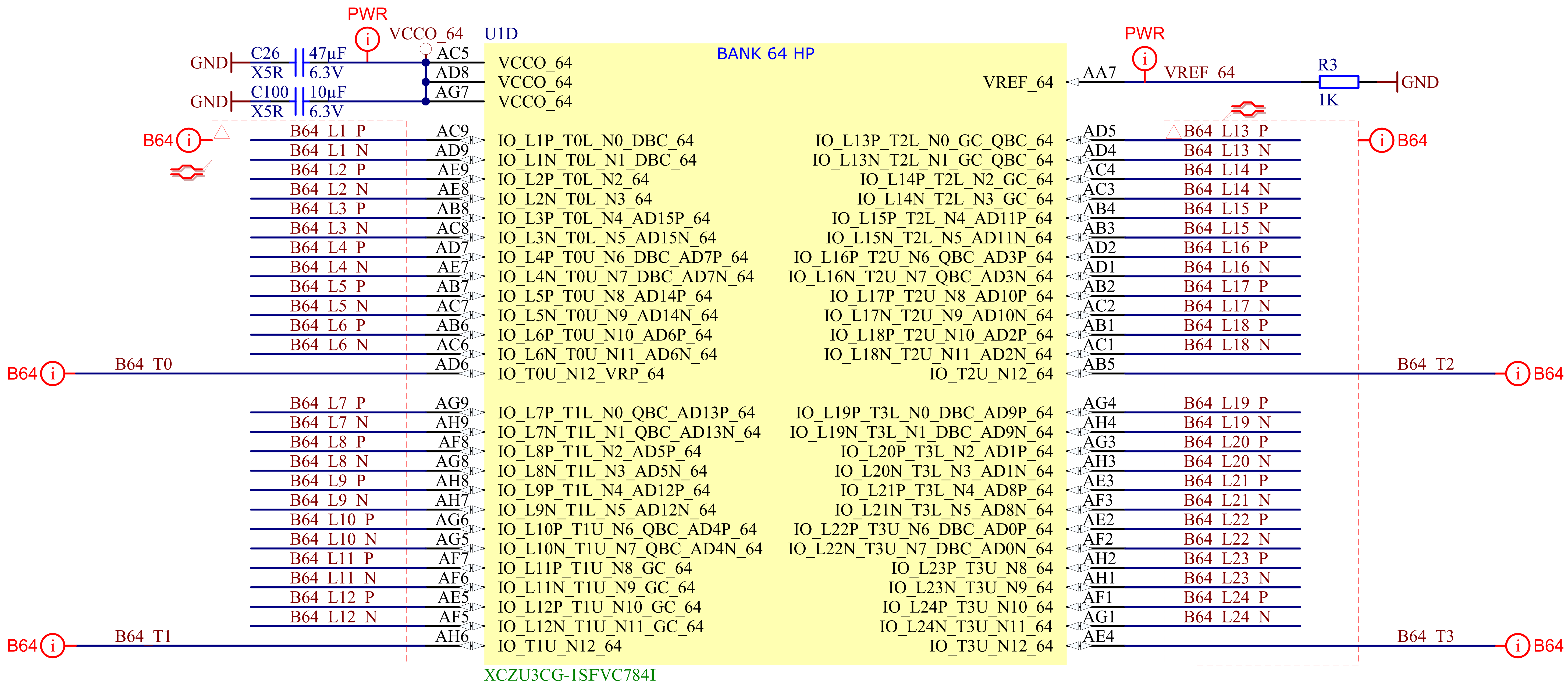




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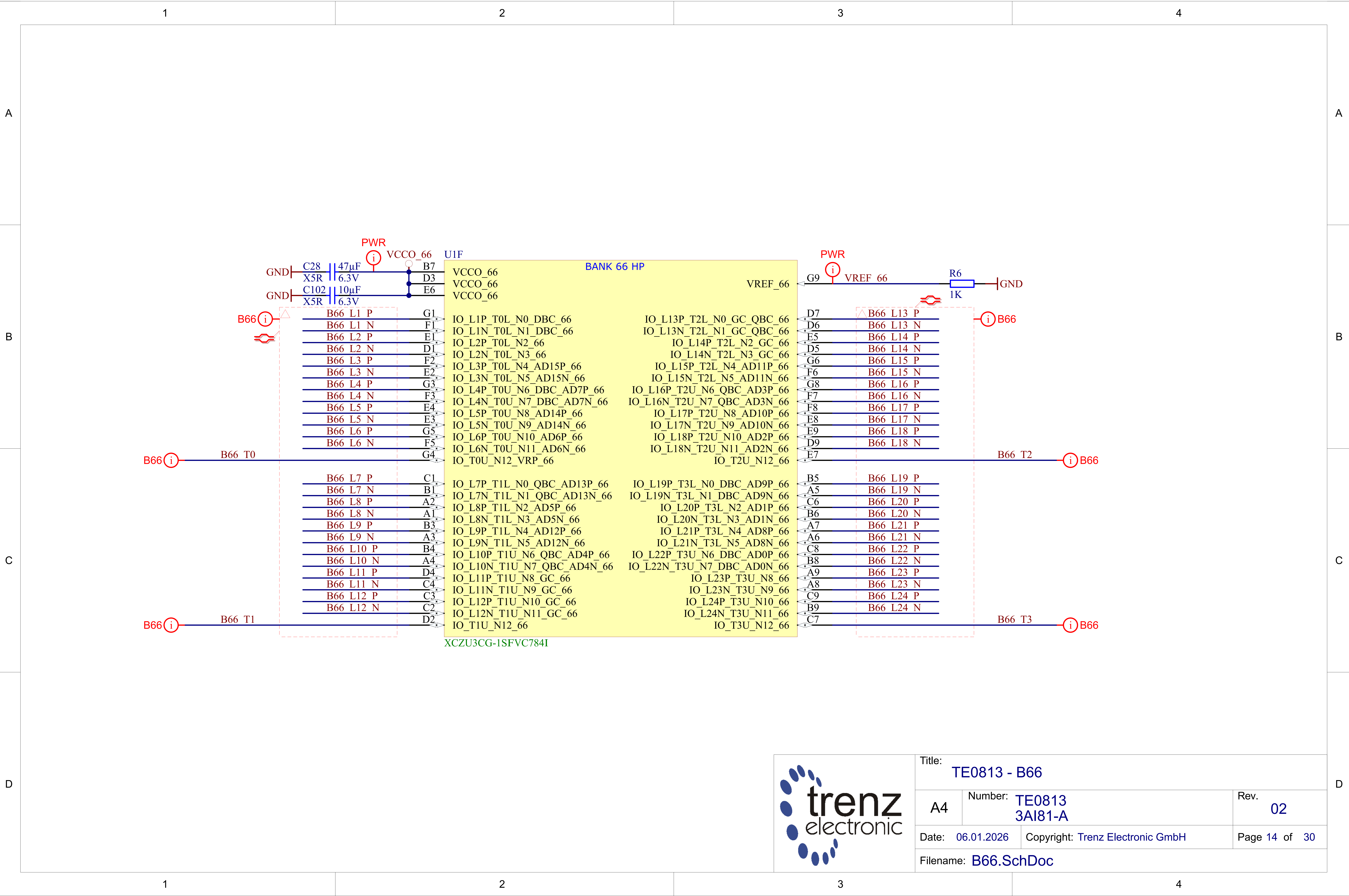


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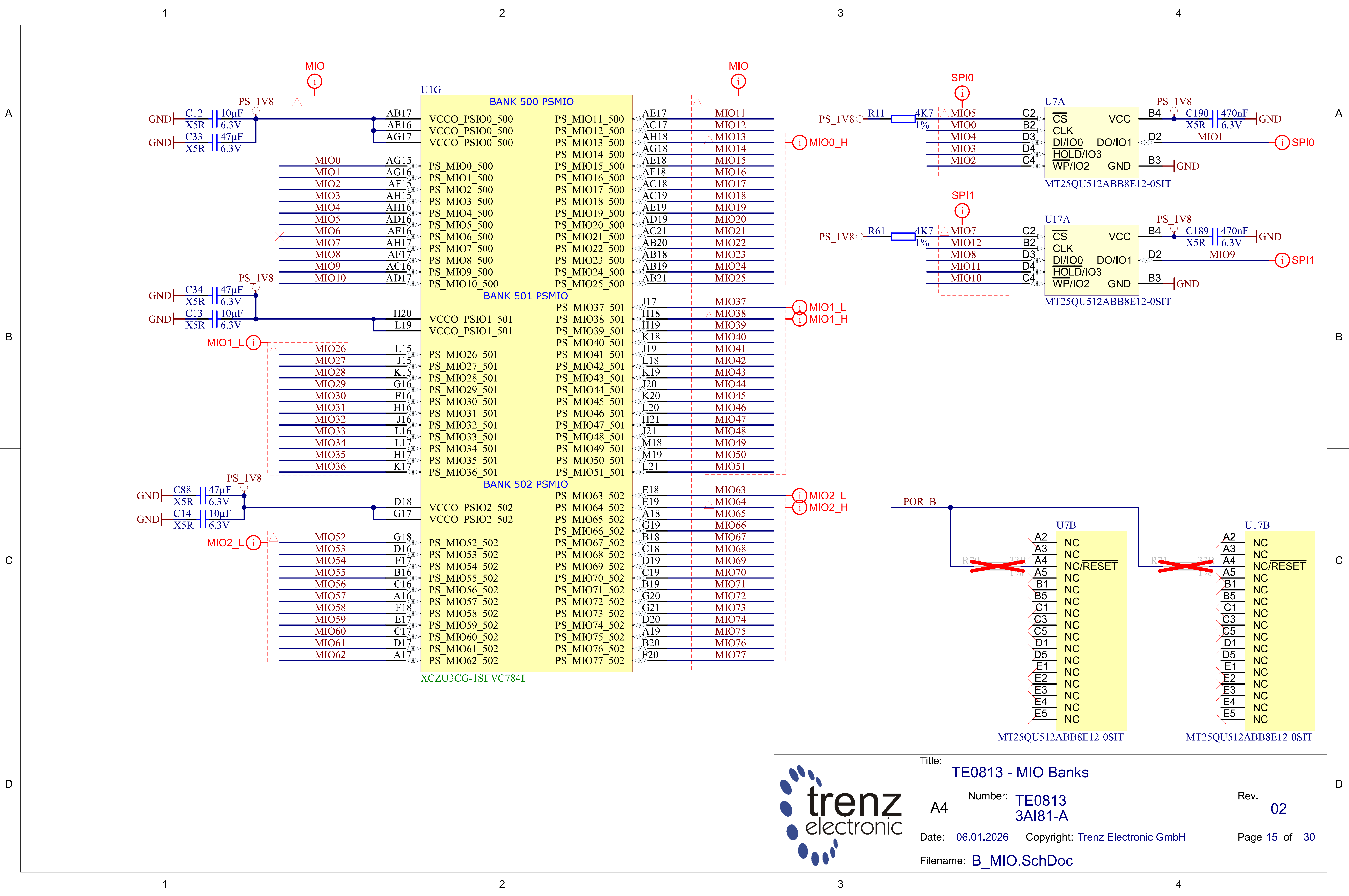
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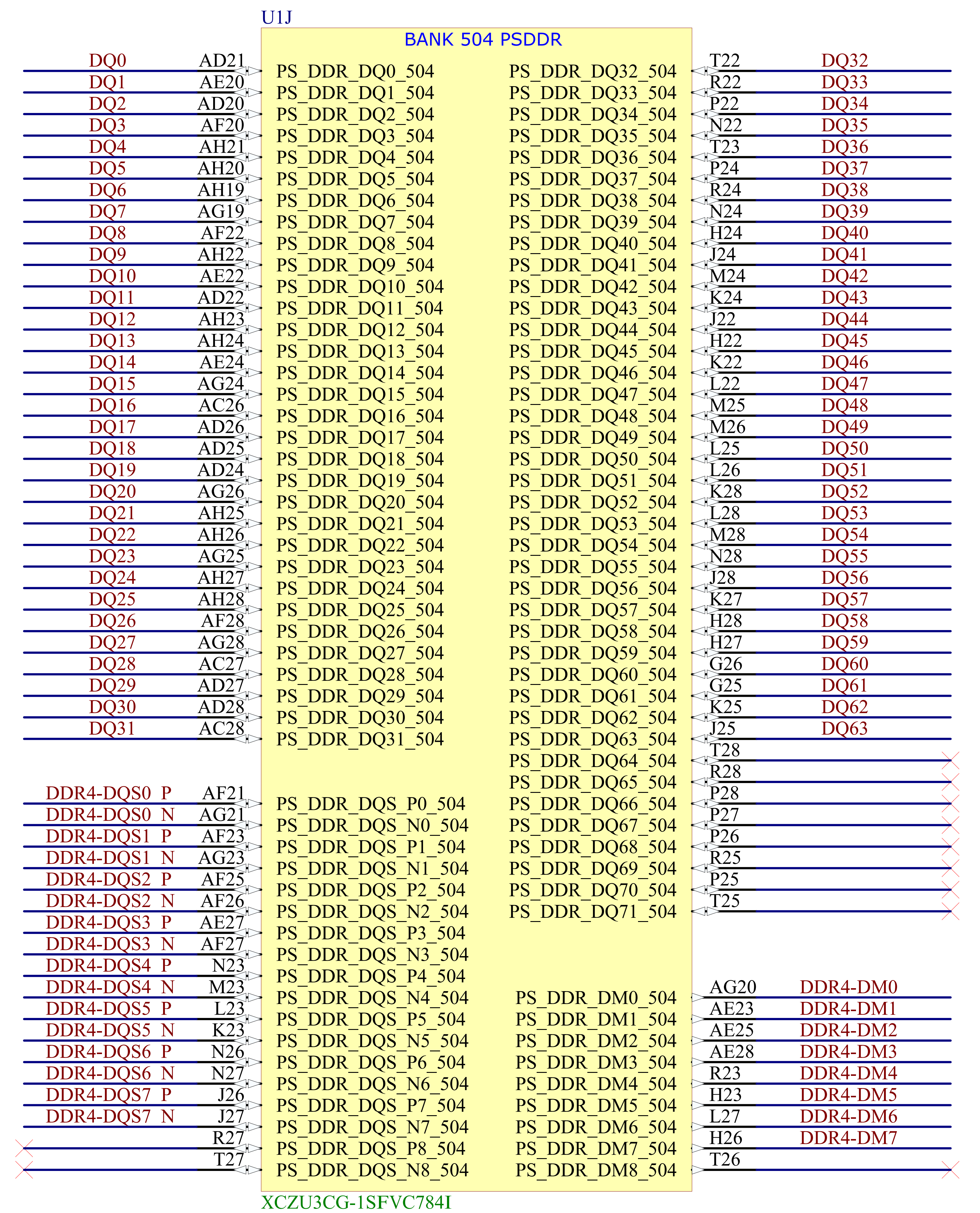
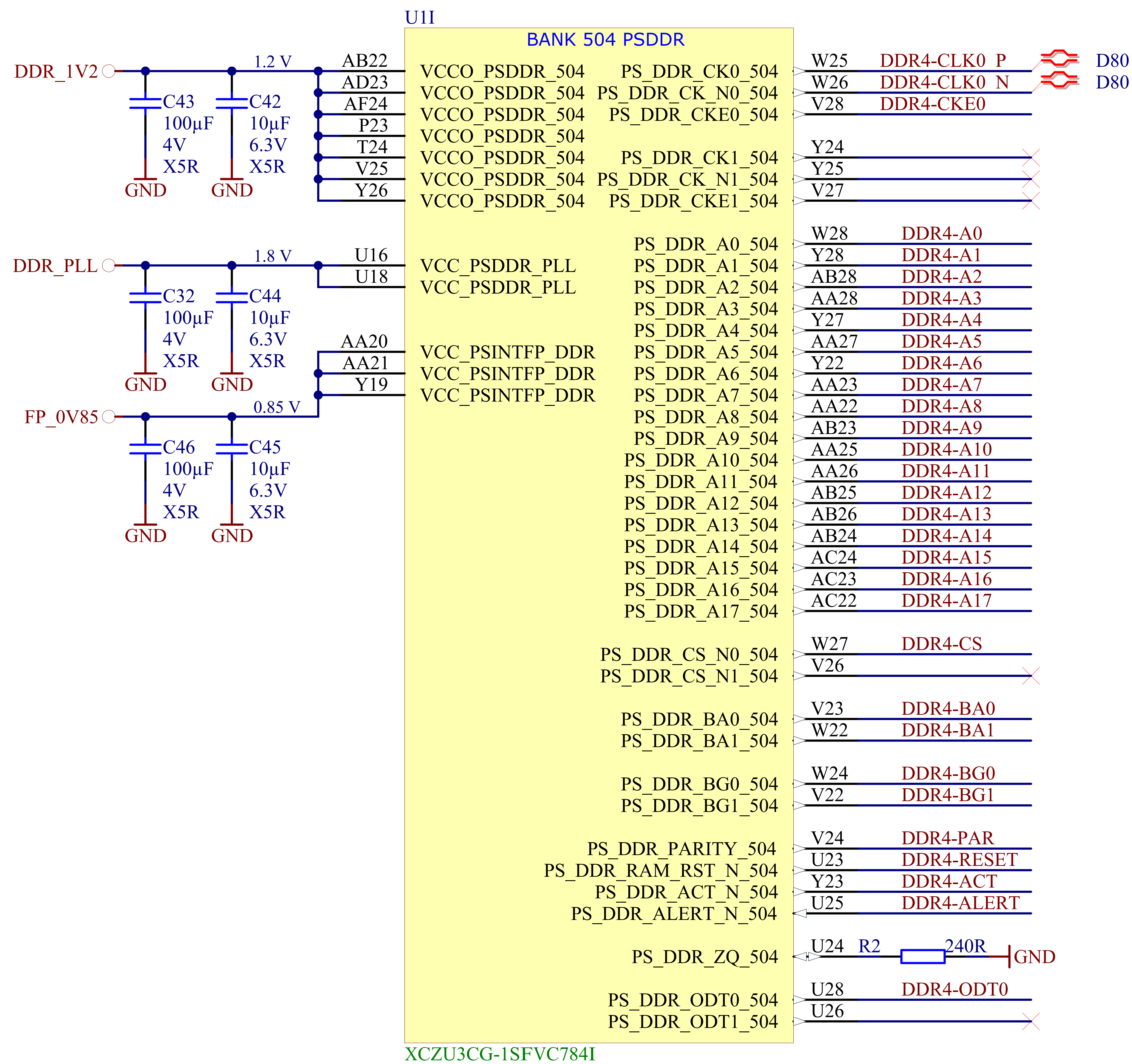


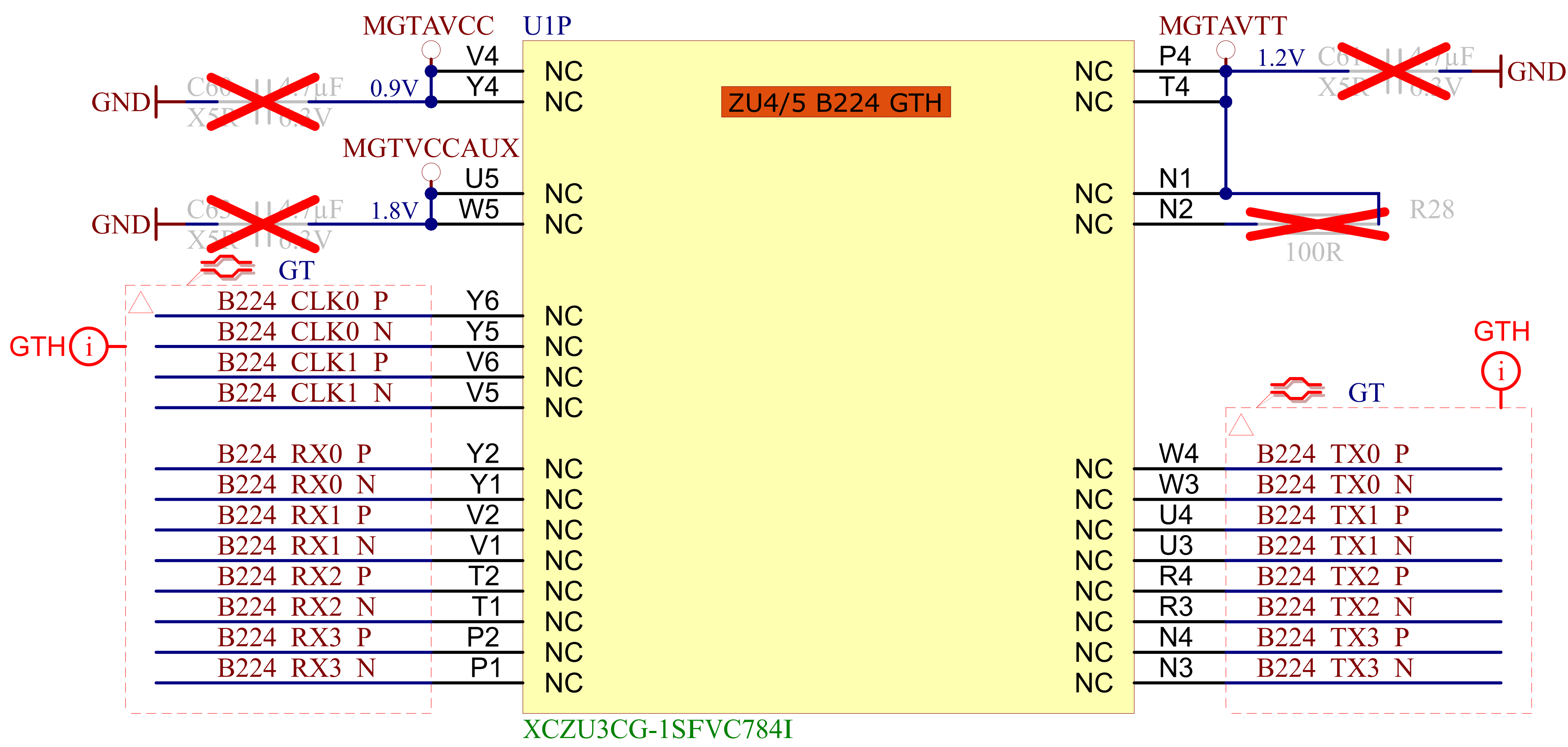
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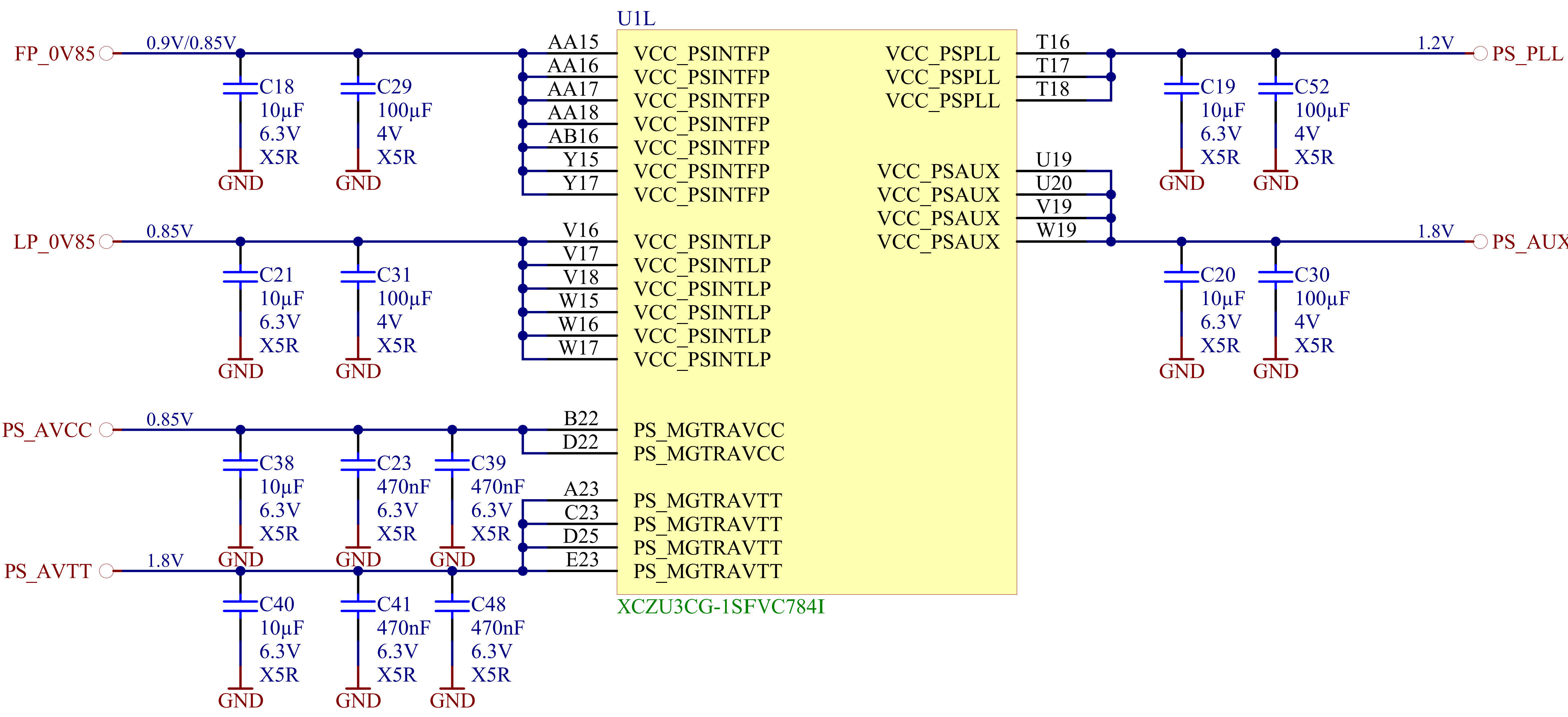
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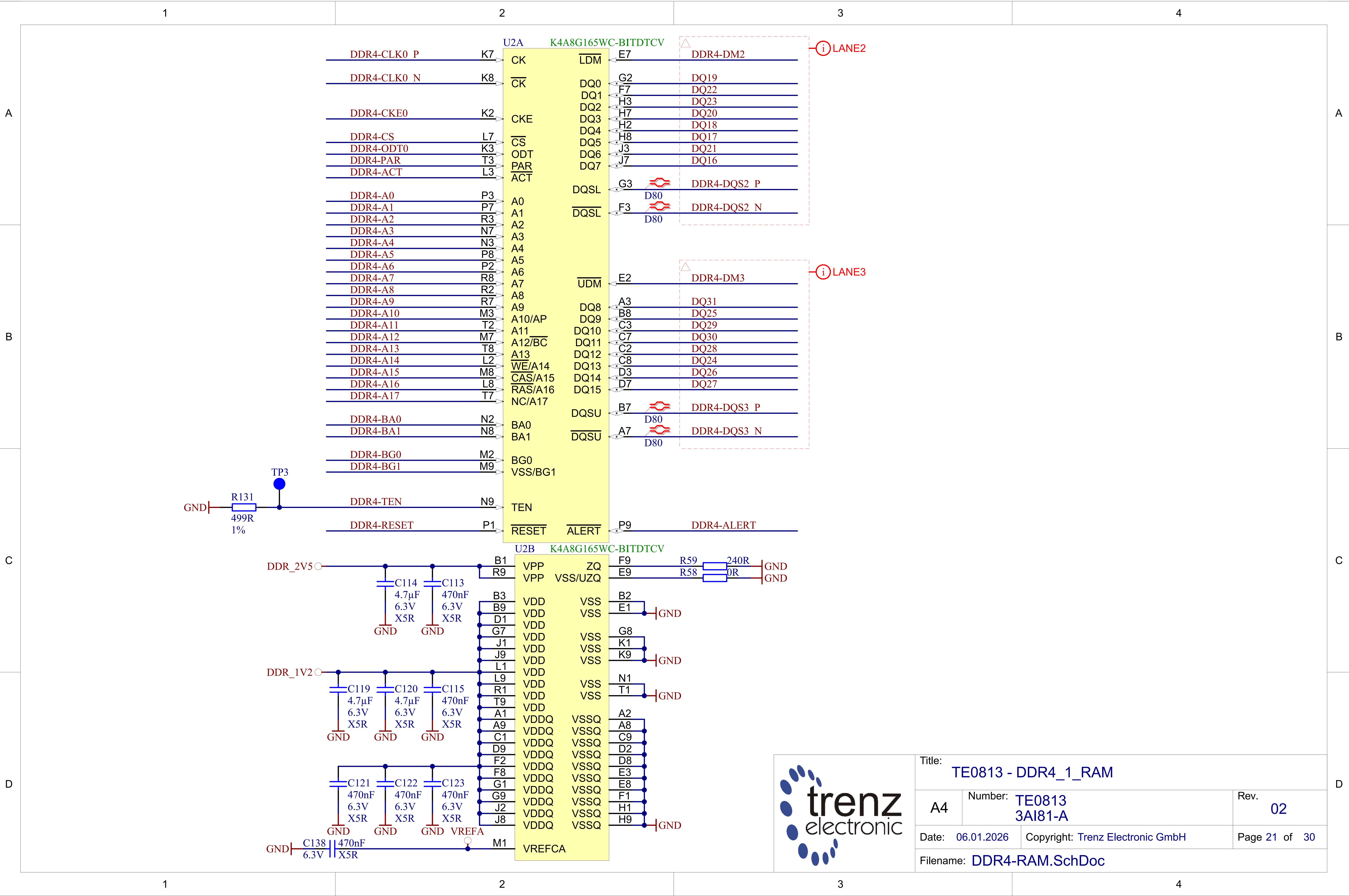


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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 19 of 30
Filename: ZU_PS_POWER.SchDoc		

D



A

B

C

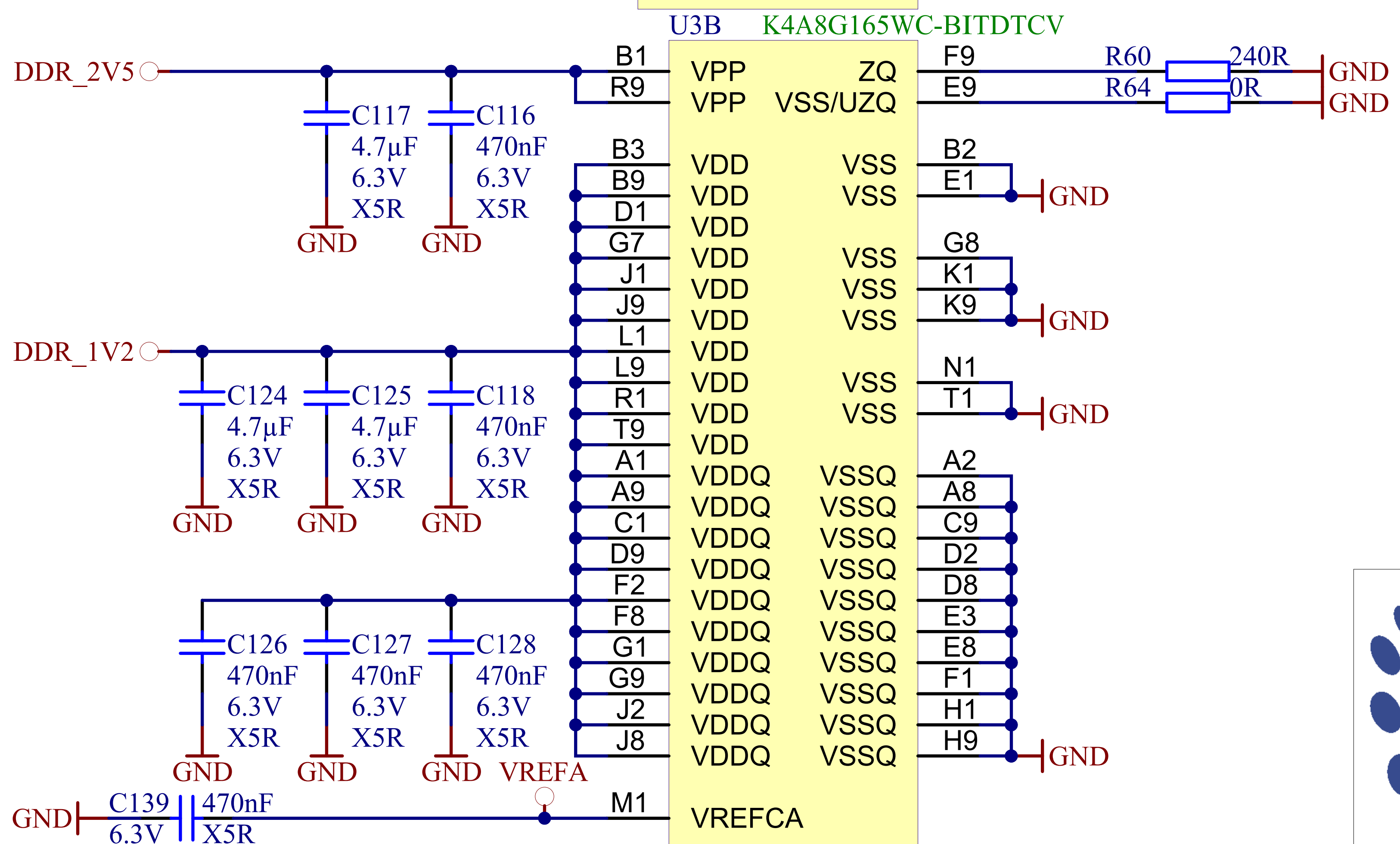
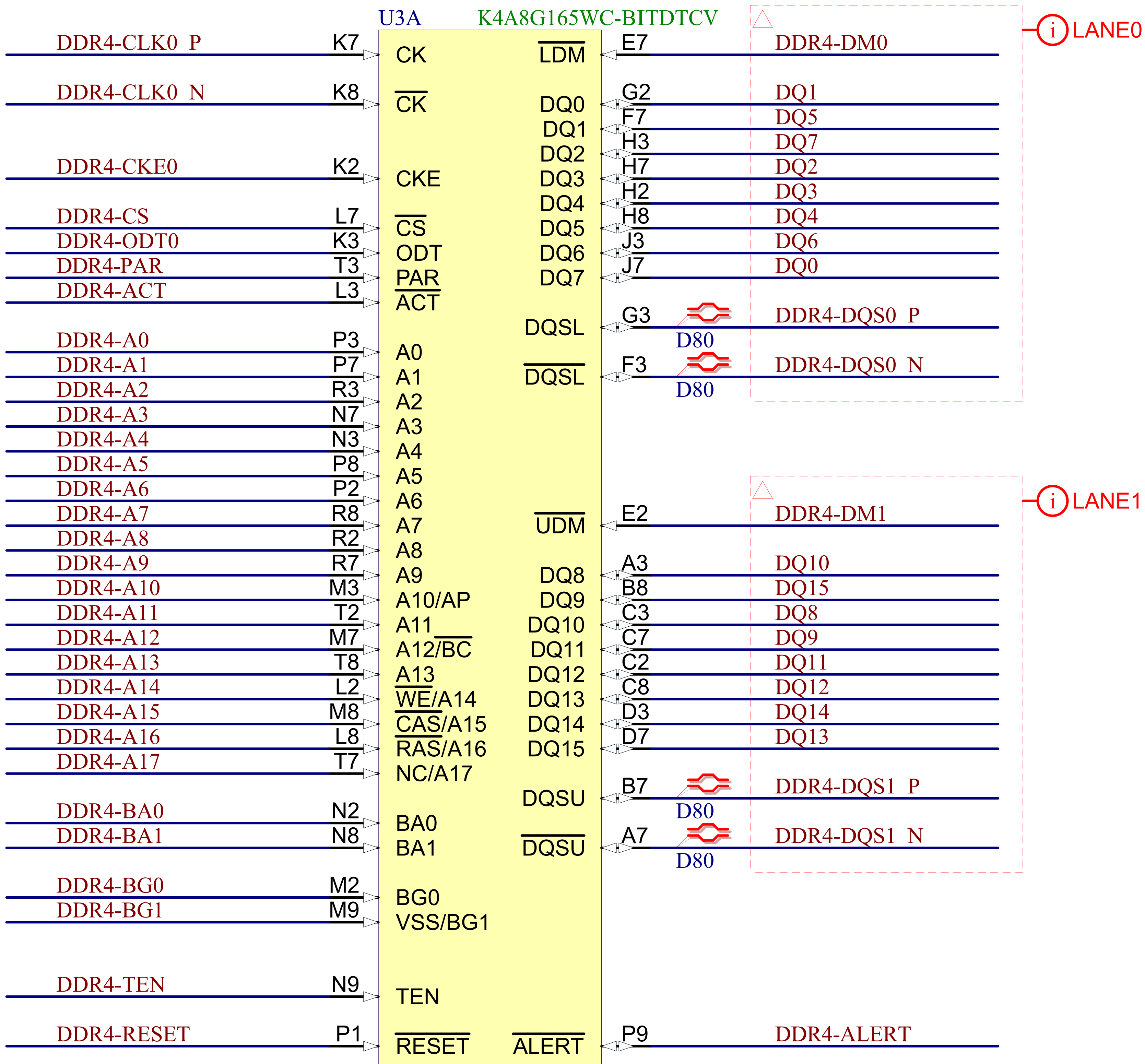
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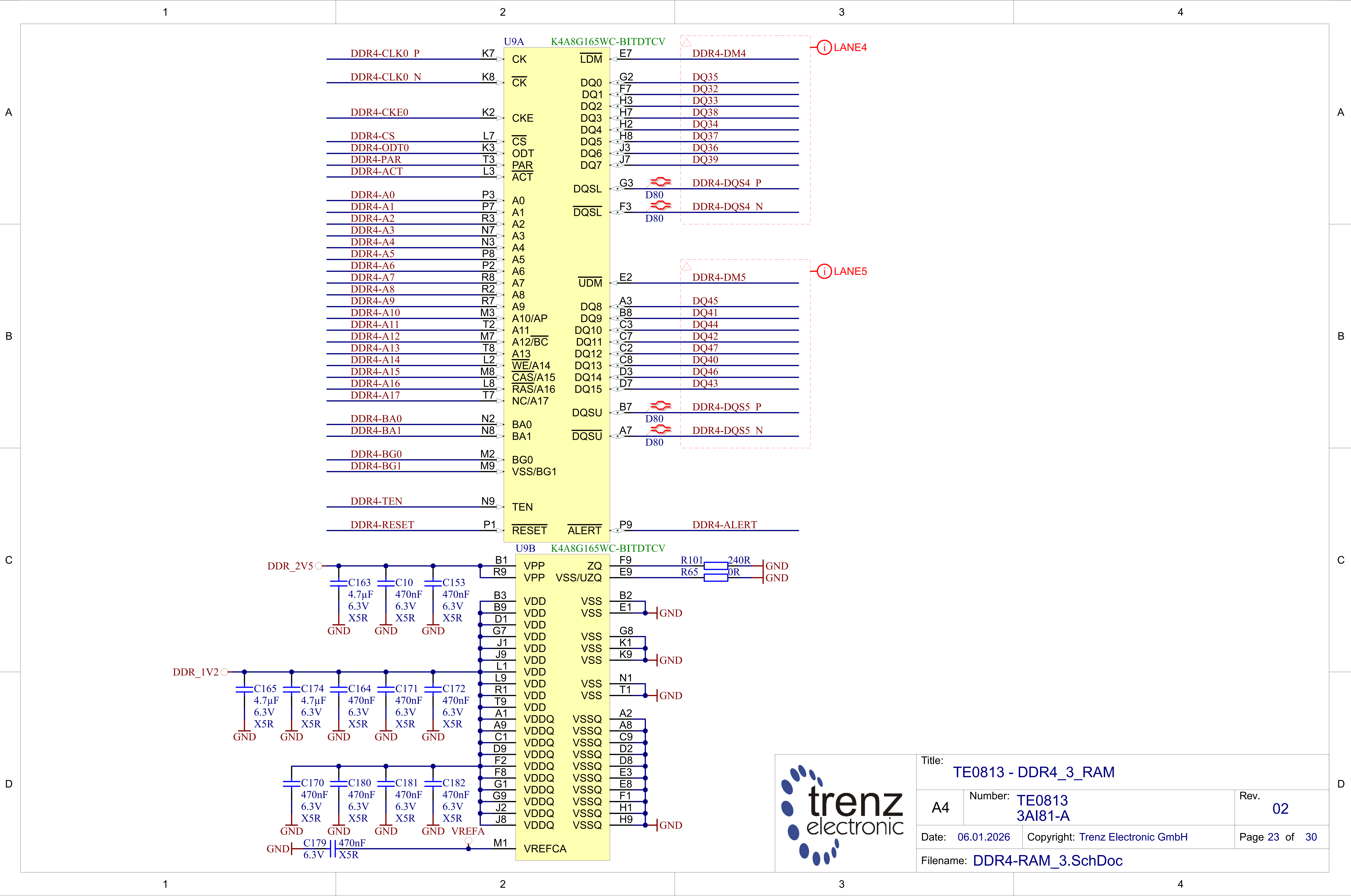
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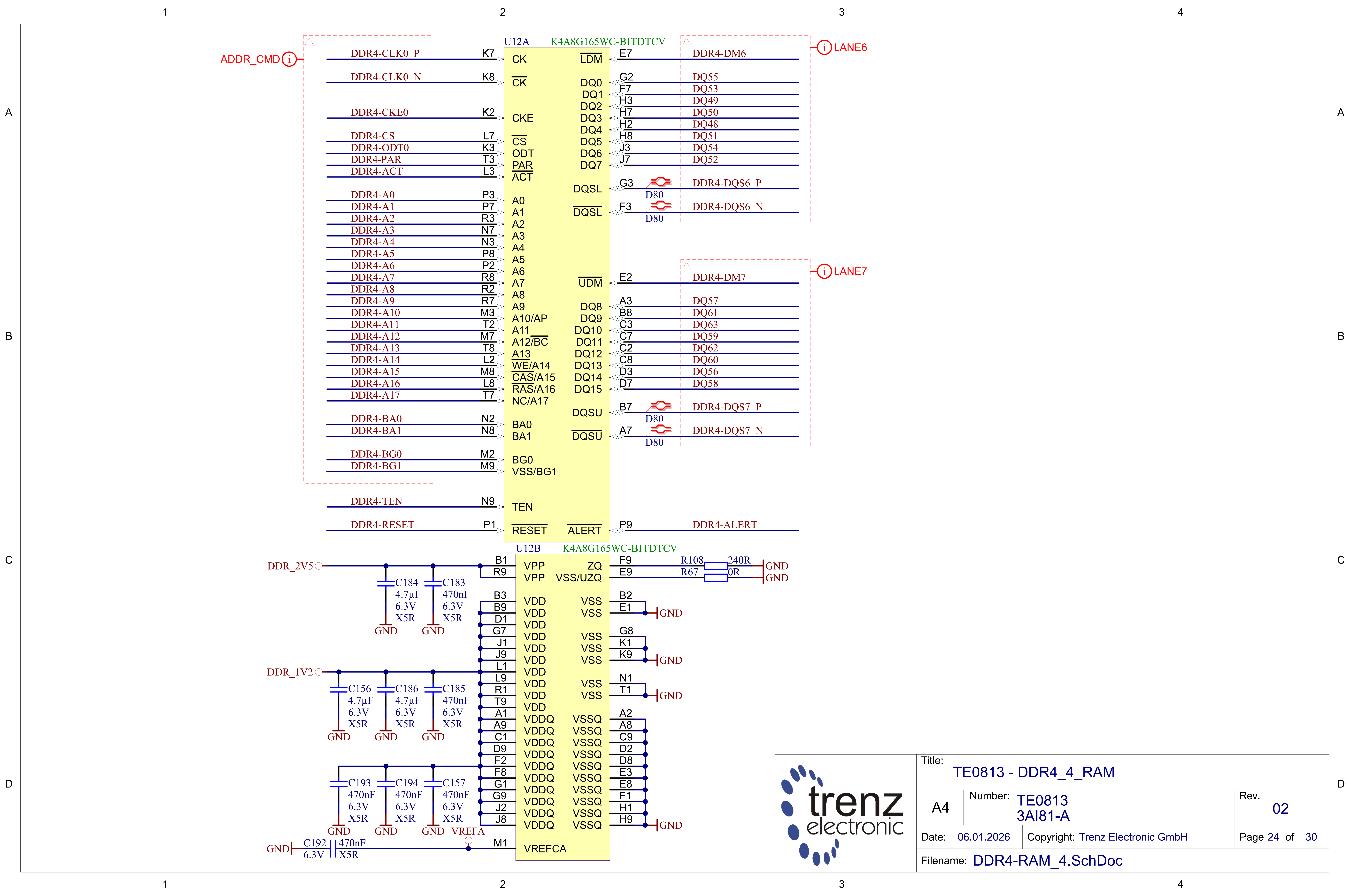
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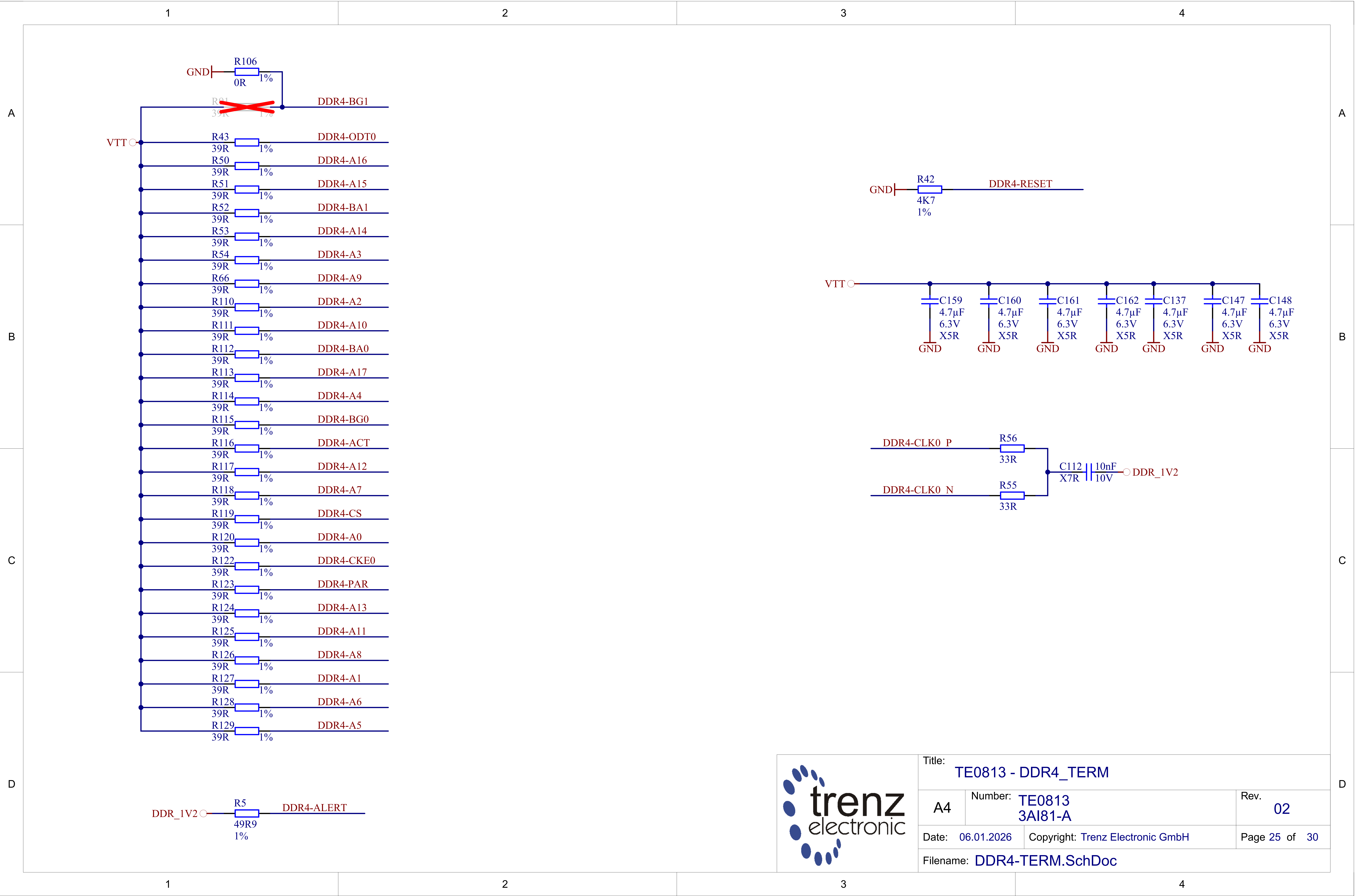
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 22 of 30
Filename: DDR4-RAM_2.SchDoc		



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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 23 of 30
Filename: DDR4-RAM_3.SchDoc		



Title: TE0813 - DDR4_4_RAM		
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 24 of 30
Filename: DDR4-RAM_4.SchDoc		



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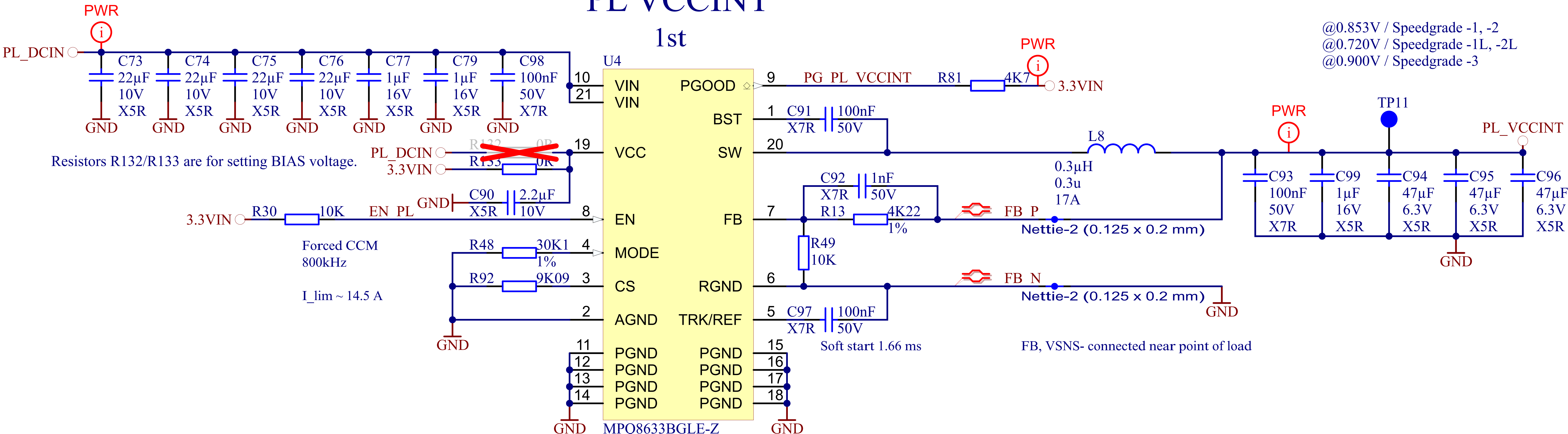
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH	Page 25 of 30

Filename: DDR4-TERM.SchDoc

U4 can be TPS548A28RWW or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

PL VCCINT

1st



FPGA Speedgrade	R13	R49	PL_VCCINT
-1LI	2 kOhm	10 kOhm	0.720 V
-2LE	2 kOhm	10 kOhm	0.720 V
-1	4.22 kOhm	10 kOhm	0.853 V
-2	4.22 kOhm	10 kOhm	0.853 V
-3E	10 kOhm	20 kOhm	0.900 V

U4 pin compatible with

- TPS548B28 (20A)
- TPS548A28 (15A)
- TPS54JA20 (12A)



Title: TE0813 - POWER_1

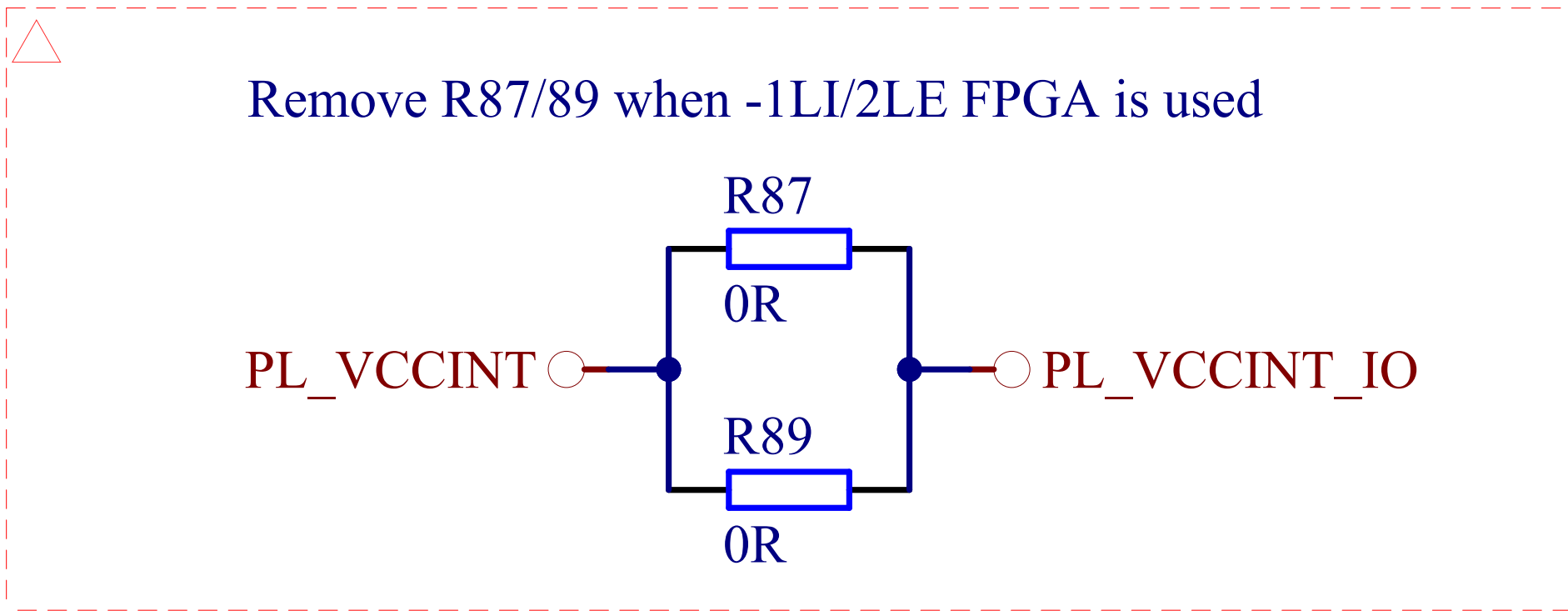
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Rev. 02

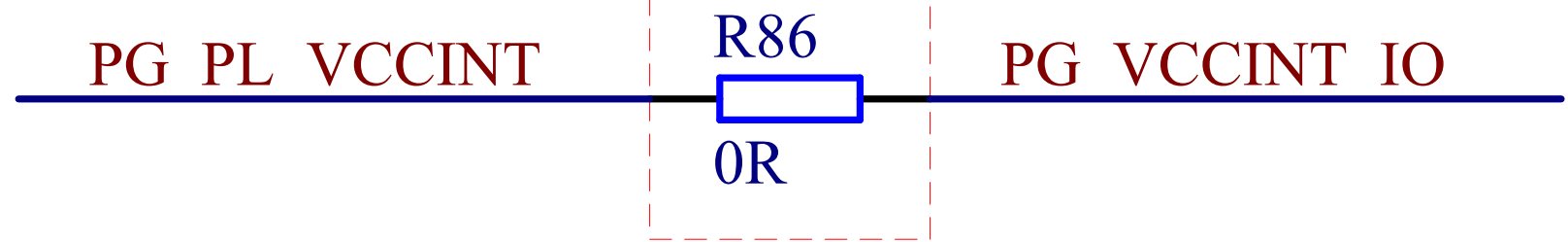
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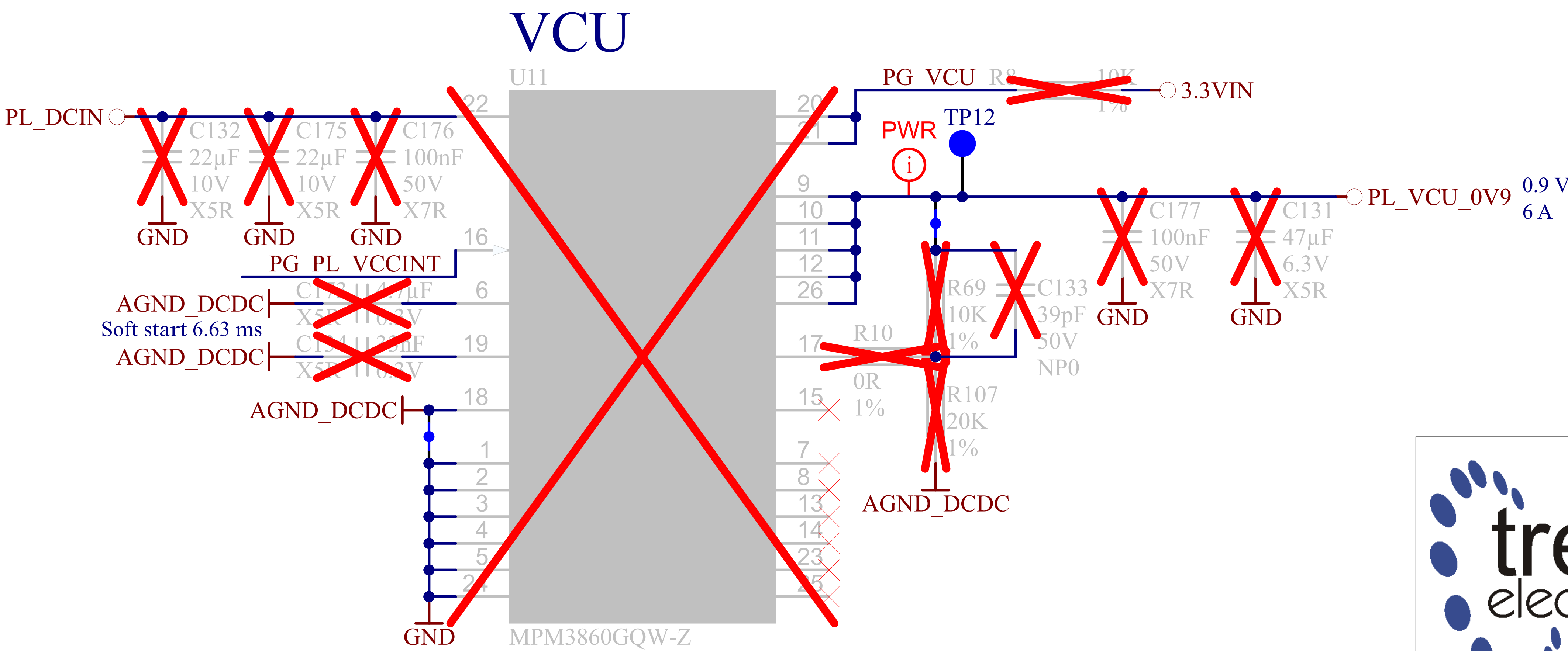
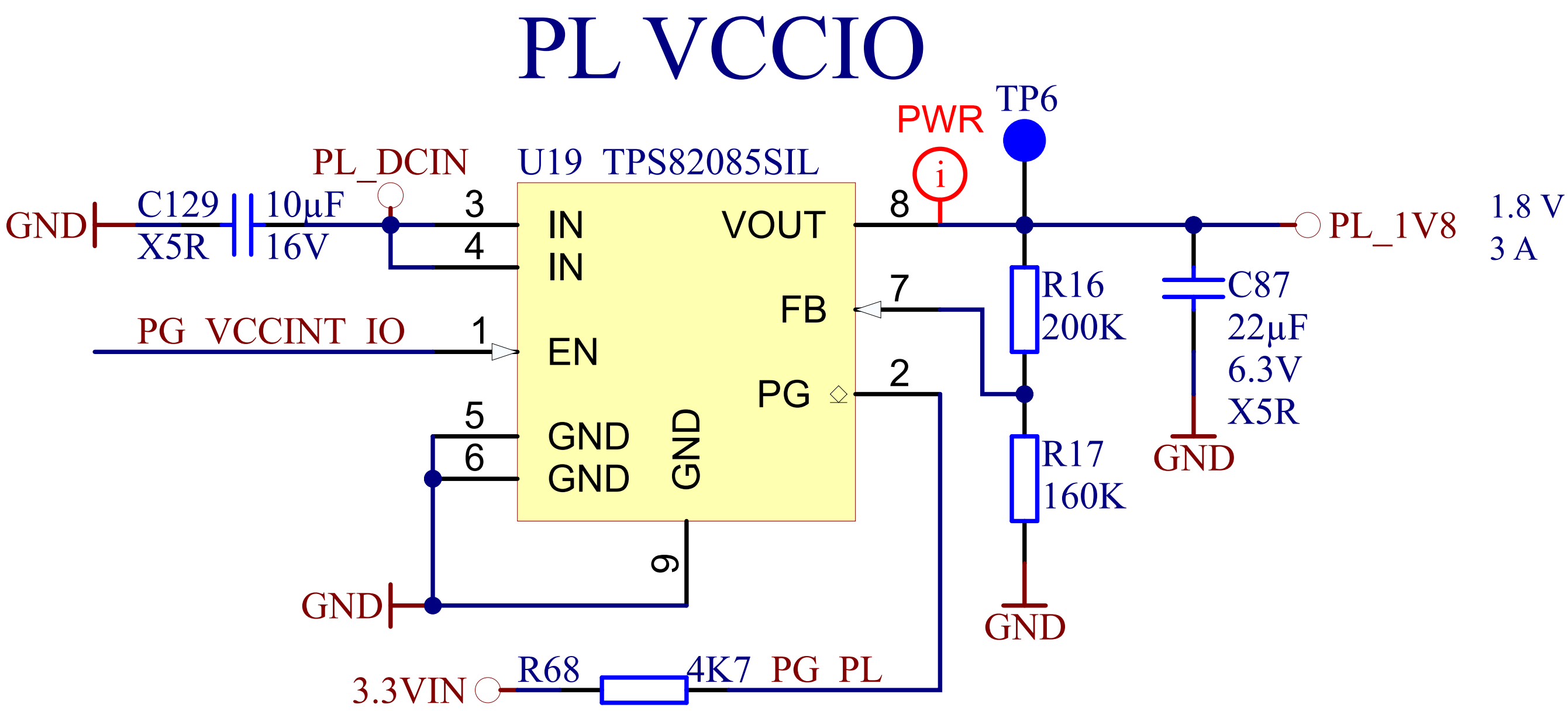
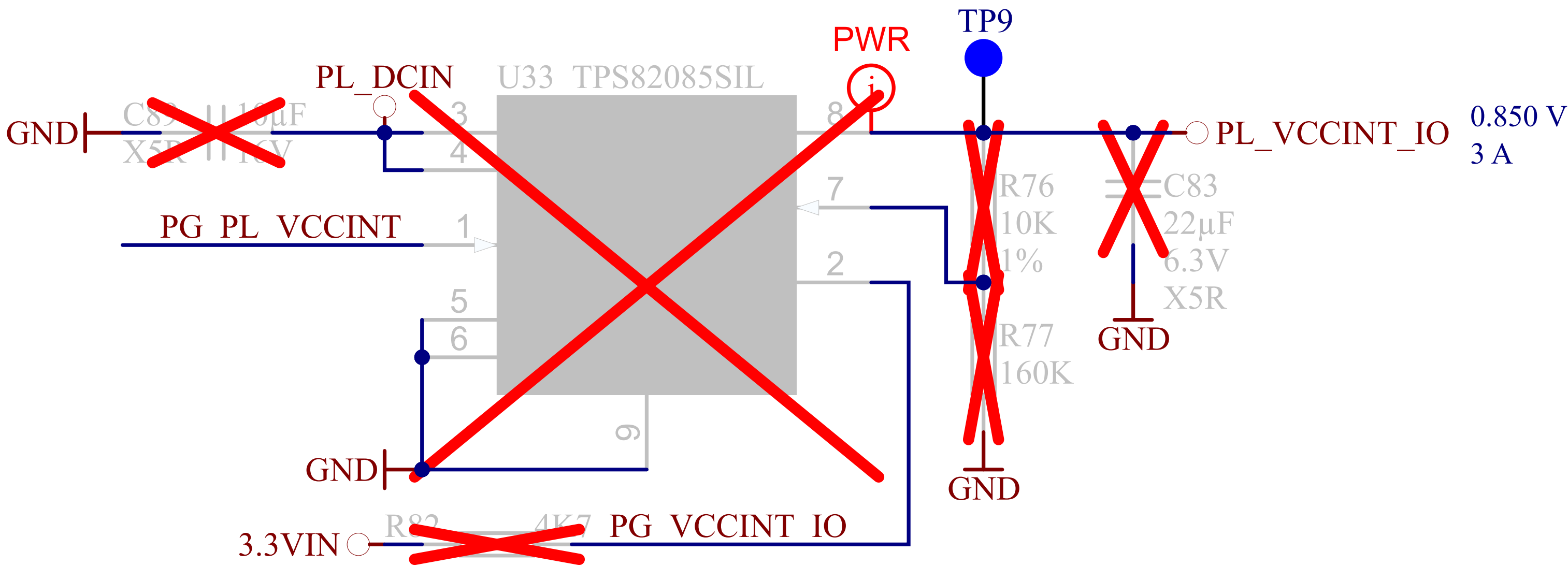


Remove R86 when -1LI/2LE FPGA is used

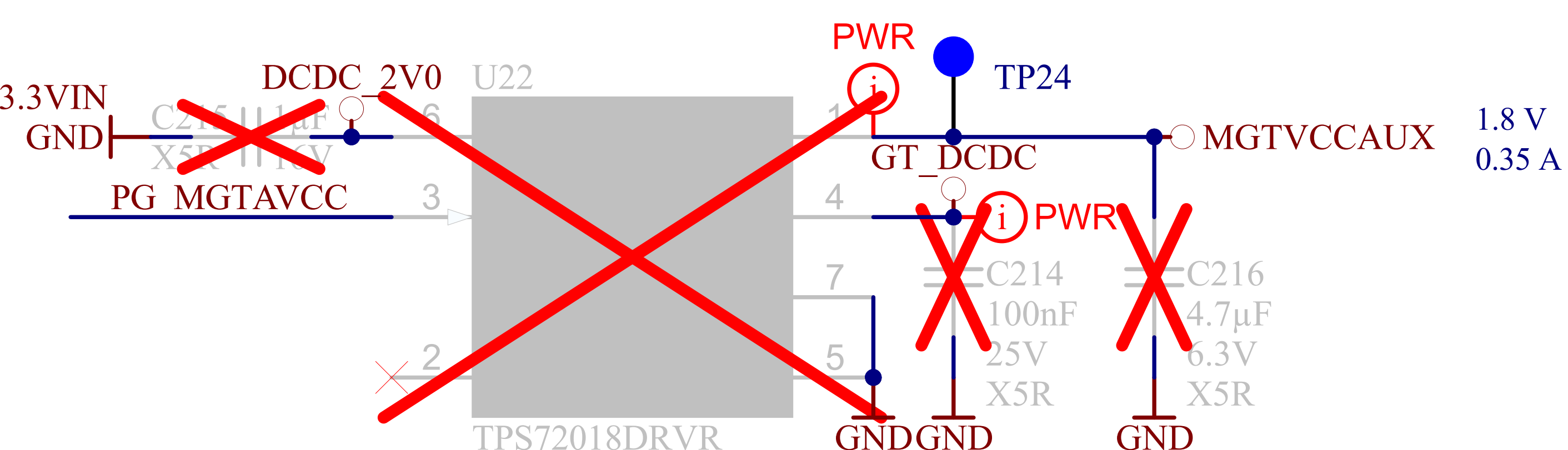
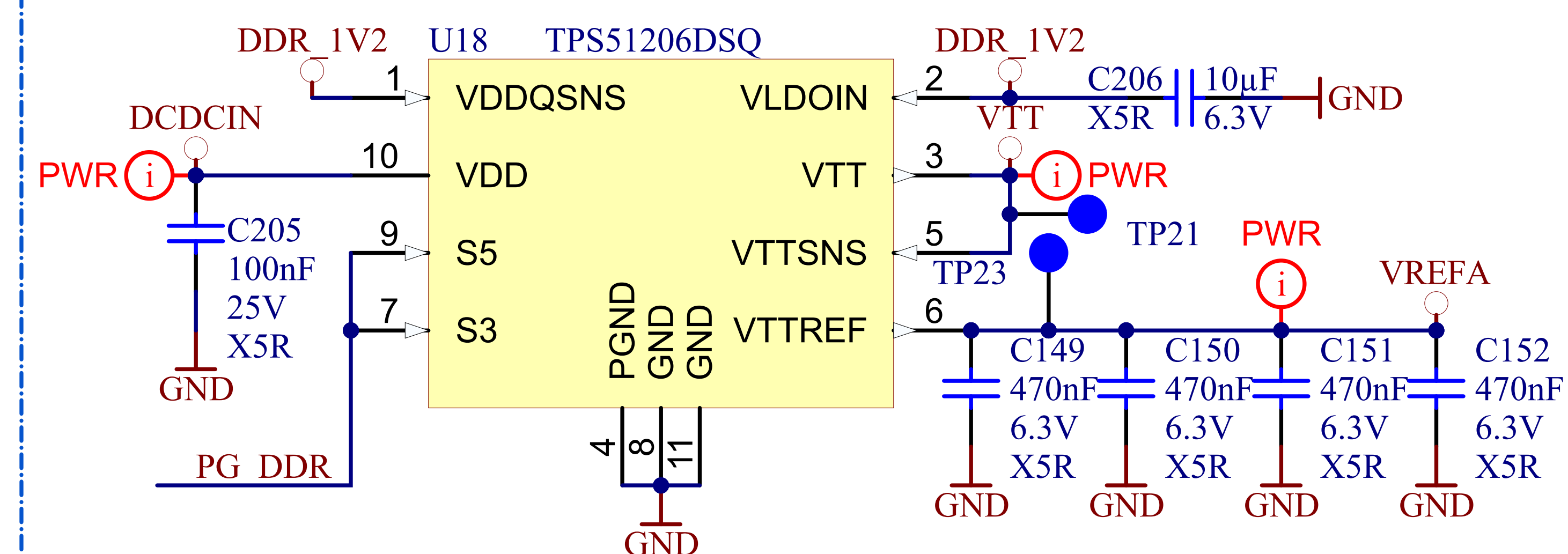
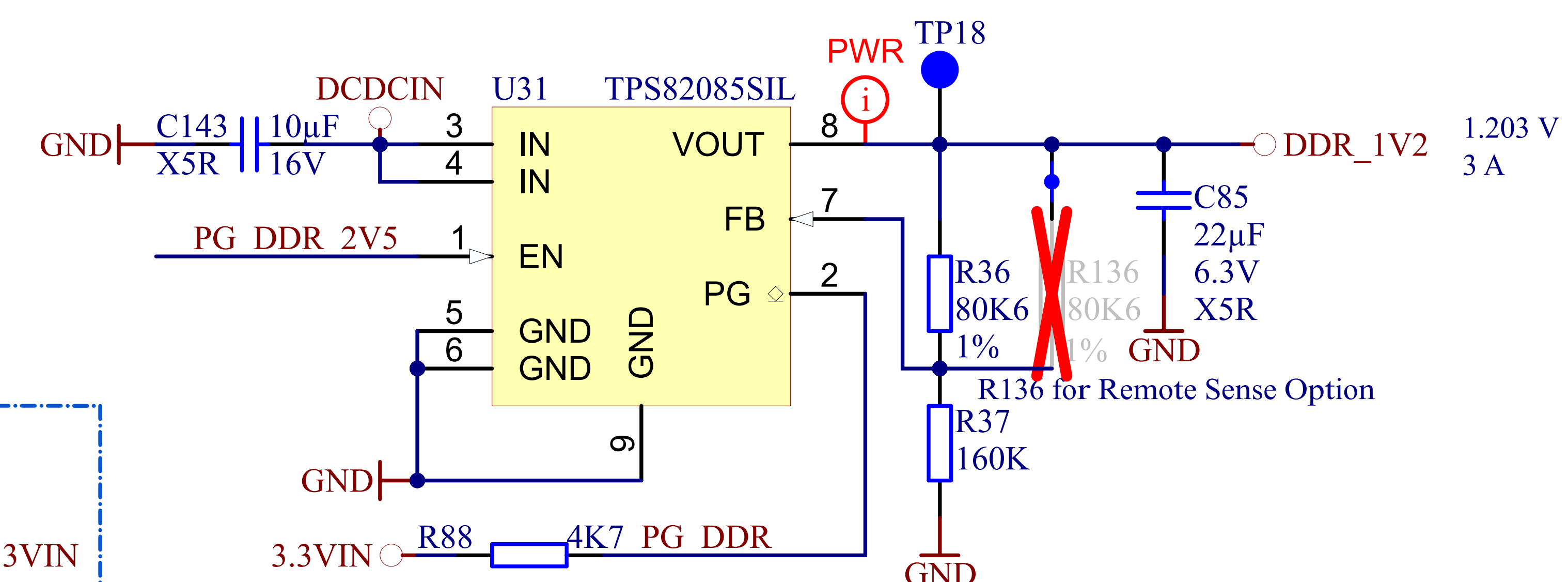
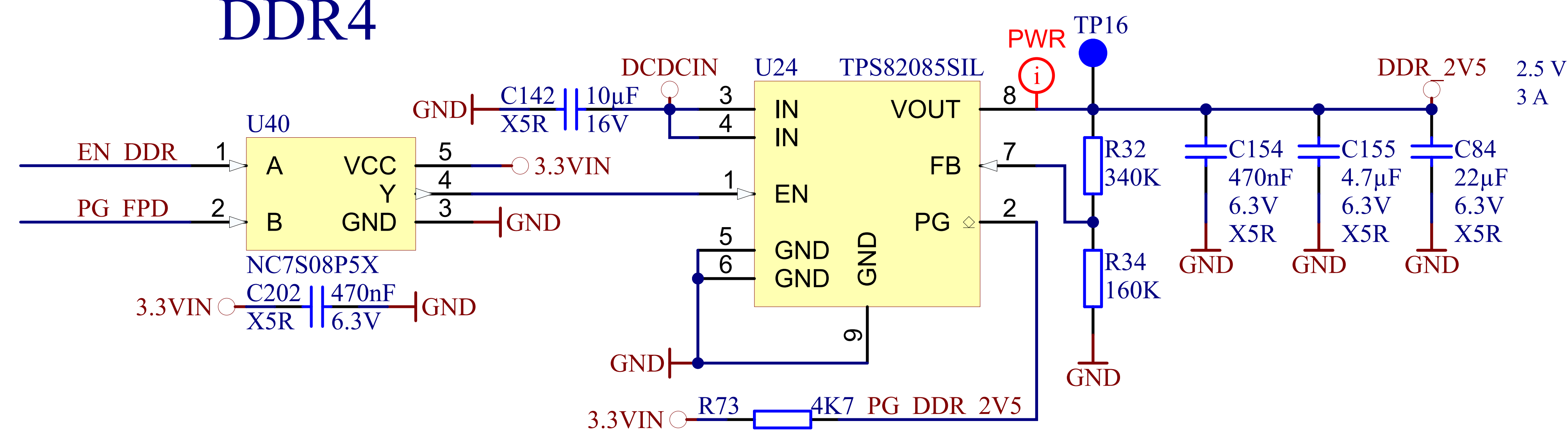
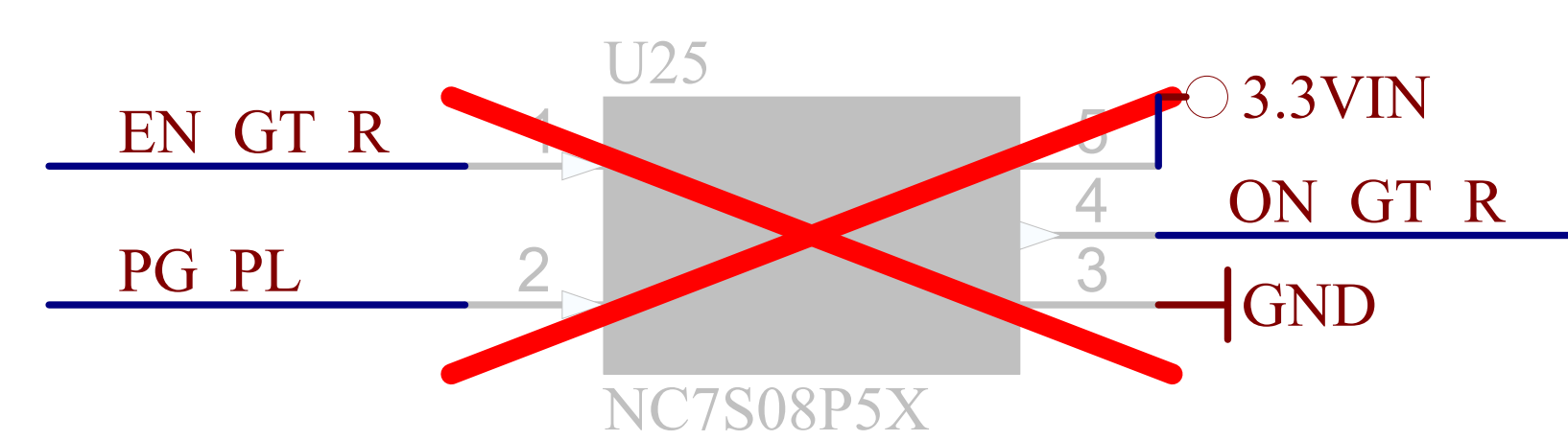
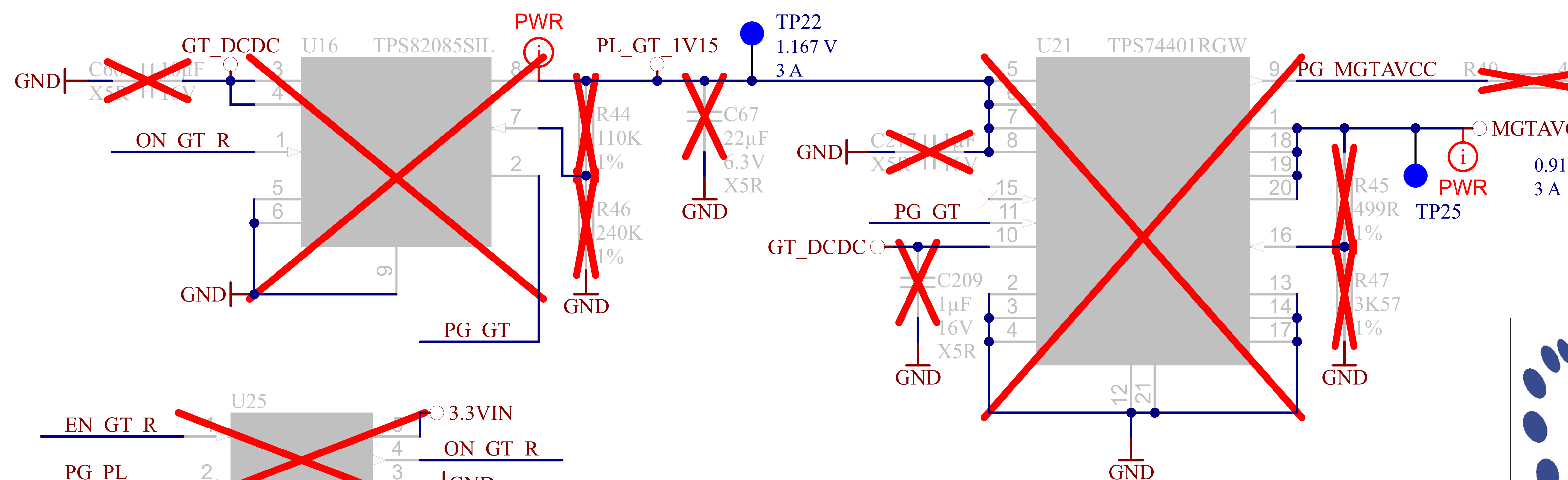
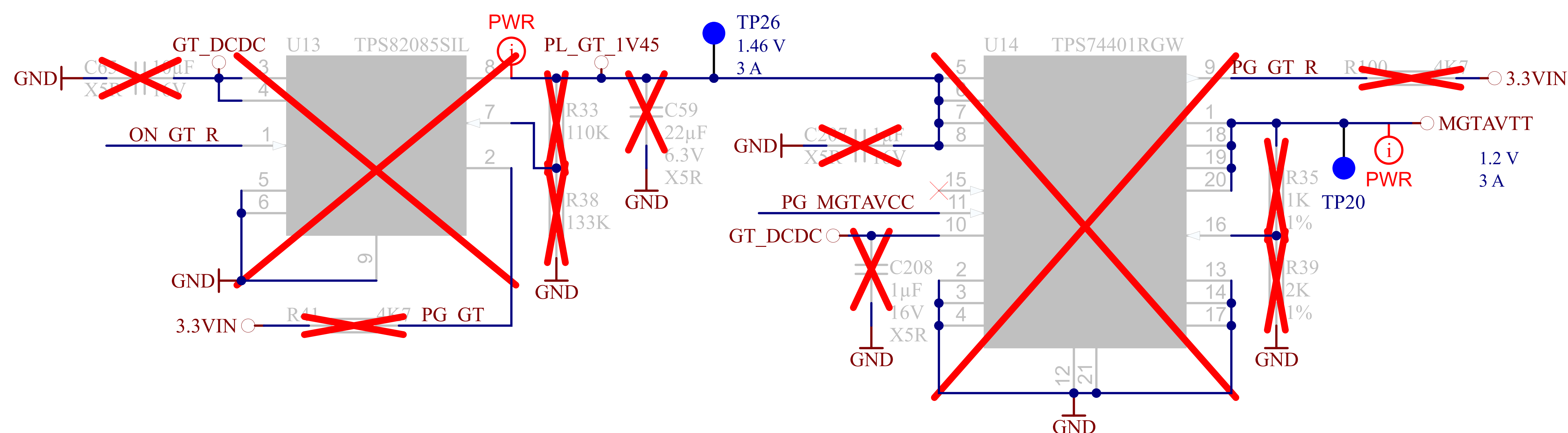
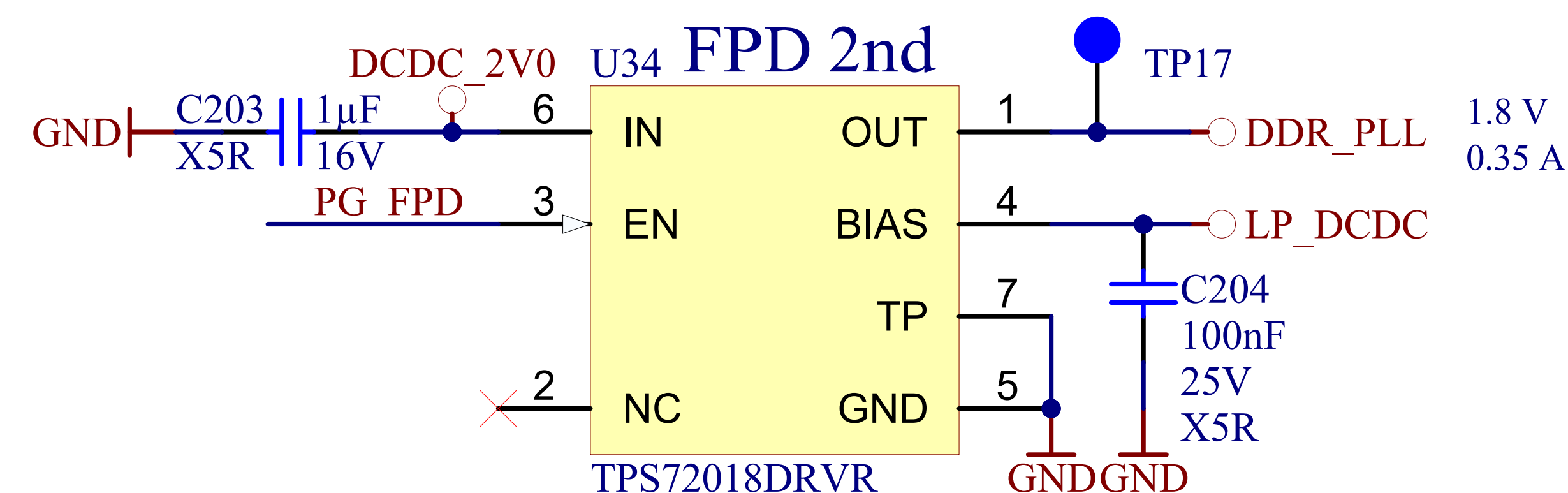
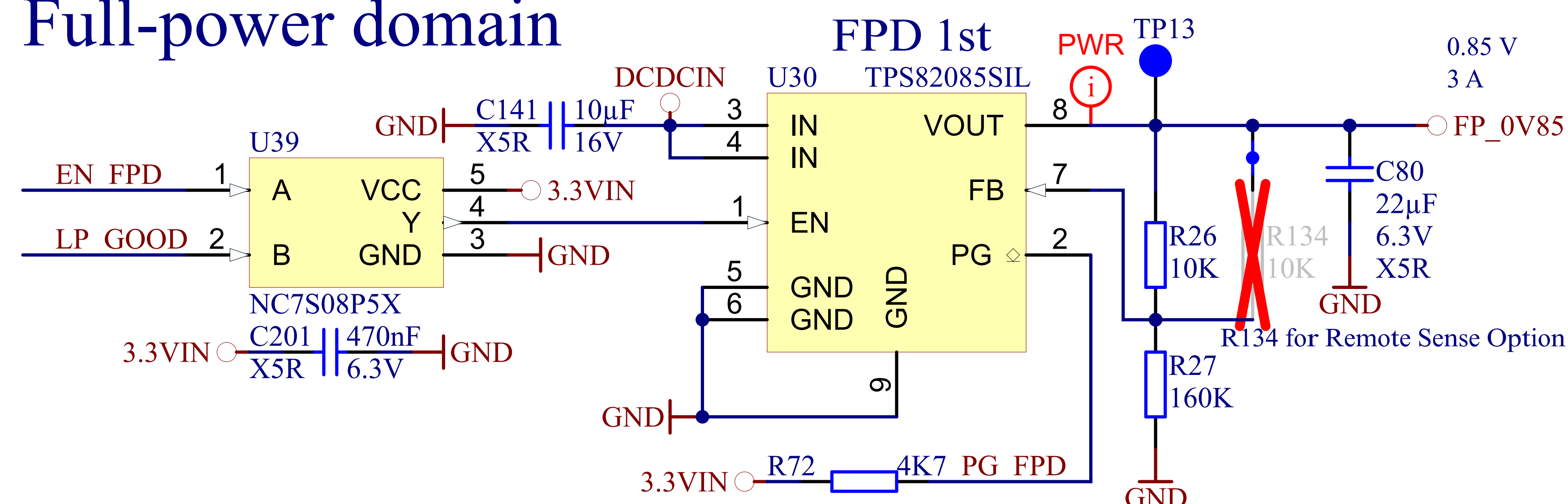


VCCINT_IO & VCCBRAM

Add U33 when -1LI/2LE FPGA is used



Title: TE0813 - POWER_2		
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Title:	TE0813 - POWER_3
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A4	Number: TE0813 3AI81-A
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Rev.	02
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Date: 06.01.2026	Copyright: Trenz Electronic GmbH
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Filename: POWER 2.SchDoc

Low-power domain

PS MGT

PS MIO VCCIO



Title: TE0813 - POWER_4		
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Net Name	Voltage Rail	Low Detect
LP_0V85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V