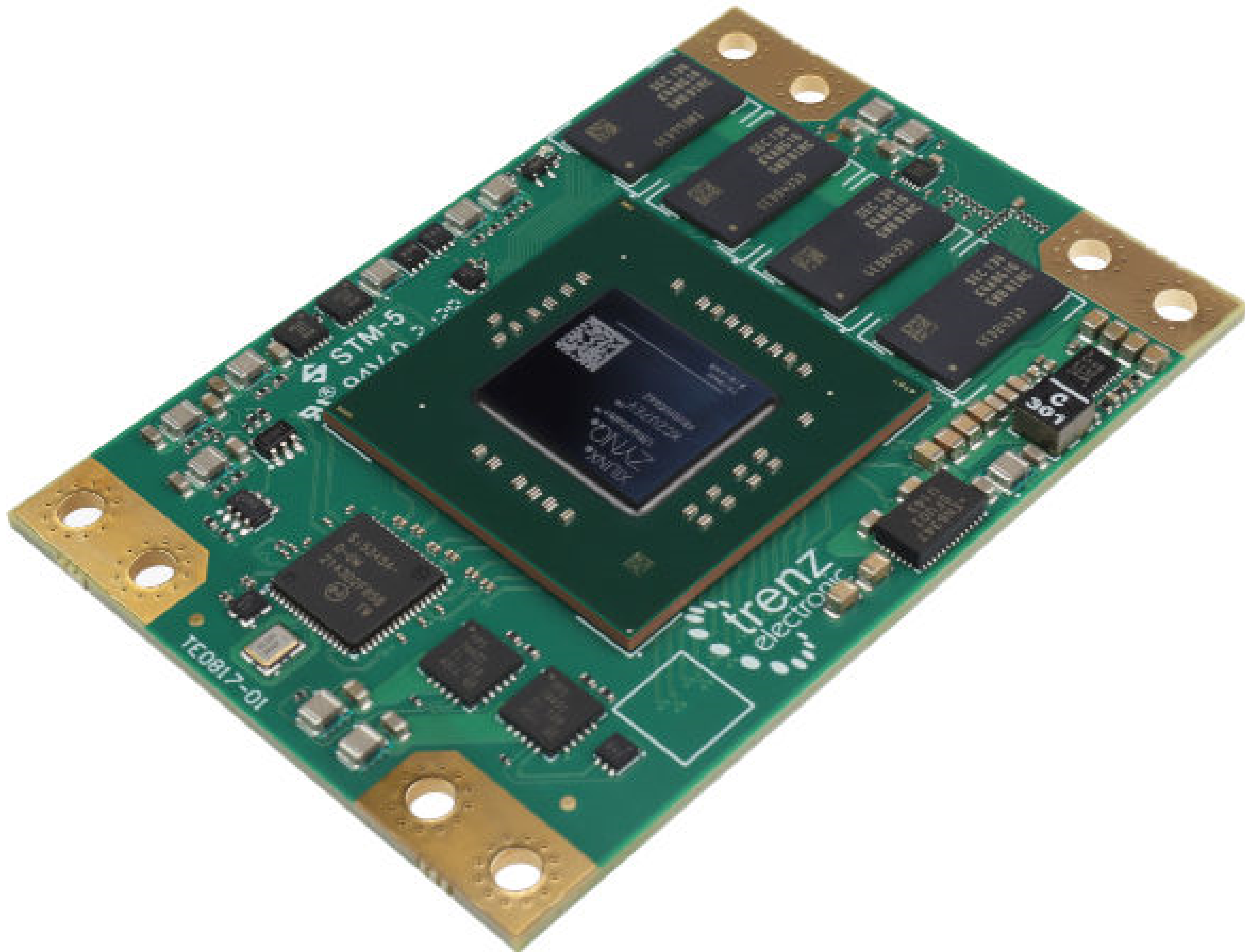
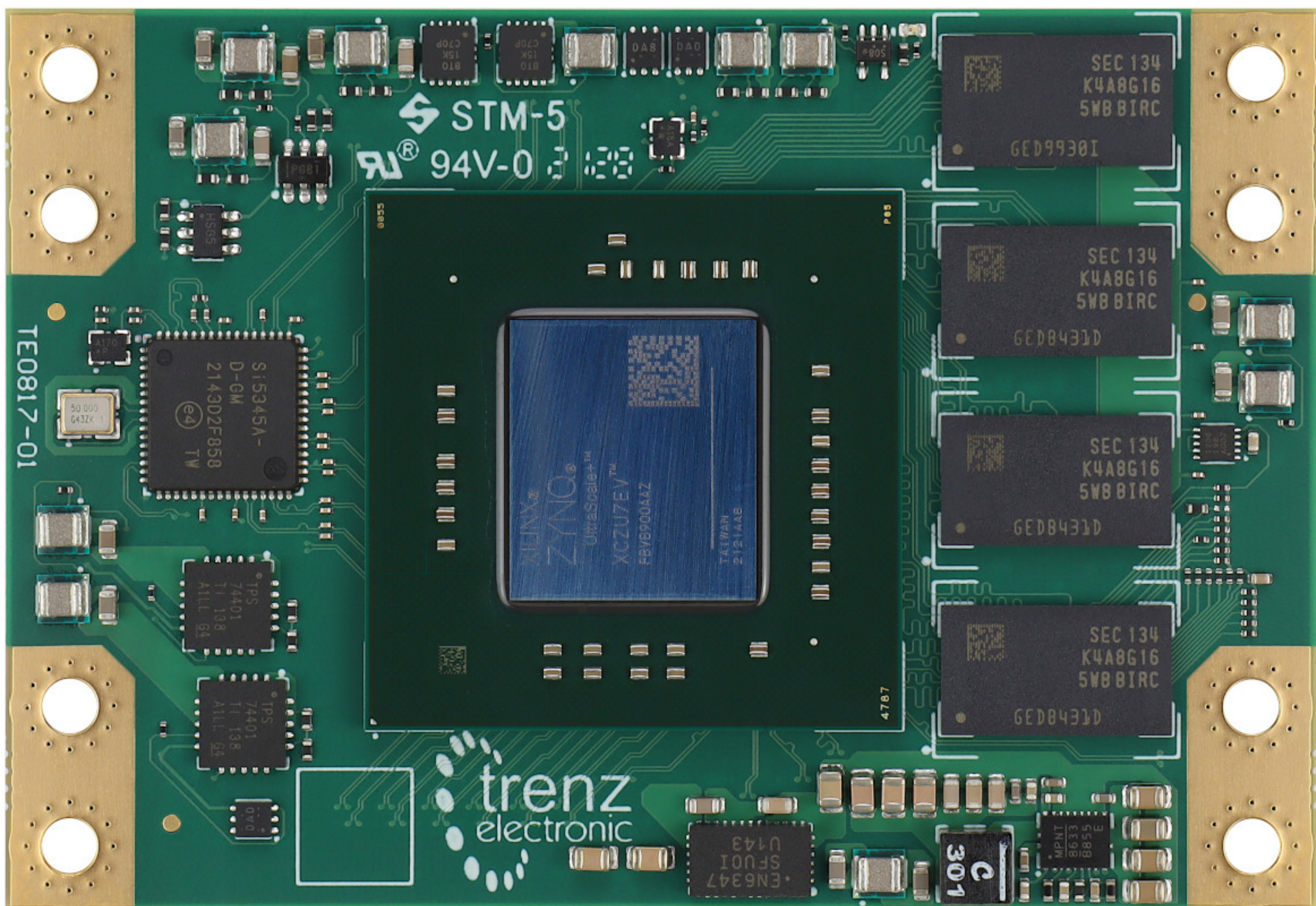
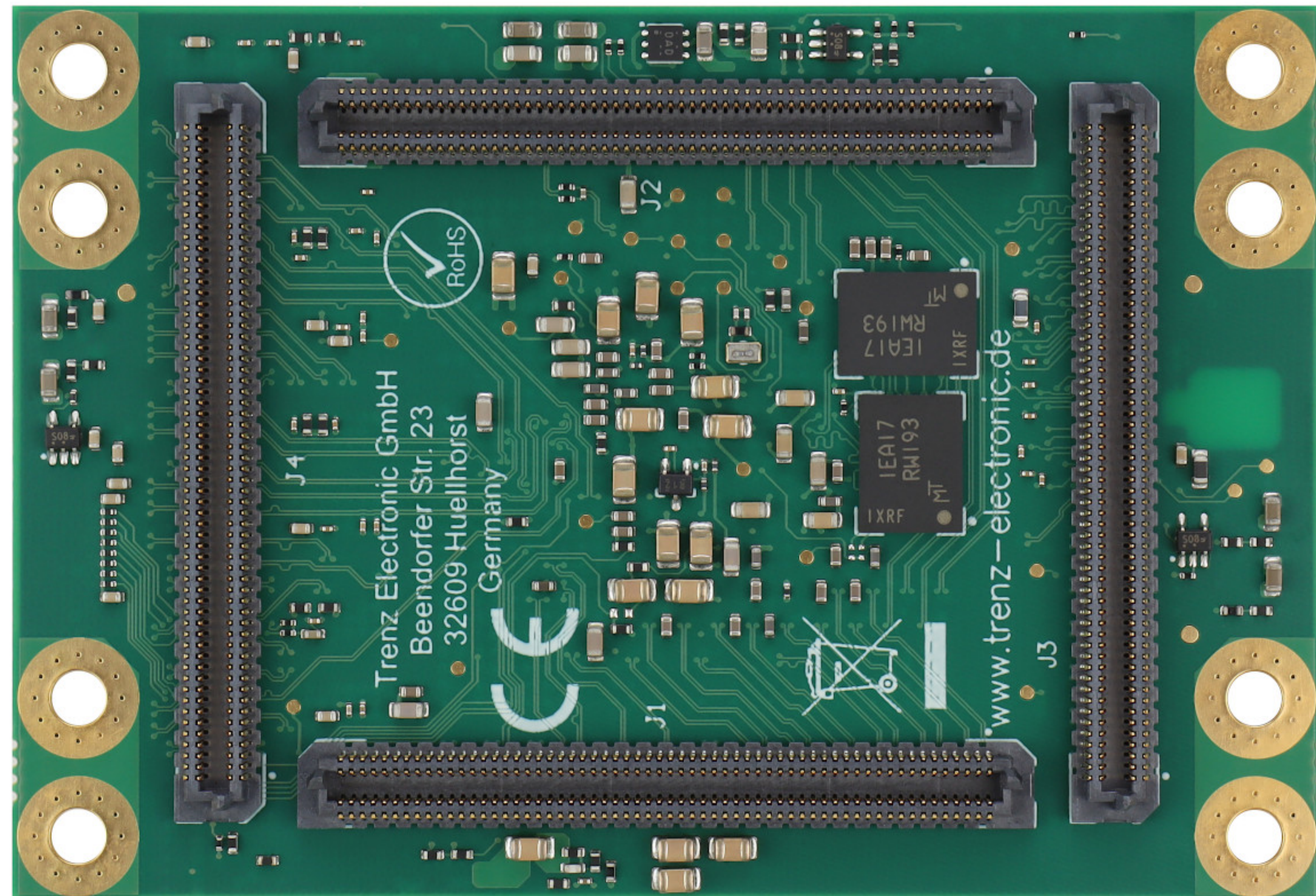


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D	Regarding the usage of our schematics and alike documentation for Trenz module TE0817. Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0817 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets. Schematics and other handouts serve for informational purposes only!												
					D								
			<table><tr><td colspan="2">Title: TE0817</td></tr><tr><td>A4</td><td>Number: TE0817 4BE61-A</td></tr><tr><td>Date: 27.08.2024</td><td>Copyright: Trenz Electronic GmbH</td></tr><tr><td colspan="2">Filename: Legal Notices Modules.SchDoc</td></tr></table>		Title: TE0817		A4	Number: TE0817 4BE61-A	Date: 27.08.2024	Copyright: Trenz Electronic GmbH	Filename: Legal Notices Modules.SchDoc		
Title: TE0817													
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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF	
	2022-11	Added Table with Supported Voltage Ranges	
-02	2024-04	1) Changed DCDC (U13) from EN6347QI to MPM3860GQW-Z and apdated according circuit.. 2) Connected DDR4-TEN signals together for U2A , U3A , U9A , and U12A and pulled them low via 499 Ohm resistor R127 . Added testpoint TP3 for signal DDR4-TEN . 3) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor R30 and changed voltage rail name PL_GT_1V35 to PL_GT_1V45 . 4) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R33 and R35 and changed voltage rail name PL_GT_1V05 to PL_GT_1V15 . 5) Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN . 6) Added capacitors C202 ... C205 for VTT voltage rail VTT . 7) Added resistors R124 (default: not fitted) and R125 to supply U4 VCC either from PL_DCIN or from 3.3VIN . 8) Changed resistor R76 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.3 A for U4 . 9) Changed inductor (L9) from XGL4030-301MEC to XGL5030-351MEC. 10) Added remote sense option (default: not fitted): 10.1) R126 for U30 . 10.2) R128 for U29 . 10.3) R129 for U31 . 11) Added decoupling capacitors: 11.1) C208 for U4 . 11.2) C211 , C212 , and C213 for U6 . 11.3) C216 for U10 . 11.4) C214 for U26 . 11.5) C215 for U27 . 11.6) C210 for U34 . 11.7) C196 for U39 . 11.8) C197 for U40 . 11.9) C198 for U42 . 11.10) C199 for U41 . 11.11) C200 for U44 . 11.12) C201 , C206 , and C207 for U1N . 12) Added pull-up resistors for HOLD (R130) and WP (R131) signals for Flash U7A . 13) Added pull-up resistors for HOLD (R132) and WP (R133) signals for Flash U17A . 14) Changed capacitor (C132) from 1 nF, X7R to 1.2 nF, NP0. 15) Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201. 16) Changed 100 nF capacitors (C37 , C95 , C96 , C130 , and C131) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402. 17) Changed capacitor (C76 , C77 , C134 , C195) from 1 µF, 16 V to 2.2 µF, 10 V. 18) Changed capacitor (C129 , C140 , C141 , C142 , C143 , C144 , C145 , C146 , C147 , C148 , C153) from 10 µF, 16 V to 22 µF, 10 V. 19) Changed 22 uF capacitor (C70 , C73 , C74 , C75) from 0805 to 0603. 20) Changed 22 uF capacitor (C78 , C80 , C81 , C82 , C83 , C84 , C85 , C86 , C87 , C110 , C152 , C154 , C178) from 6.3 V to 10 V. 21) Changed 100 Ohm resistors (R7 , R10) from 0201, 0.05 W to 0402, 0.063 W. 22) Changed resistor R77 from 12 kOhm to 10 kOhm. 23) Changed resistors R41 and R58 from 2 kOhm to 2.49 kOhm. 24) Added testpoints TP4 , TP10 , TP11 , TP13 , TP14 , TP19 , TP21 , TP22 , TP33 ... TP72 . 25) Added UKCA logo. 26) Updated from library. 27) Changed signal trace length. 28) Updated documentation.	ED

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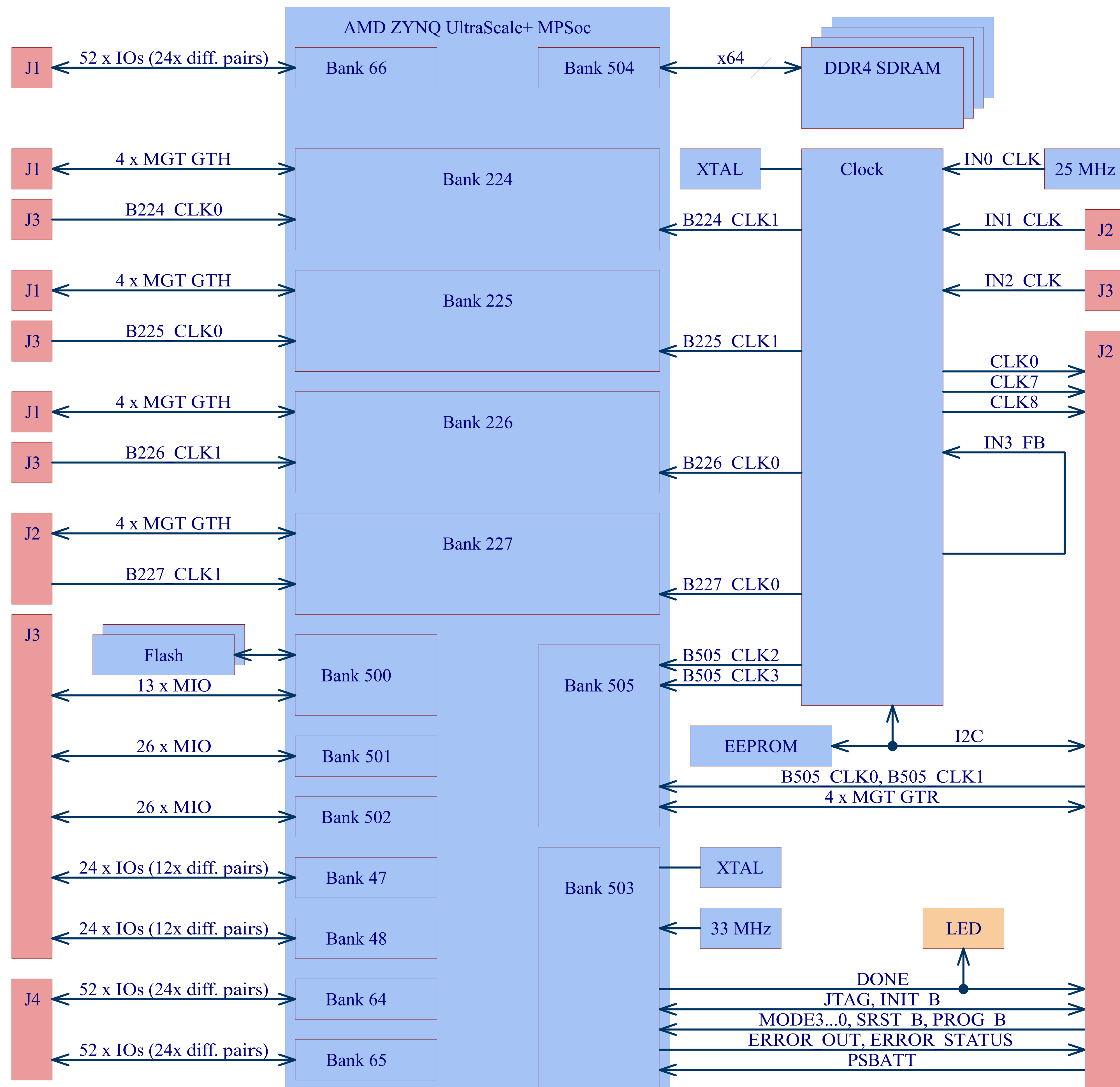
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Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3 V	+/- 5 %	Micromodule Power	-
PL_DCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Programmable Logic
LP_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	Low-Power Domain
GT_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	GTH/GTY Transceiver
DCDCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	-
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3 V	+/- 5 %	PLL Core Power	-
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Processing System
DDR4_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x69	-
EEPROM U11	0x50	-

Legend:

- B2B Connector
- LED Interface
- On-board Components



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Rev. 02

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Filename: **TE0817-Overview.SchDoc**

Title: TE0817			
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Filename: Power Diagram.SchDoc			

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Special notes:

PM1

FIDU-DOT - mini

PM2

FIDU-DOT - mini

PM3

FIDU-DOT - mini

PM4

FIDU-DOT - mini

PM6

FIDU-DOT - mini

PM5

FIDU-DOT - mini

Serial1

Serial

Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT

MECH1

TE Address Overlay

LOGO ADDRESS

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

RoHS

RoHS-TOPOVERLAY

WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

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Filename: TE0817.SchDoc

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Design drawn by: ED

Checked by: MT

Assembly variant: 4BE61-A

Created by: VG

Modified by: VG

Modified at: 2025-12-17

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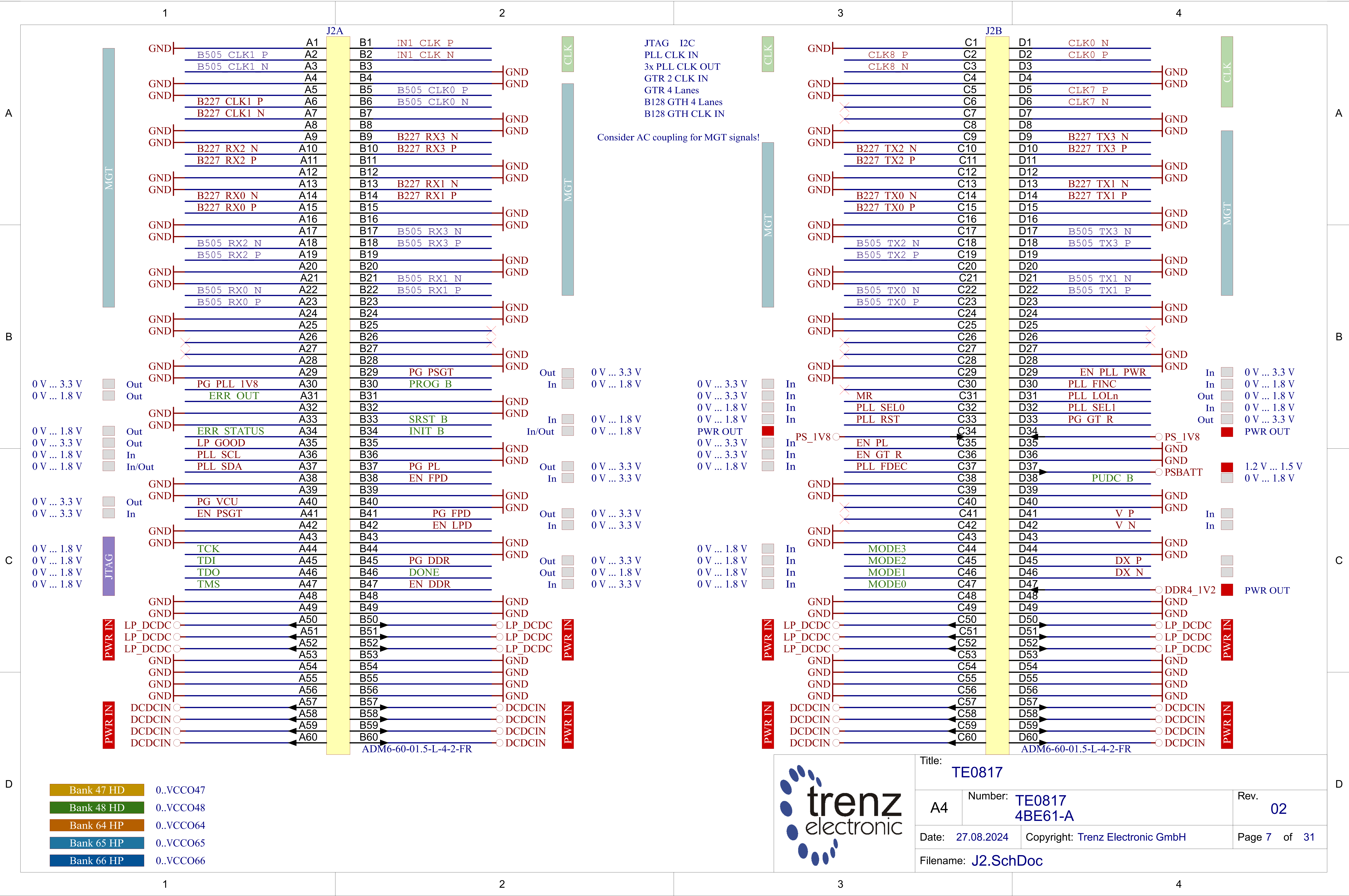
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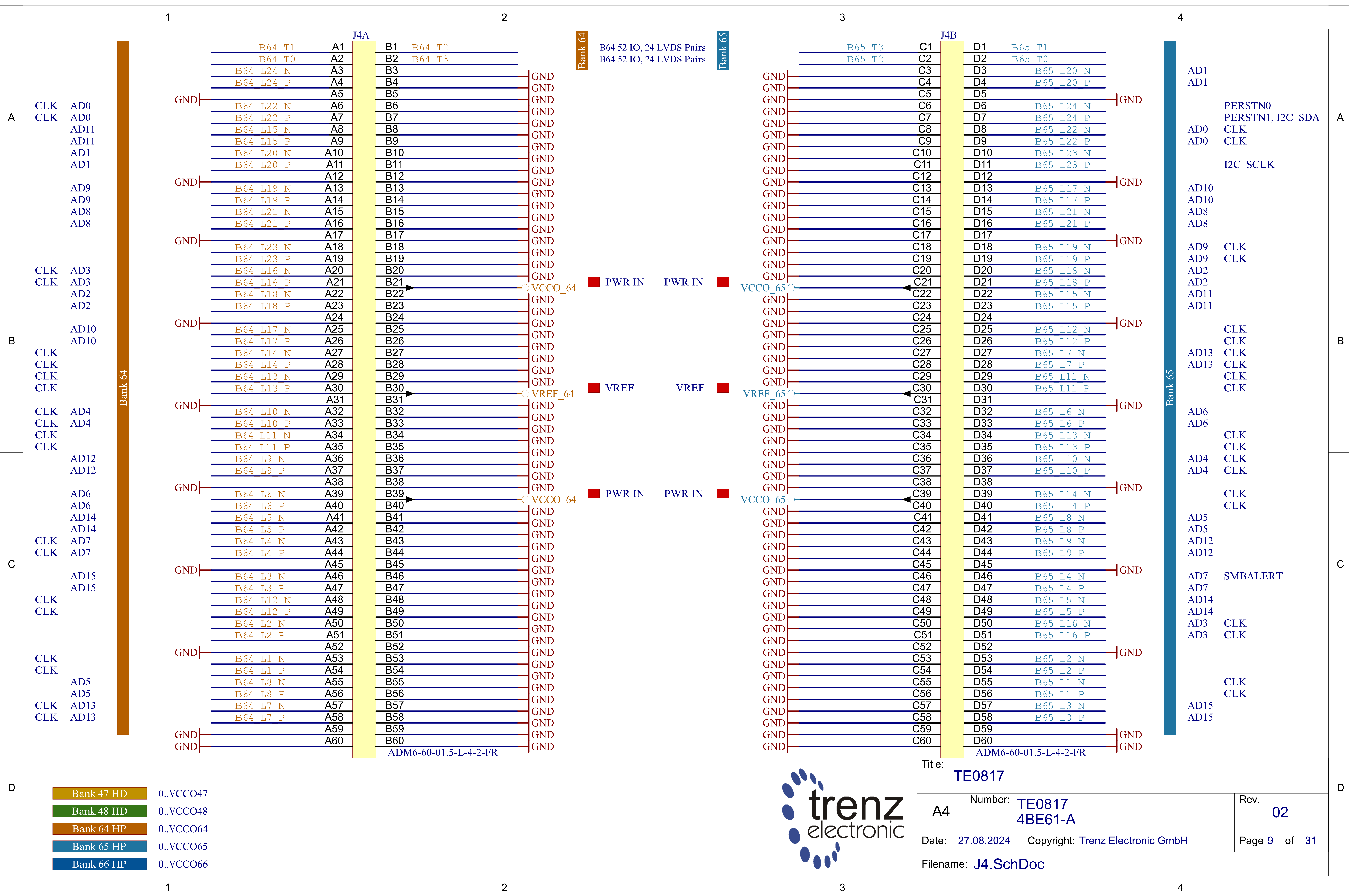
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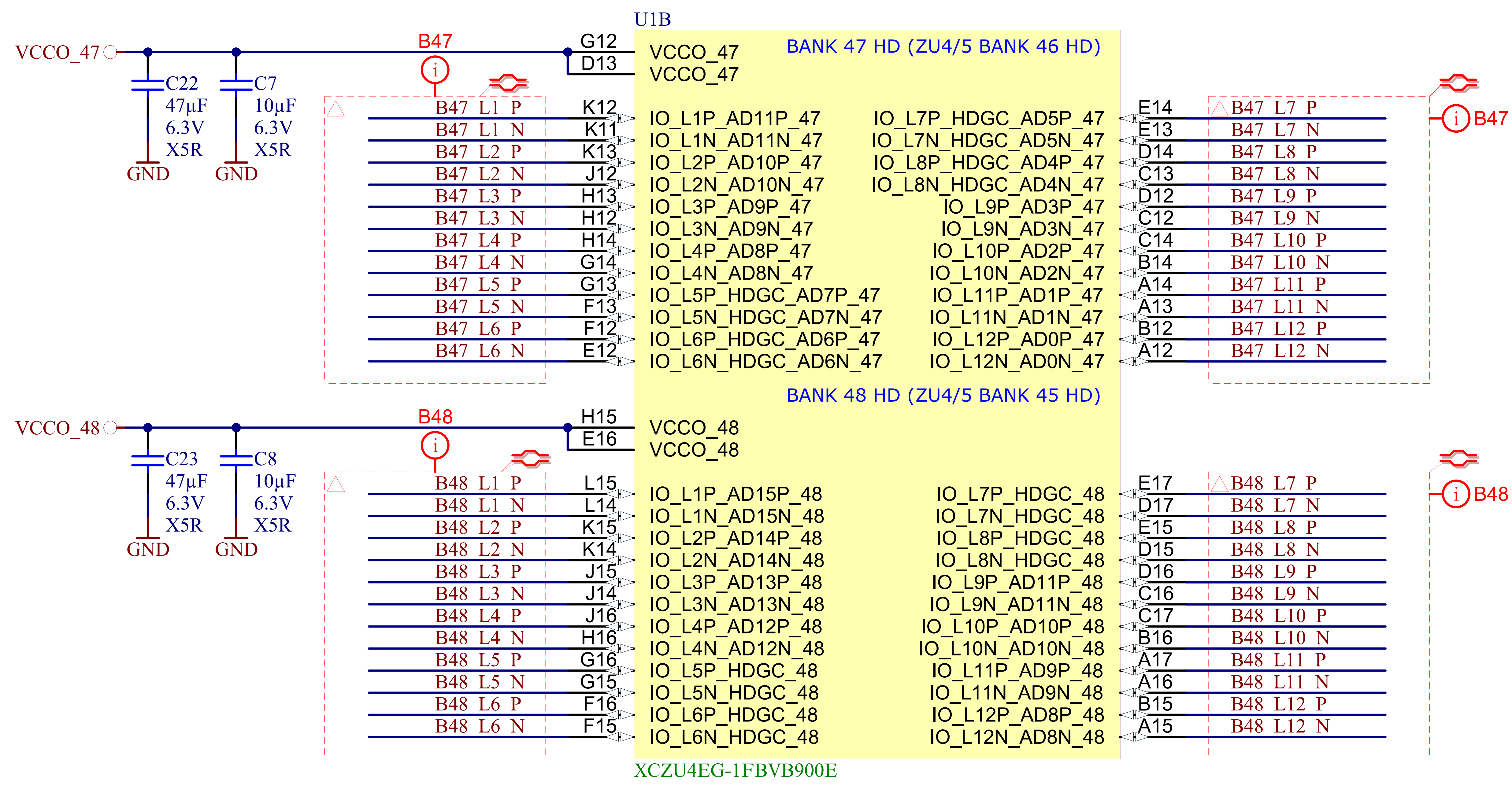
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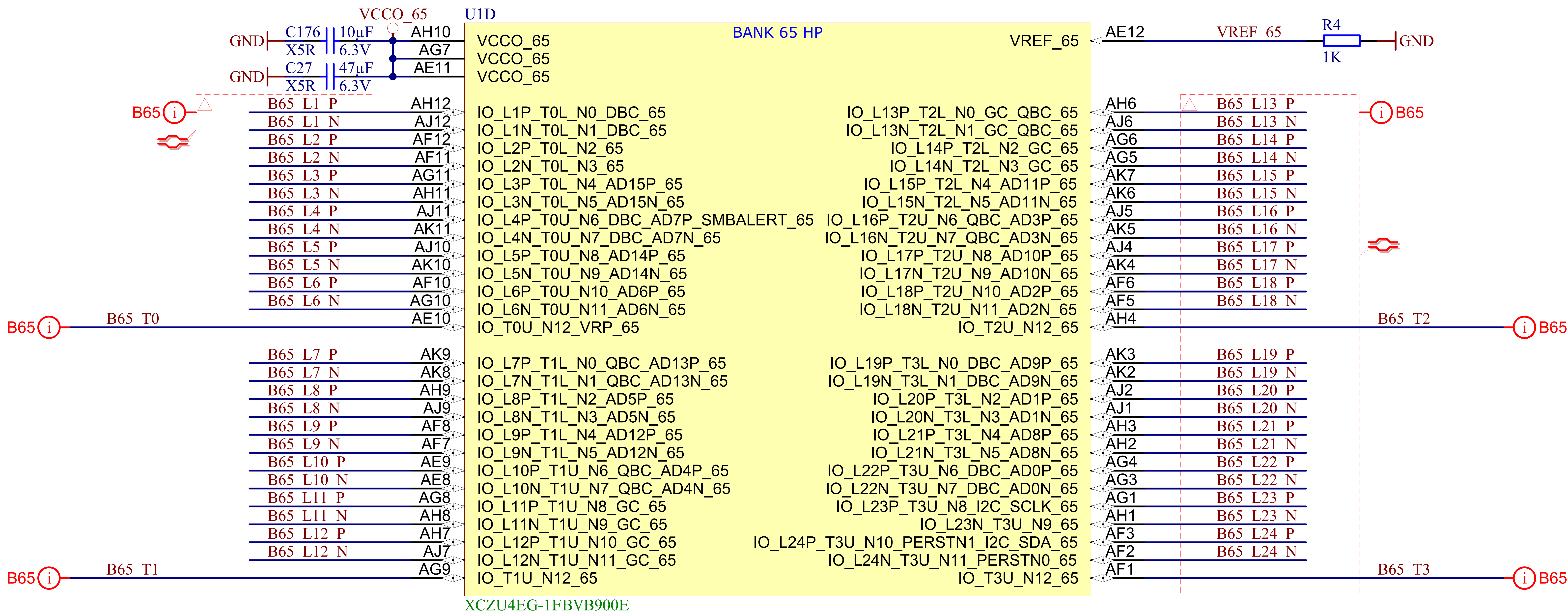
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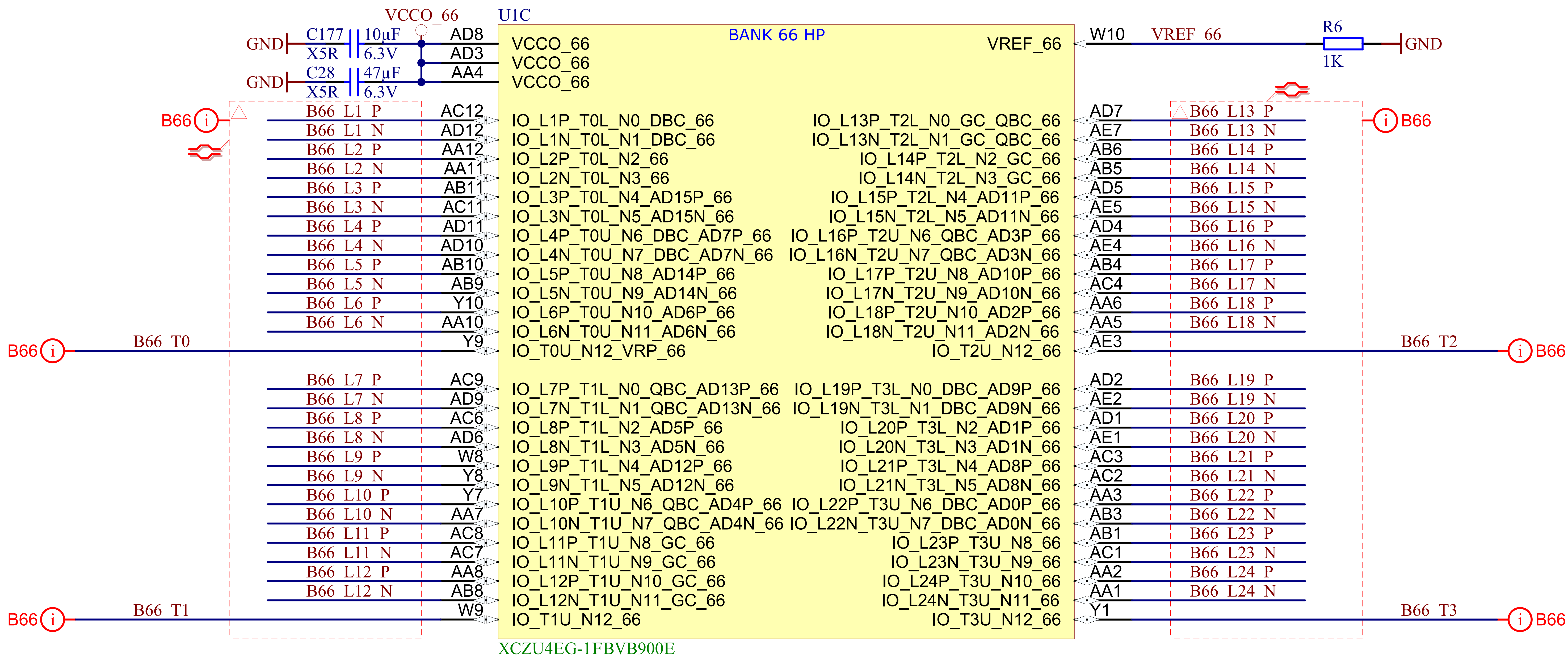
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Date: 27.08.2024	Copyright: Trenz Electronic GmbH	Page 12 of 31
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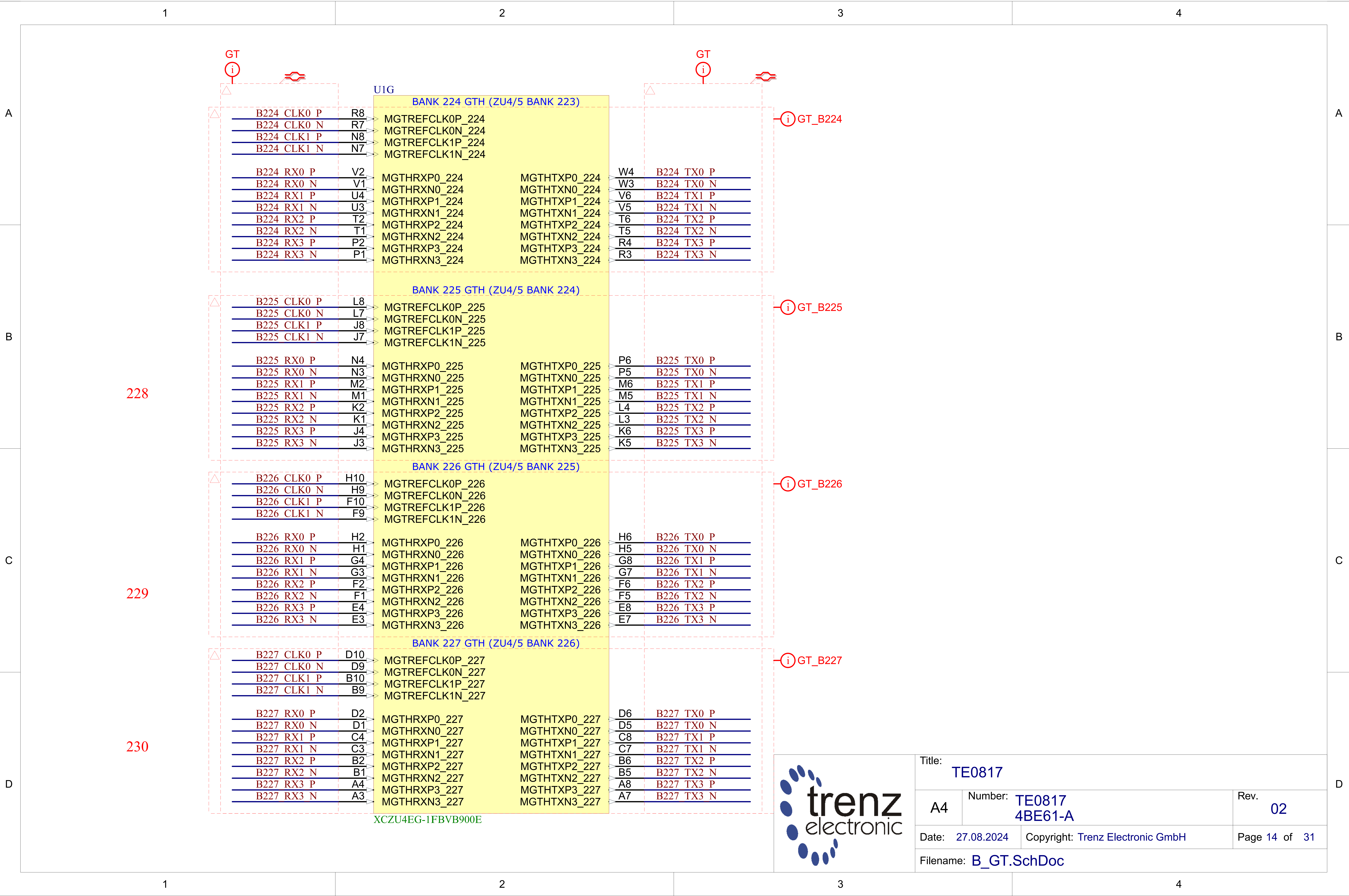
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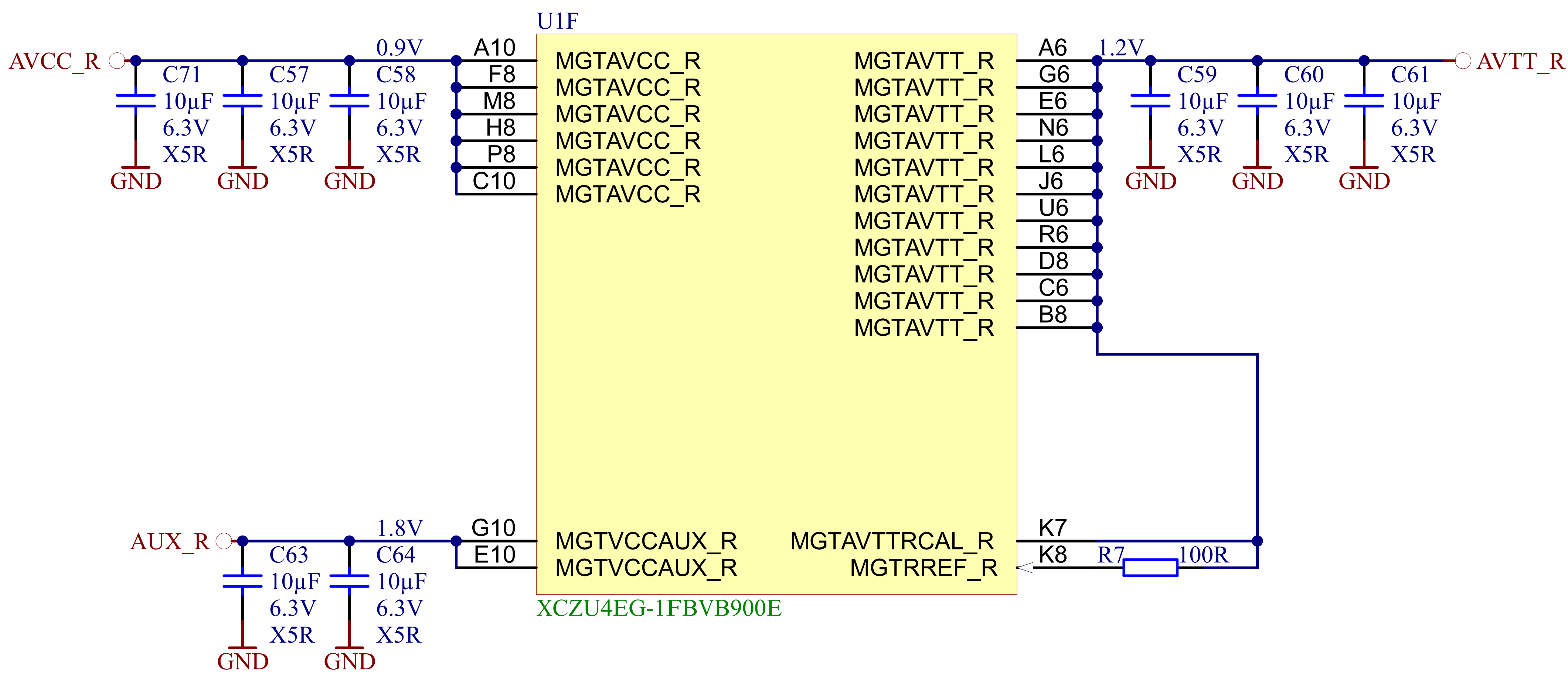
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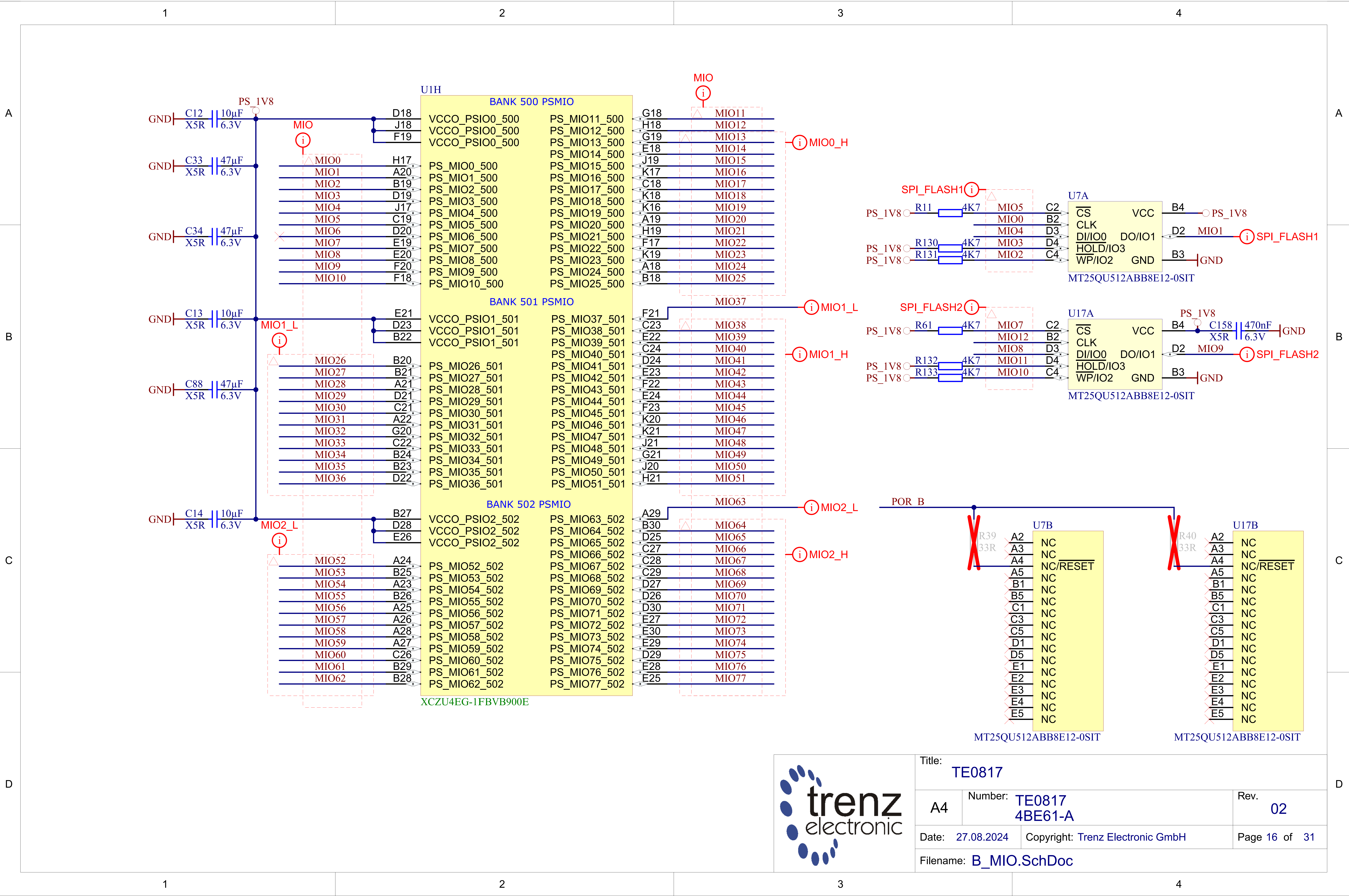
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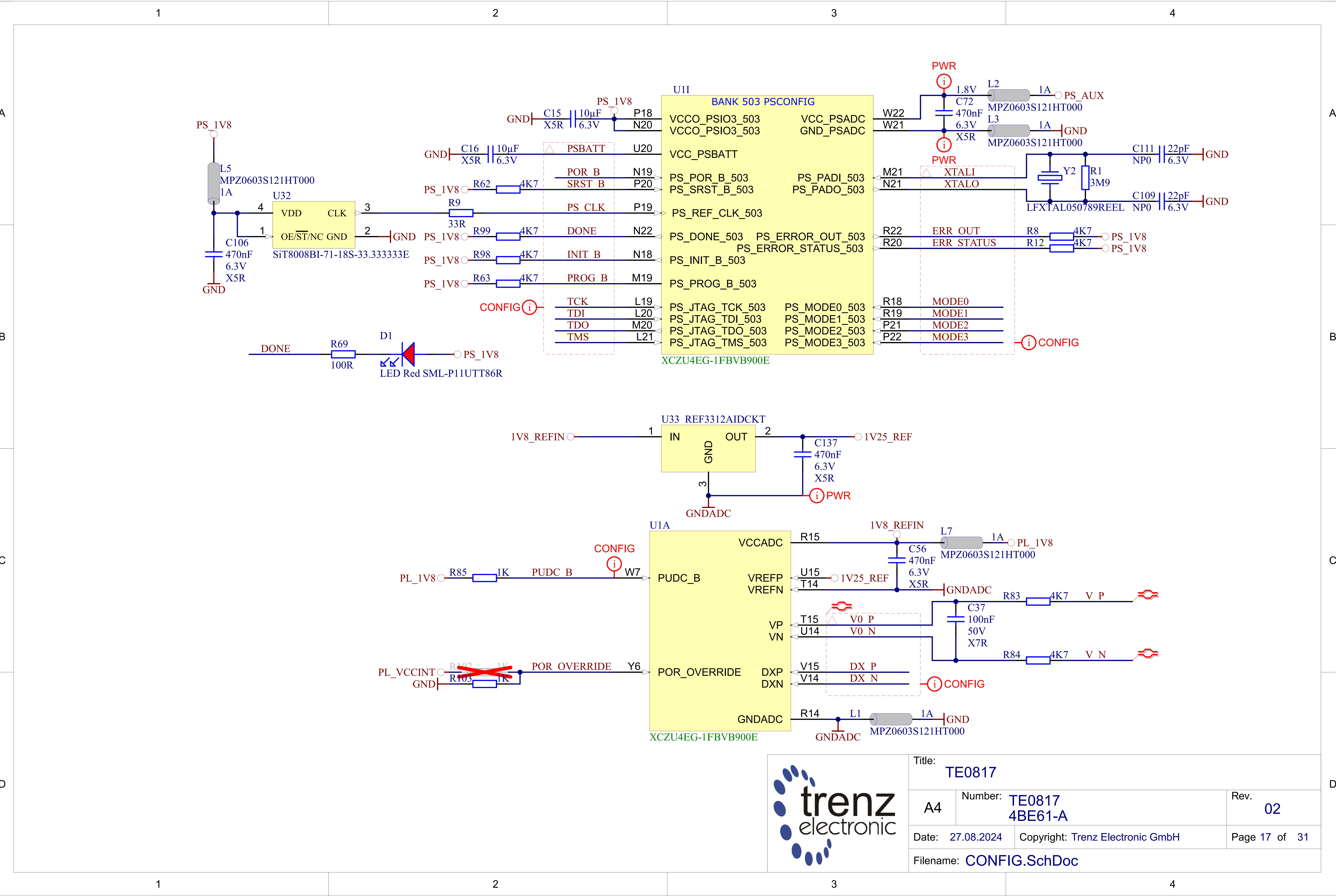
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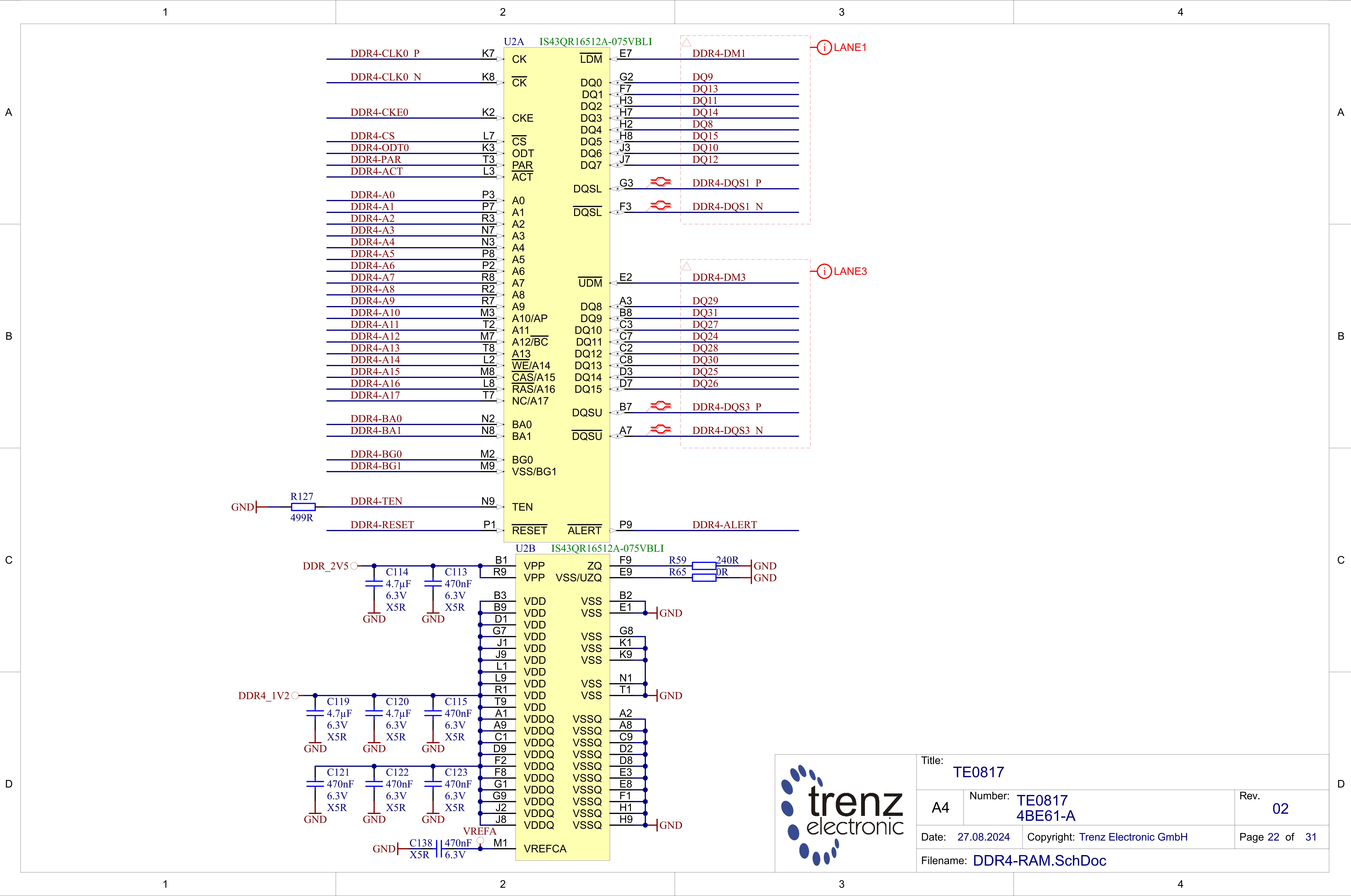
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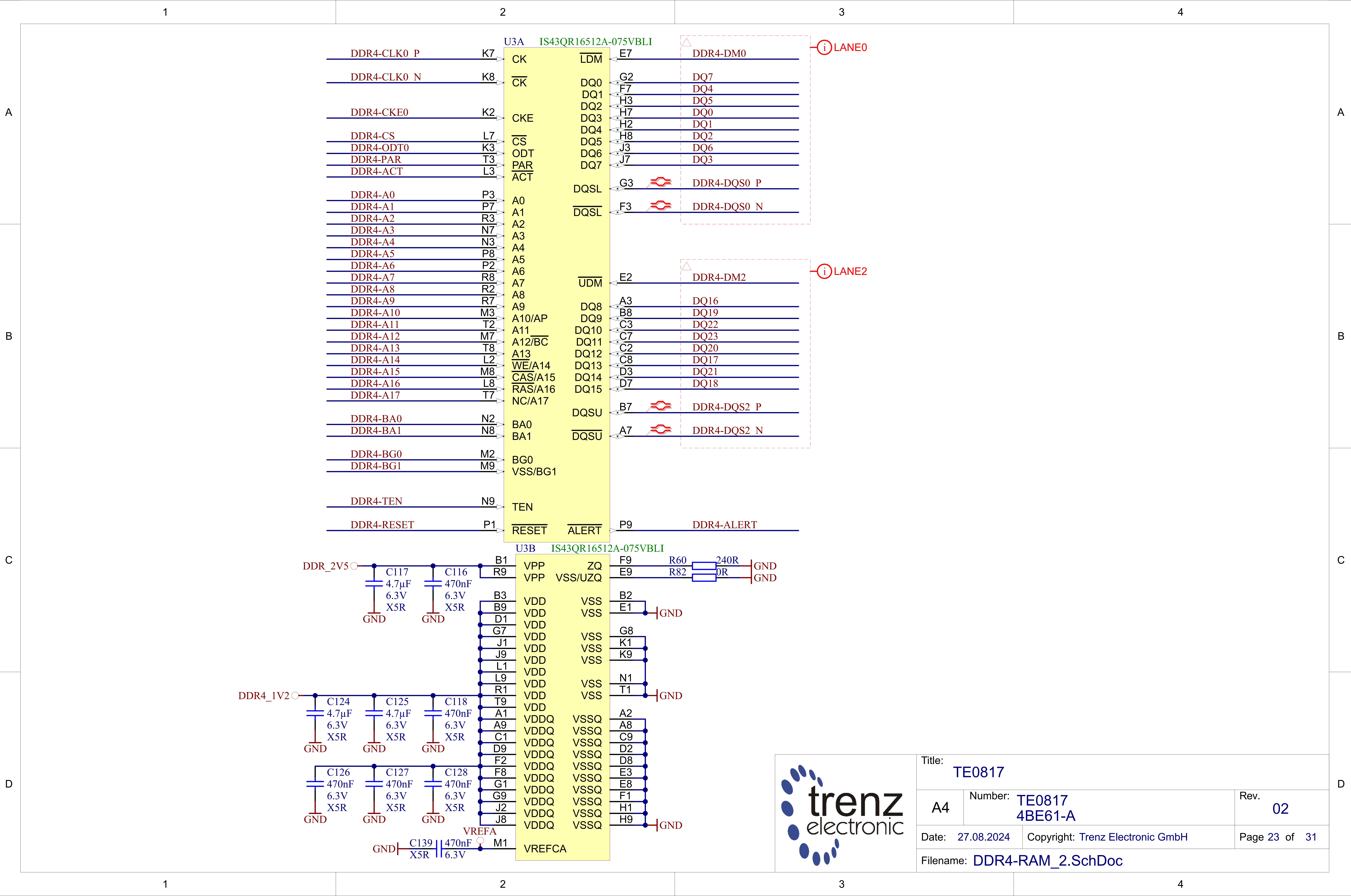
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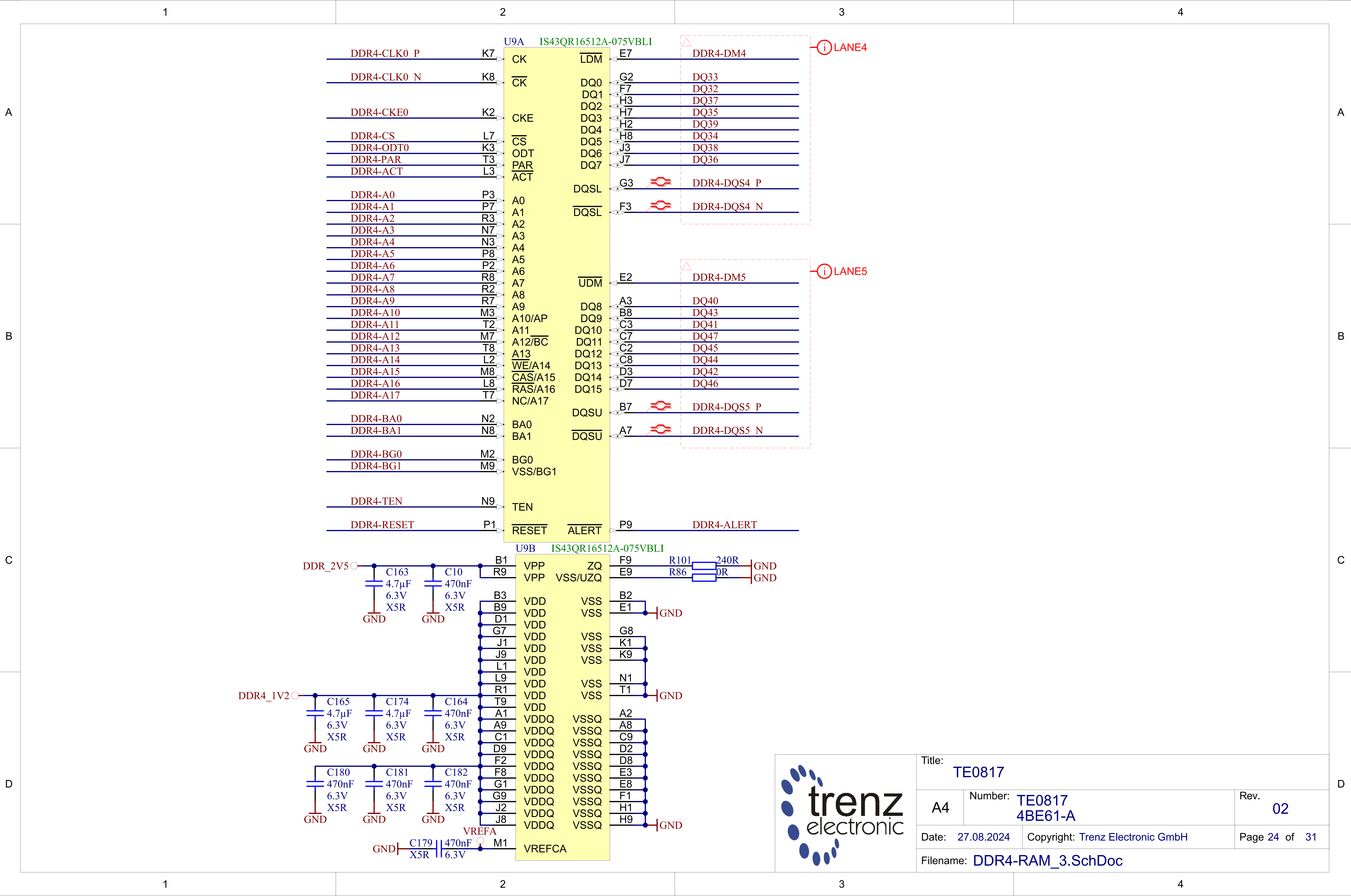


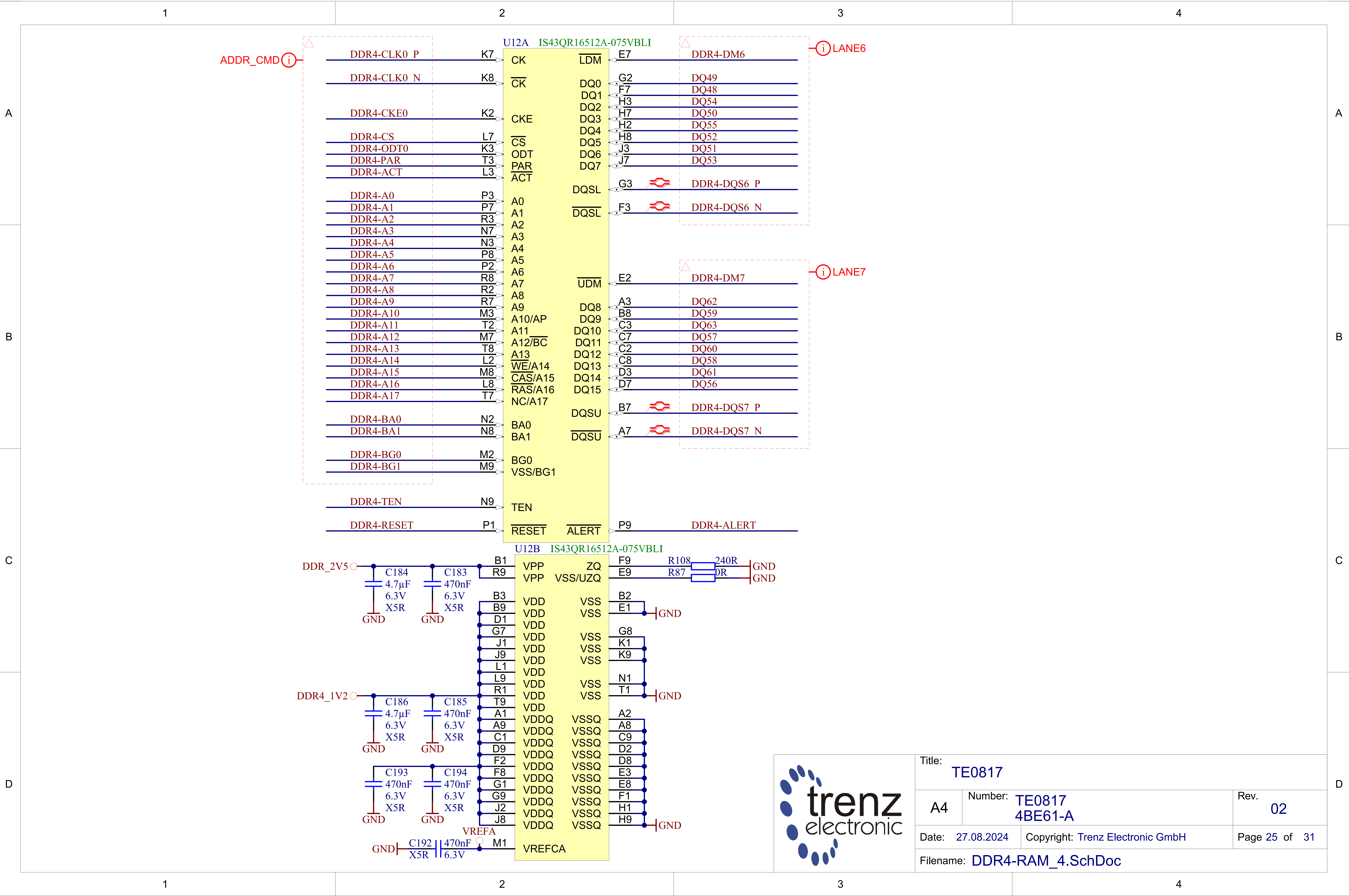


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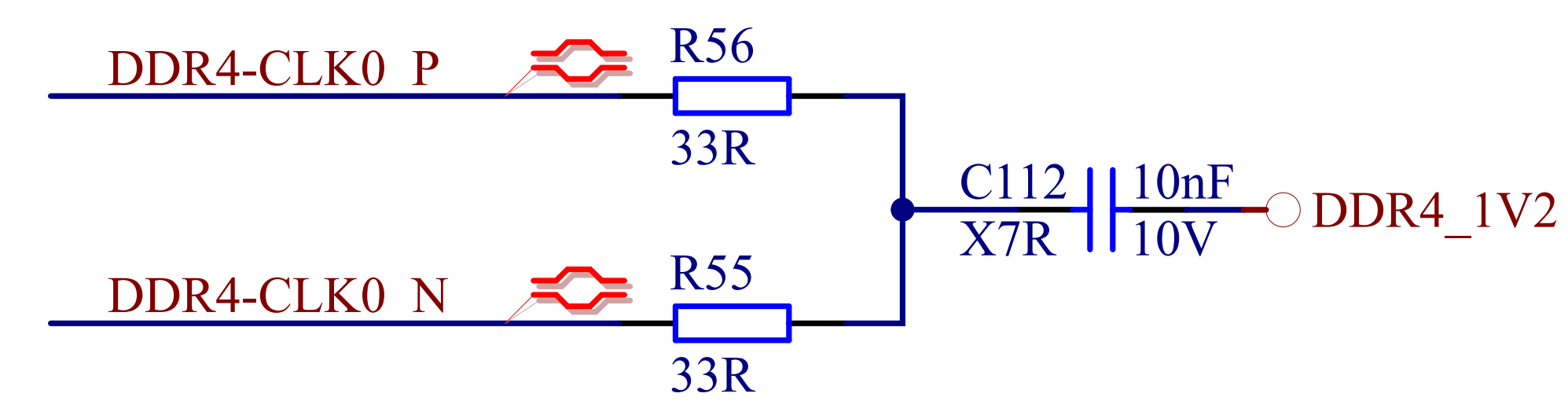




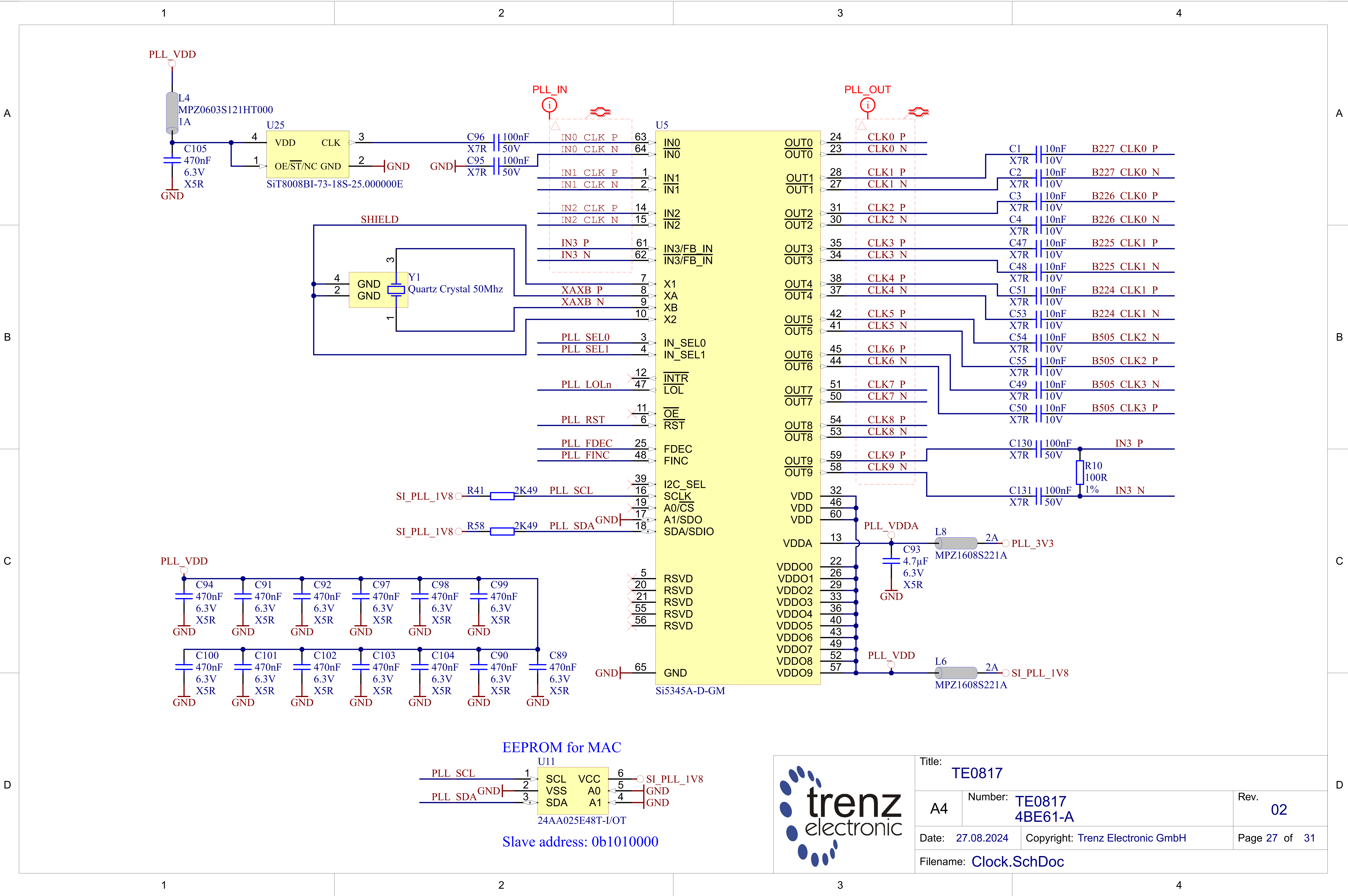




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Date: 27.08.2024	Copyright: Trenz Electronic GmbH	Page 25 of 31
Filename: DDR4-RAM_4.SchDoc		



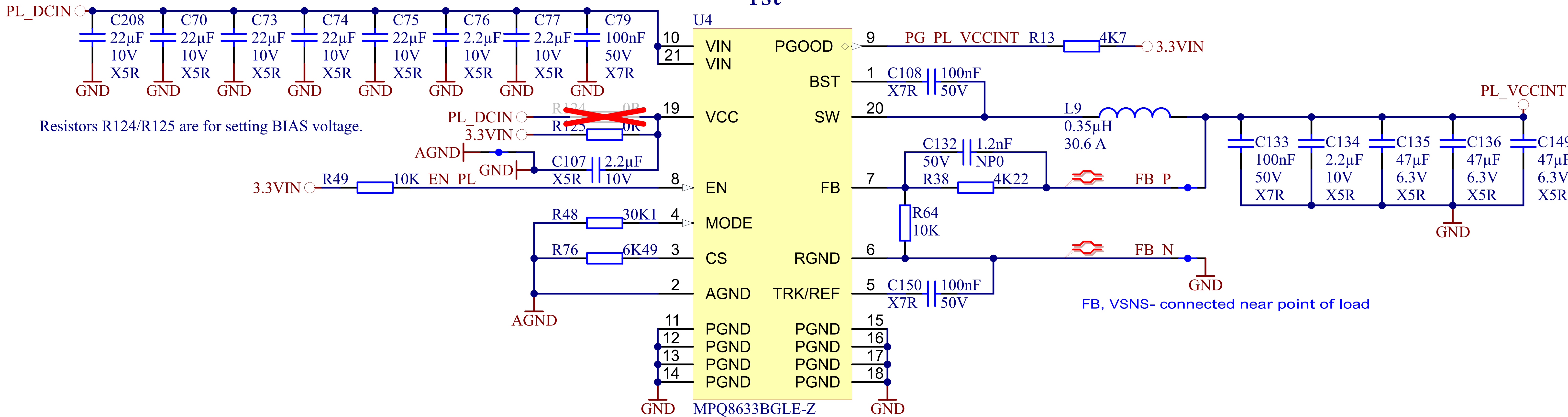
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A4	Number: TE0817 4BE61-A	Rev. 02
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Filename: DDR4-TERM.SchDoc		



U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

PL VCCINT

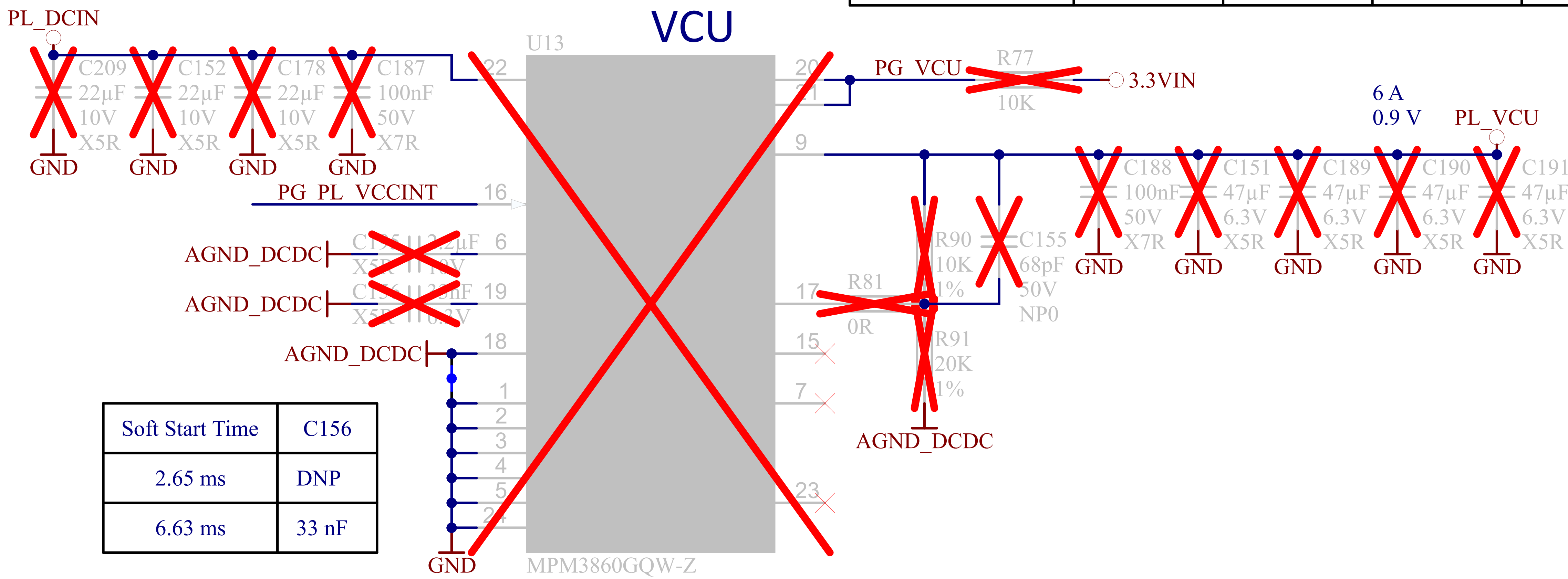
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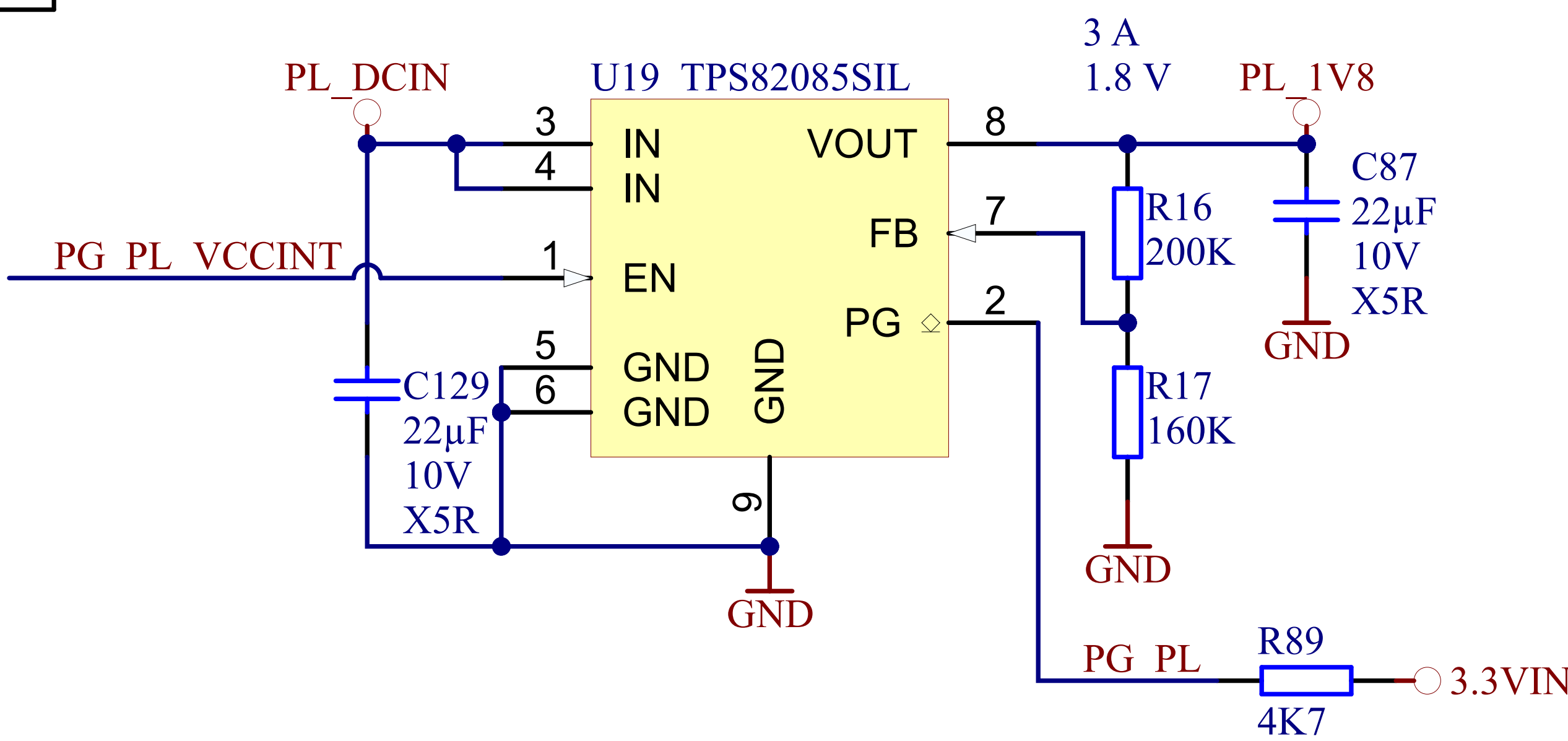
DCDC U4 (pin compatible)	Current Capability	Current Limit*	R76	Light-Load Mode	Frequency	R48	Soft Start Time	C150
TPS548A28	15 A	13.9 A	4.70 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
TPS548B28	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
MPQ8633BGLE-Z	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF

* Current limit depends on input and output voltage.

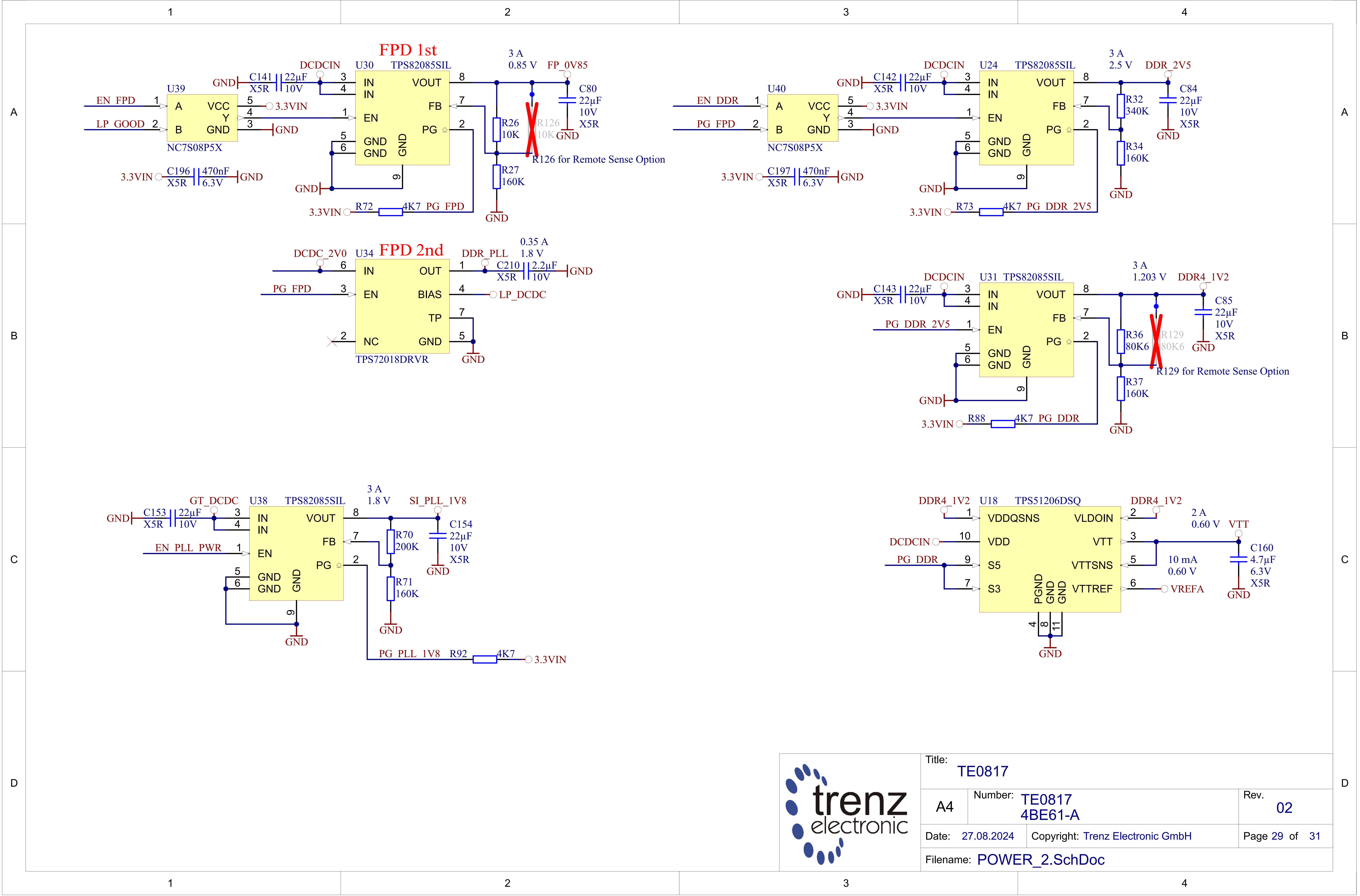
FPGA Speedgrade	R38	R64	PL_VCCINT	C132
-1	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-2	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-3	10 kOhm	20 kOhm	0.900 V	560 pF



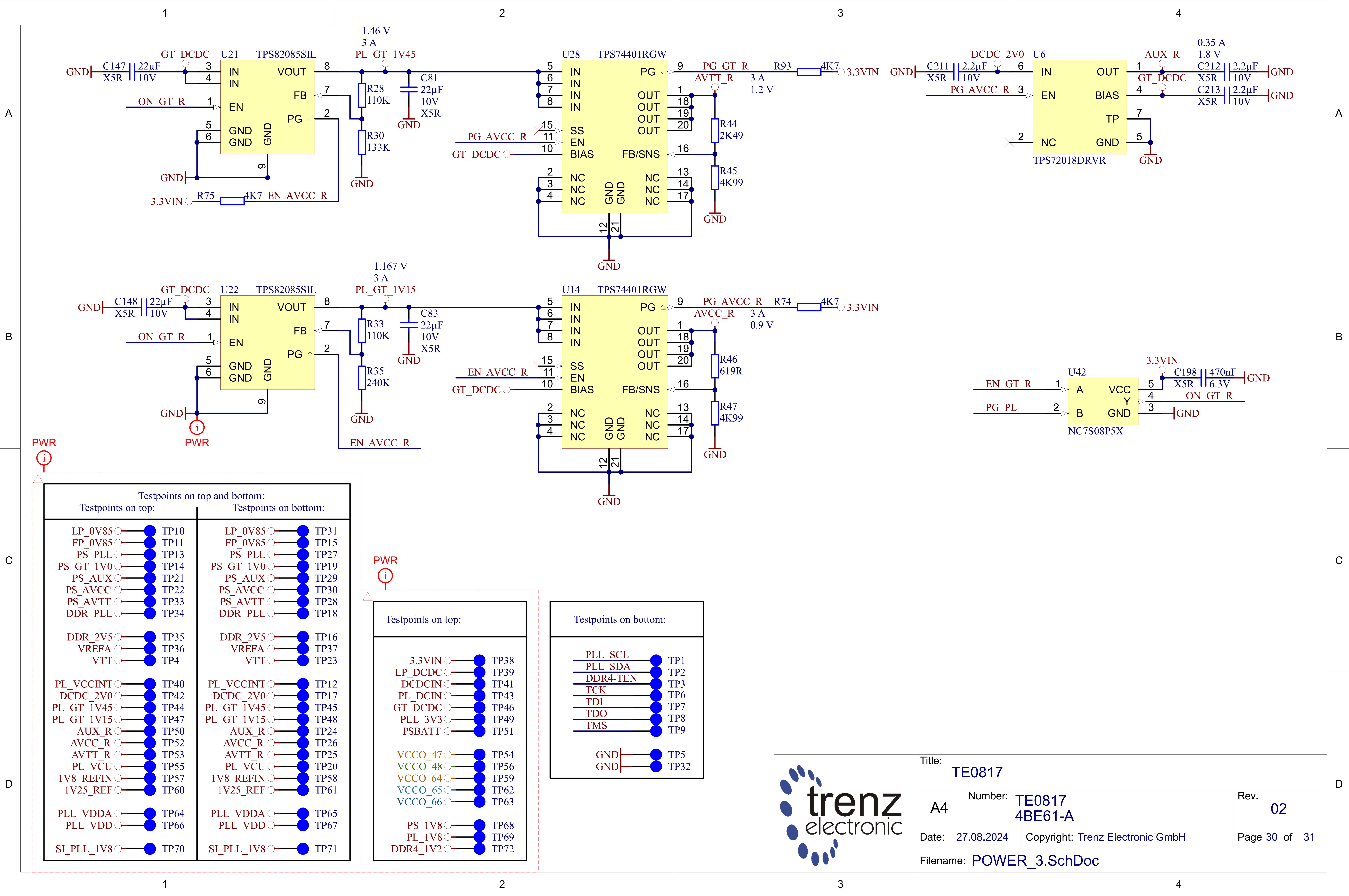
Soft Start Time	C156
2.65 ms	DNP
6.63 ms	33 nF

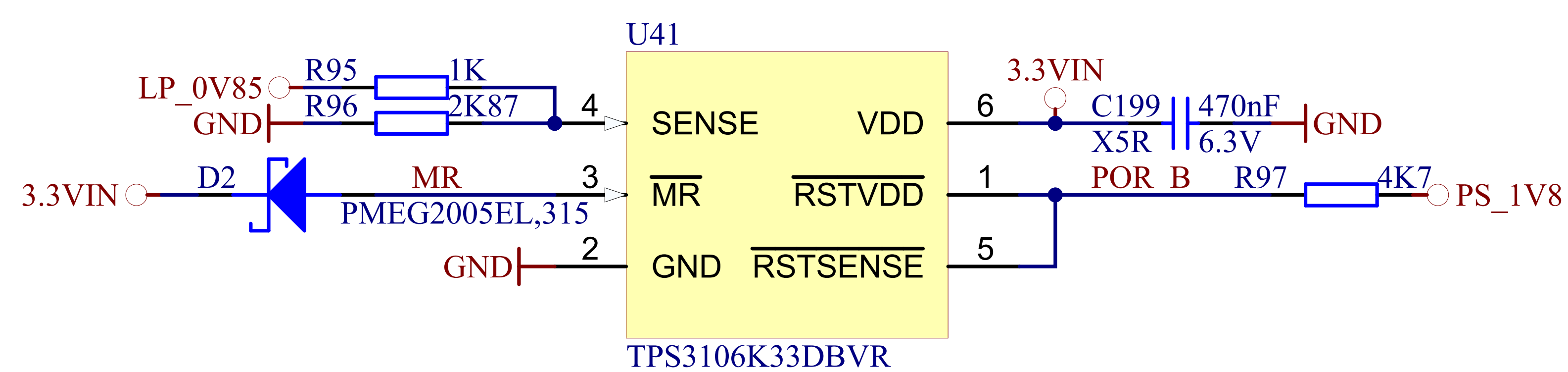
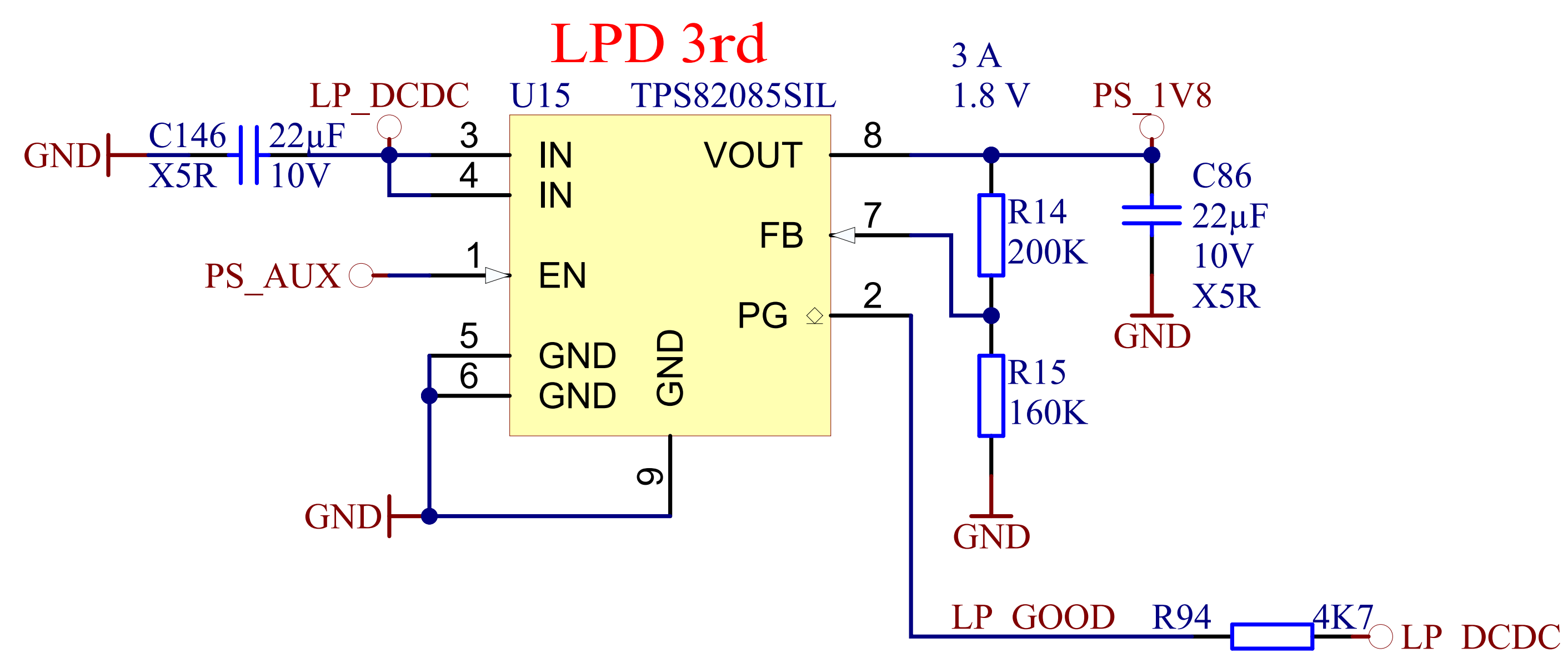
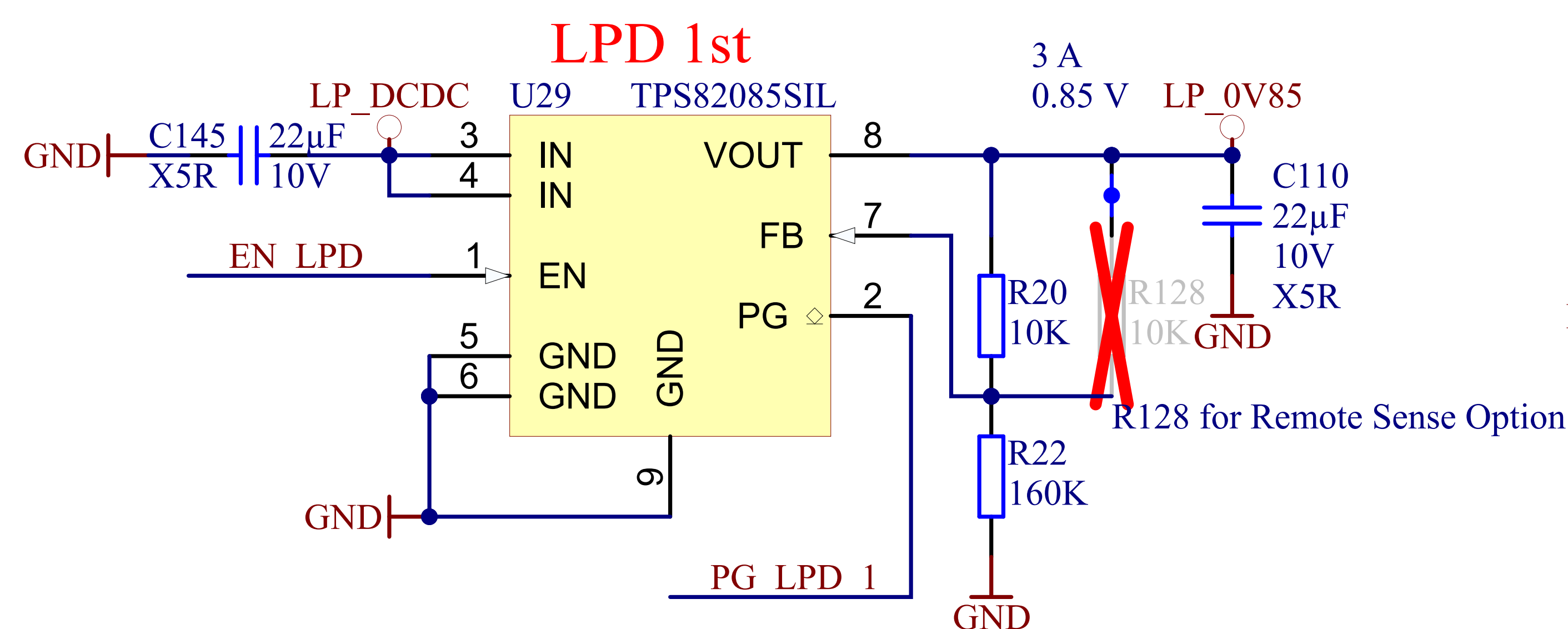
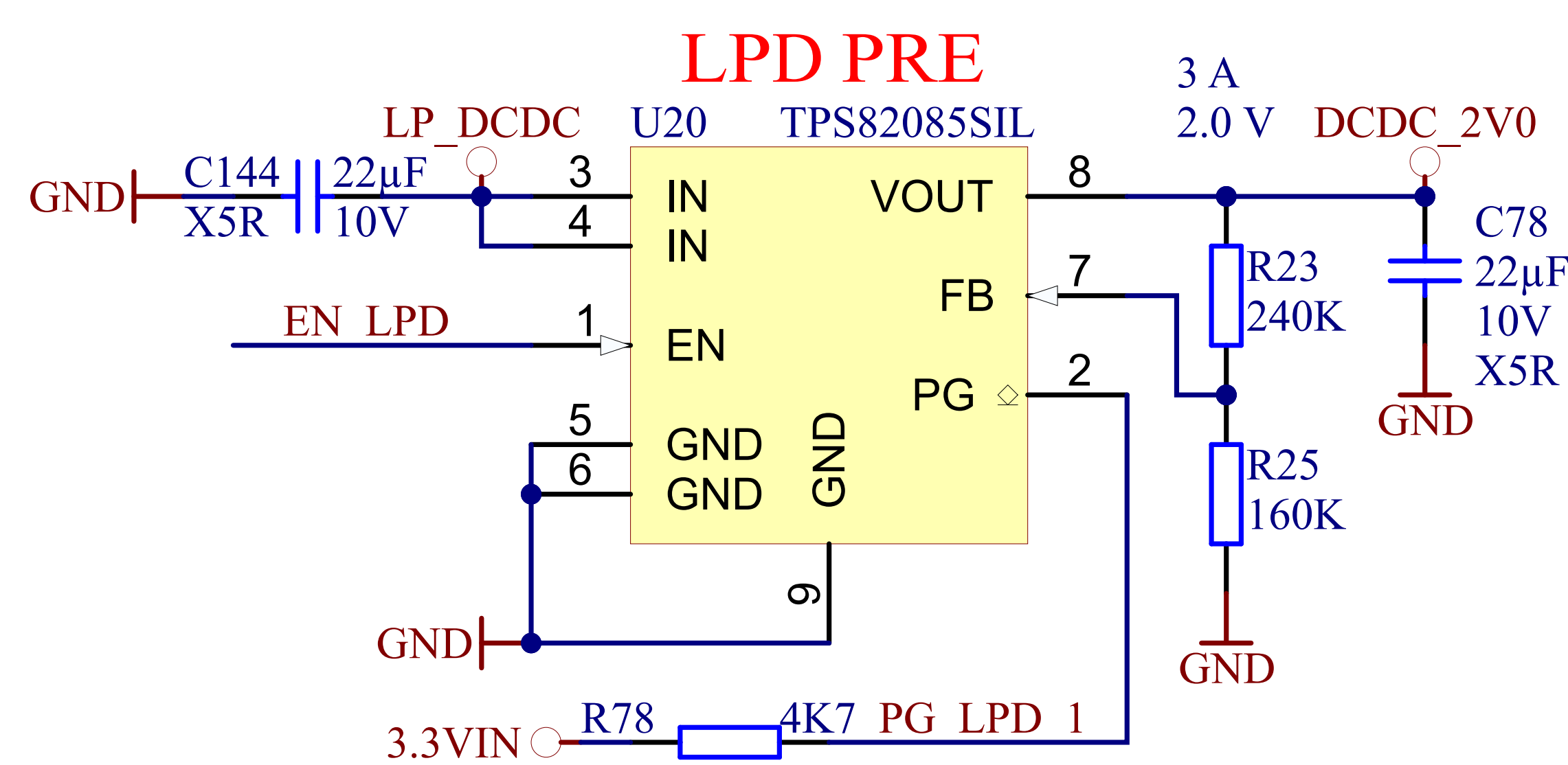


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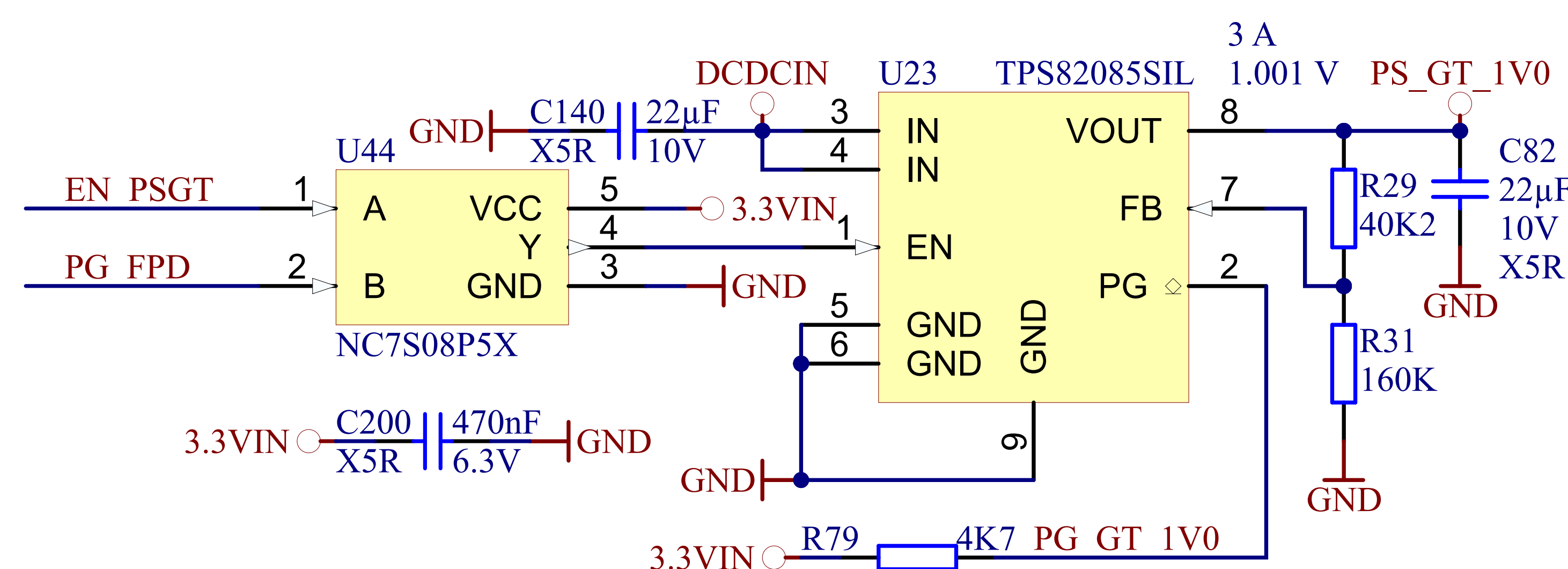
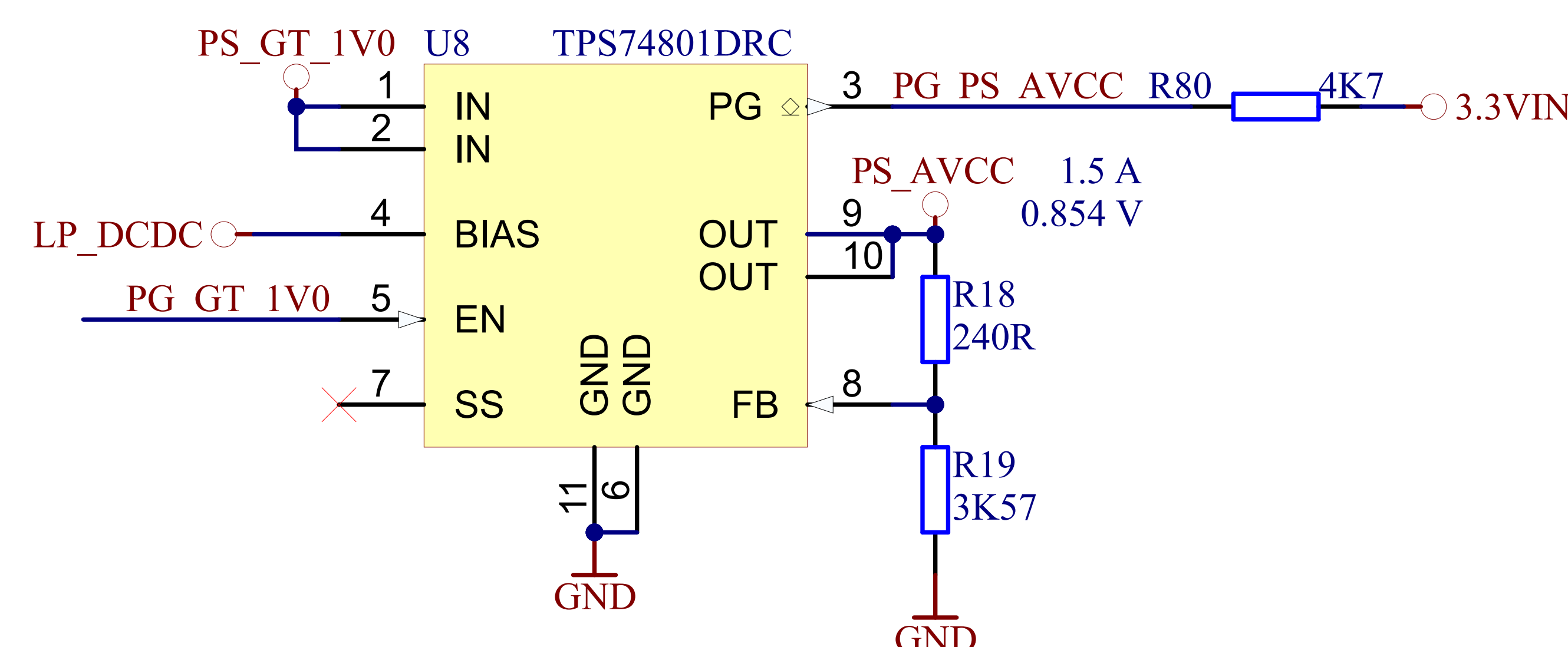
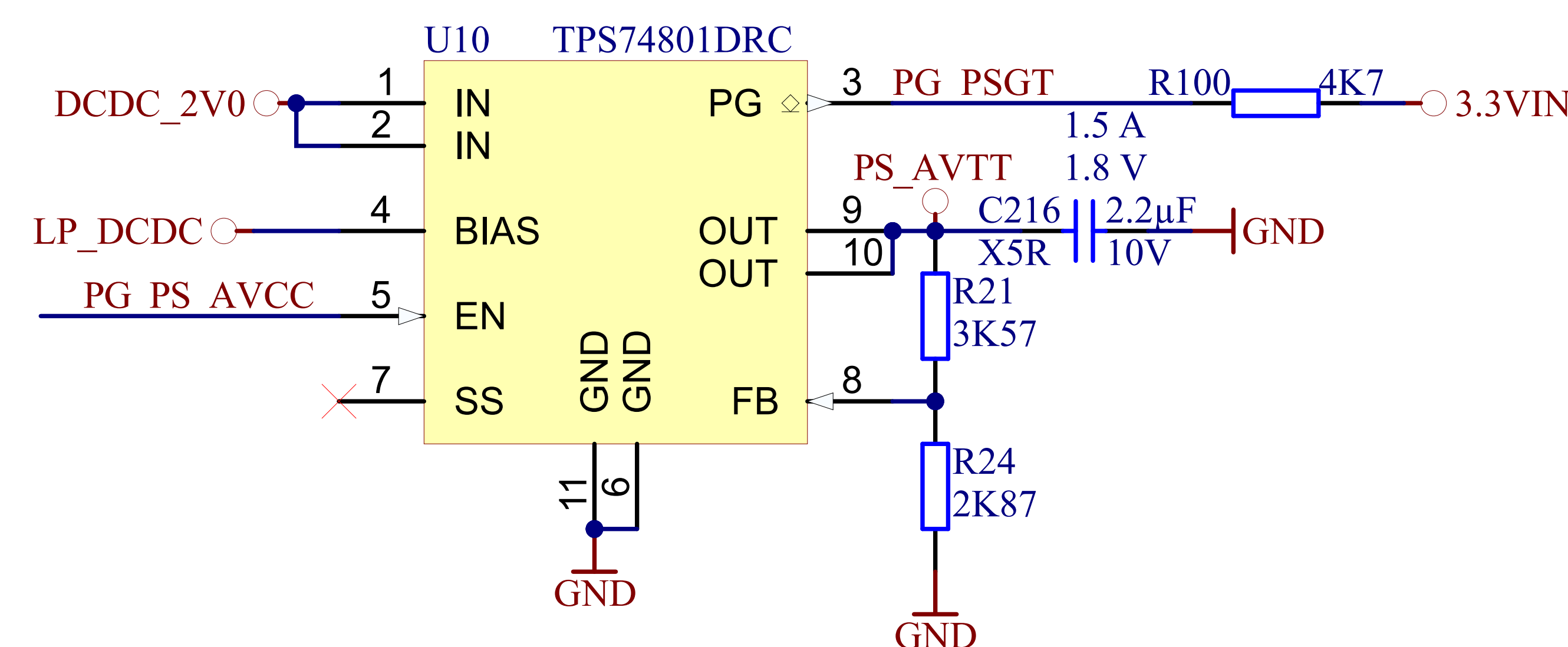
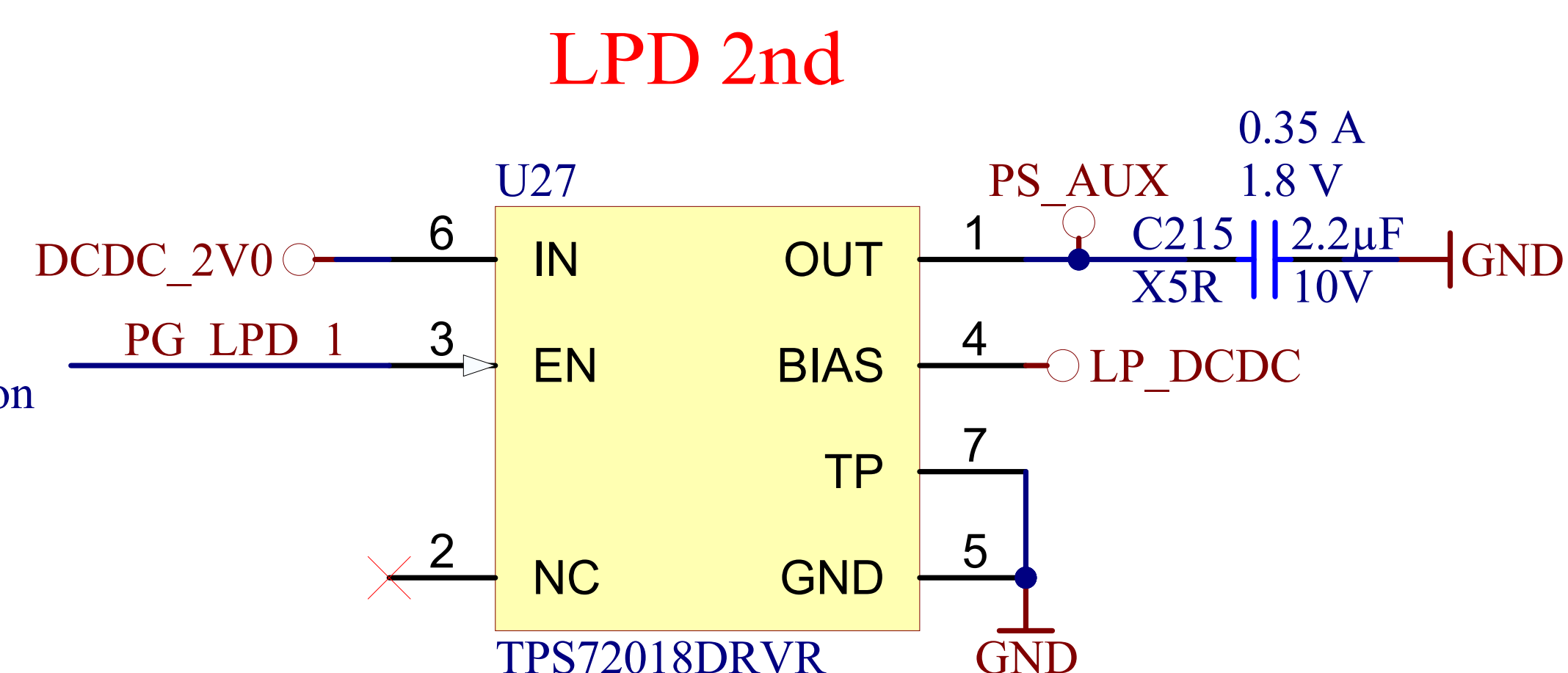
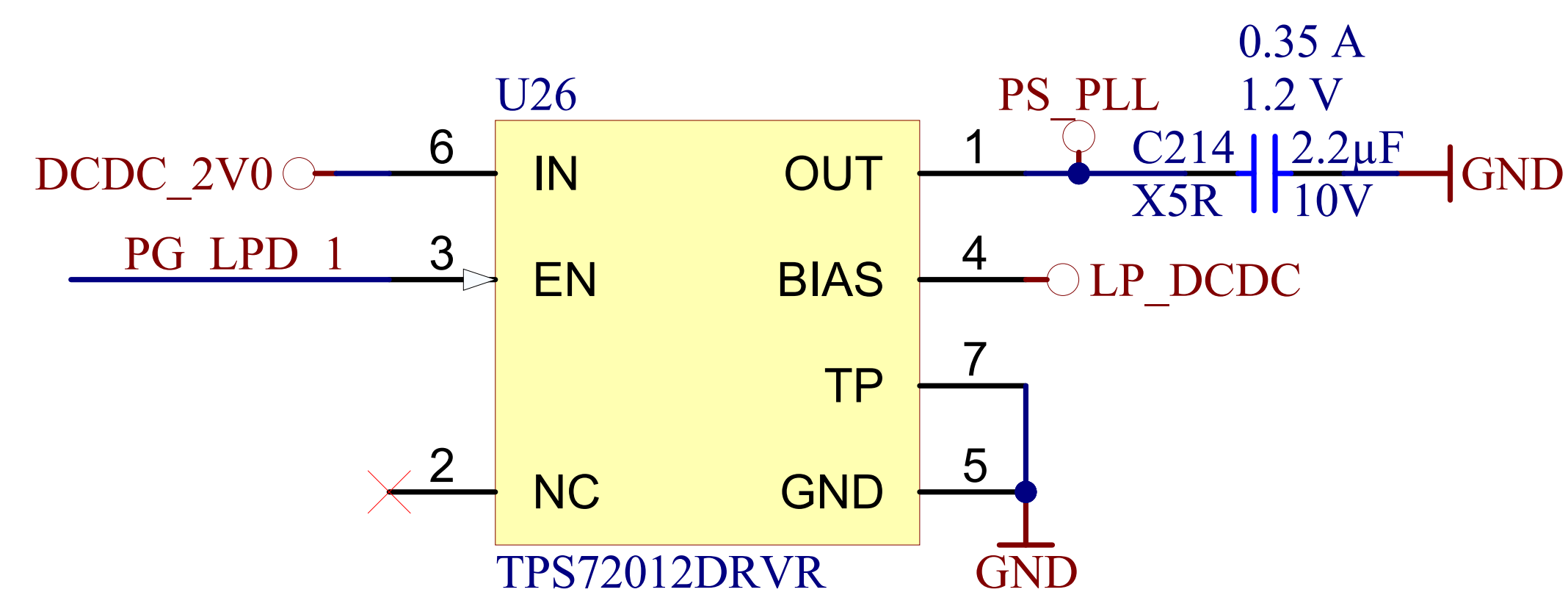


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Net Name	Voltage Rail	Low Detect
LP_0V85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V



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Rev.	02
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