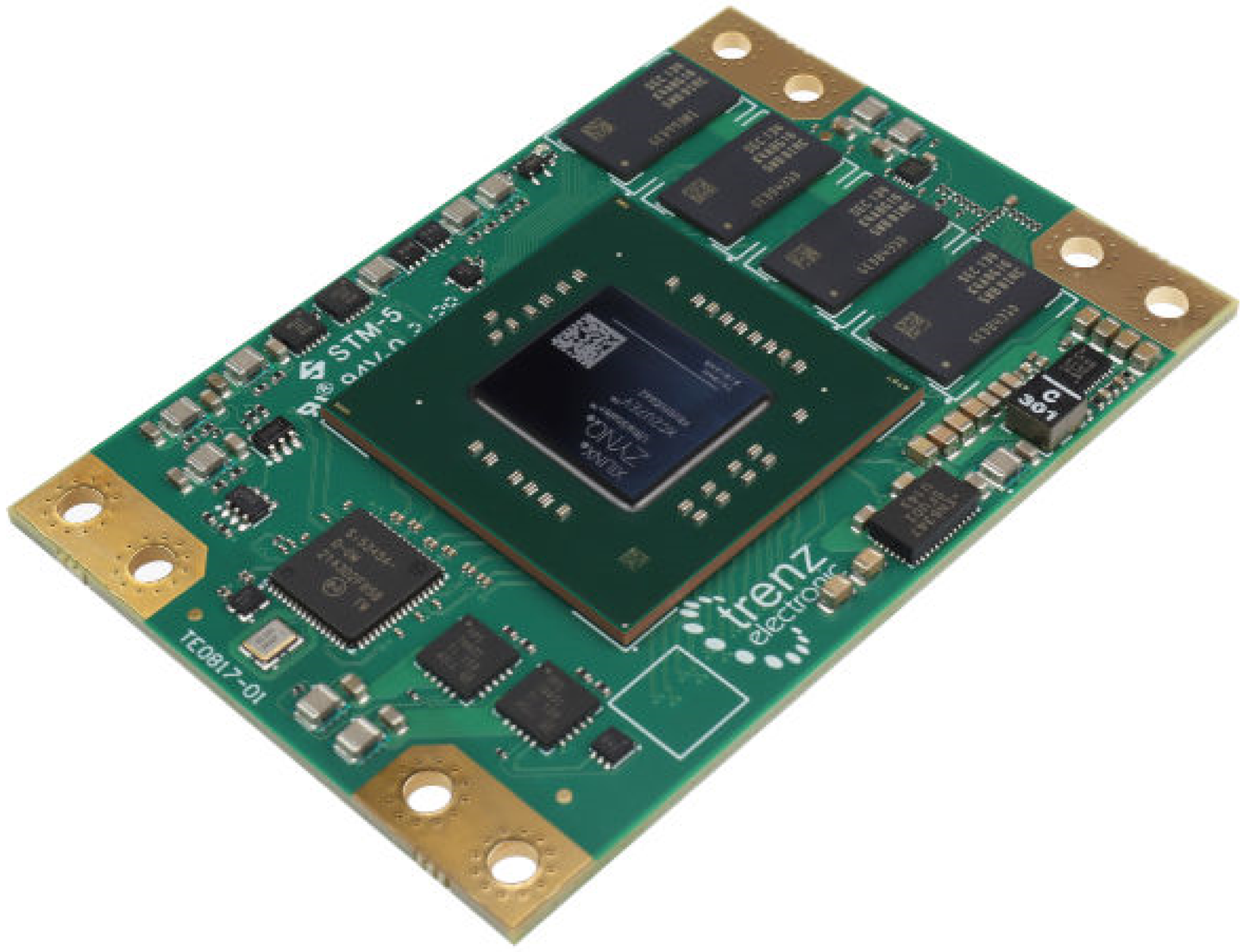
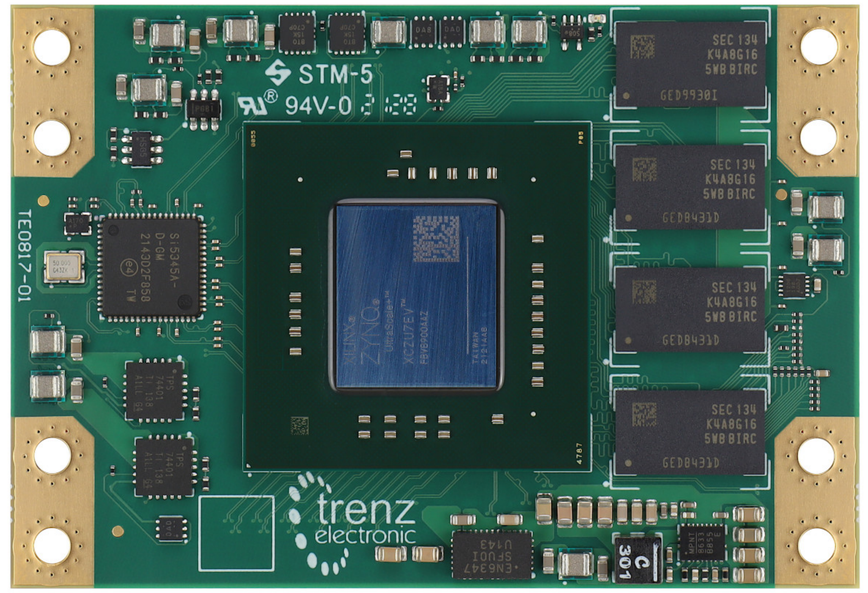
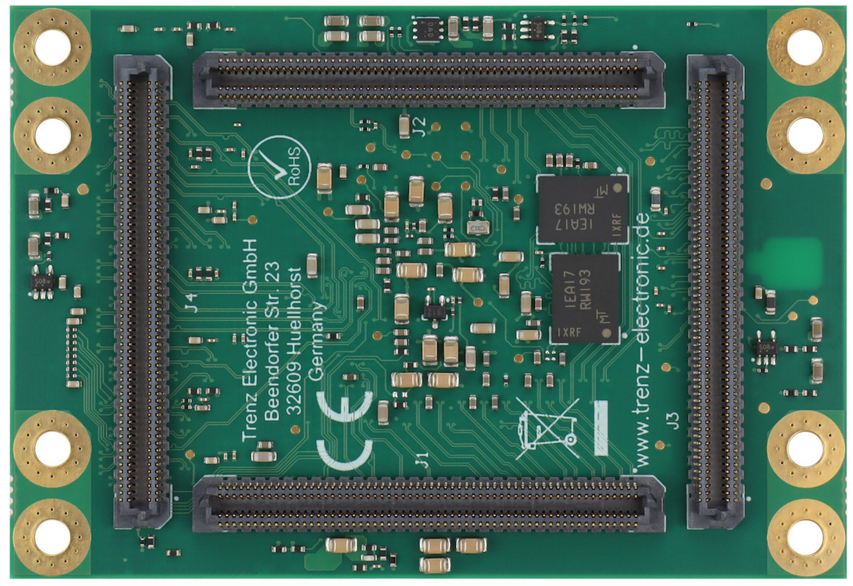






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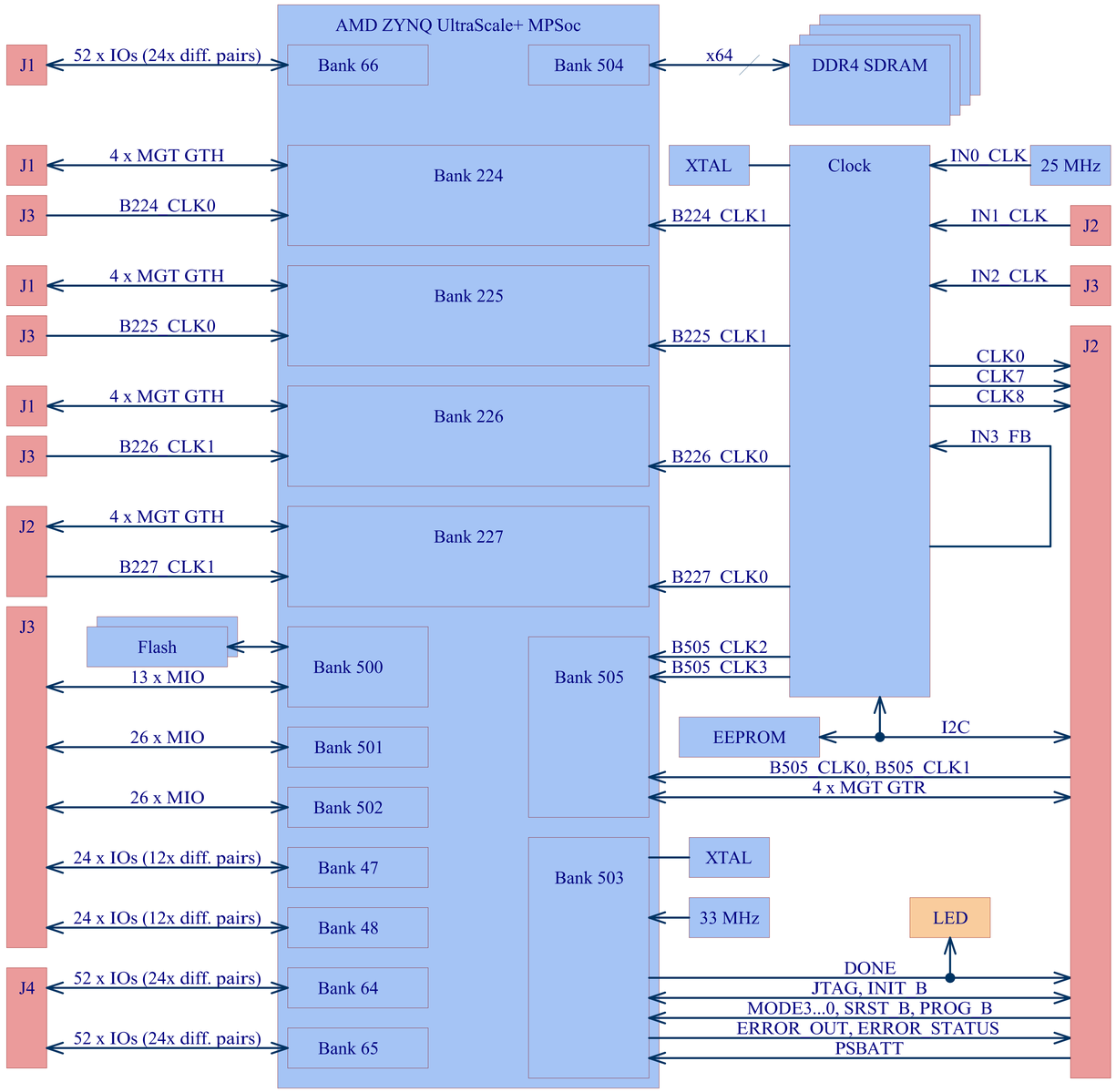
Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0817	
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REV	DATE	Description	
-01	2021-05	Initial revision	VT
	2022-05 2022-11	Changed DCDC U4 TPS548A28 to MPQ8633BGLE-Z Changed C132 100nF to 1nF Added Table with Supported Voltage Ranges	
-02	2024-04	1) Changed DCDC (U13) from EN6347QI to MPM3860GQW-Z and apdated according circuit.. 2) Connected DDR4-TEN signals together for U2A , U3A , U9A , and U12A and pulled them low via 499 Ohm resistor R127 . Added testpoint TP3 for signal DDR4-TEN . 3) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor R30 and changed voltage rail name PL_GT_1V35 to PL_GT_1V45 . 4) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R33 and R35 and changed voltage rail name PL_GT_1V05 to PL_GT_1V15 . 5) Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN . 6) Added capacitors C202 ... C205 for VTT voltage rail VTT . 7) Added resistors R124 (default: not fitted) and R125 to supply U4 VCC either from PL_DCIN or from 3.3VIN . 8) Changed resistor R76 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.3 A for U4 . 9) Changed inductor (L9) from XGL4030-301MEC to XGL5030-351MEC. 10) Added remote sense option (default: not fitted): 10.1) R126 for U30 . 10.2) R128 for U29 . 10.3) R129 for U31 . 11) Added decoupling capacitors: 11.1) C208 for U4 . 11.2) C211 , C212 , and C213 for U6 . 11.3) C216 for U10 . 11.4) C214 for U26 . 11.5) C215 for U27 . 11.6) C210 for U34 . 11.7) C196 for U39 . 11.8) C197 for U40 . 11.9) C198 for U42 . 11.10) C199 for U41 . 11.11) C200 for U44 . 11.12) C201 , C206 , and C207 for U1N . 12) Added pull-up resistors for HOLD (R130) and WP (R131) signals for Flash U7A . 13) Added pull-up resistors for HOLD (R132) and WP (R133) signals for Flash U17A . 14) Changed capacitor (C132) from 1 nF, X7R to 1.2 nF, NP0. 15) Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201. 16) Changed 100 nF capacitors (C37 , C95 , C96 , C130 , and C131) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402. 17) Changed capacitor (C76 , C77 , C134 , C195) from 1 µF, 16 V to 2.2 µF, 10 V. 18) Changed capacitor (C129 , C140 , C141 , C142 , C143 , C144 , C145 , C146 , C147 , C148 , C153) from 10 µF, 16 V to 22 µF, 10 V. 19) Changed 22 uF capacitor (C70 , C73 , C74 , C75) from 0805 to 0603. 20) Changed 22 uF capacitor (C78 , C80 , C81 , C82 , C83 , C84 , C85 , C86 , C87 , C110 , C152 , C154 , C178) from 6.3 V to 10 V. 21) Changed 100 Ohm resistors (R7 , R10) from 0201, 0.05 W to 0402, 0.063 W. 22) Changed resistor R77 from 12 kOhm to 10 kOhm. 23) Changed resistors R41 and R58 from 2 kOhm to 2.49 kOhm. 24) Added testpoints TP4 , TP10 , TP11 , TP13 , TP14 , TP19 , TP21 , TP22 , TP33 ... TP72 . 25) Added UKCA logo. 26) Updated from library. 27) Changed signal trace length. 28) Updated documentation.	ED

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Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
3.3VIN	IN	3.3 V	+/- 5 %	Micromodule Power	-
PL_DCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Programmable Logic
LP_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	Low-Power Domain
GT_DCDC	IN	3.3 V - 5.0 V	+/- 3 %	Micromodule Power	GTH/GTY Transceiver
DCDCIN	IN	3.3 V - 5.0 V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	-
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3 V	+/- 5 %	PLL Core Power	-
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Processing System
DDR4_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x69	-
EEPROM U11	0x50	-

Legend:

- B2B Connector
- LED Interface
- On-board Components

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DDR4-TERM	ZU_GT_2	ZU_PS_POWER	POWER_2	POWER_4

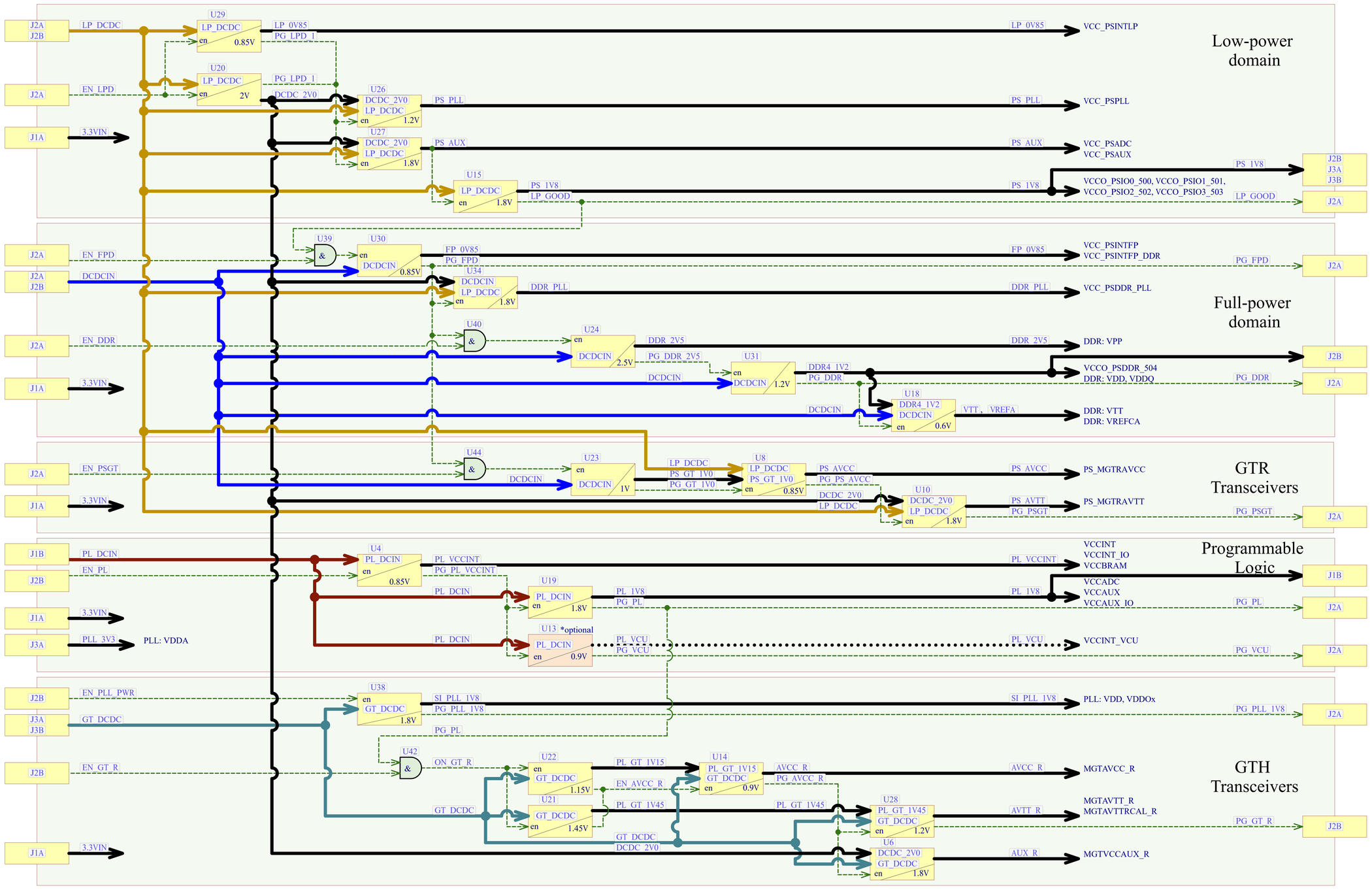
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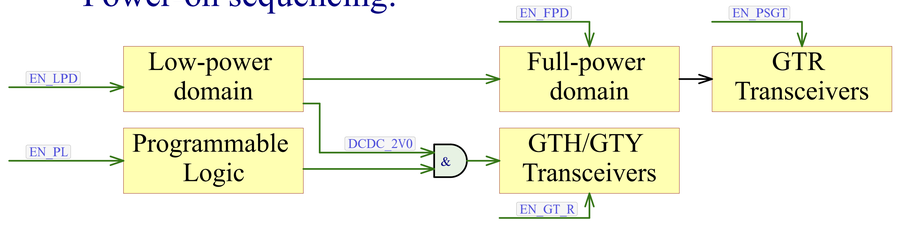
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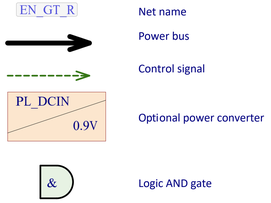
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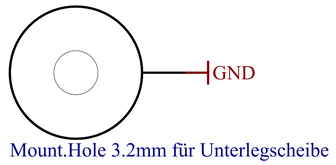




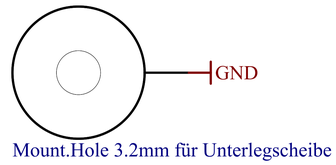
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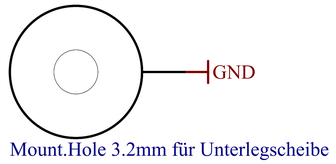
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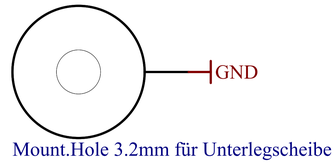
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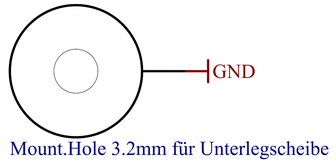
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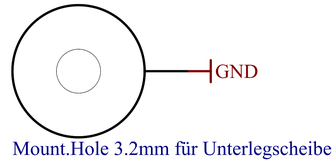
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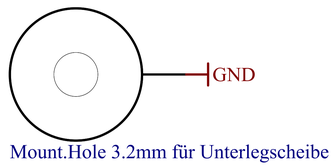
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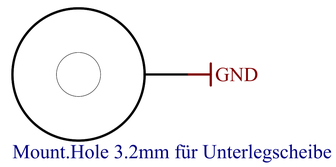
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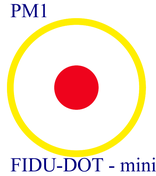


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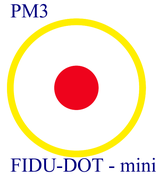
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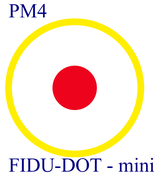
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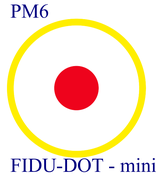
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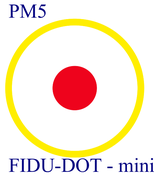
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PM6


FIDU-DOT - mini

PM5


FIDU-DOT - mini

Serial1

Serial

Serialnumber 6,3 x 6.3mm

LOGO1

TE Logo PRINT Layer

LOGO PRINT

MECH1

TE Address Overlay

LOGO ADDRESS

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

RoHS

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WEEE

WEEE Logo on Top Overlay

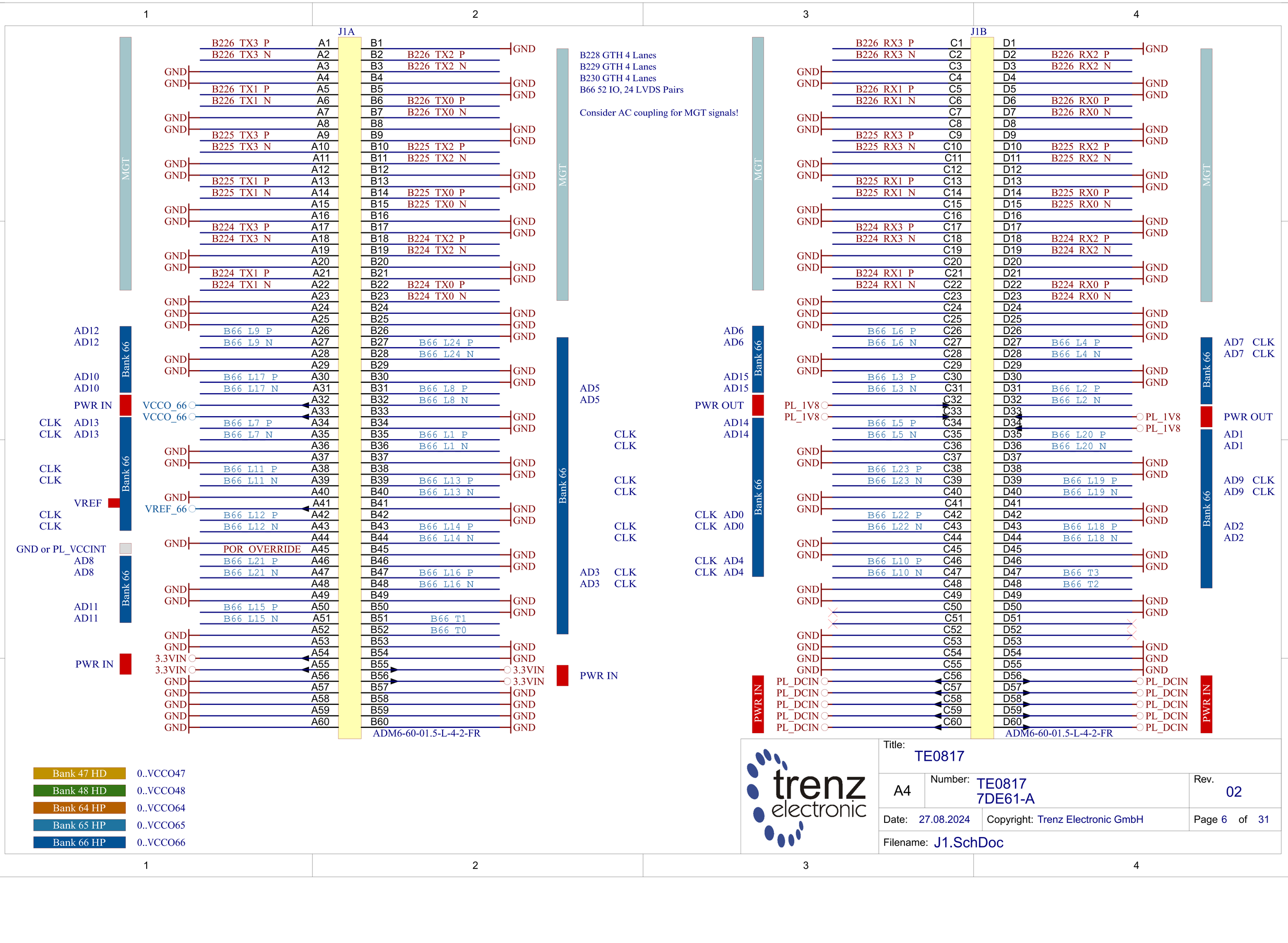
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Checked by:	MT
Assembly variant:	7DE61-A
Created by:	VG
Modified by:	VG
Modified at:	2025-12-17

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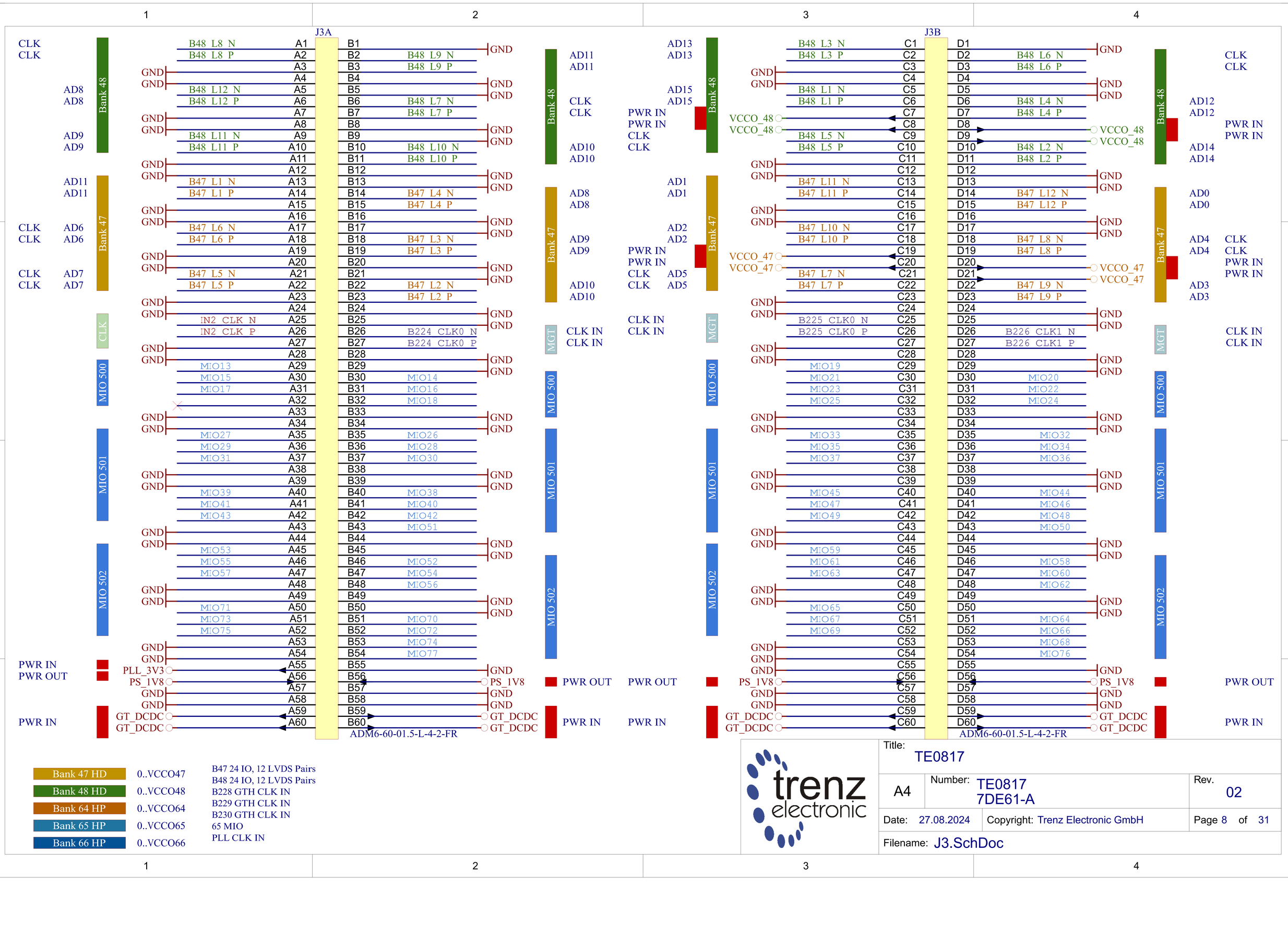
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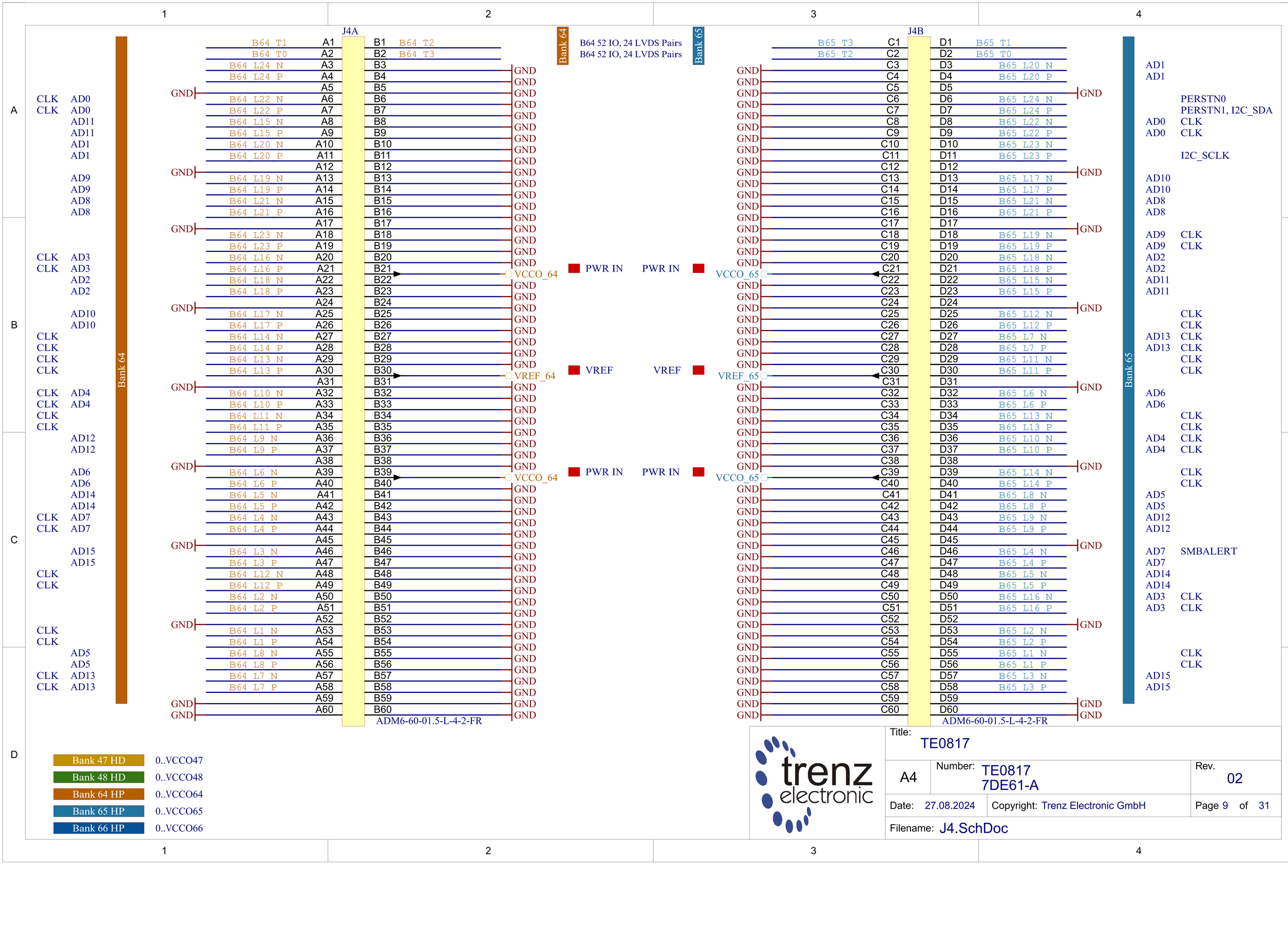


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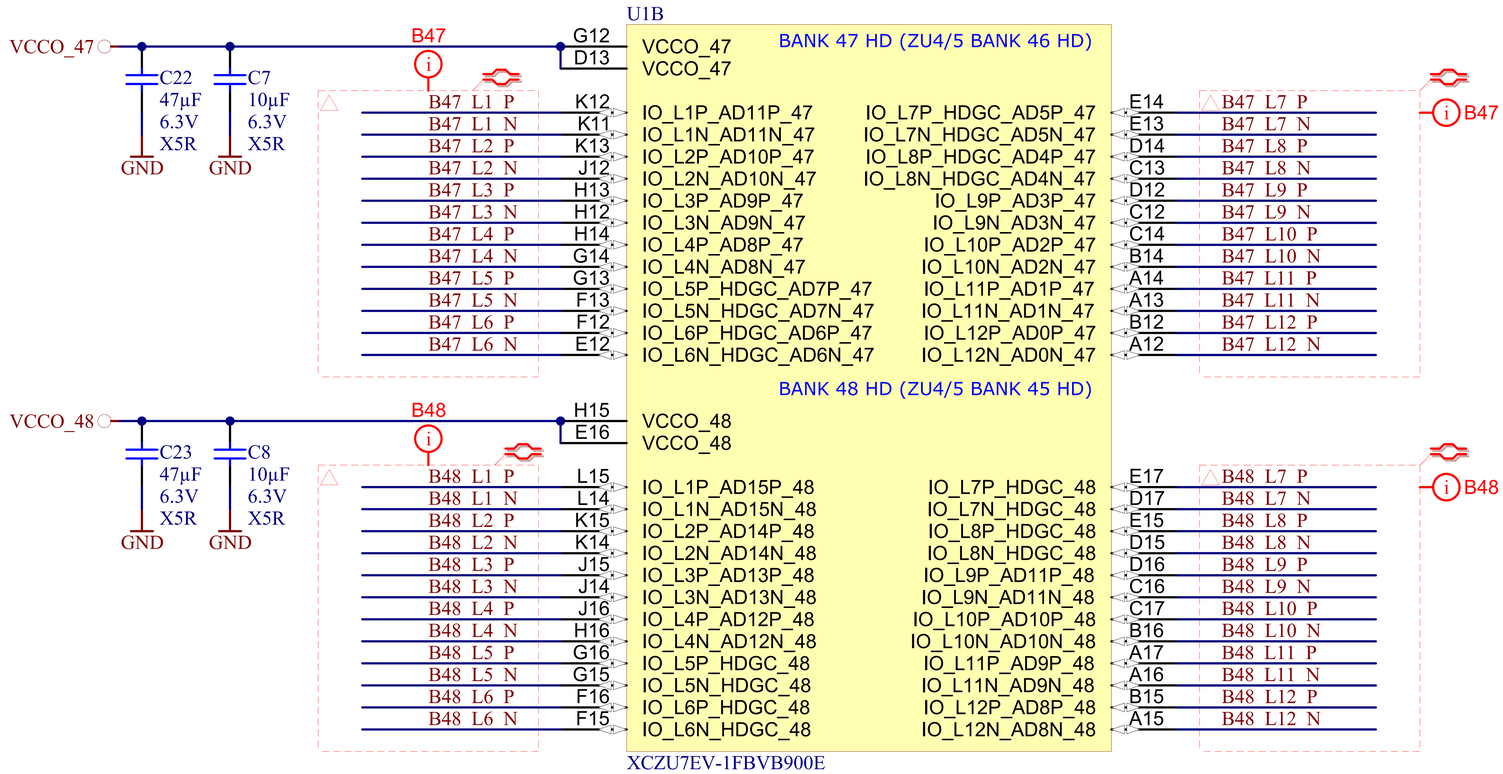


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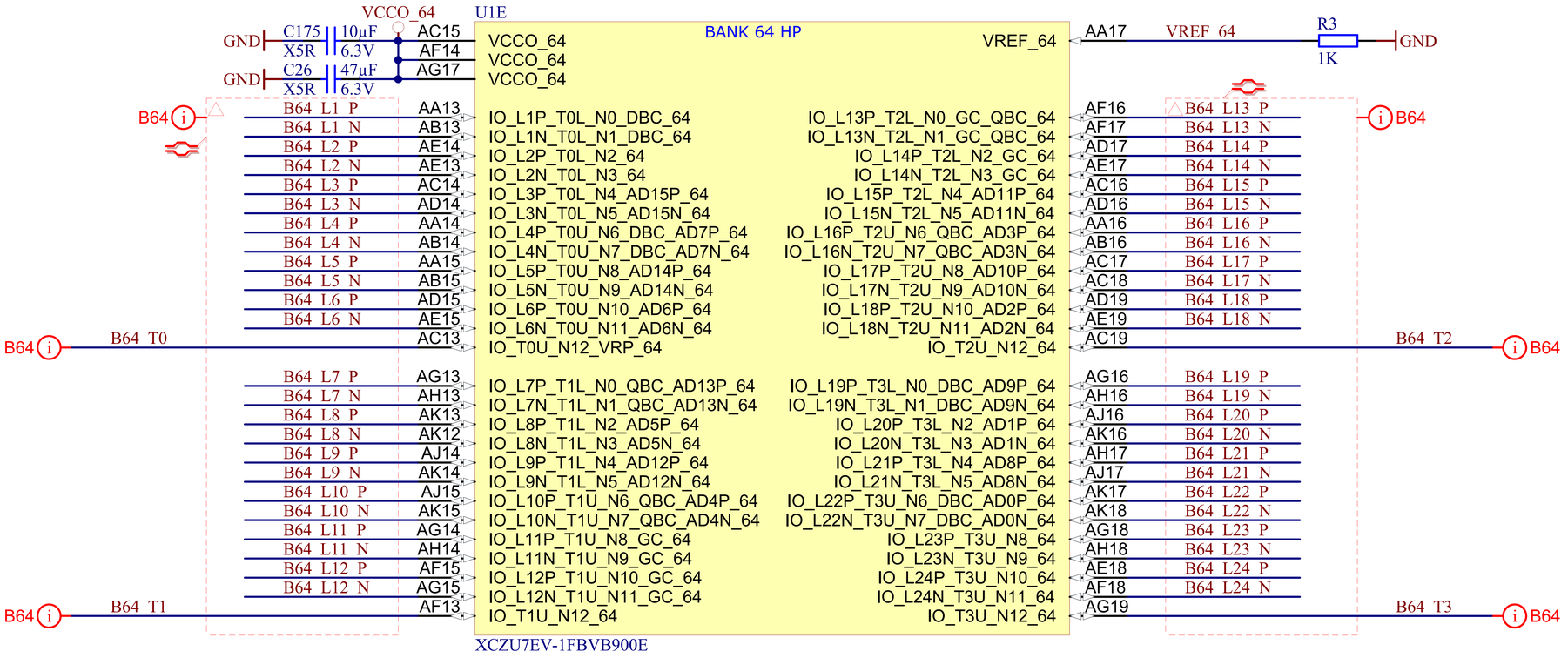
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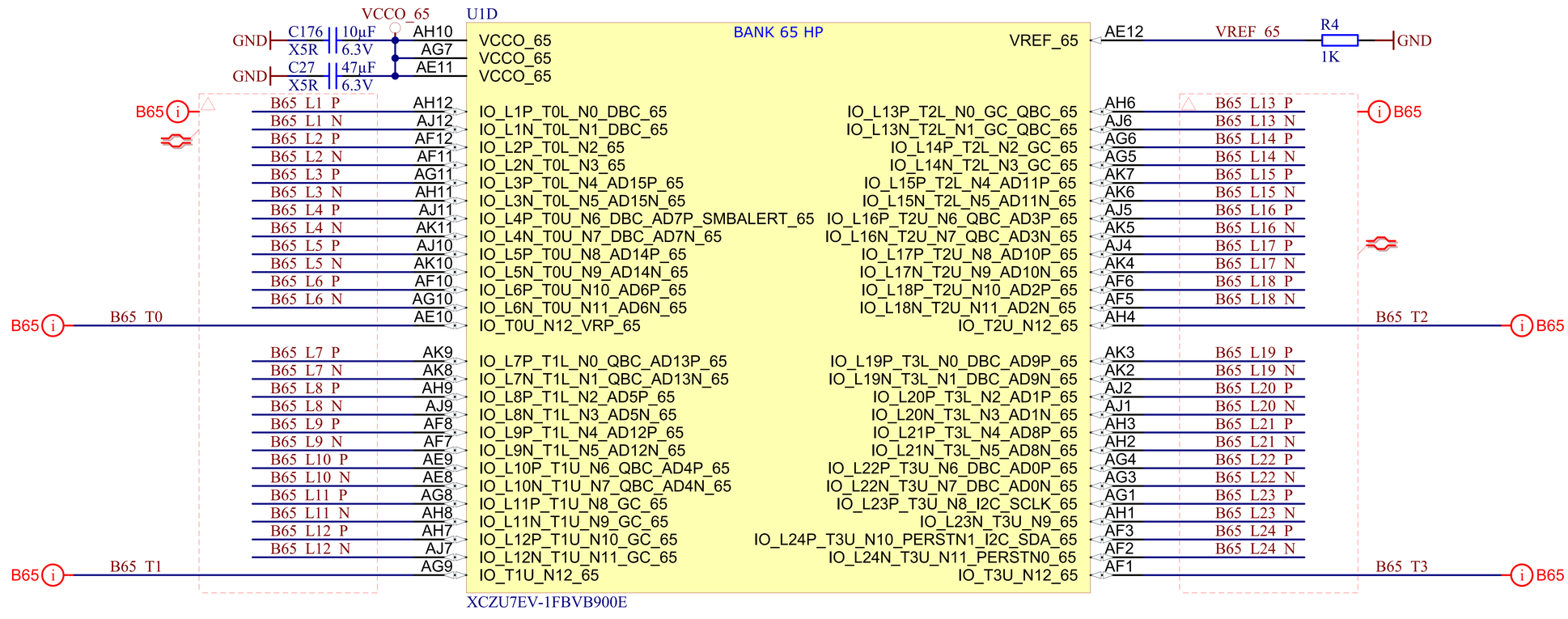
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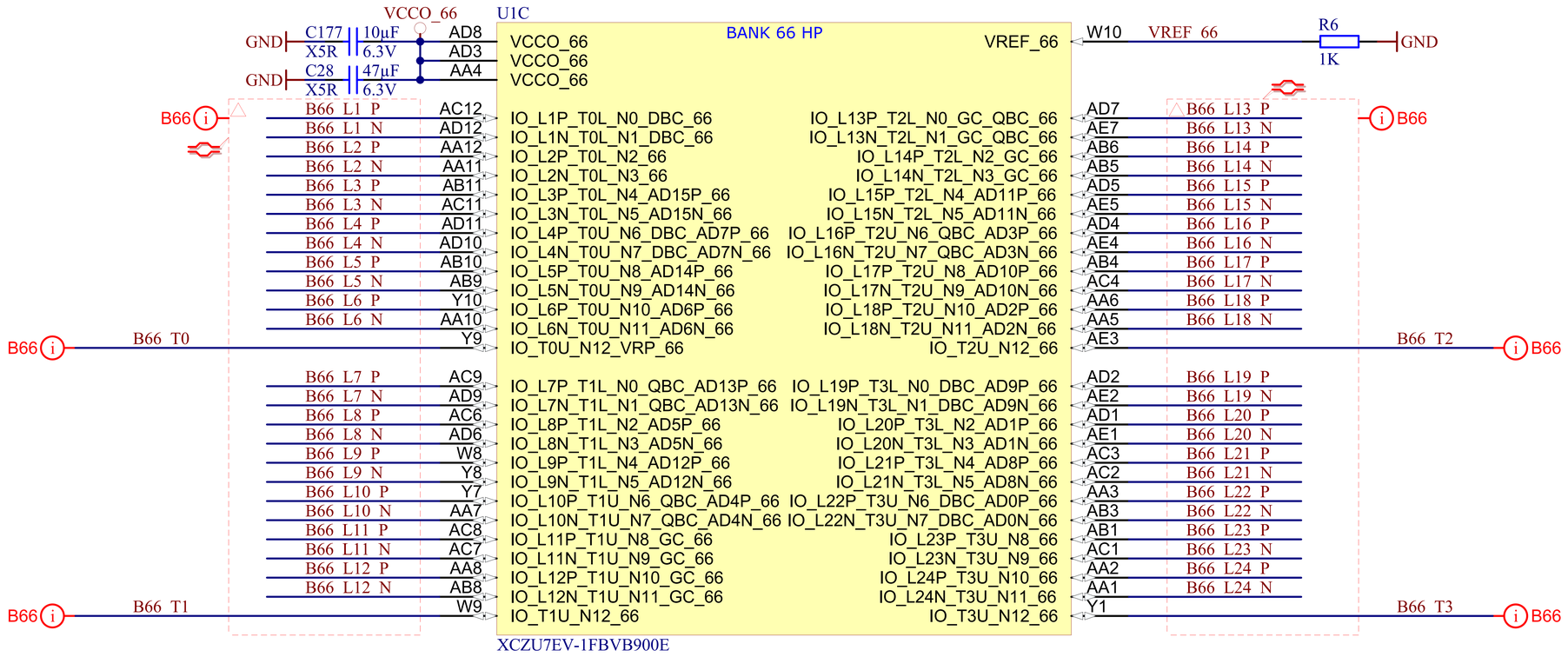
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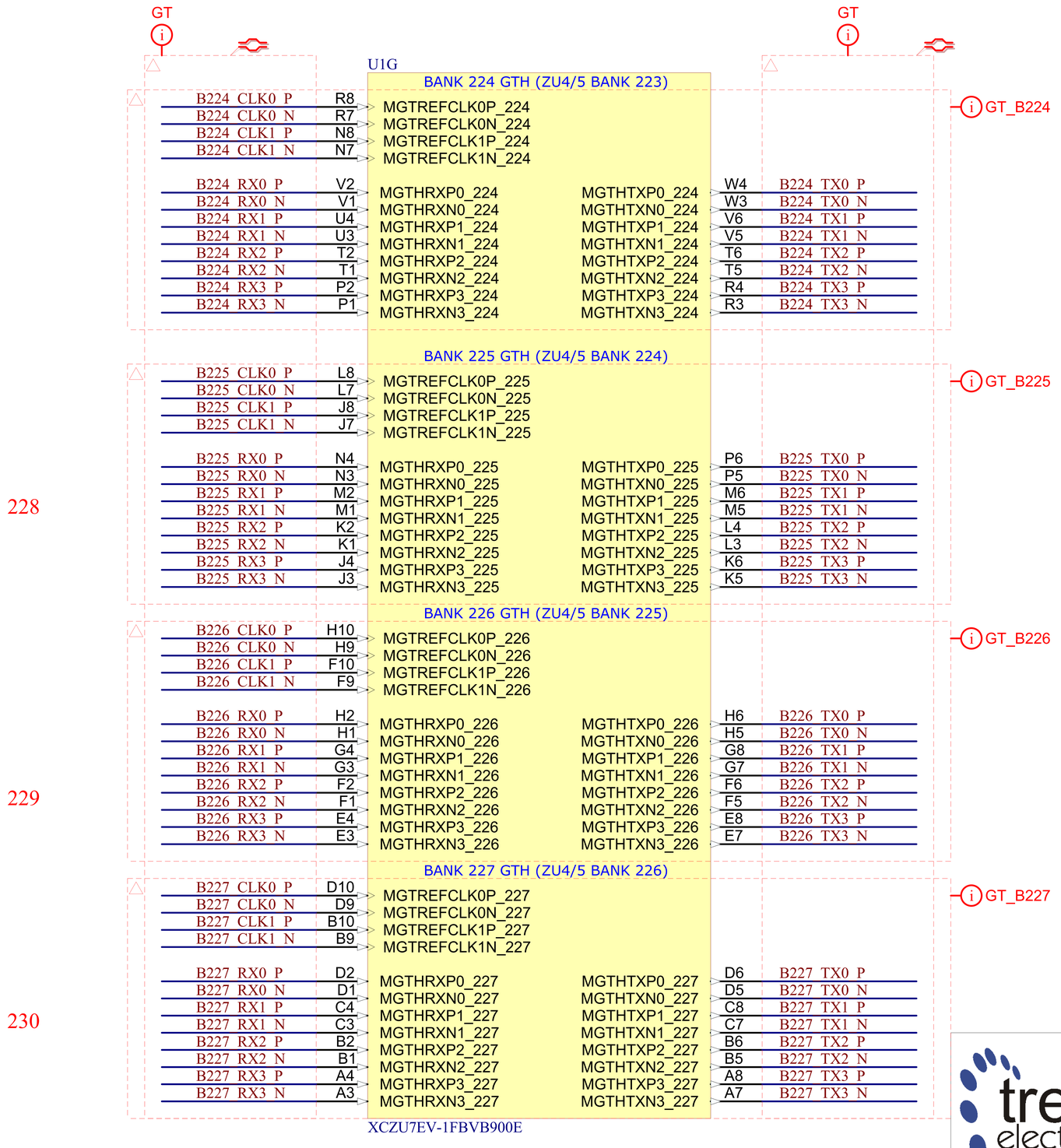
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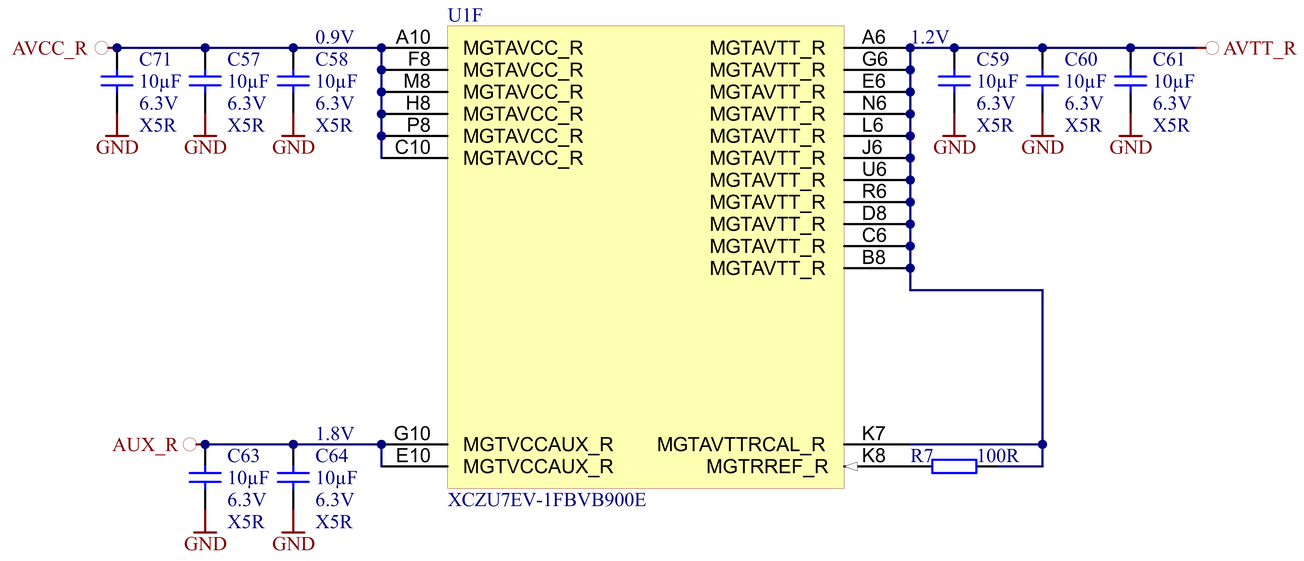
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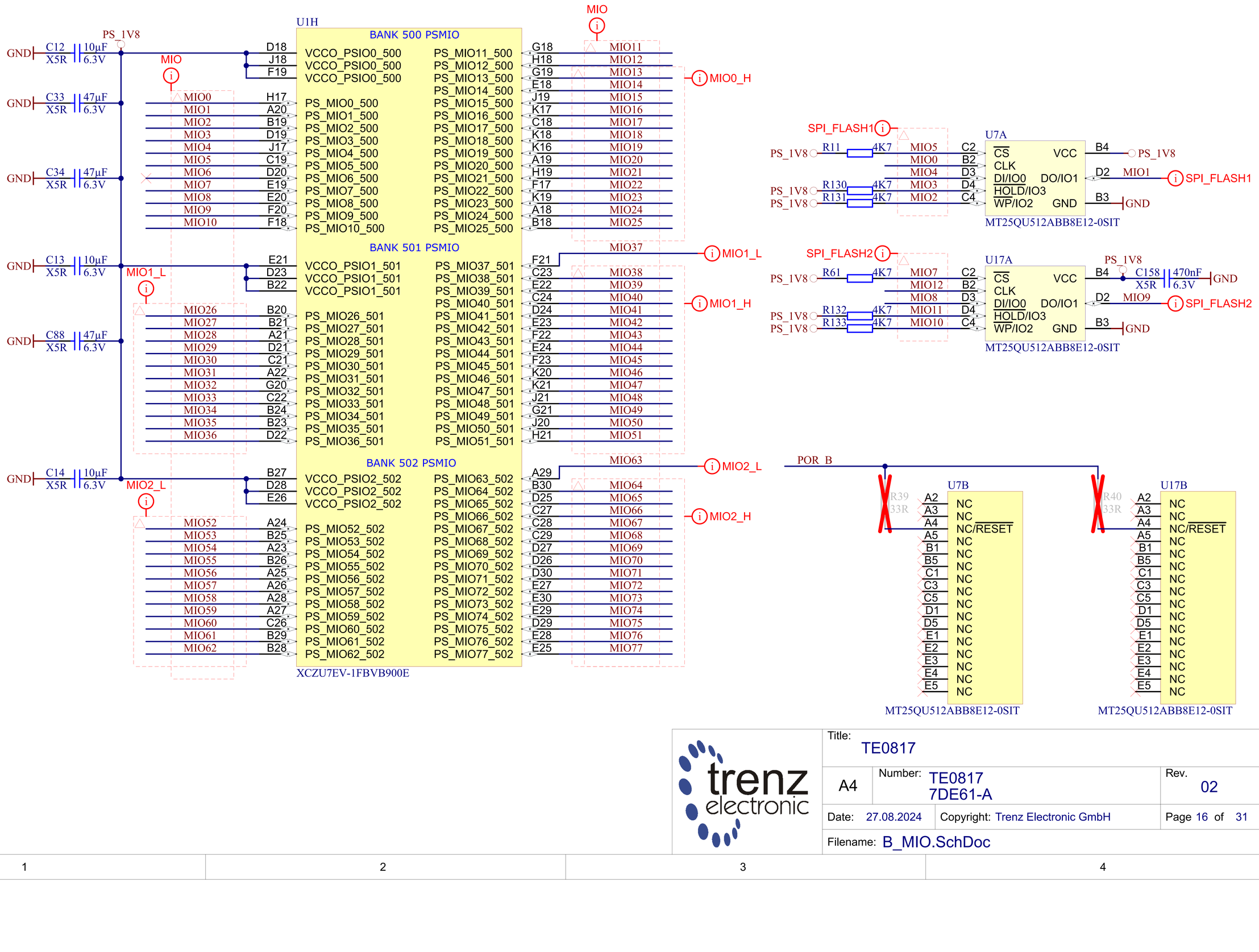
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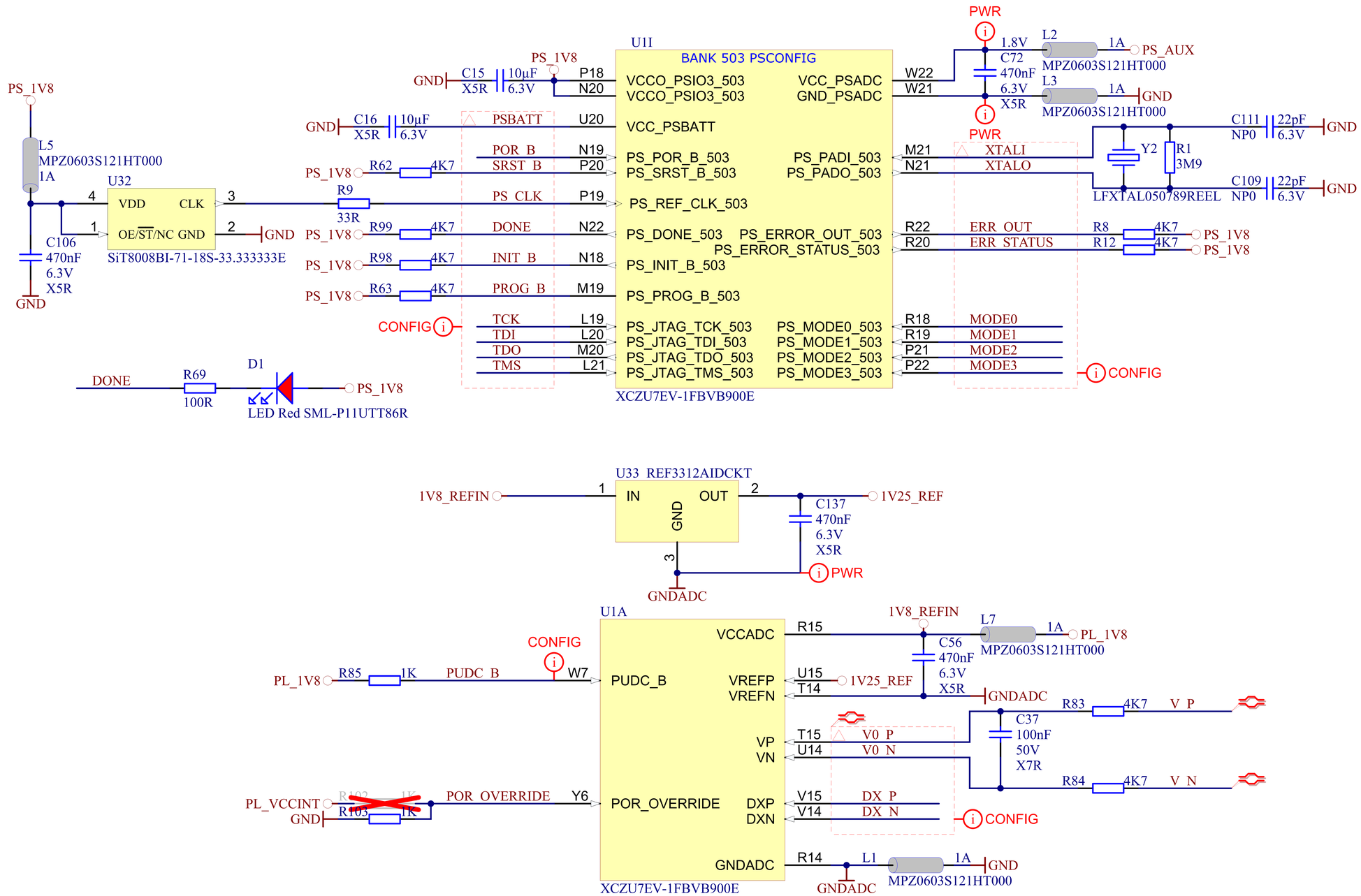
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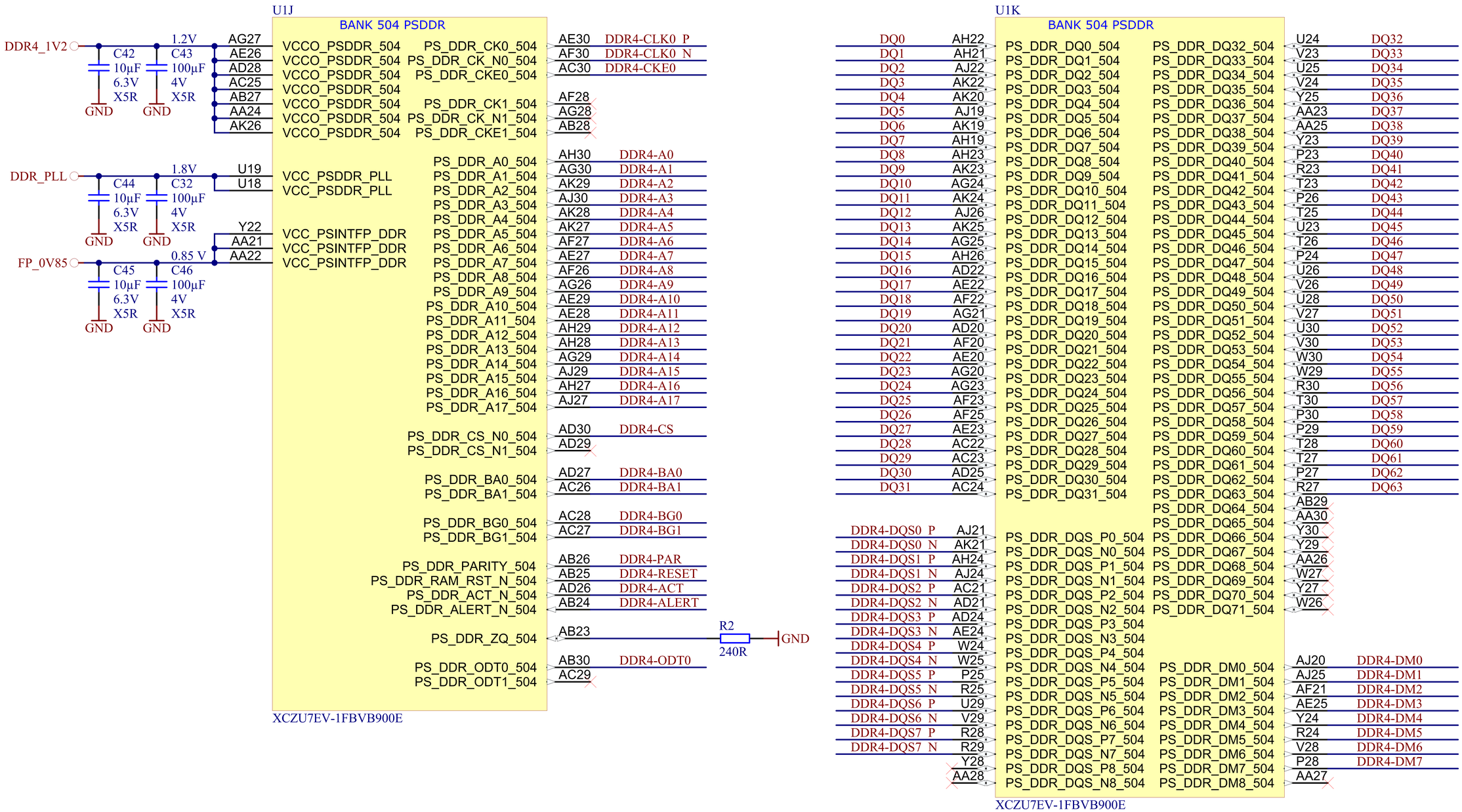
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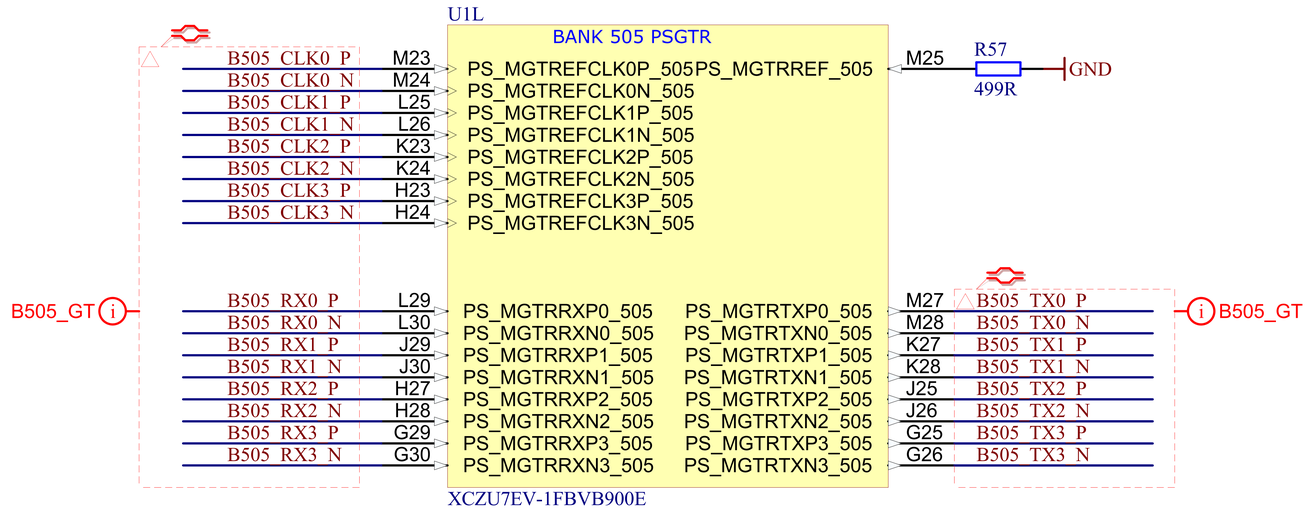
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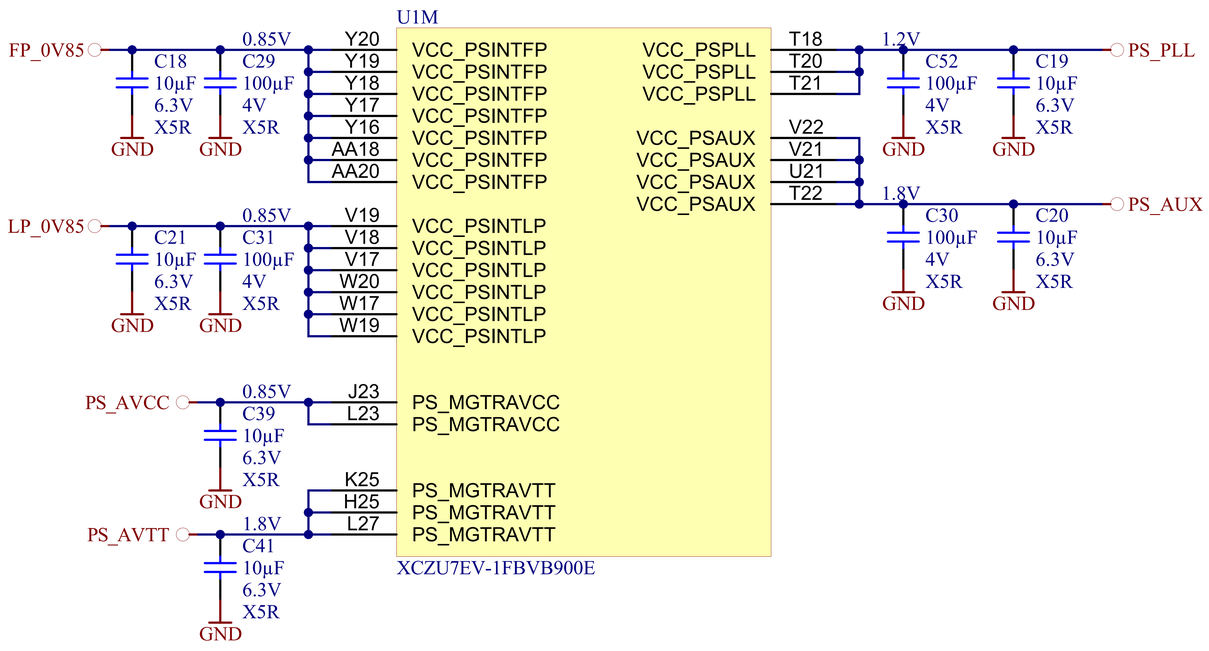
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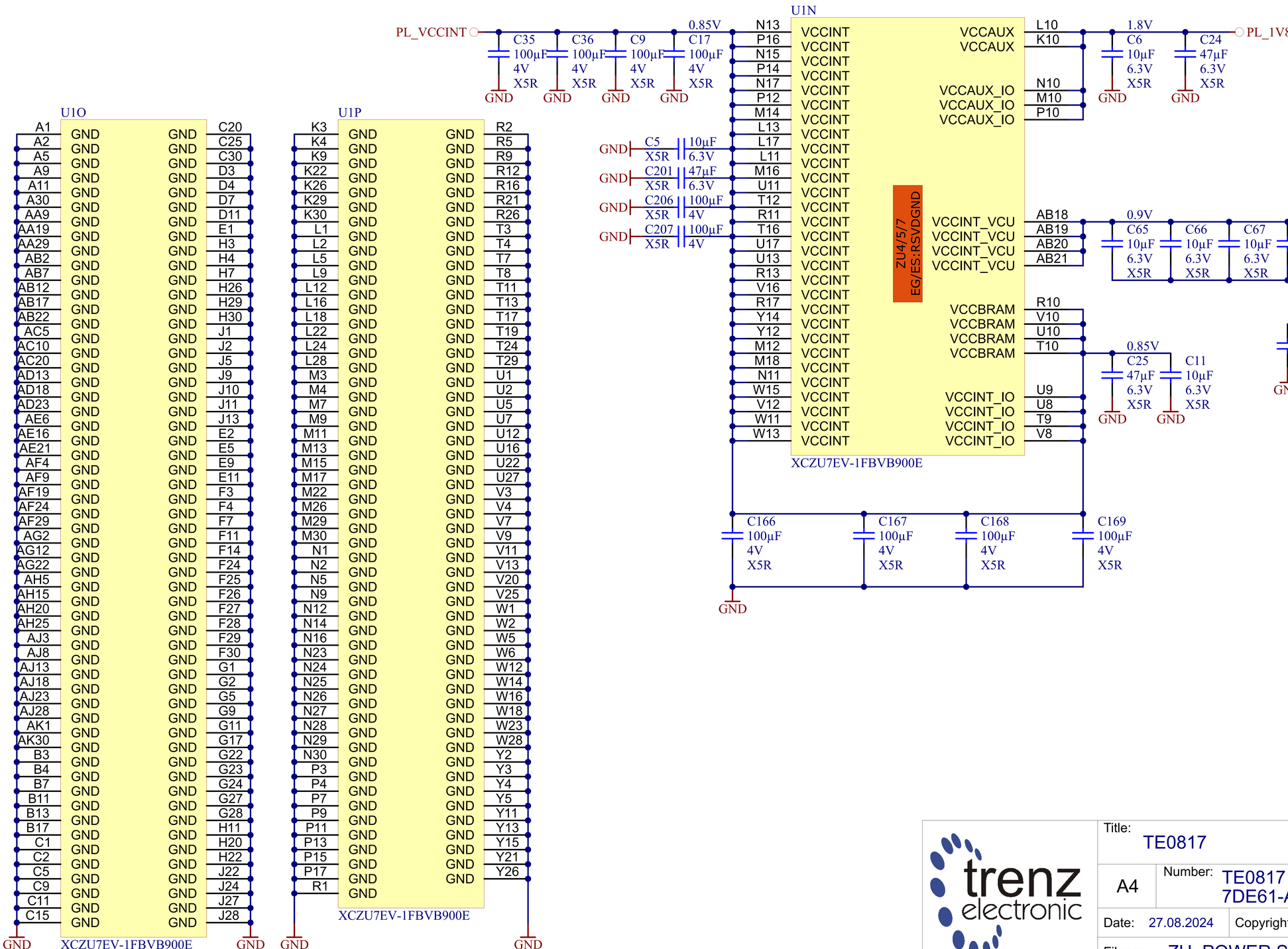
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	Date: 27.08.2024	Copyright: Trenz Electronic GmbH	Page 18 of 31
	Filename: PS_DDR.SchDoc		



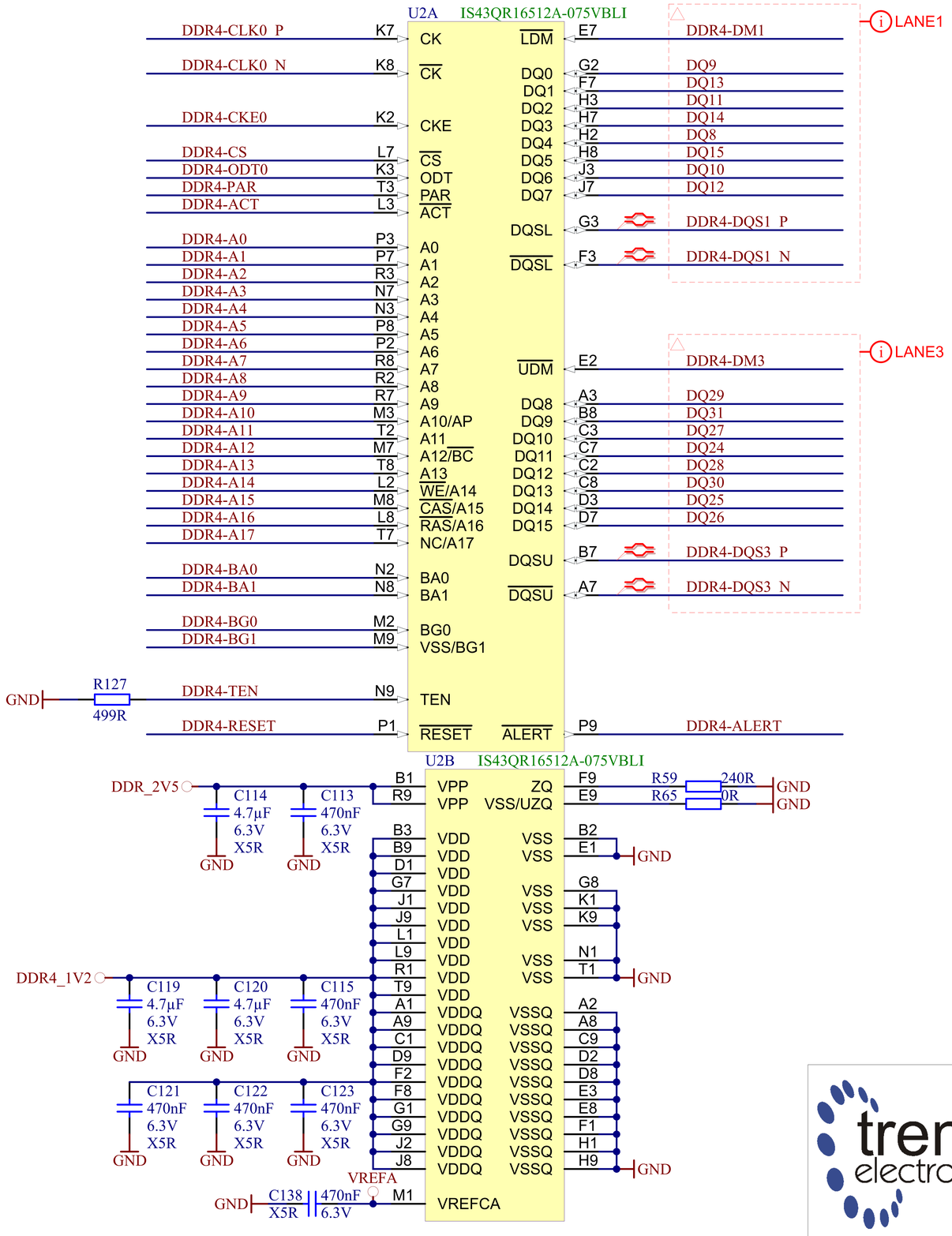
Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
Date: 27.08.2024	Copyright: Trenz Electronic GmbH		Page 19 of 31
Filename: B_PS_GT.SchDoc			



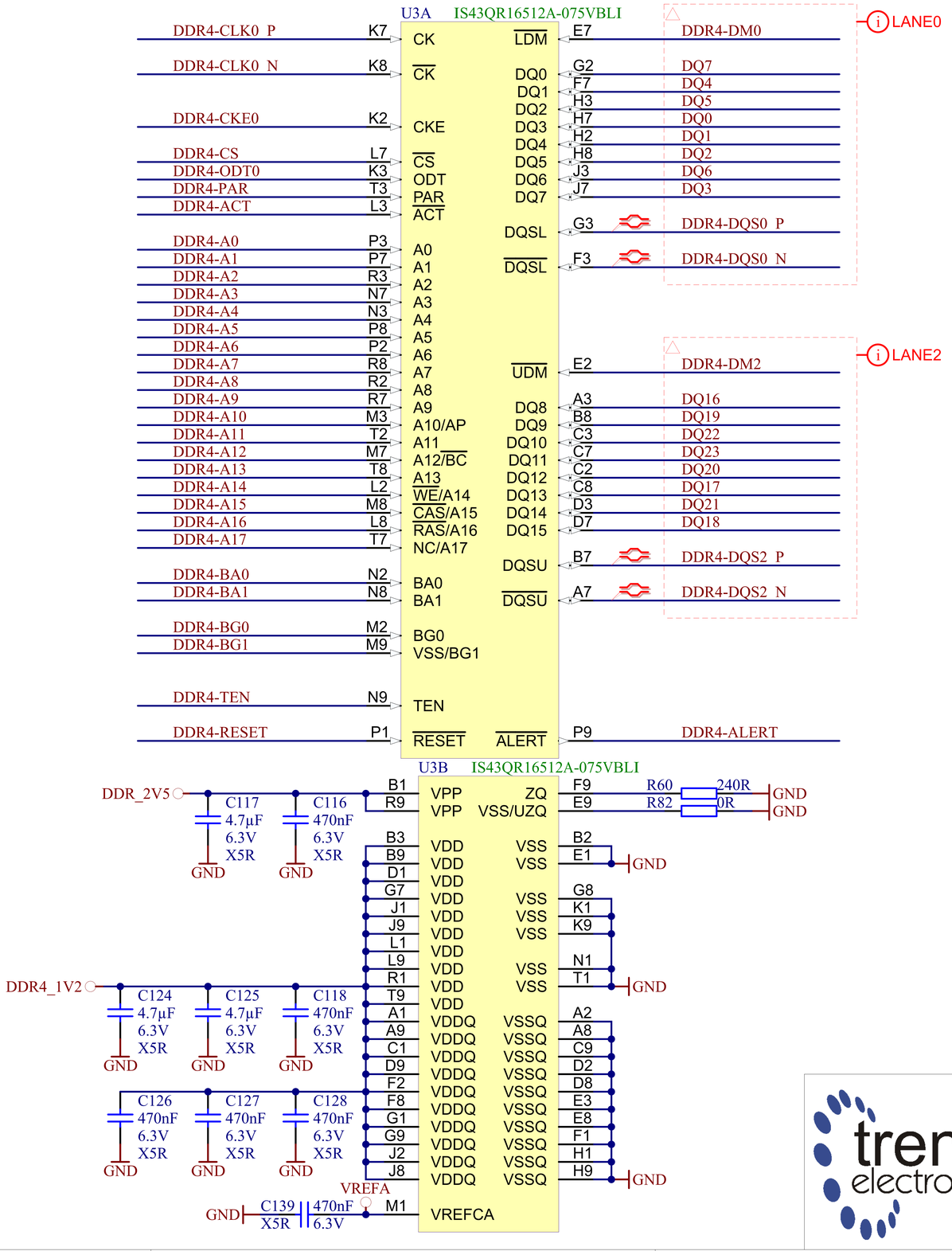
trenz electronic	Title: TE0817		
	A4	Number: TE0817 7DE61-A	Rev. 02
	Date: 27.08.2024	Copyright: Trenz Electronic GmbH	Page 20 of 31
	Filename: ZU_PS_POWER.SchDoc		



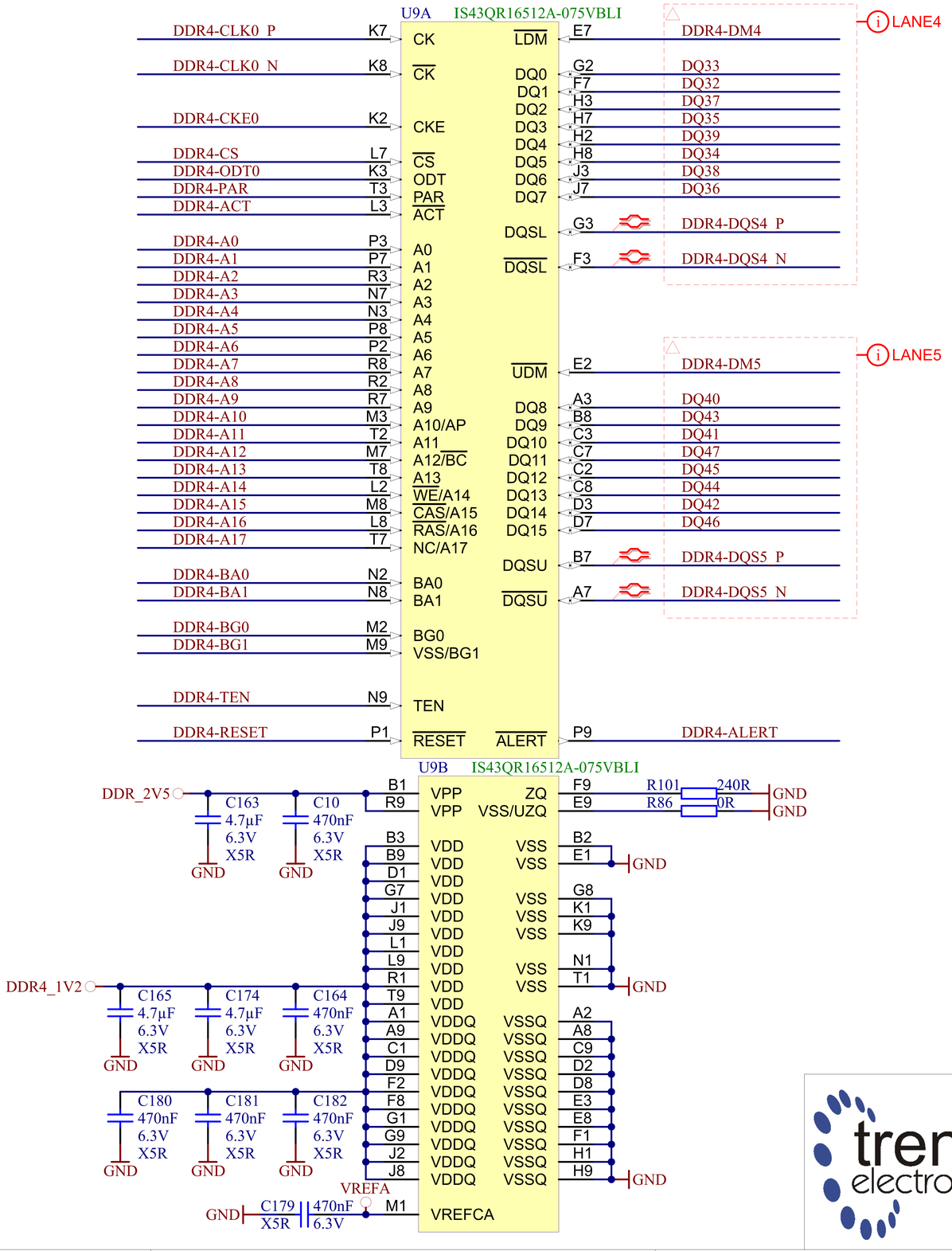
Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
Date: 27.08.2024	Copyright: Trenz Electronic GmbH		Page 21 of 31
Filename: ZU_POWER.SchDoc			



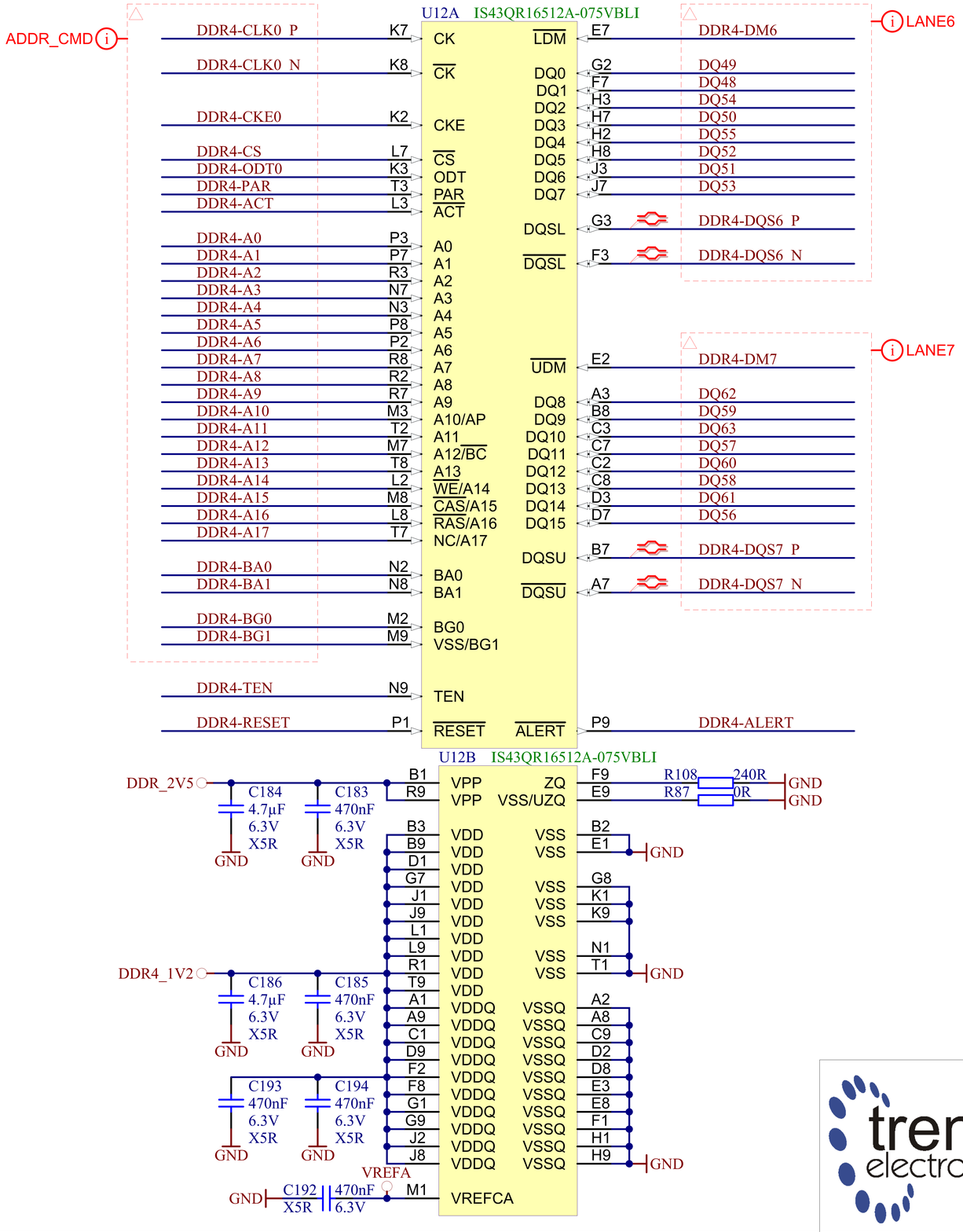
Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
Date: 27.08.2024	Copyright: Trenz Electronic GmbH		Page 22 of 31
Filename: DDR4-RAM.SchDoc			

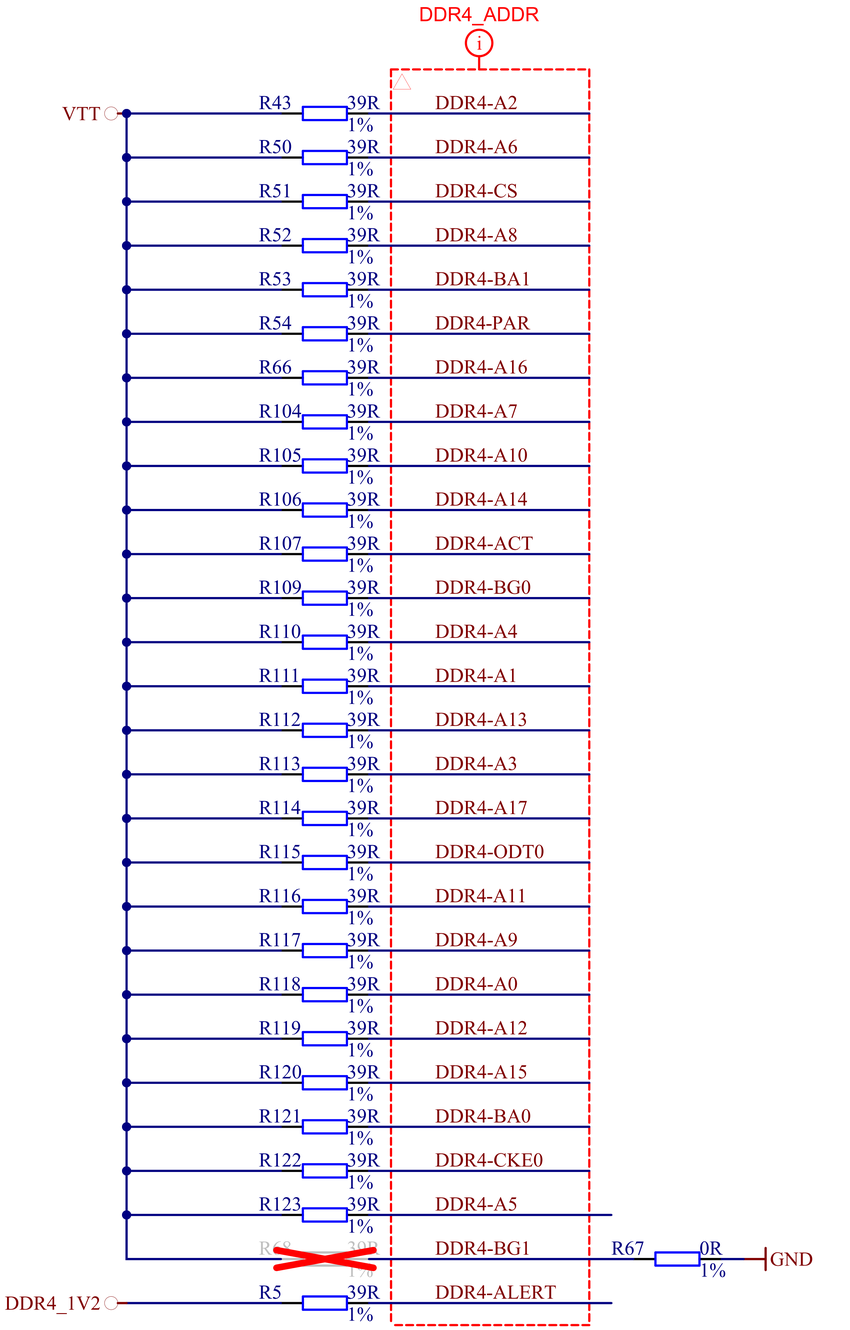


Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
Date: 27.08.2024	Copyright: Trenz Electronic GmbH		Page 23 of 31
Filename: DDR4-RAM_2.SchDoc			

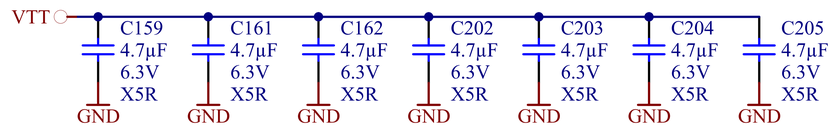


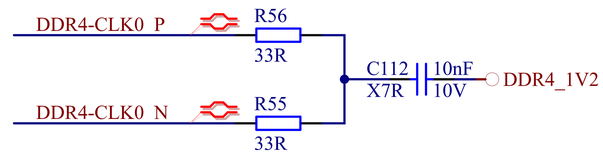
Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
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Filename: DDR4-RAM_3.SchDoc			


U12A IS43QR16512A-075VBLI
ADDR_CMD
DDR4-CLK0_P
DDR4-CLK0_N
DDR4-CKE0
DDR4-CS
DDR4-ODT0
DDR4-PAR
DDR4-ACT
DDR4-A0
DDR4-A1
DDR4-A2
DDR4-A3
DDR4-A4
DDR4-A5
DDR4-A6
DDR4-A7
DDR4-A8
DDR4-A9
DDR4-A10
DDR4-A11
DDR4-A12
DDR4-A13
DDR4-A14
DDR4-A15
DDR4-A16
DDR4-A17
DDR4-BA0
DDR4-BA1
DDR4-BG0
DDR4-BG1
DDR4-TEN
DDR4-RESET
CK
CK
CKE
CS
ODT
PAR
ACT
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
WE/A14
CAS/A15
RAS/A16
NC/A17
BA0
BA1
BG0
VSS/BG1
TEN
RESET
ALERT
DDR4-ALERT
LDM
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQSL
DQSL
UDM
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQSU
DQSU
DDR4-DM6
DDR4-DQS6_P
DDR4-DQS6_N
LANE6
DDR4-DM7
DDR4-DQS7_P
DDR4-DQS7_N
LANE7
U12B IS43QR16512A-075VBLI
DDR_2V5
DDR4_1V2
C184 4.7µF 6.3V X5R
C183 470nF 6.3V X5R
C186 4.7µF 6.3V X5R
C185 470nF 6.3V X5R
C193 470nF 6.3V X5R
C194 470nF 6.3V X5R
C192 470nF 6.3V X5R
GND
VREFA
VPP
VPP
VDD
VSS
VDDQ
VSSQ
ZQ
VSS/UZQ
R108 240R
R87 0R
GND
Title: TE0817
A4
Number: TE0817 7DE61-A
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Filename: DDR4-RAM_4.SchDoc



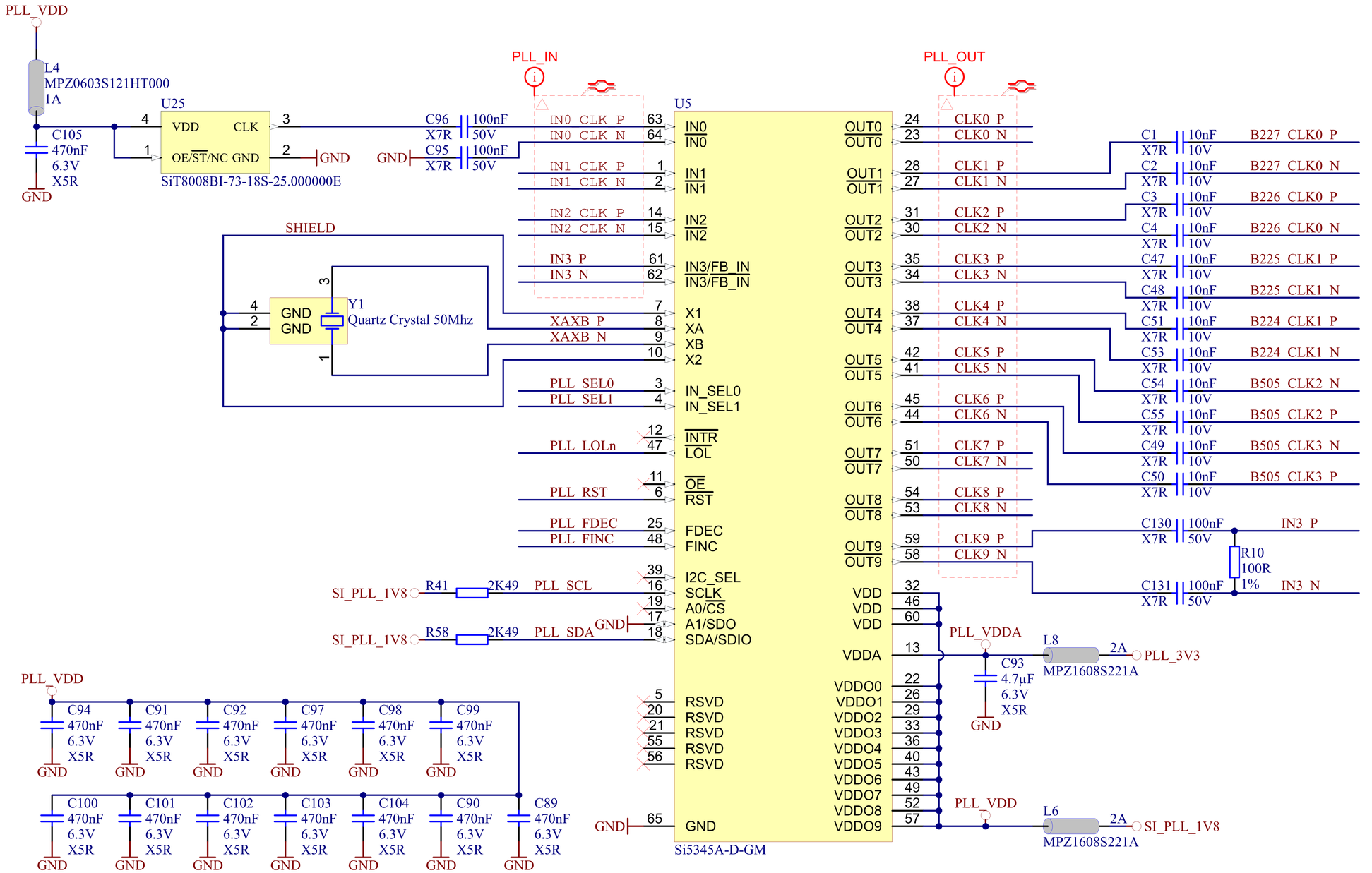






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Title: TE0817		
A4	Number: TE0817 7DE61-A	Rev. 02
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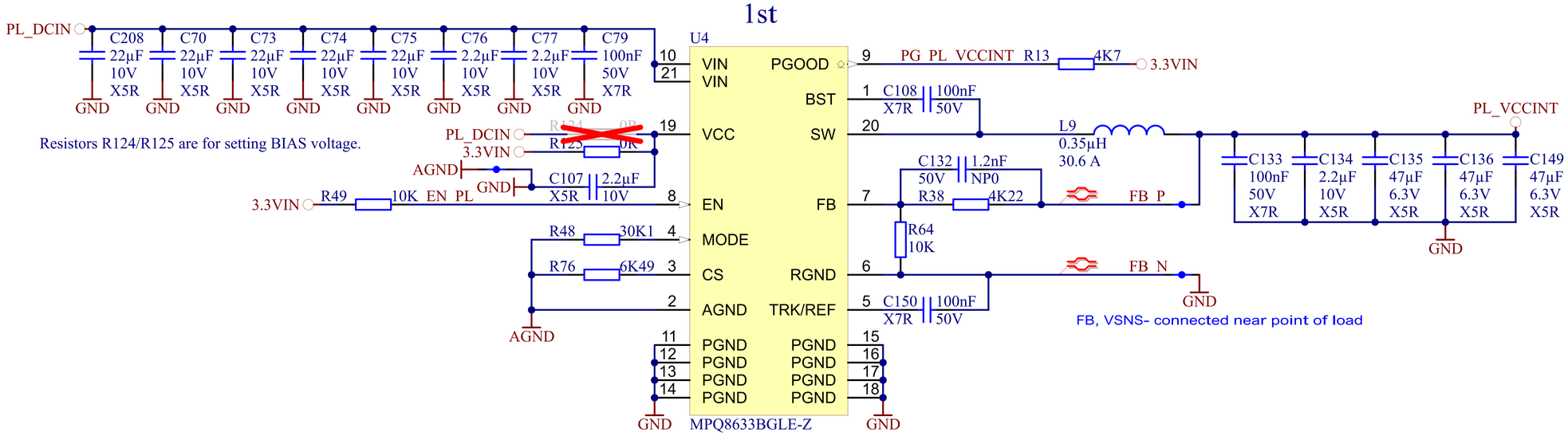


Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
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Filename: Clock.SchDoc			

U4 can be TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.

PL VCCINT

1st

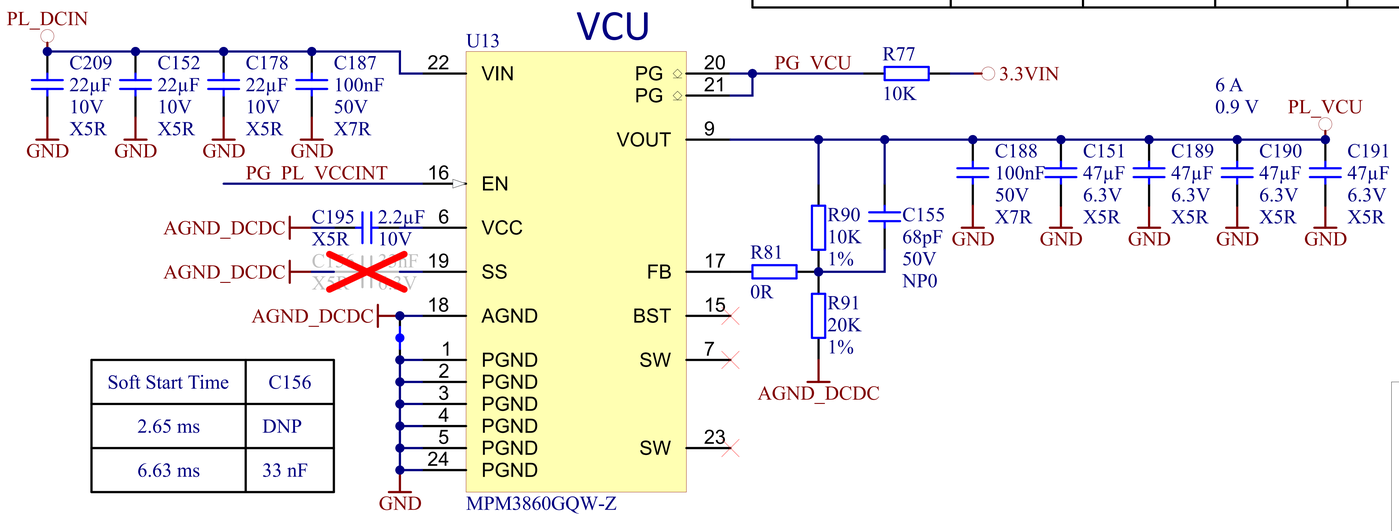


DCDC U4 (pin compatible)	Current Capabililty	Current Limit*	R76	Light-Load Mode	Frequency	R48	Soft Start Time	C150
TPS548A28	15 A	13.9 A	4.70 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
TPS548B28	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF
MPQ8633BGLE-Z	20 A	19.7 A	6.49 kOhm	CCM	800 kHz	30.1 kOhm	1.66 ms	100 nF

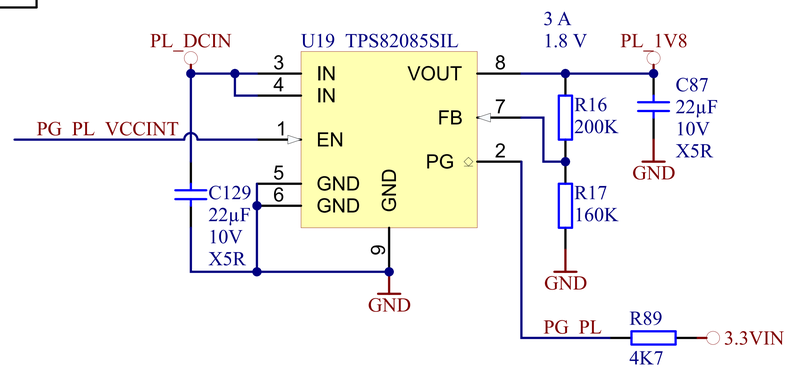
* Current limit depends on input and output voltage.

FPGA Speedgrade	R38	R64	PL_VCCINT	C132
-1	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-2	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-3	10 kOhm	20 kOhm	0.900 V	560 pF

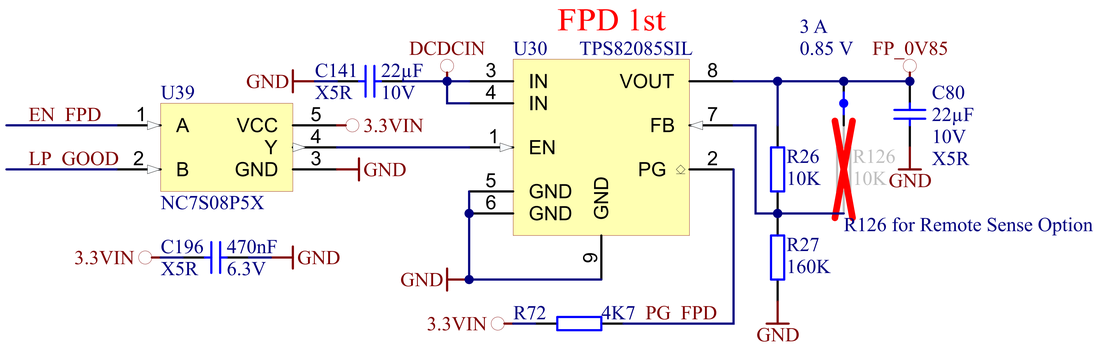
VCU

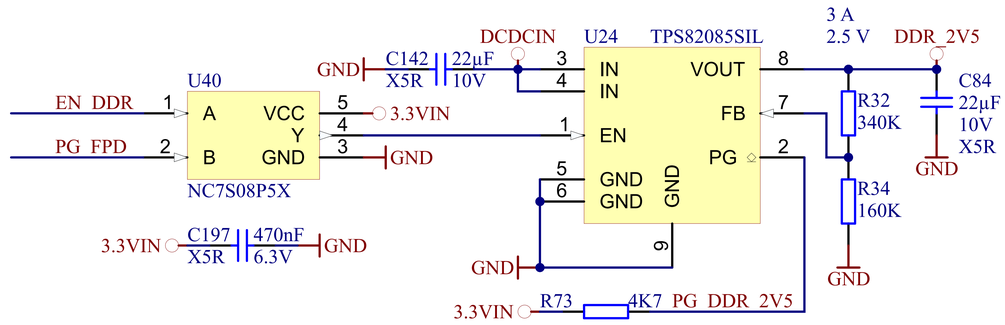


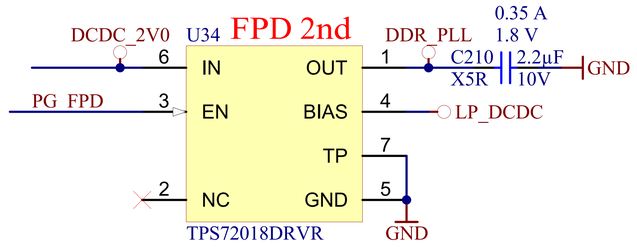
Soft Start Time	C156
2.65 ms	DNP
6.63 ms	33 nF

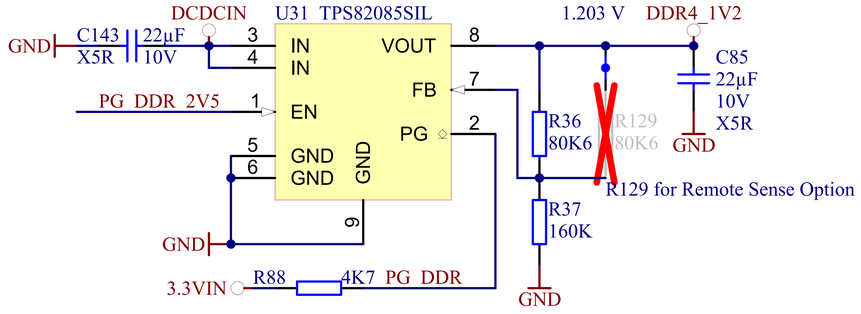


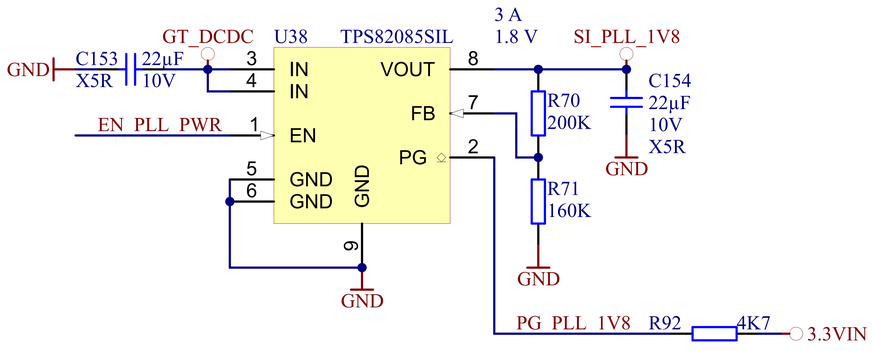
Title: TE0817			
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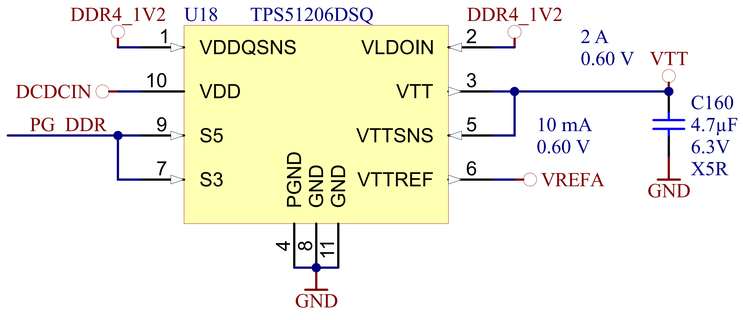






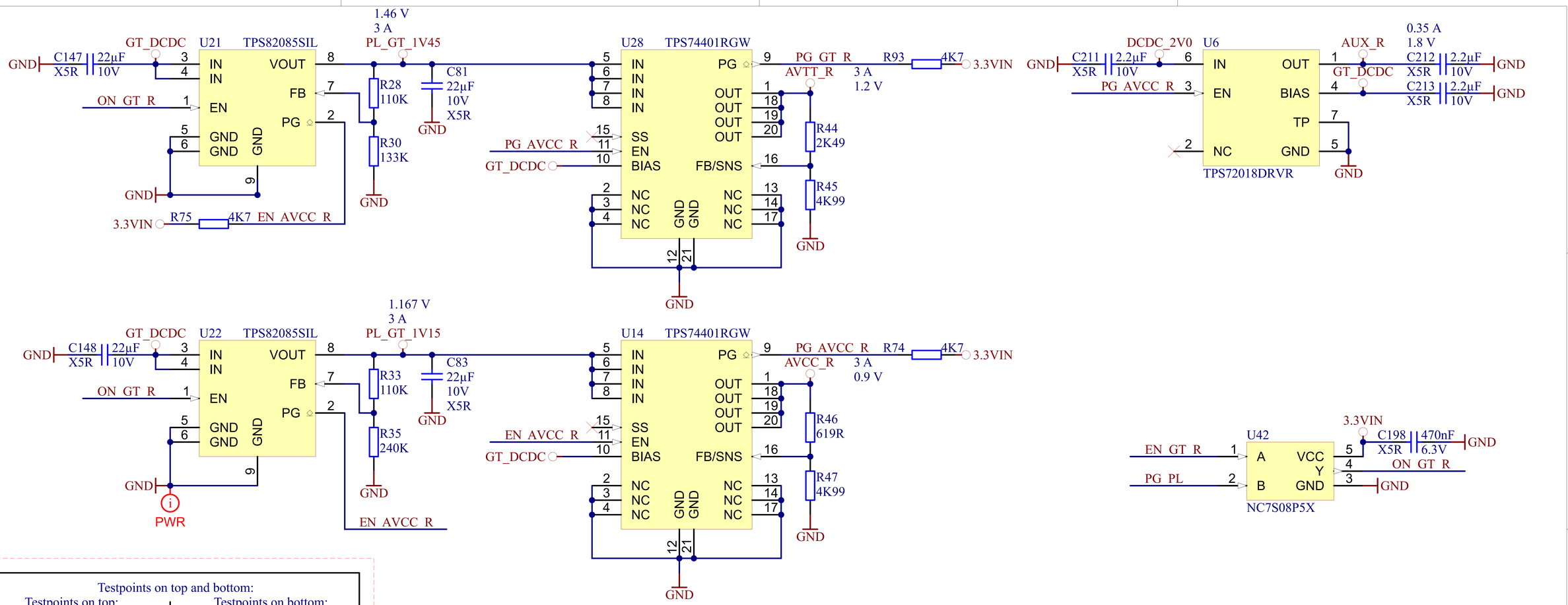






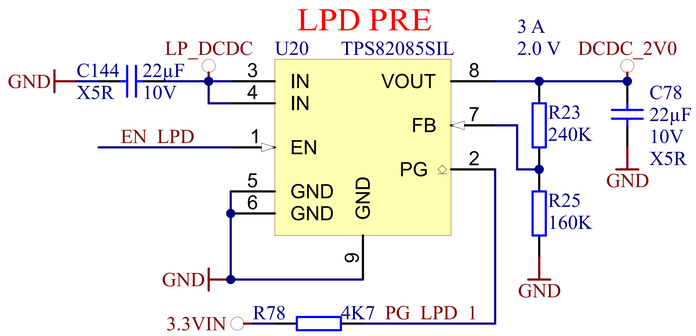
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A4	Number: TE0817 7DE61-A	Rev. 02
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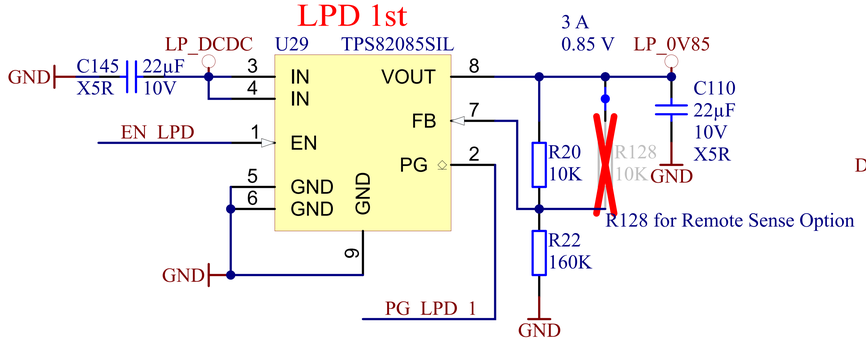


Title: TE0817			
A4	Number: TE0817 7DE61-A		Rev. 02
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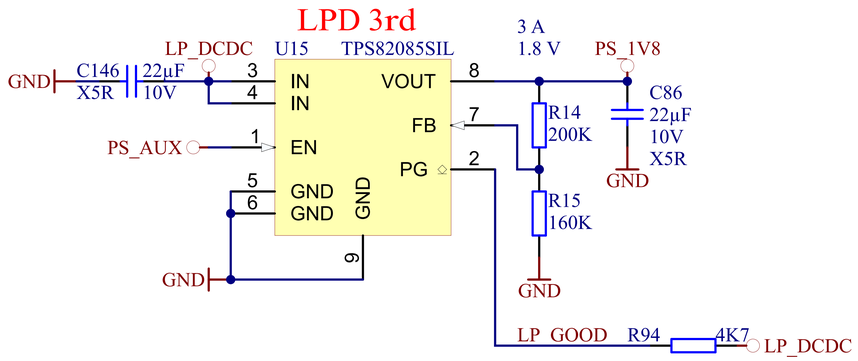
LPD PRE

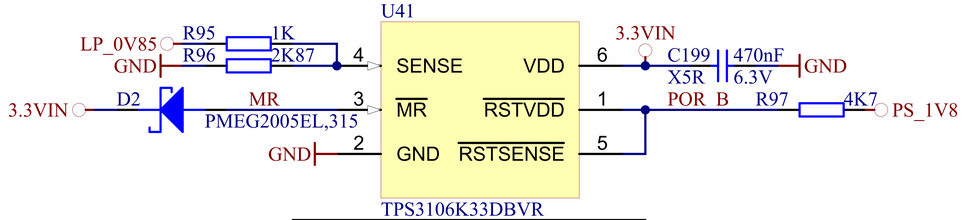


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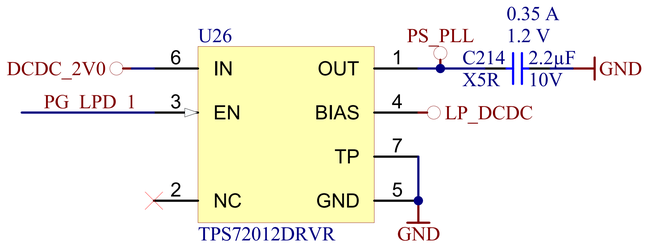


LPD 3rd

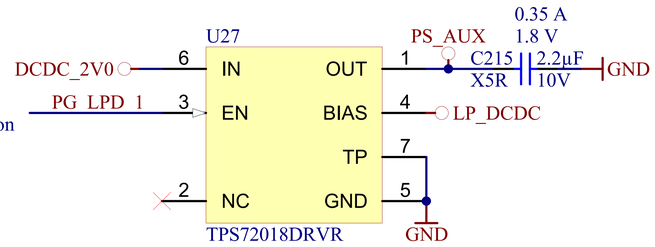


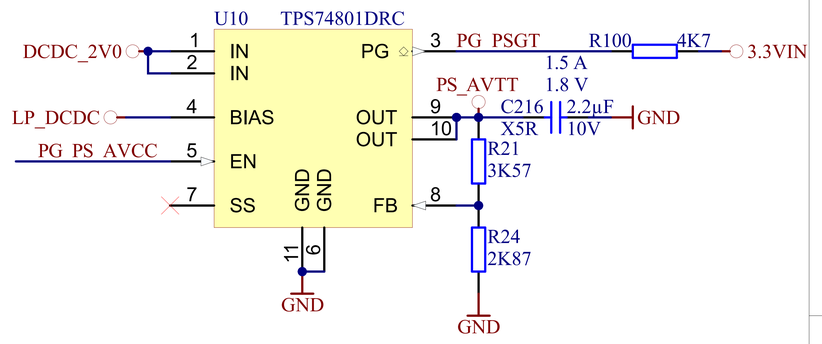


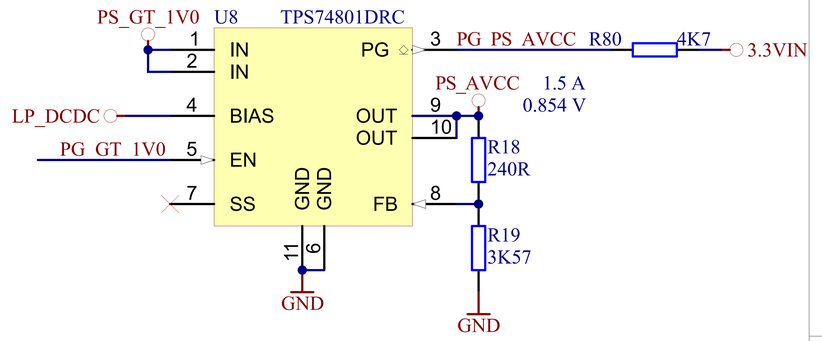
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LP_0V85	0.85 V	0.743 V
3.3VIN	3.3 V	2.941 V

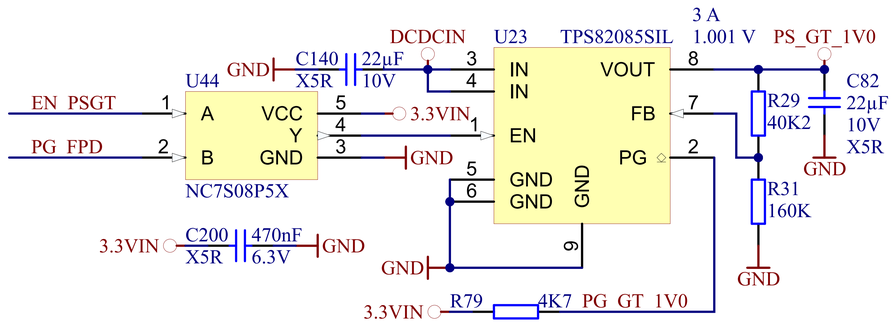


LPD 2nd









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