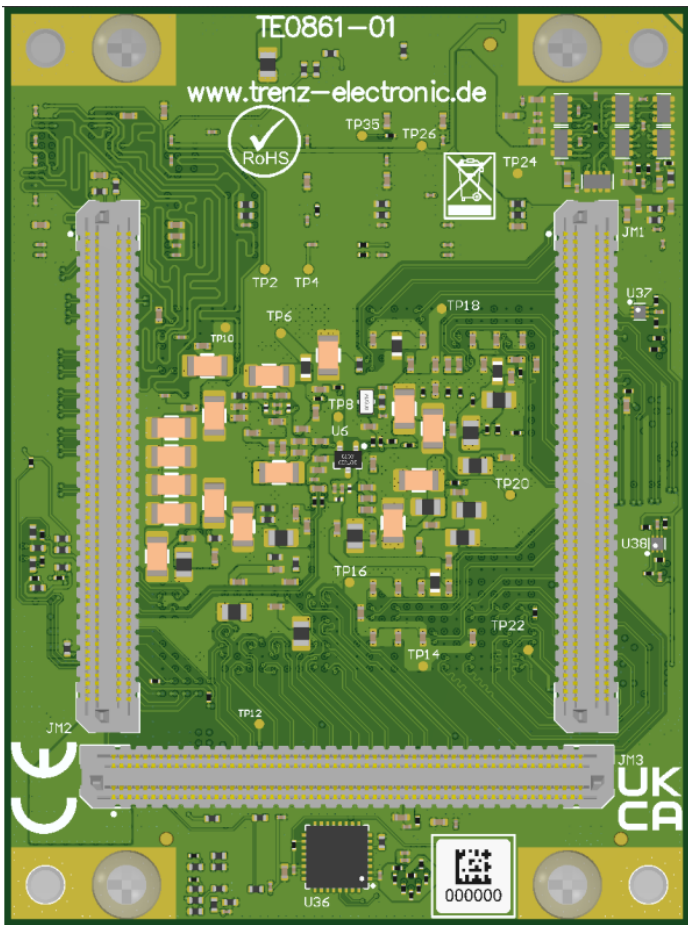
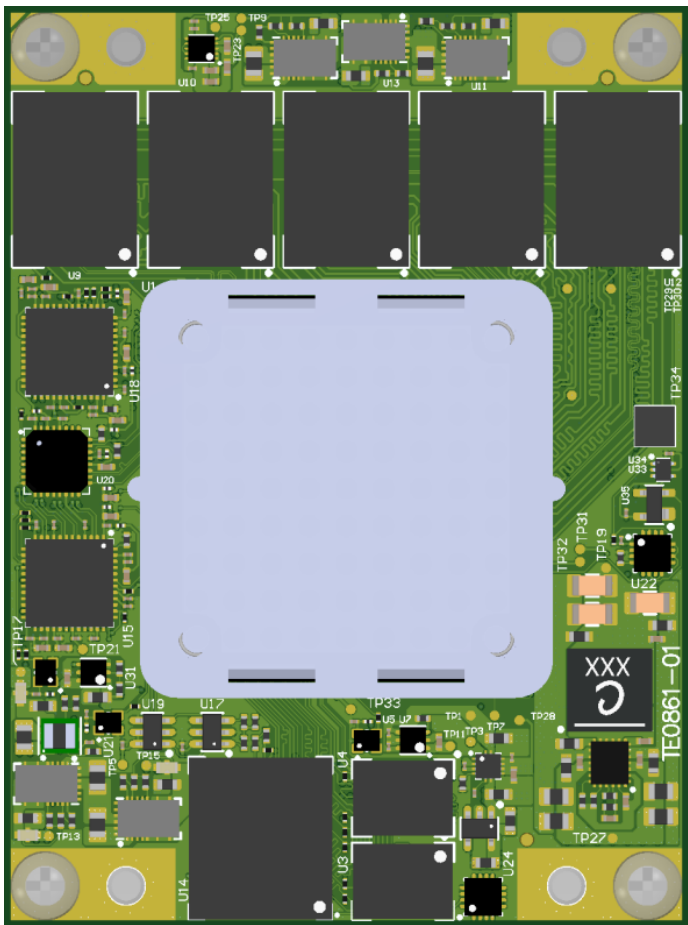




Regarding the usage of our schematics and alike documentation for Trenz module TE0861.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.

TE0861 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0861 – Legal Notices Modules		
	A4	Number: TE0861 6BE51QA	Rev. 01
	Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 1 of 35
	Filename: Legal Notices Modules.SchDoc		

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REV	Description	
-01	Initial revision	ED/VY



Title: TE0861 – Revision Changes		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 2 of 35
Filename: Revision_Changes.SchDoc		

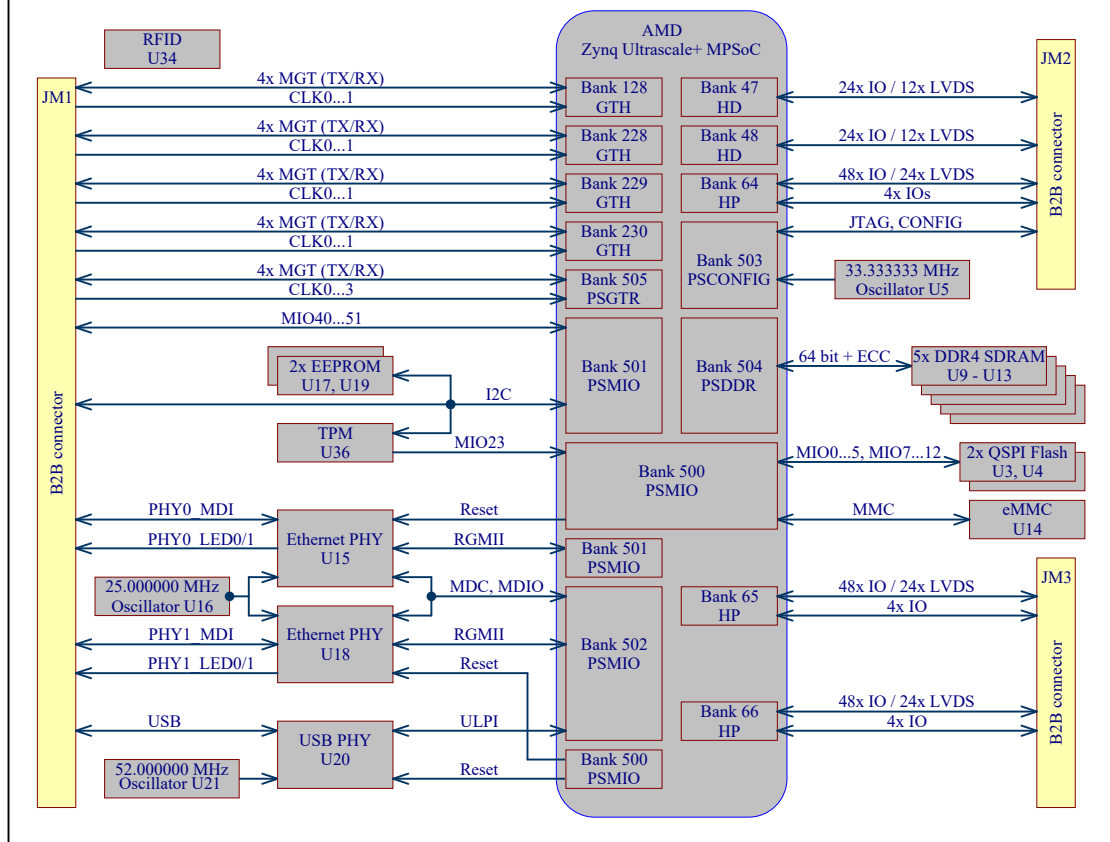
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System Overview



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	5 V - 12 V	+/- 10 %	Module main power supply	-
VCCO_47	IN	1.2 V - 3.3 V	1)	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	1)	HD IO Bank 48	-
VCCO_64	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 66	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
3V3	OUT	3.3 V	+/- 3 %	Periphery supply	-
1V8	OUT	1.8 V	+/- 3 %	Periphery supply	-

1) +/- 5 %, - 5 % / +3 % for 3.3 V

I2C Addresses:

Device	Address	Note
MPSoC U1H	-	AMD Zynq Ultrascale+ MPSoC PS
B2B JM1A	-	B2B connector
TPM U36	0x2E	Trusted Platform Modul
EEPROM U17	0x50	MAC-EEPROM with user area
EEPROM U19	0x51	MAC-EEPROM with user area

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_POWER_1
POWER_1.SchDoc

U_POWER_2
POWER_2.SchDoc

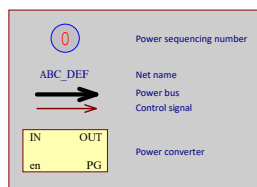
U_POWER_3
POWER_3.SchDoc

U_POWER_4
POWER_4.SchDoc

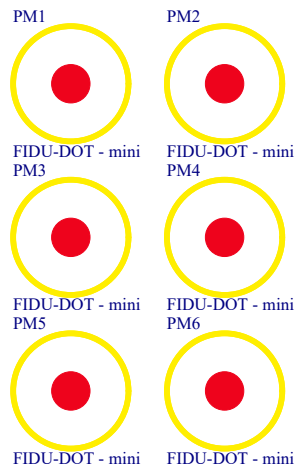
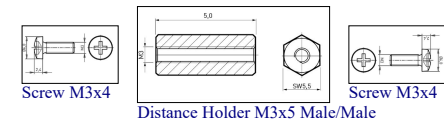
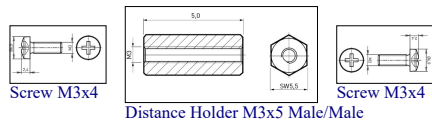
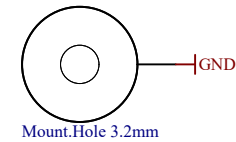
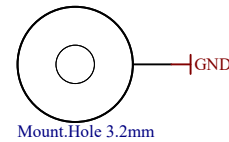
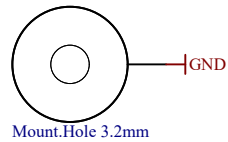
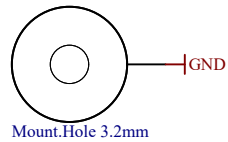
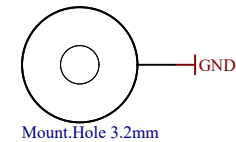
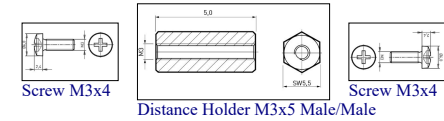
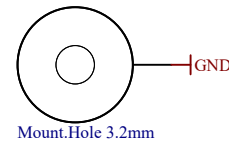
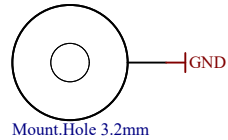
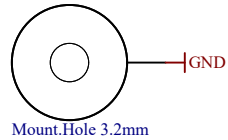
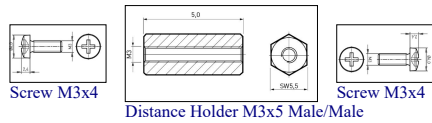


Title: TE0861 – System Overview

A4	Number: TE0861 6BE51QA	Rev. 01
Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 3 of 35
Filename: TE0861-Overview.SchDoc		



Special notes:



Serial1
Serial
Serialnumber 6,3 x 6.3mm
RoHS1

RoHS Logo on Top Overlay

RoHS-TOOVERLAY
WEEE1

WEEE Logo on Top Overlay

WEEE-TOOVERLAY
CE1

CE Logo on Top Overlay

CE-TOOVERLAY
UKCA1

UKCA Logo on Top Overlay

UKCA-TOOVERLAY

Design drawn by: ED
Checked by: MR
Assembly variant: 6BE51QA
Created by: VG
Modified by: VG
Modified at: 2026-02-02



Title: TE0861

A4

Number: TE0861
6BE51QA

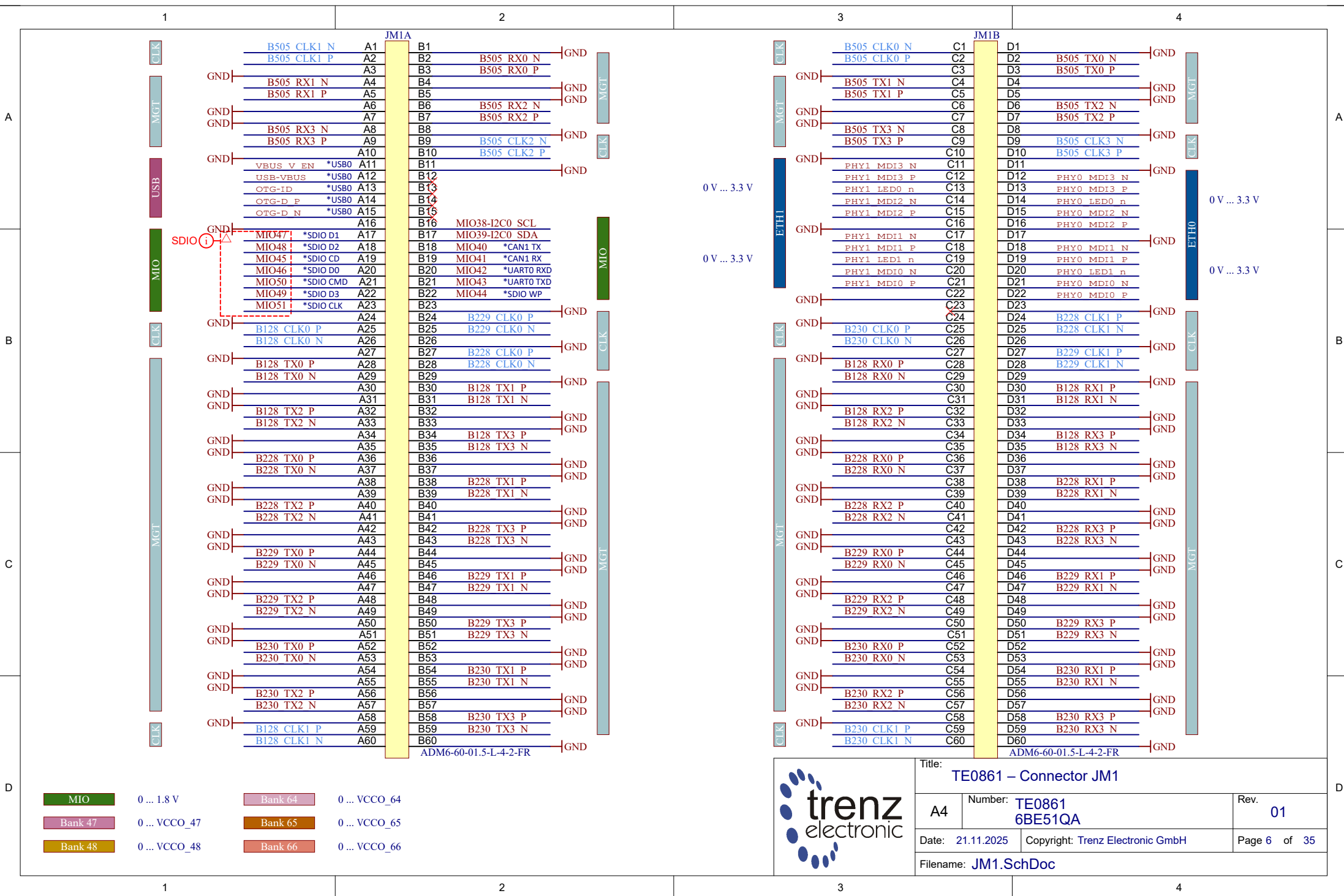
Rev. 01

Date: 21.11.2025

Copyright: Trenz Electronic GmbH

Page 5 of 35

Filename: TE0861.SchDoc



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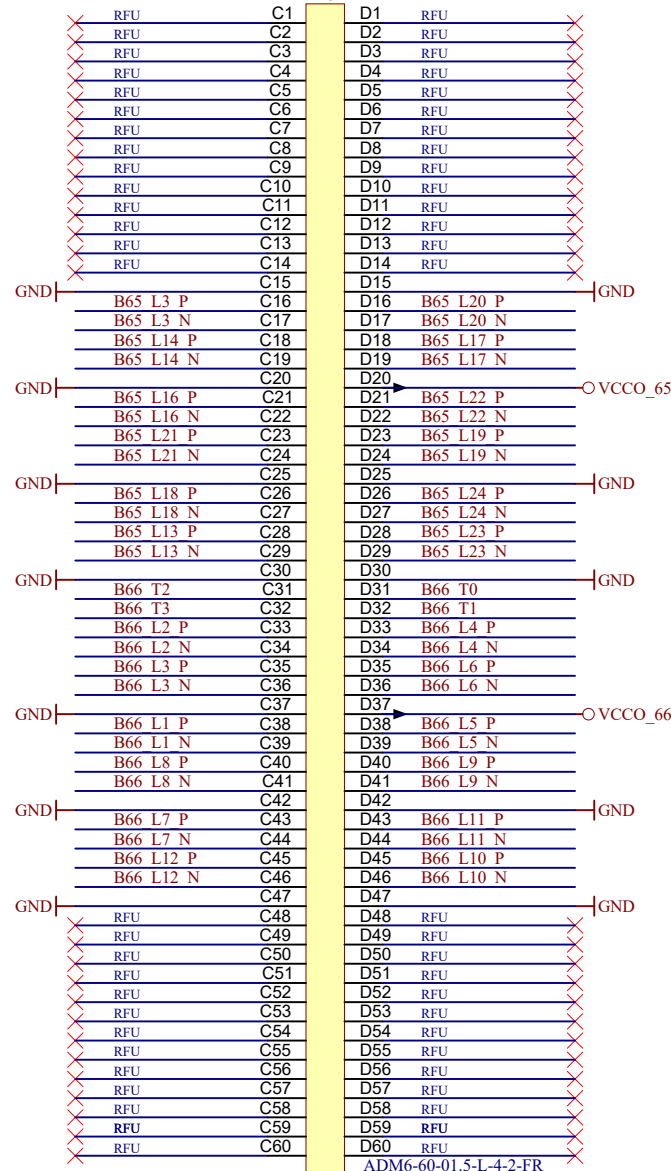
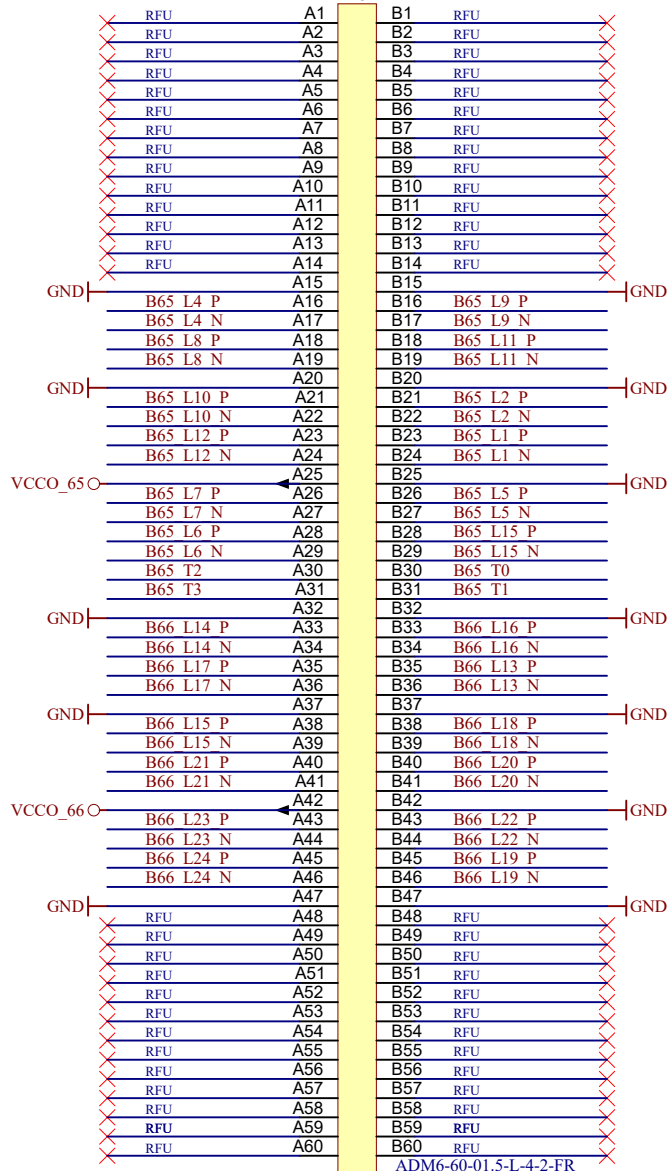
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JM3A

JM3B



ADM6-60-01.5-L-4-2-FR

ADM6-60-01.5-L-4-2-FR

MIO	0 ... 1.8 V	Bank 64	0 ... VCCO_64
Bank 47	0 ... VCCO_47	Bank 65	0 ... VCCO_65
Bank 48	0 ... VCCO_48	Bank 66	0 ... VCCO_66



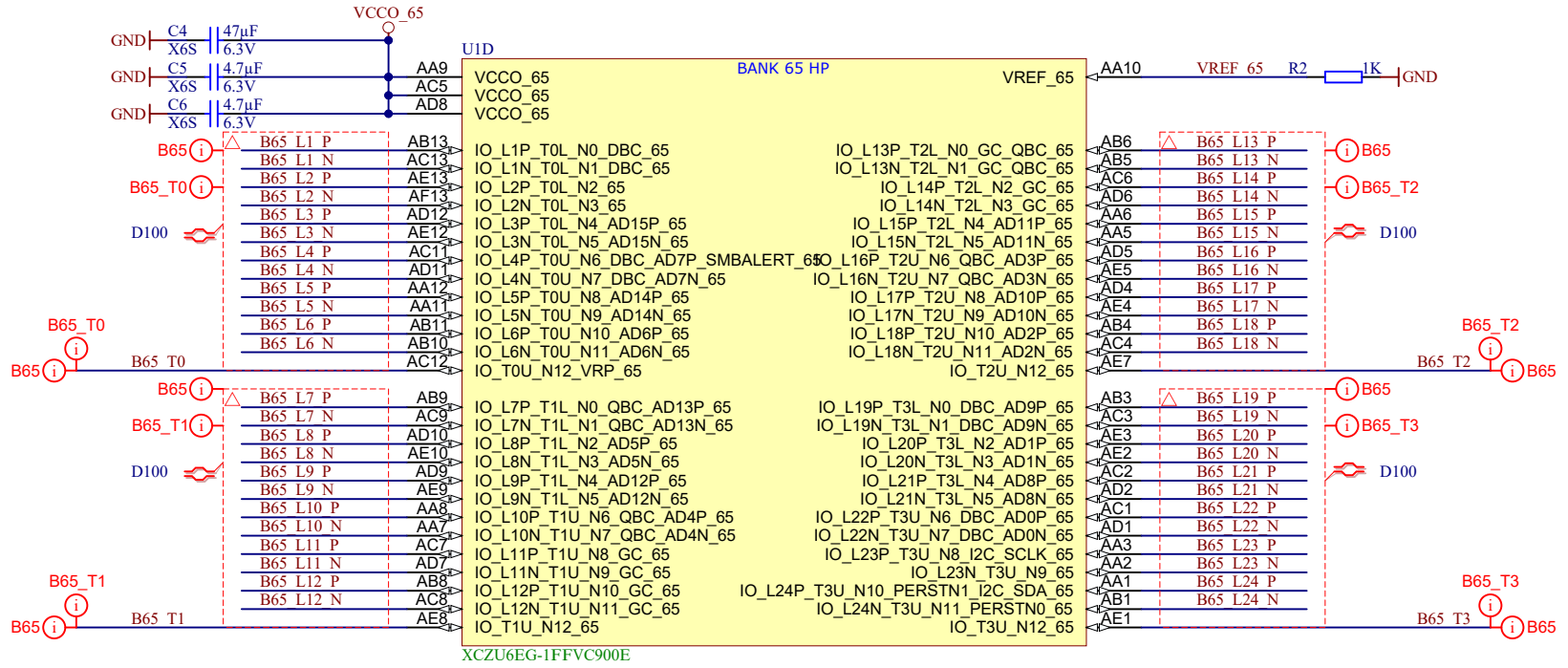
Title: TE0861 – Connector JM3		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 8 of 35
Filename: JM3.SchDoc		

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Title:TE0861 – B65

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Number:TE0861
6BE51QA

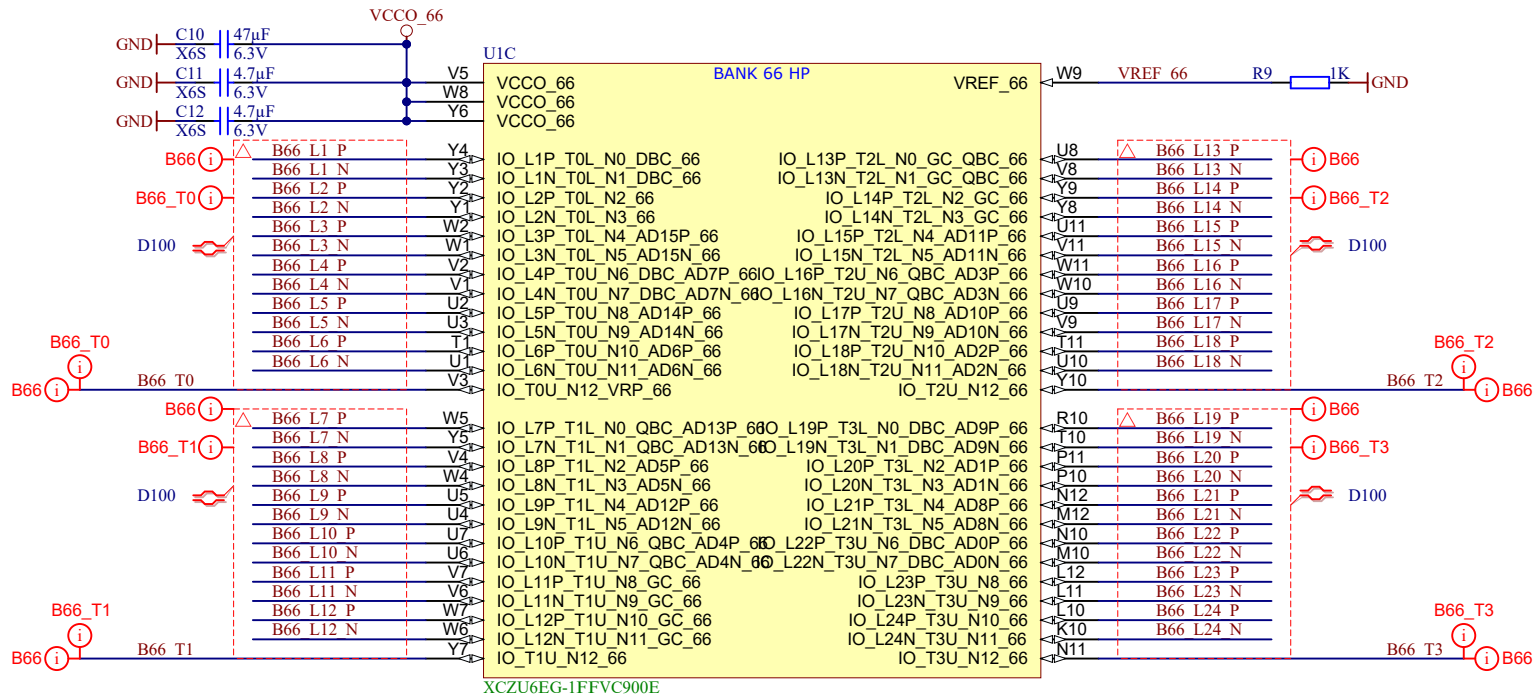
Rev.01

Date:21.11.2025

Copyright: Trenz Electronic GmbH

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Filename: B65.SchDoc





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UIJ

BANK 504 PSDDR

VCCO_PSDDR_504 PS_DDR_CK0
VCCO_PSDDR_504 PS_DDR_CK_N0
VCCO_PSDDR_504 PS_DDR_CKE0
VCCO_PSDDR_504 PS_DDR_CK1
VCCO_PSDDR_504 PS_DDR_CK_N1
VCCO_PSDDR_504 PS_DDR_CKE1

VCC_PSDDR_PLL PS_DDR_A0
VCC_PSDDR_PLL PS_DDR_A1
VCC_PSDDR_PLL PS_DDR_A2
VCC_PSDDR_PLL PS_DDR_A3
VCC_PSDDR_PLL PS_DDR_A4
VCC_PSDDR_PLL PS_DDR_A5
VCC_PSDDR_PLL PS_DDR_A6
VCC_PSDDR_PLL PS_DDR_A7
VCC_PSDDR_PLL PS_DDR_A8
VCC_PSDDR_PLL PS_DDR_A9
VCC_PSDDR_PLL PS_DDR_A10
VCC_PSDDR_PLL PS_DDR_A11
VCC_PSDDR_PLL PS_DDR_A12
VCC_PSDDR_PLL PS_DDR_A13
VCC_PSDDR_PLL PS_DDR_A14
VCC_PSDDR_PLL PS_DDR_A15
VCC_PSDDR_PLL PS_DDR_A16
VCC_PSDDR_PLL PS_DDR_A17

VCC_PSINTFP_DDR PS_DDR_CS_N0
VCC_PSINTFP_DDR PS_DDR_CS_N1
VCC_PSINTFP_DDR PS_DDR_BA0
VCC_PSINTFP_DDR PS_DDR_BA1
VCC_PSINTFP_DDR PS_DDR_BG0
VCC_PSINTFP_DDR PS_DDR_BG1
VCC_PSINTFP_DDR PS_DDR_PARITY
VCC_PSINTFP_DDR PS_DDR_RAM_RST_N
VCC_PSINTFP_DDR PS_DDR_ACT_N
VCC_PSINTFP_DDR PS_DDR_ALERT_N
VCC_PSINTFP_DDR PS_DDR_ZQ
VCC_PSINTFP_DDR PS_DDR_ODT0
VCC_PSINTFP_DDR PS_DDR_ODT1

XCZU6EG-1FFVC900E

AJ26 DDR4-CLK0 P
AJ27 DDR4-CLK0 N
AJ25 DDR4-CKE0

AG23
AG24
AH27

AK25 DDR4-A0
AK28 DDR4-A1
AK27 DDR4-A2
AH24 DDR4-A3
AK24 DDR4-A4
AJ30 DDR4-A5
AE22 DDR4-A6
AE25 DDR4-A7
AE23 DDR4-A8
AE24 DDR4-A9
AD22 DDR4-A10
AH23 DDR4-A11
AF21 DDR4-A12
AG21 DDR4-A13
AF22 DDR4-A14
AF23 DDR4-A15
AD21 DDR4-A16
AD20 DDR4-A17

AJ24 DDR4-CS
AG25

AG26 DDR4-BA0
AF25 DDR4-BA1

AF26 DDR4-BG0
AD26 DDR4-BG1

AC14 DDR4-PAR
AC16 DDR4-RESET
AC17 DDR4-ACT
AD19 DDR4-ALERT

AC23 R17 240R GND

AJ29 DDR4-ODT0
AH26

DQ0
DQ1
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DQ11
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DQ18
DQ19
DQ20
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DQ27
DQ28
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DQ30
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AK17
AH17
AJ17
AH16
AK15
AK14
AJ14
AH14
AK19
AK18
AJ19
AH19
AK21
AK22
AE22
AE25
AG14
AG15
AG16
AF16
AD14
AD15
AD16
AE17
AE18
AE20
AE19
AG18
AH18
AG19
AG20

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
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PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
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PS_DDR_DQ31

DDR4-DQS0 P
DDR4-DQS0 N
DDR4-DQS1 P
DDR4-DQS1 N
DDR4-DQS2 P
DDR4-DQS2 N
DDR4-DQS3 P
DDR4-DQS3 N
DDR4-DQS4 P
DDR4-DQS4 N
DDR4-DQS5 P
DDR4-DQS5 N
DDR4-DQS6 P
DDR4-DQS6 N
DDR4-DQS7 P
DDR4-DQS7 N
DDR4-DQS8 P
DDR4-DQS8 N

D80

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BANK 504 PSDDR

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
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PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
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PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

PS_DDR_DQ32
PS_DDR_DQ33
PS_DDR_DQ34
PS_DDR_DQ35
PS_DDR_DQ36
PS_DDR_DQ37
PS_DDR_DQ38
PS_DDR_DQ39
PS_DDR_DQ40
PS_DDR_DQ41
PS_DDR_DQ42
PS_DDR_DQ43
PS_DDR_DQ44
PS_DDR_DQ45
PS_DDR_DQ46
PS_DDR_DQ47
PS_DDR_DQ48
PS_DDR_DQ49
PS_DDR_DQ50
PS_DDR_DQ51
PS_DDR_DQ52
PS_DDR_DQ53
PS_DDR_DQ54
PS_DDR_DQ55
PS_DDR_DQ56
PS_DDR_DQ57
PS_DDR_DQ58
PS_DDR_DQ59
PS_DDR_DQ60
PS_DDR_DQ61
PS_DDR_DQ62
PS_DDR_DQ63
PS_DDR_DQ64
PS_DDR_DQ65
PS_DDR_DQ66
PS_DDR_DQ67
PS_DDR_DQ68
PS_DDR_DQ69
PS_DDR_DQ70
PS_DDR_DQ71

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

PS_DDR_DQ0
PS_DDR_DQ1
PS_DDR_DQ2
PS_DDR_DQ3
PS_DDR_DQ4
PS_DDR_DQ5
PS_DDR_DQ6
PS_DDR_DQ7
PS_DDR_DQ8
PS_DDR_DQ9
PS_DDR_DQ10
PS_DDR_DQ11
PS_DDR_DQ12
PS_DDR_DQ13
PS_DDR_DQ14
PS_DDR_DQ15
PS_DDR_DQ16
PS_DDR_DQ17
PS_DDR_DQ18
PS_DDR_DQ19
PS_DDR_DQ20
PS_DDR_DQ21
PS_DDR_DQ22
PS_DDR_DQ23
PS_DDR_DQ24
PS_DDR_DQ25
PS_DDR_DQ26
PS_DDR_DQ27
PS_DDR_DQ28
PS_DDR_DQ29
PS_DDR_DQ30
PS_DDR_DQ31

XCZU6EG-1FFVC900E



Title:

TE0861 – PS_DDR

A4

Number:

TE0861
6BE51QA

Rev.

01

Date: 21.11.2025

Copyright: Trenz Electronic GmbH

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Filename: PS_DDR.SchDoc

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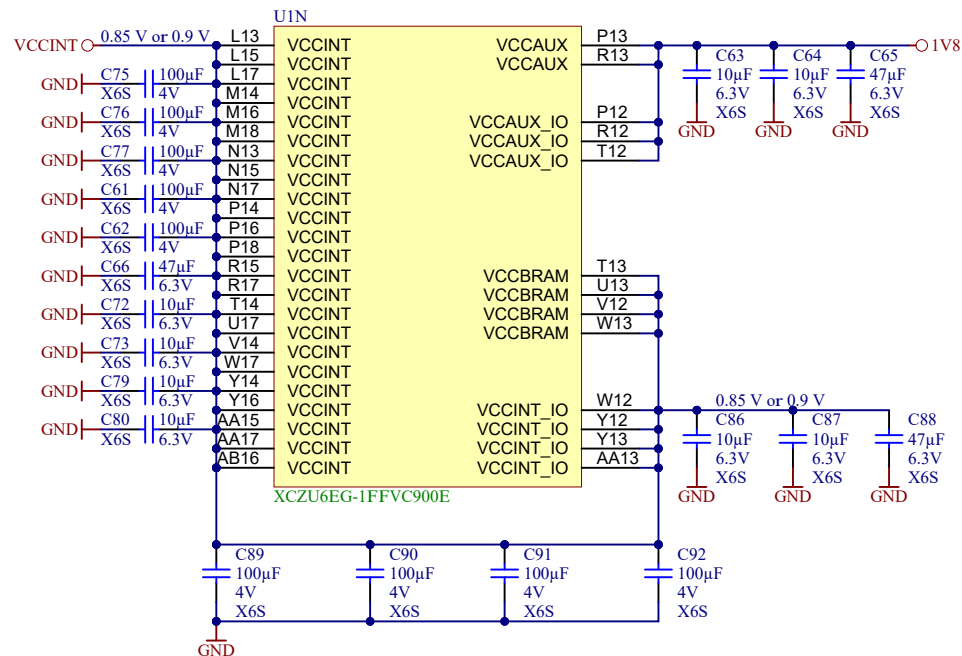
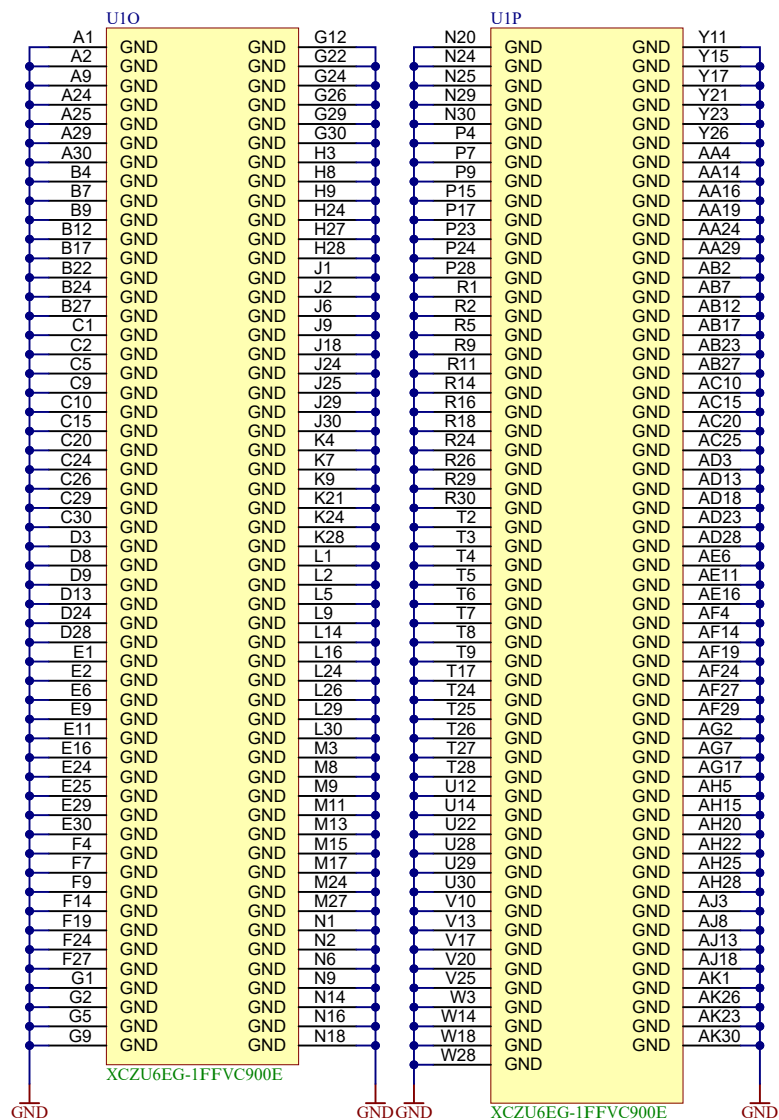
4

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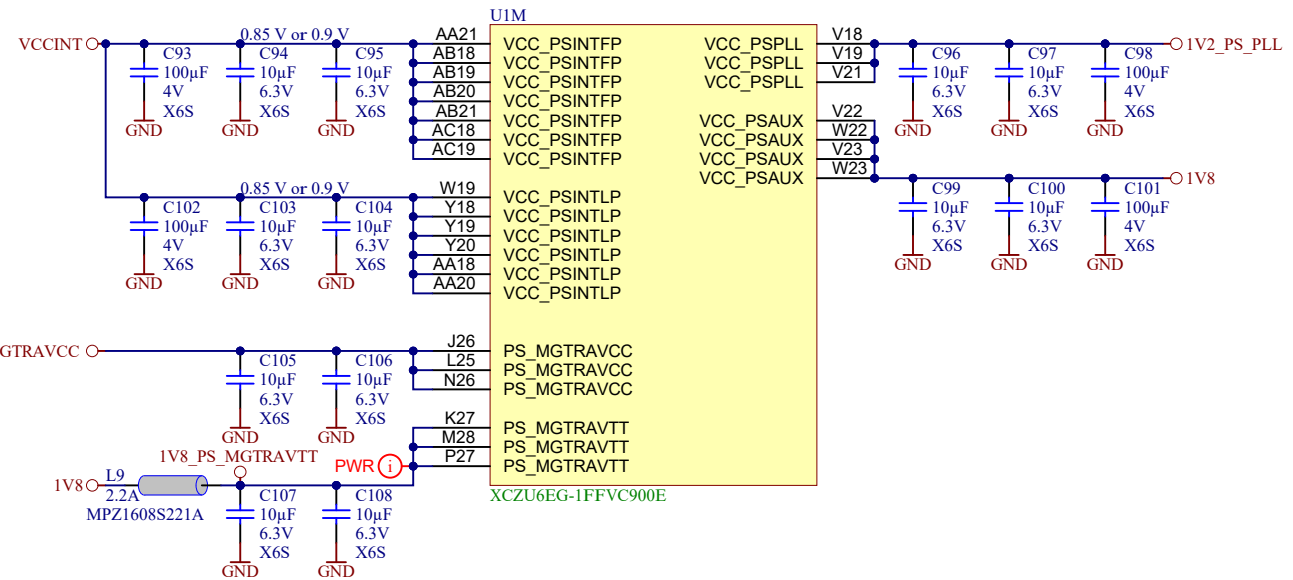
Title: TE0861 – ZU_POWER		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 19 of 35
Filename: ZU_POWER.SchDoc		

1

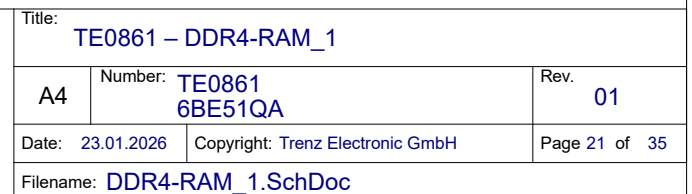
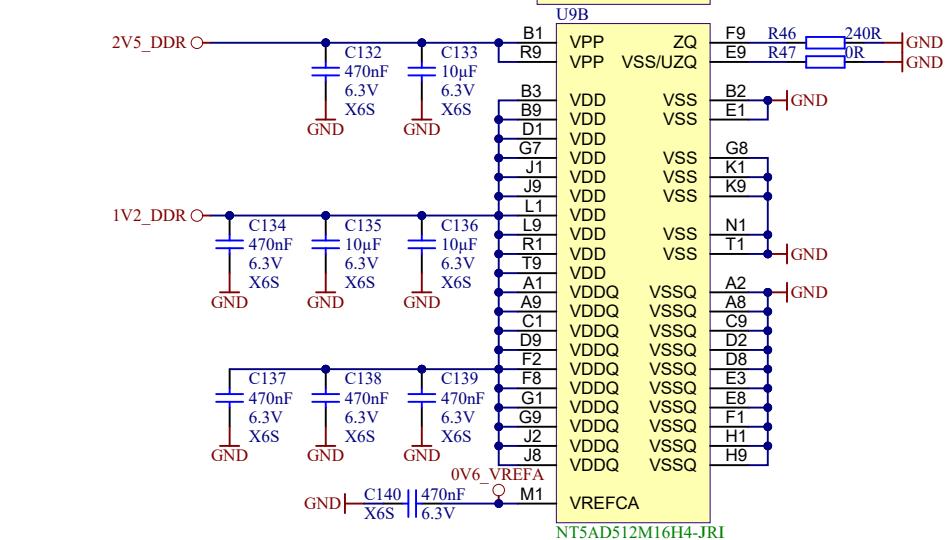
2

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Title: TE0861 – ZU_PS_POWER		
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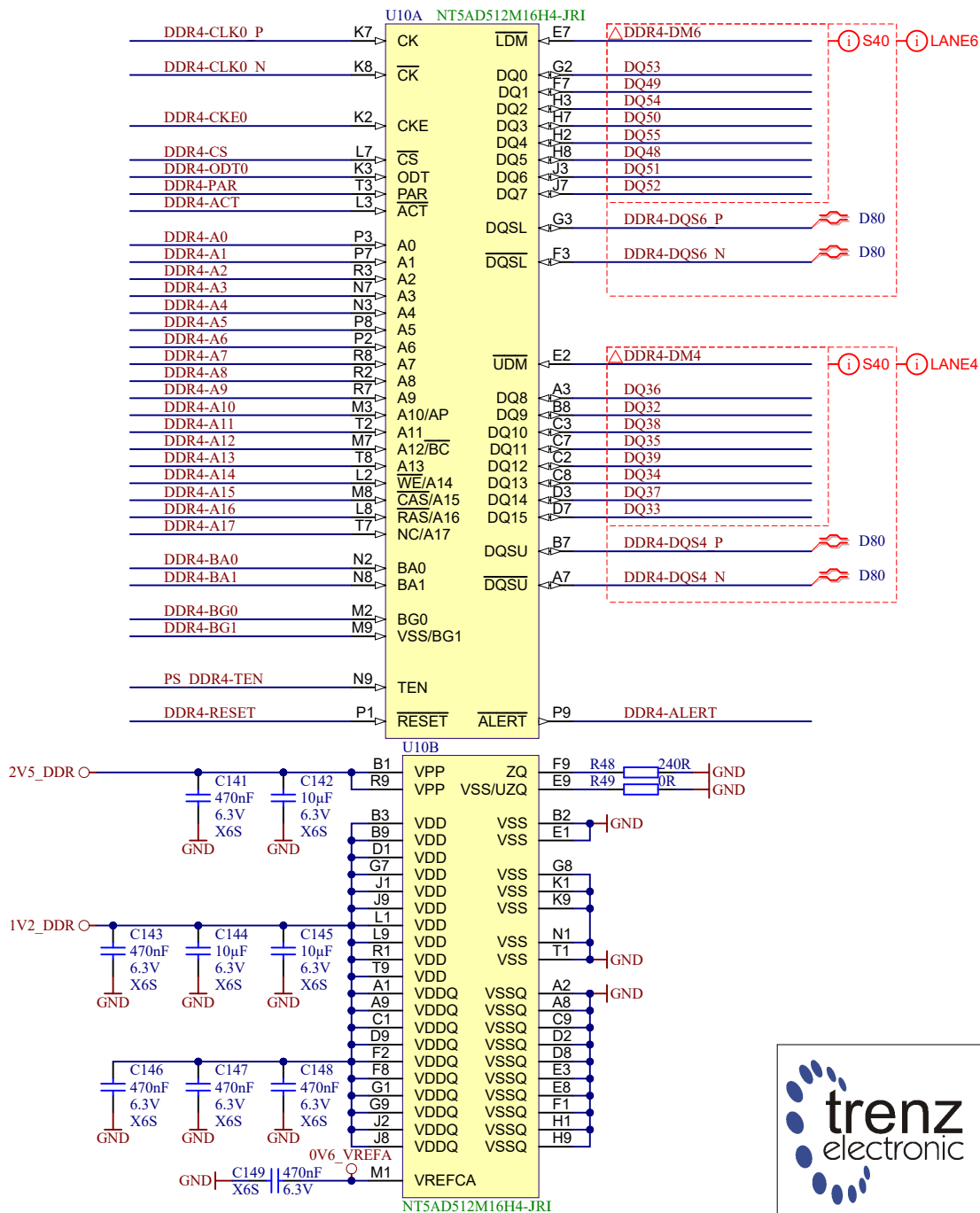
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Title: TE0861 – DDR4-RAM_2		
A4	Number: TE0861 6BE51QA	Rev. 01
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Filename: DDR4-RAM_2.SchDoc		

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A

B

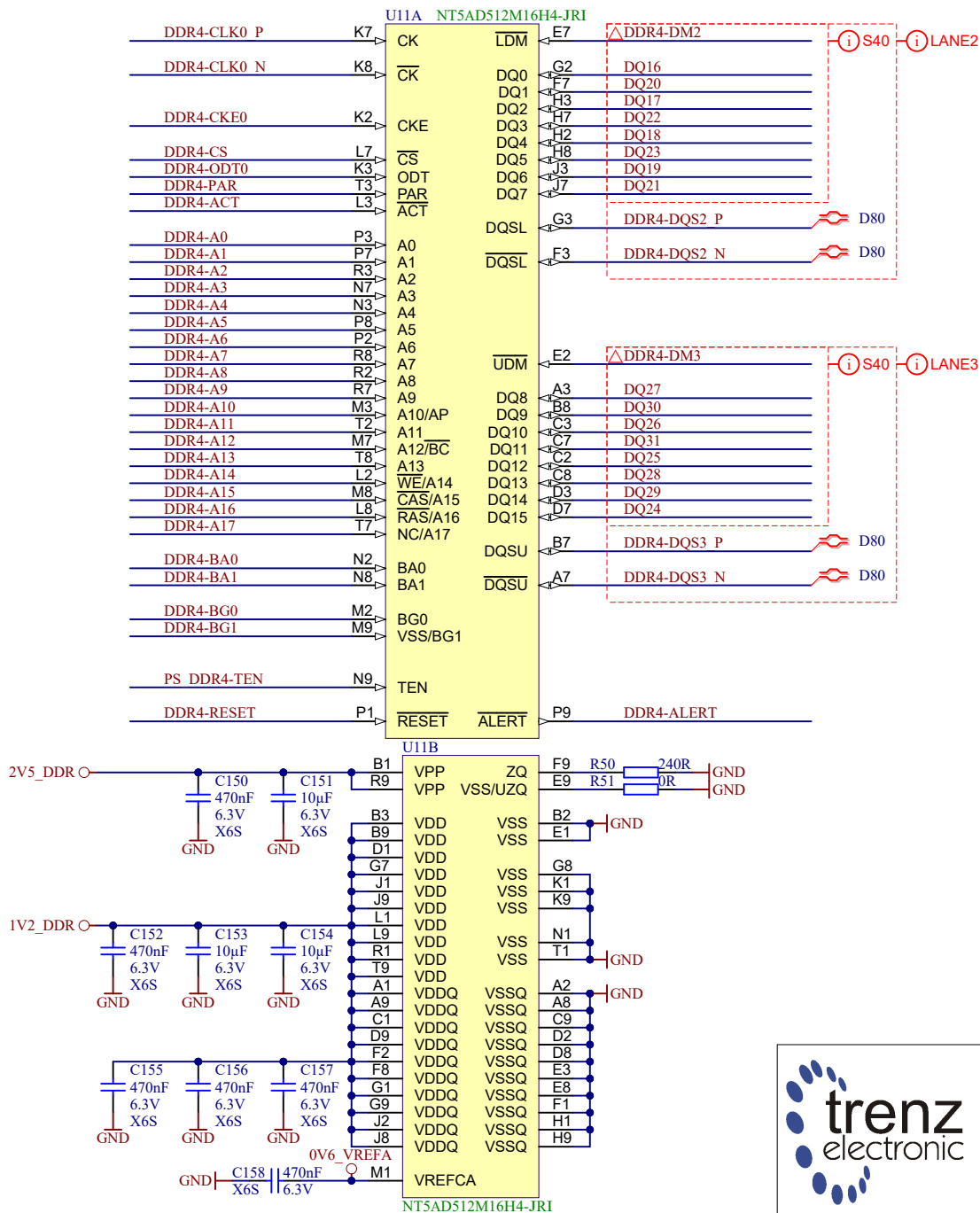
B

C

C

D

D



Title: TE0861 – DDR4-RAM_3		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 23.01.2026	Copyright: Trenz Electronic GmbH	Page 23 of 35
Filename: DDR4-RAM_3.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

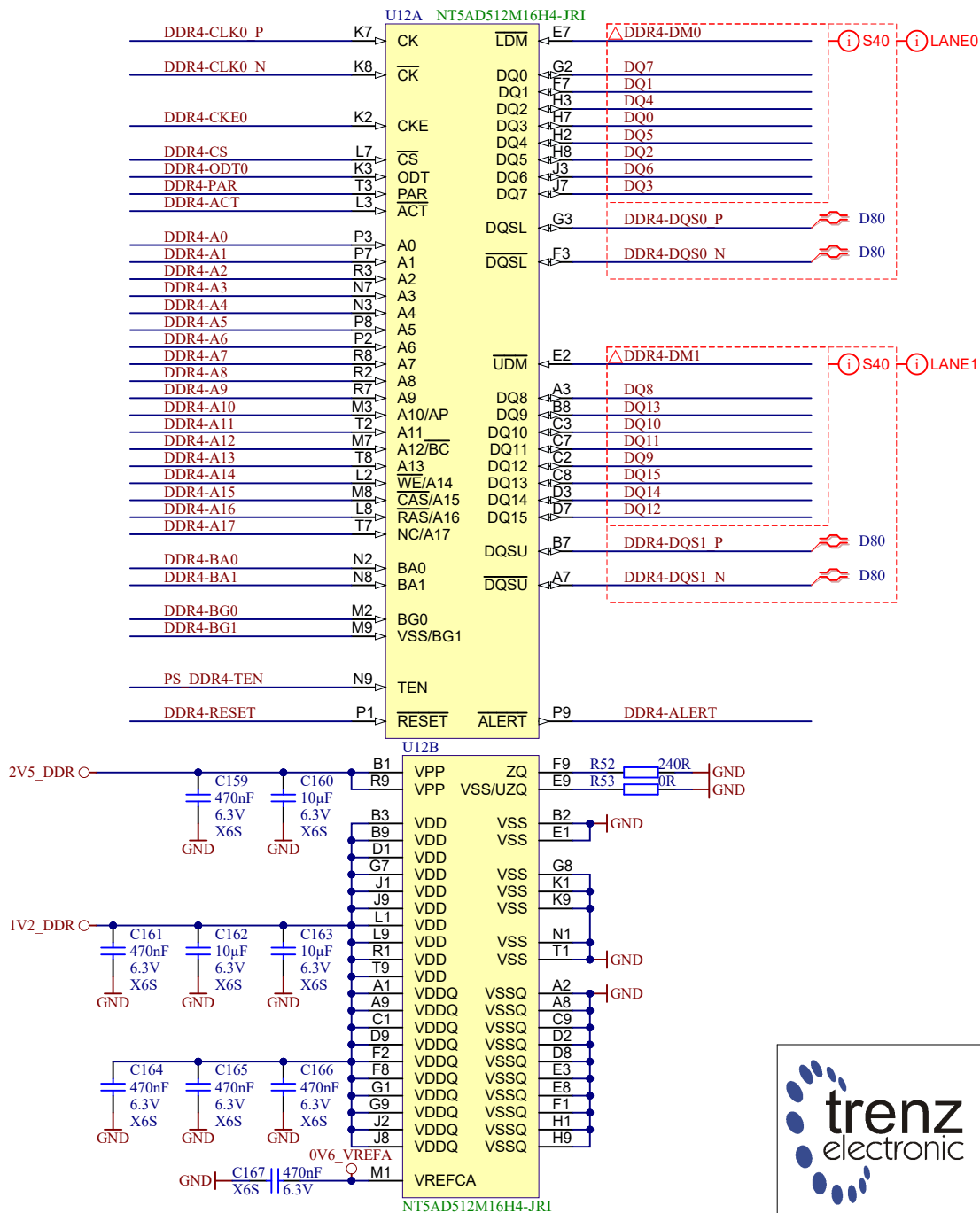
B

C

C

D

D



Title: TE0861 – DDR4-RAM_4		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 23.01.2026	Copyright: Trenz Electronic GmbH	Page 24 of 35
Filename: DDR4-RAM_4.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

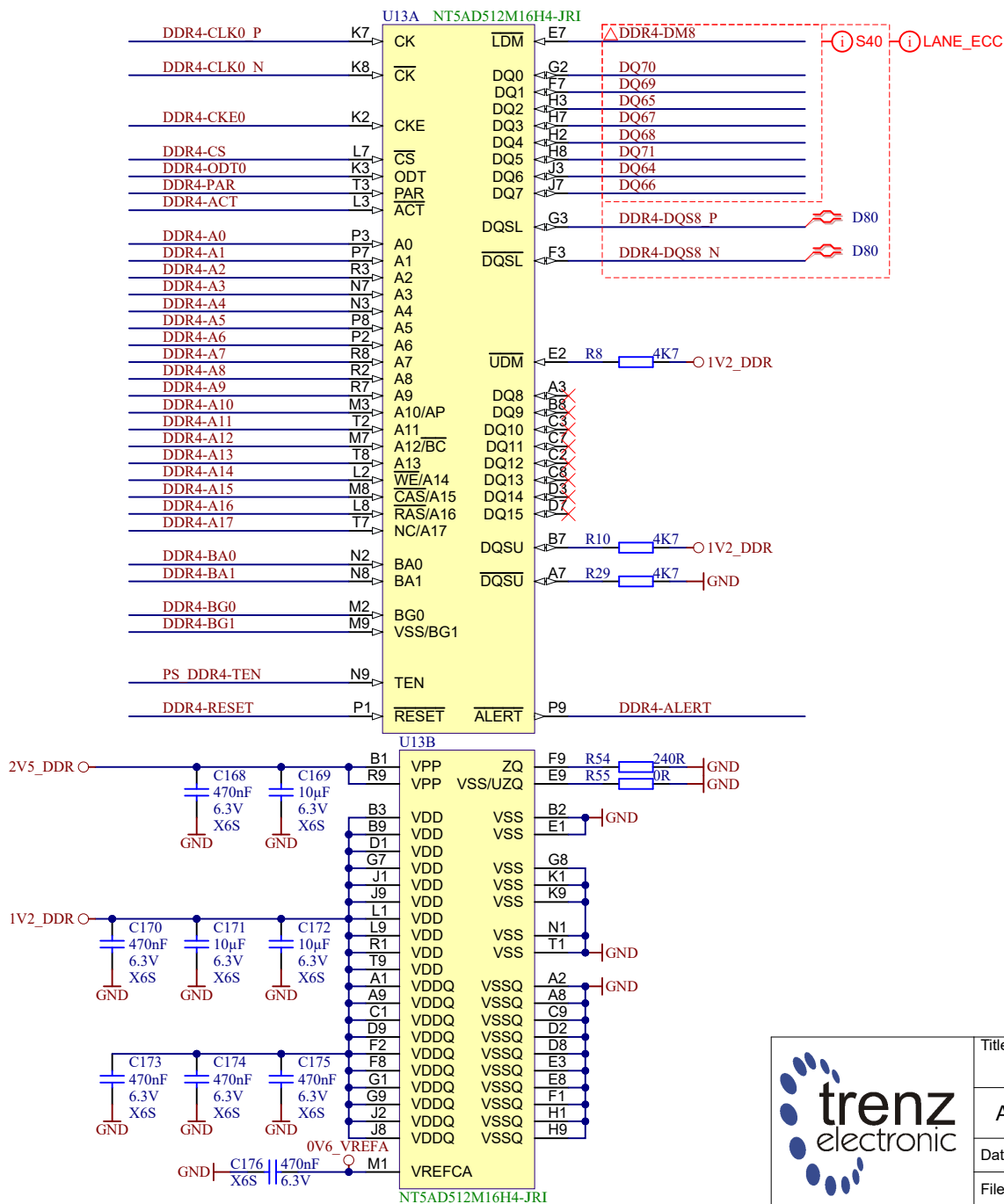
B

C

C

D

D



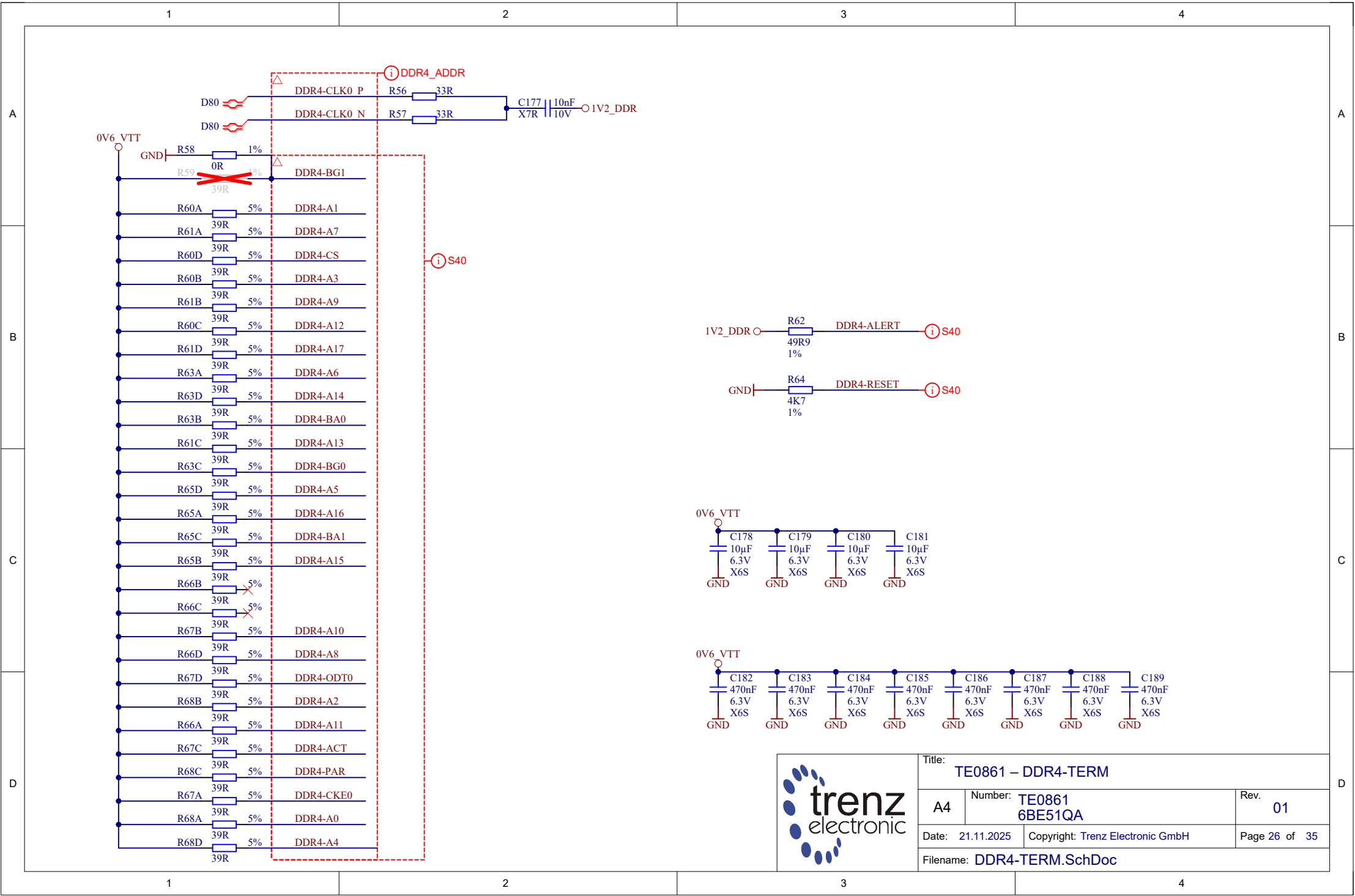
Title: TE0861 – DDR4-RAM_5		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 23.01.2026	Copyright: Trenz Electronic GmbH	Page 25 of 35
Filename: DDR4-RAM_5.SchDoc		

1

2

3

4



1

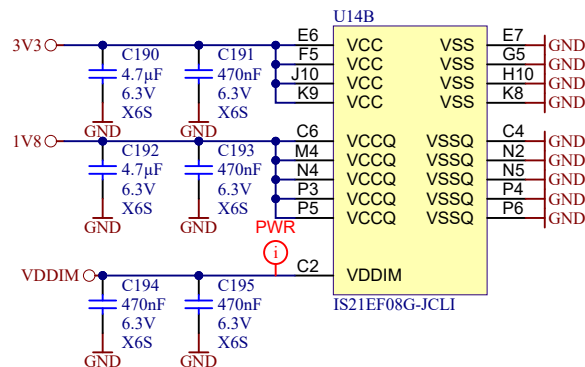
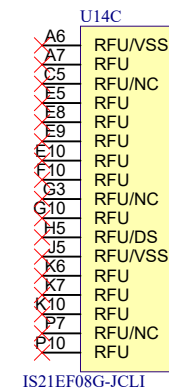
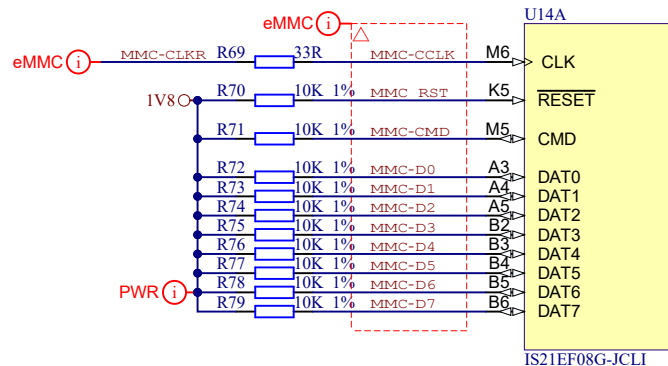
2

3

4

U14D			
A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M1
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

IS21EF08G-JCLI



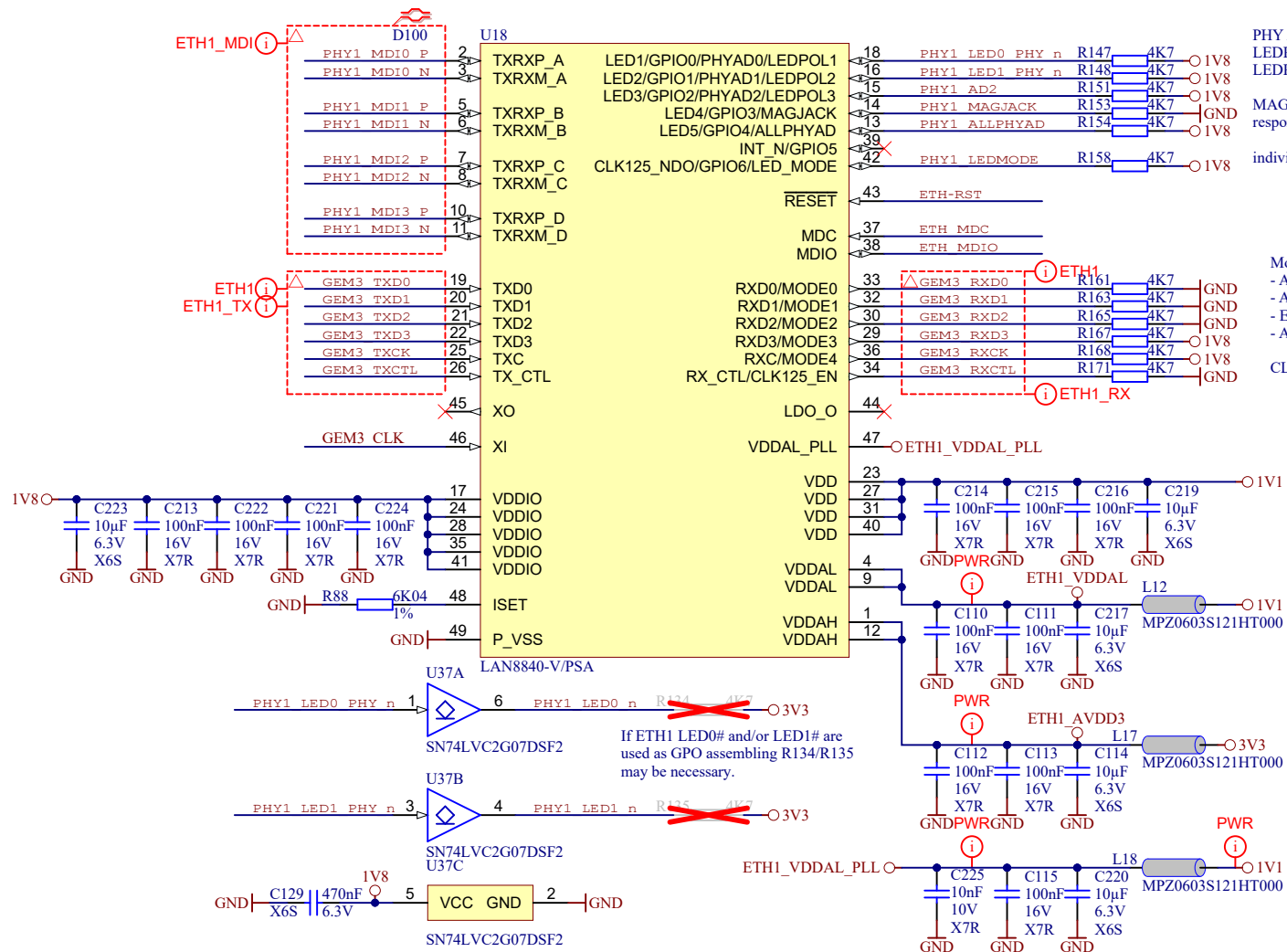
Title: TE0861 – eMMC		
A4	Number: TE0861 6BE51QA	Rev. 01
Date: 21.11.2025	Copyright: Trenz Electronic GmbH	Page 27 of 35
Filename: eMMC.SchDoc		

1

2

3

4



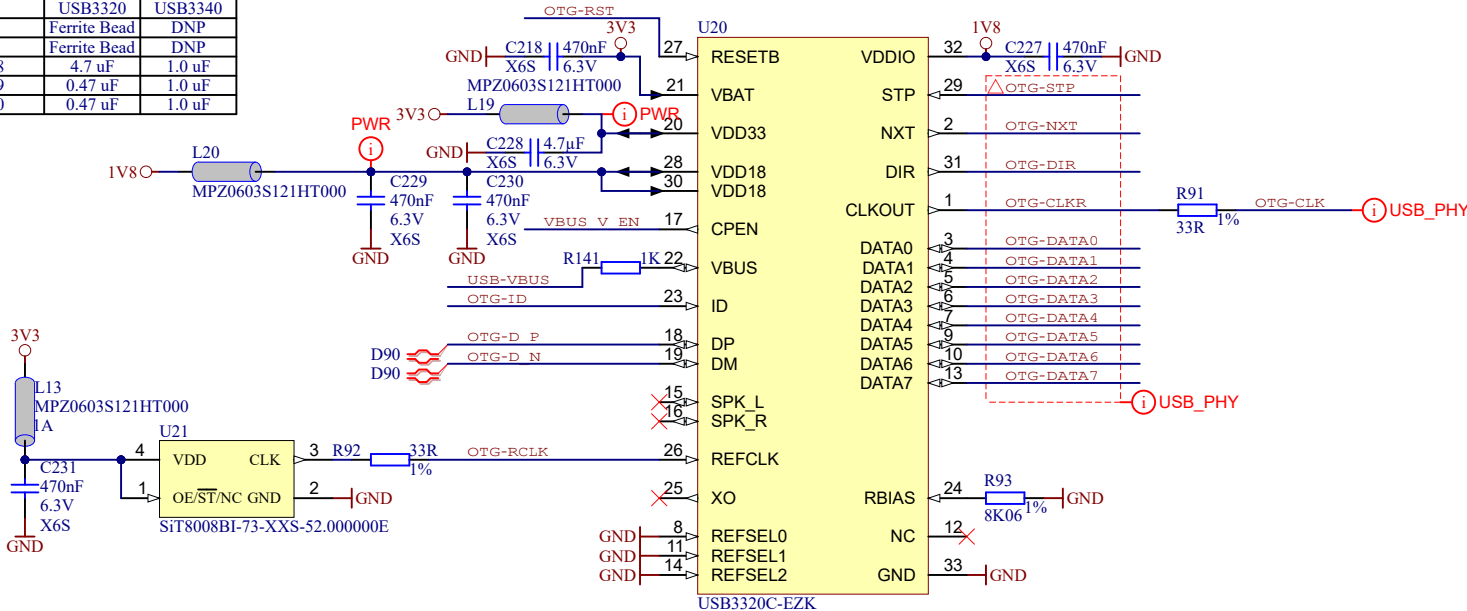
PHY Addr: 0x07
LEDPOL -> Active Low
LEDPOL -> Active Low
MAGJACK normal mode
responds only to assigned PHY Addr.
individual LED mode

Mode:
- Auto-Neg. Enabled
- Auto MDIX Enabled
- EEE Enabled
- Asym & Sym Pause Advertised
CLK125 disabled



Title: TE0861 – ETH1-PHY		
A4	Number: TE0861 6BE51QA	Rev. 01
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	USB3320	USB3340
L19	Ferrite Bead	DNP
L20	Ferrite Bead	DNP
C228	4.7 uF	1.0 uF
C229	0.47 uF	1.0 uF
C230	0.47 uF	1.0 uF



Title:	TE0861 – USB-PHY
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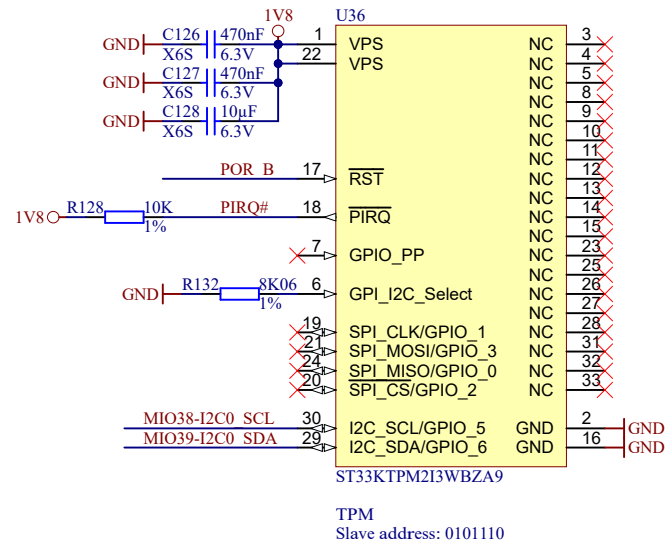
A4	Number: TE0861 6BE51QA
----	---------------------------

Date: 21.11.2025	Copyright: Trenz Electronic GmbH
------------------	----------------------------------

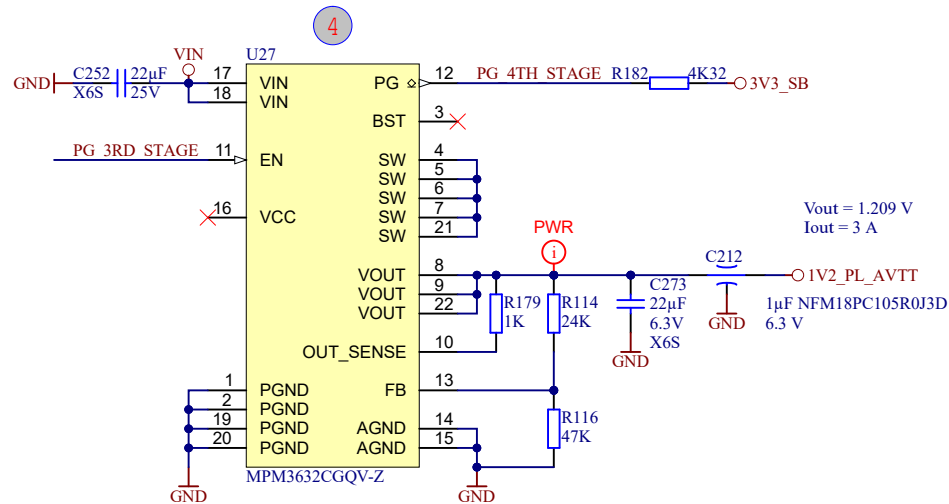
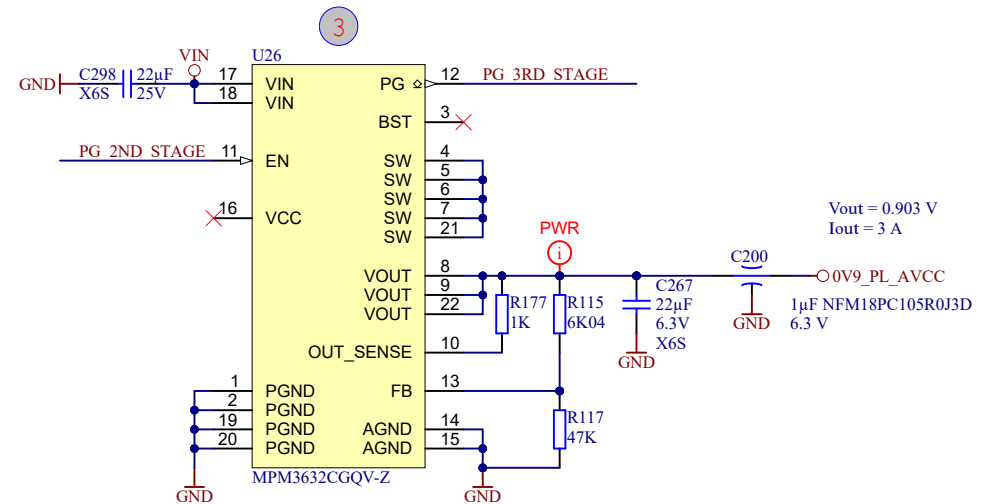
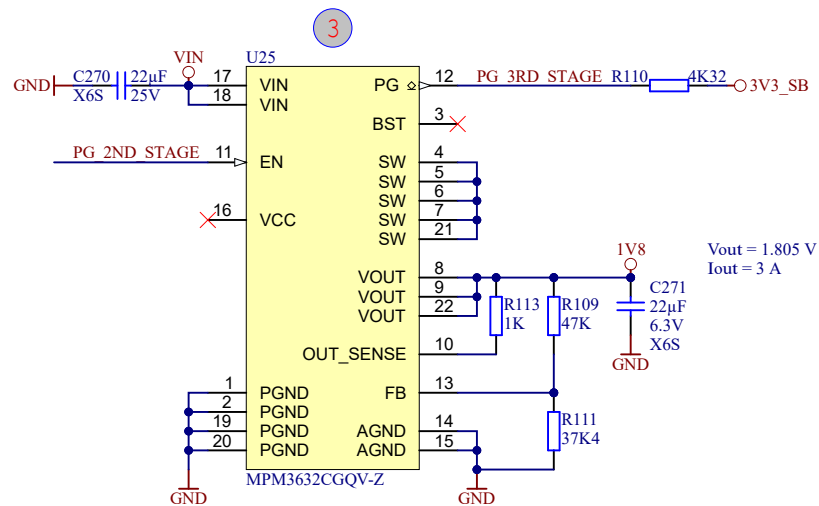
Filename: USB-PHY.SchDoc

Rev.	01
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Title: TE0861 – TPM		
A4	Number: TE0861 6BE51QA	Rev. 01
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Title: TE0861 – POWER 2		
A4	Number: TE0861 6BE51QA	Rev. 01
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Filename: POWER_2.SchDoc		



