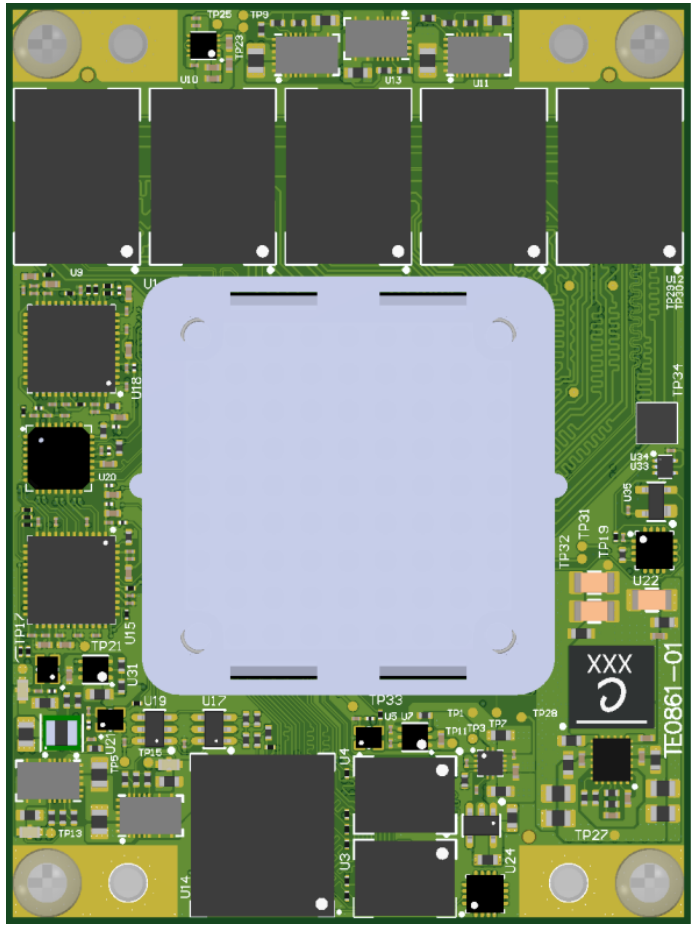

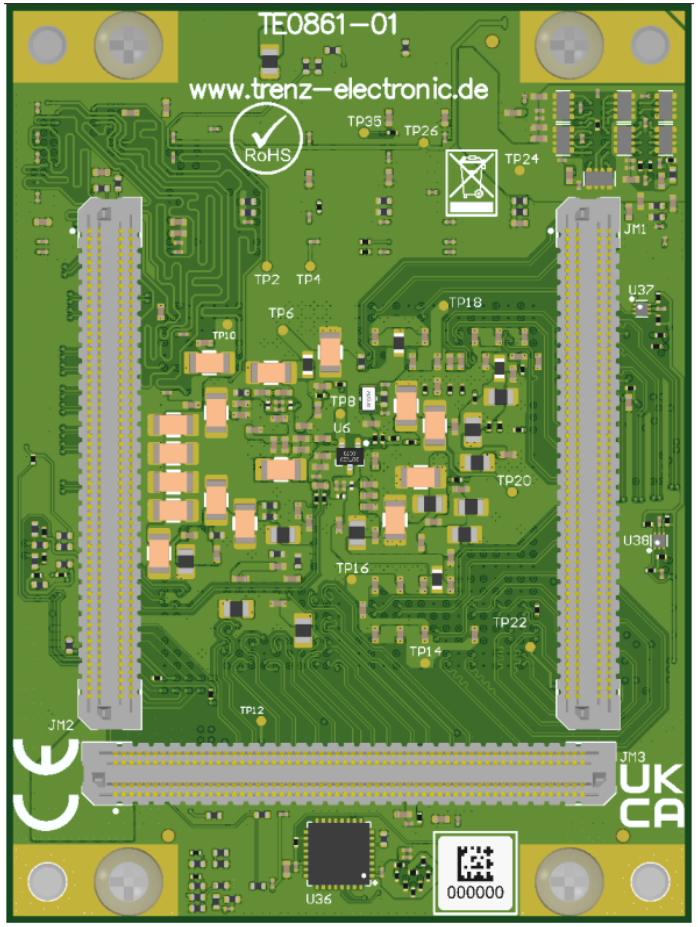

Regarding the usage of our schematics and alike documentation for Trenz module TE0861.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.

TE0861 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0861 – Legal Notices Modules		
	A4	Number: TE0861 6BI61QA	Rev. 01
	Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 1 of 35
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	ED/VY

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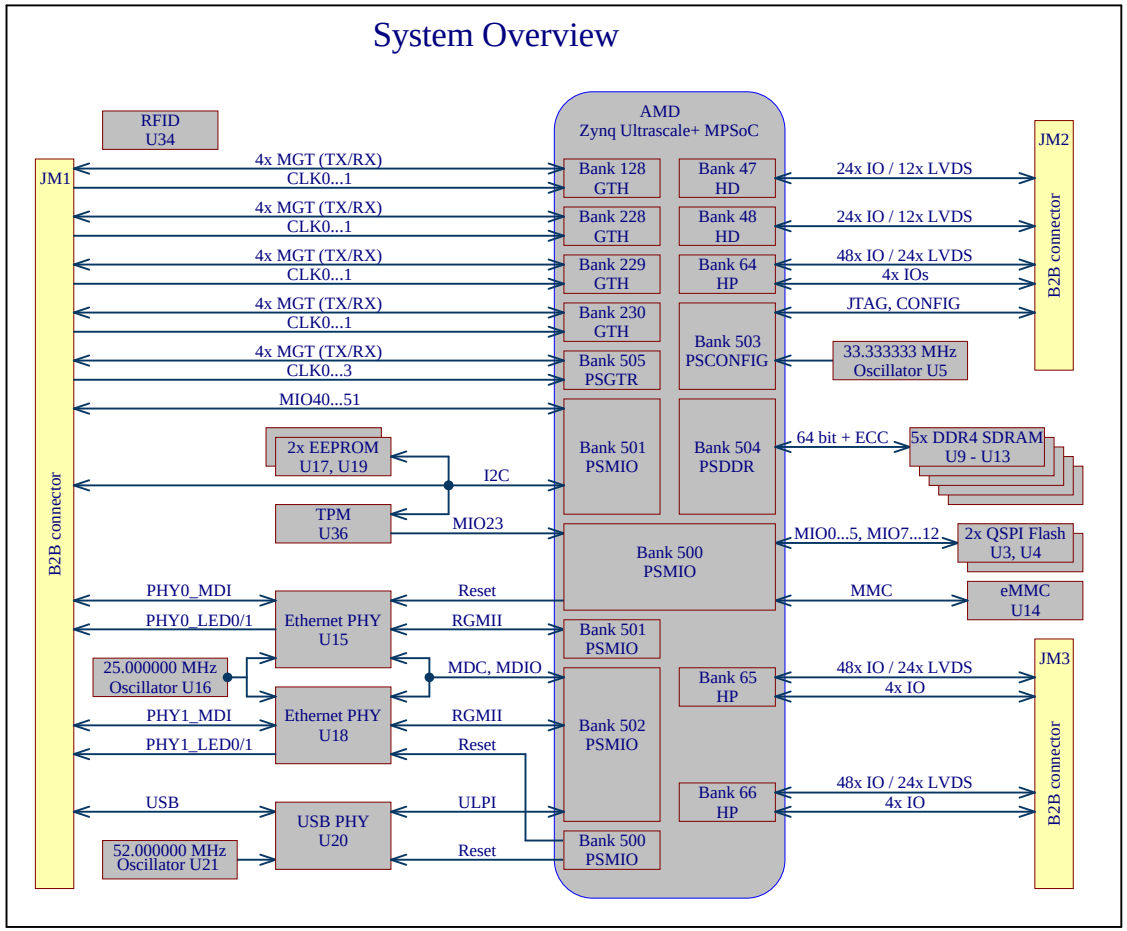
Title: TE0861 – Revision Changes		
A4	Number: TE0861 6BI61QA	Rev. 01
Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 2 of 35
Filename: Revision_Changes.SchDoc		

System Overview



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	5 V - 12 V	+/- 10 %	Module main power supply	-
VCCO_47	IN	1.2 V - 3.3 V	1)	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	1)	HD IO Bank 48	-
VCCO_64	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V ... 1.8 V	+/- 5 %	HP IO Bank 66	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
3V3	OUT	3.3 V	+/- 3 %	Periphery supply	-
1V8	OUT	1.8 V	+/- 3 %	Periphery supply	-

1) +/- 5 %, - 5 % / +3 % for 3.3 V

I2C Addresses:

Device	Address	Note
MPSoC U1H	-	AMD Zynq Ultrascale+ MPSoC PS
B2B JM1A	-	B2B connector
TPM U36	0x2E	Trusted Platform Modul
EEPROM U17	0x50	MAC-EEPROM with user area
EEPROM U19	0x51	MAC-EEPROM with user area

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_POWER_1
POWER_1.SchDoc

U_POWER_2
POWER_2.SchDoc

U_POWER_3
POWER_3.SchDoc

U_POWER_4
POWER_4.SchDoc

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Title: TE0861 – System Overview

A4	Number: TE0861 6BI61QA	Rev. 01
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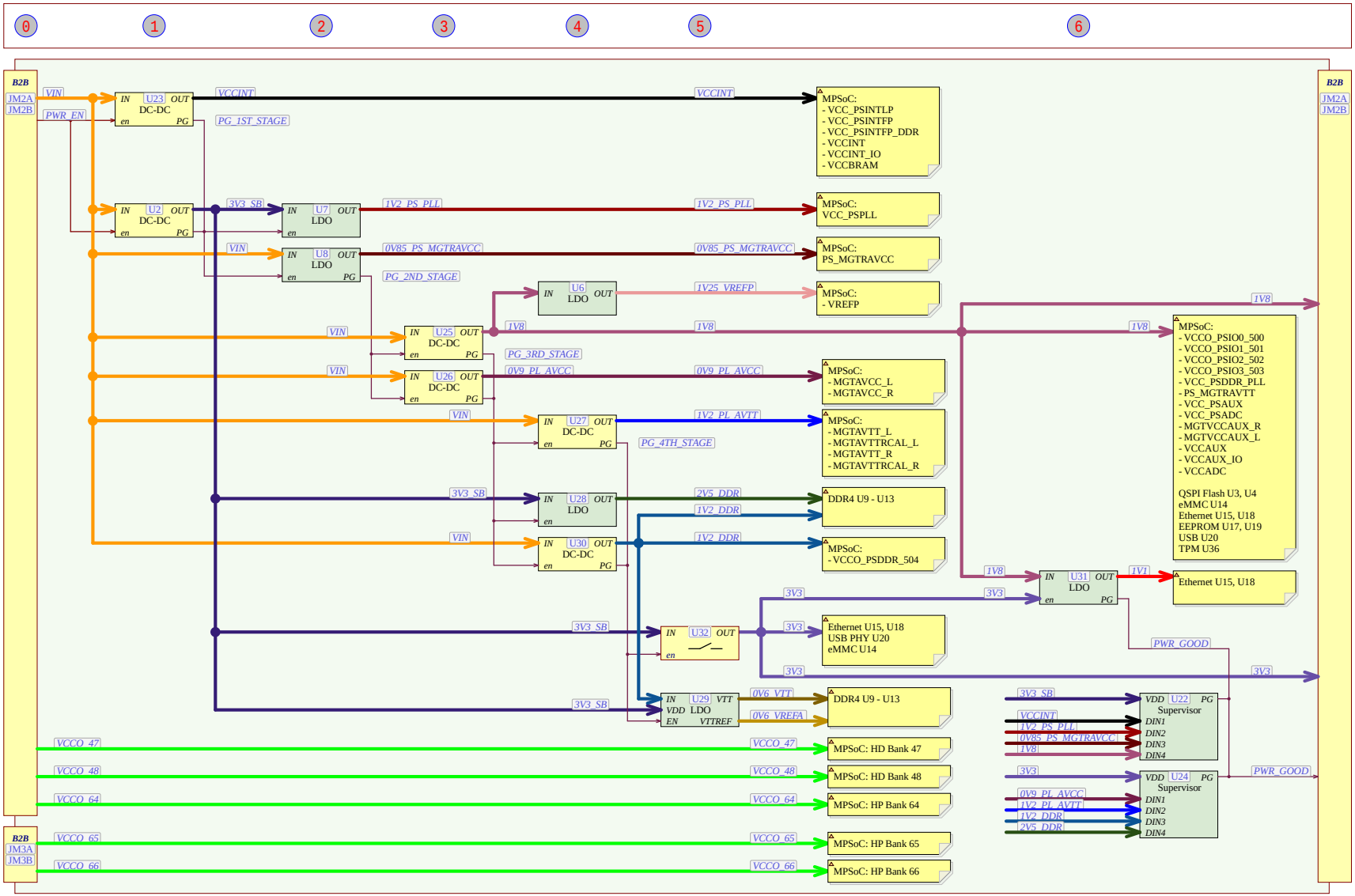
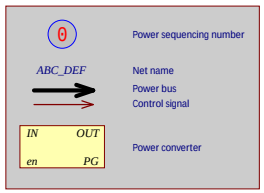
Filename: TE0861-Overview.SchDoc		

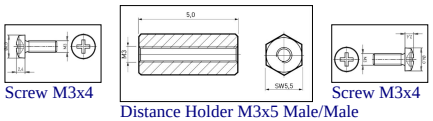
Power Supply and Power Sequencing

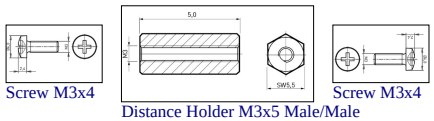


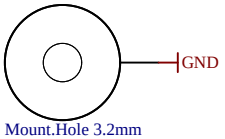


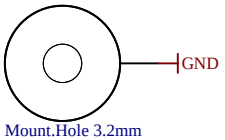
Title: TE0861 – POWER Overview			
A3	Nummer: TE0861 6BI61QA		Rev. 01
Datum: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 4 of 35
Filename: POWER_Overview.SchDoc			

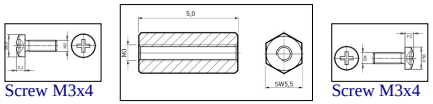
Special notes:

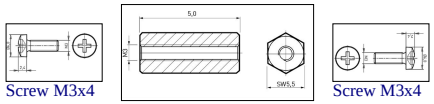












Serial1
Serial
Serialnumber 6,3 x 6.3mm
RoHS1

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY
WEEE1

WEEE Logo on Top Overlay

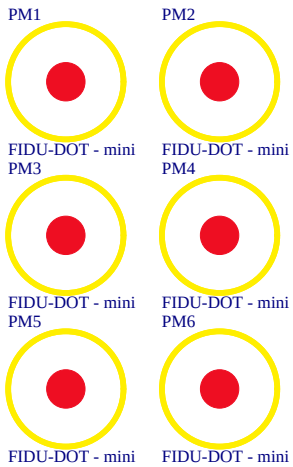
WEEE-TOPOVERLAY
CE1

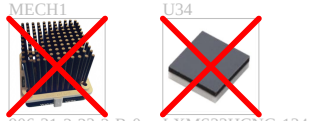
CE Logo on Top Overlay

CE-TOPOVERLAY
UKCA1

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY





Design drawn by:	ED
Checked by:	MR
Assembly variant:	6BI61QA
Created by:	ED
Modified by:	ED
Modified at:	2025-10-01

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Title: TE0861		
A4	Number: TE0861 6BI61QA	Rev. 01
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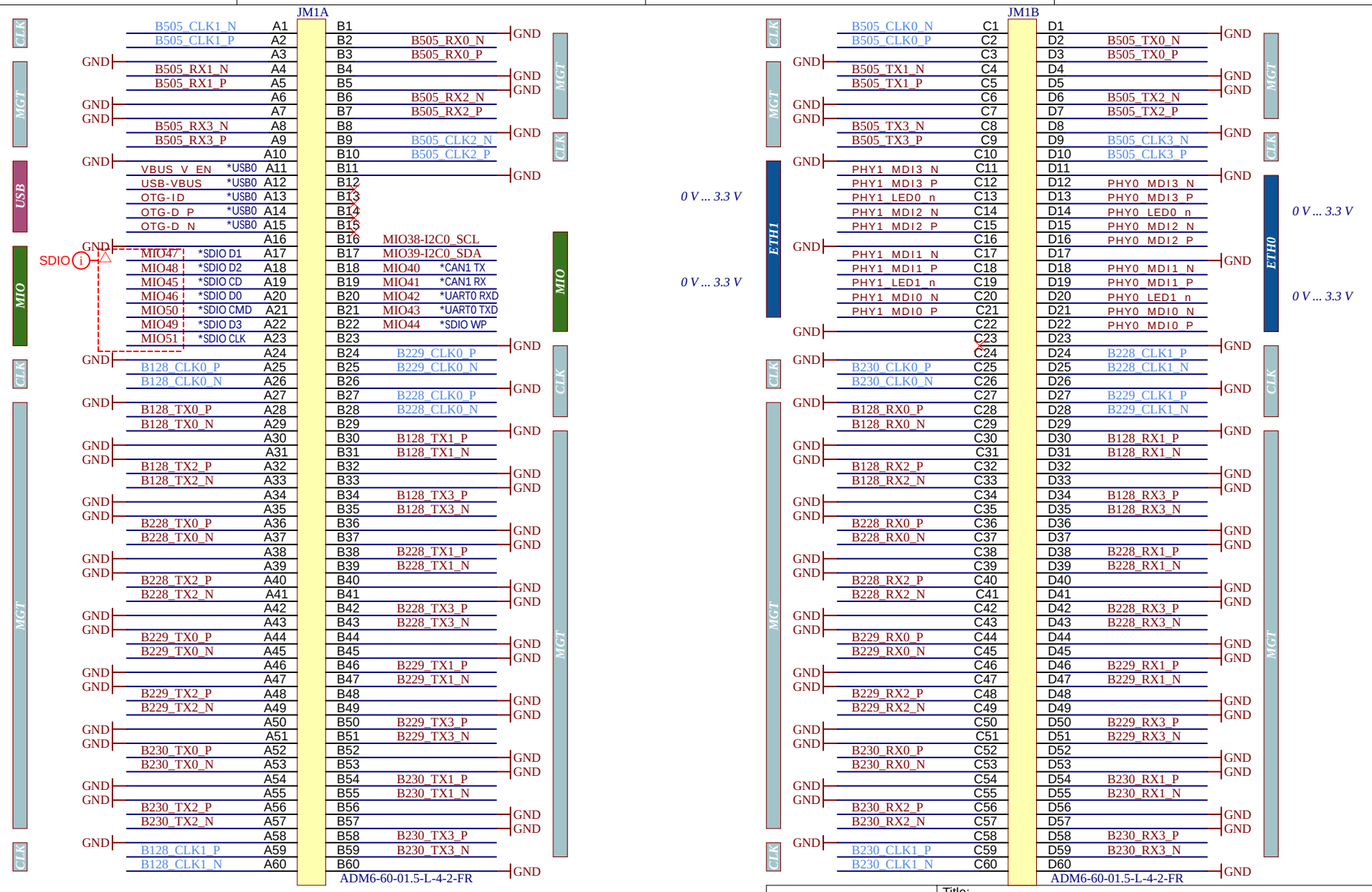
Filename: TE0861.SchDoc		



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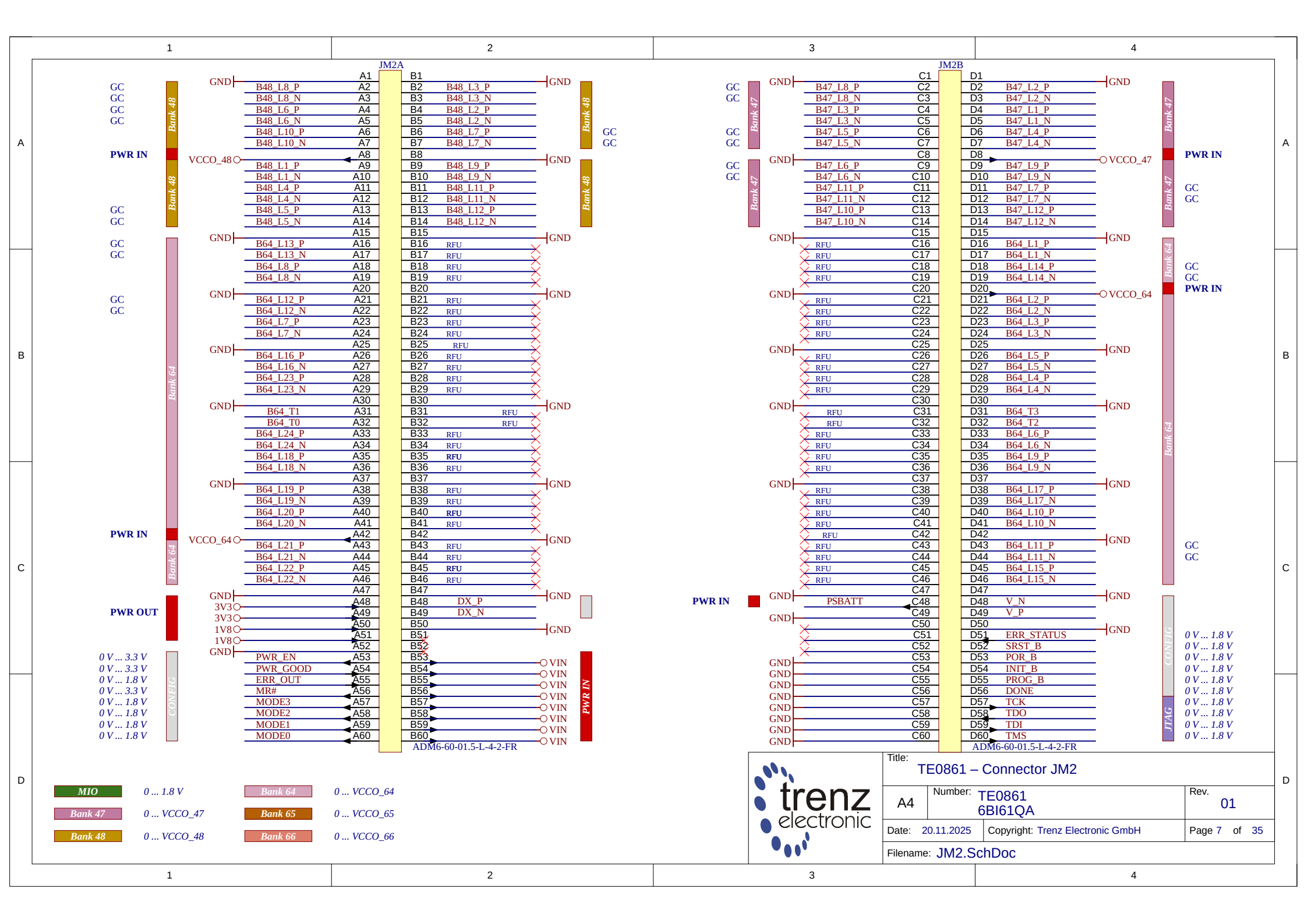
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 6 of 35
Filename: JM1.SchDoc			



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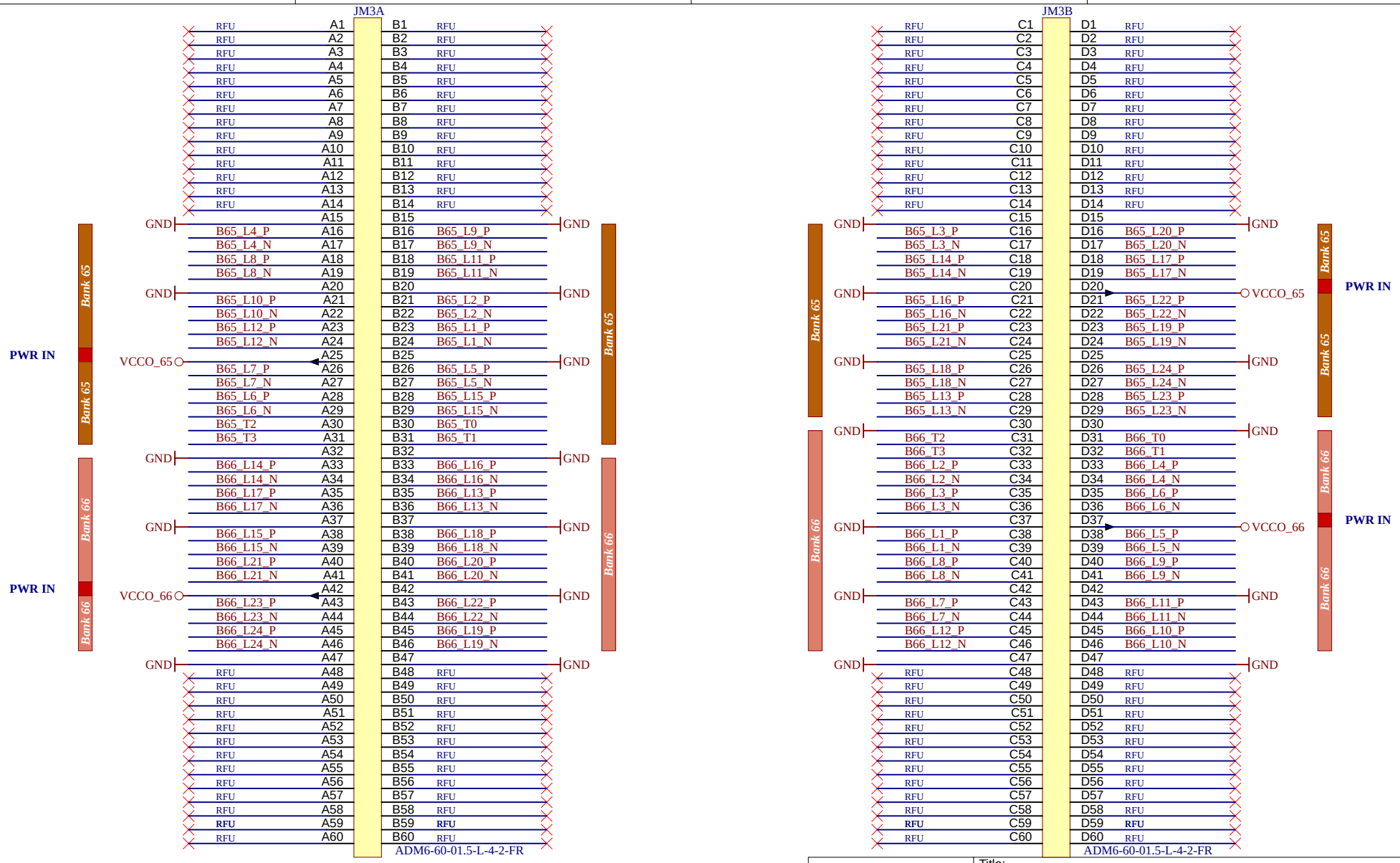
	Rev. 01
Date: 20.11.2025	Copyright: Trenz Electronic GmbH
	Page 7 of 35
Filename:	JM2.SchDoc



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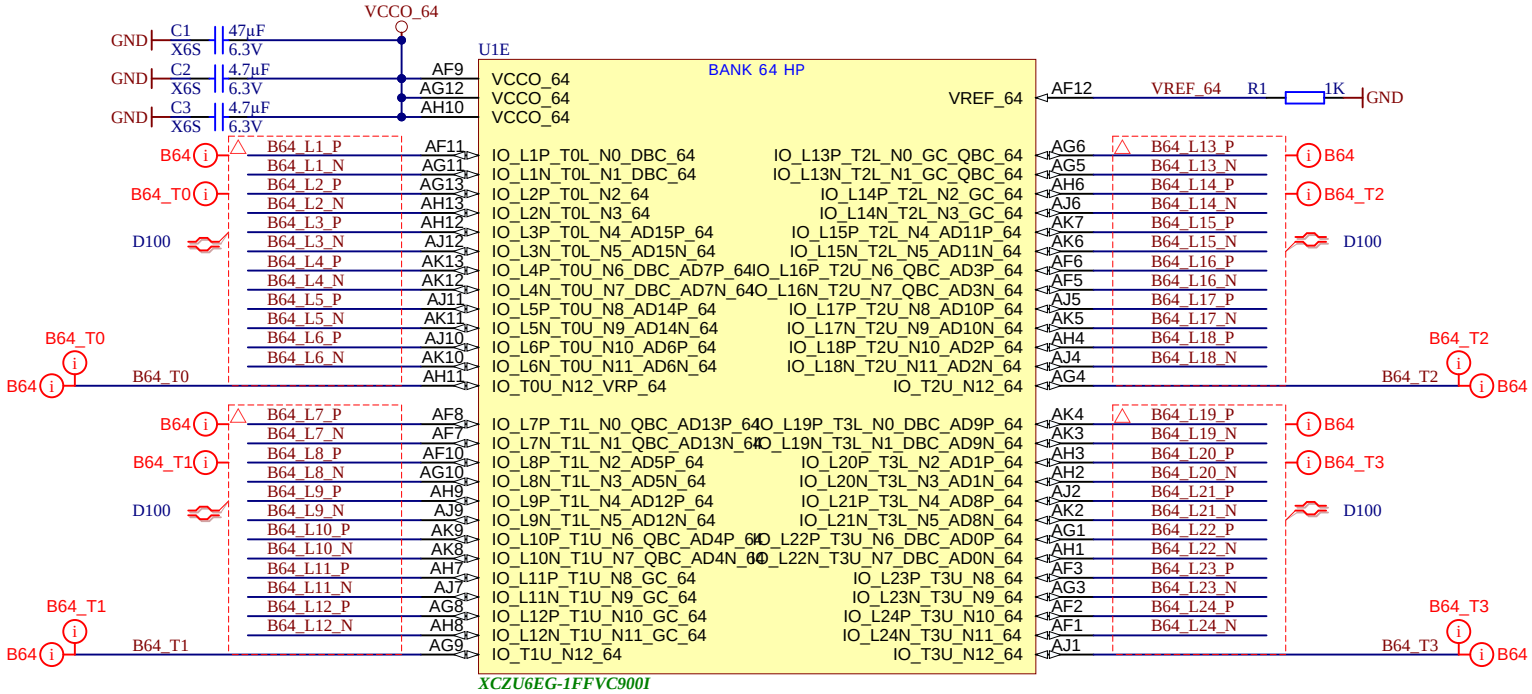
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 8 of 35
Filename: JM3.SchDoc			



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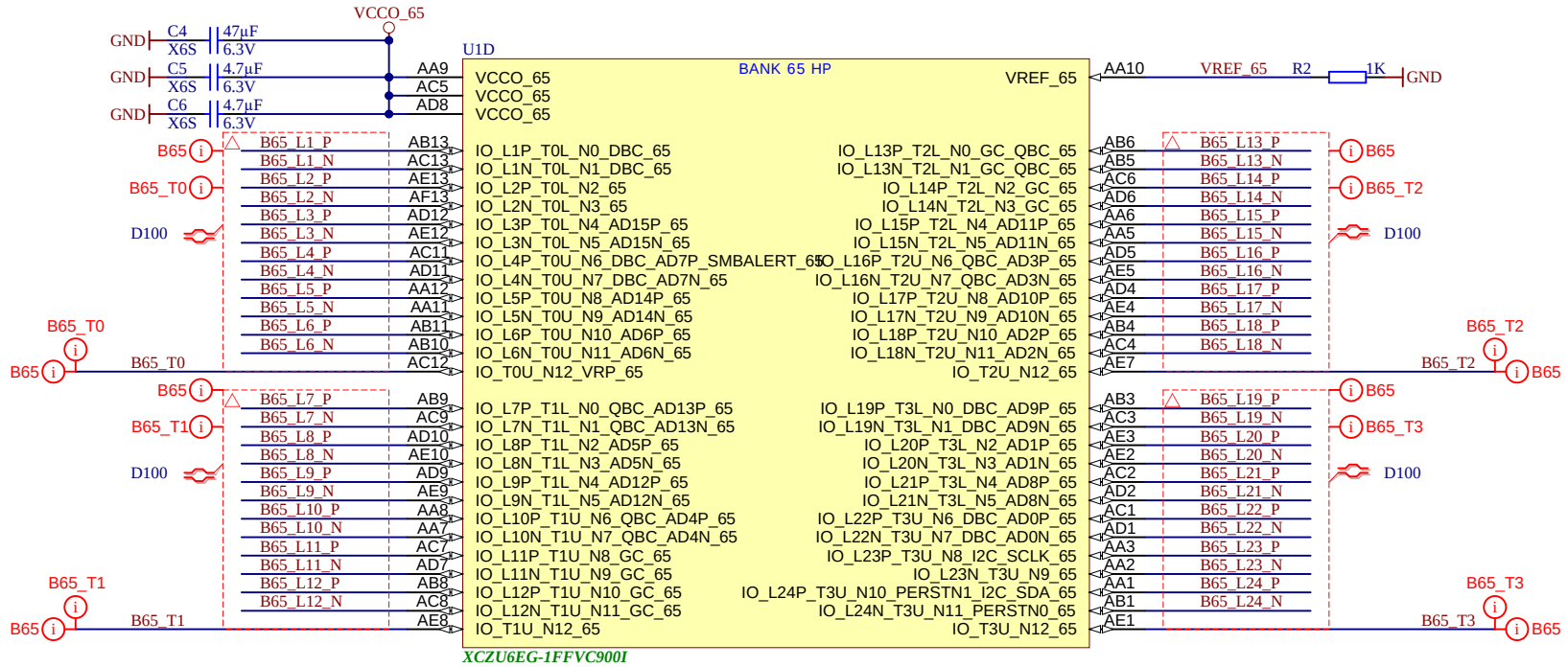
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 9 of 35
Filename: B64.SchDoc			



trenz electronic	Title: TE0861 – B65		
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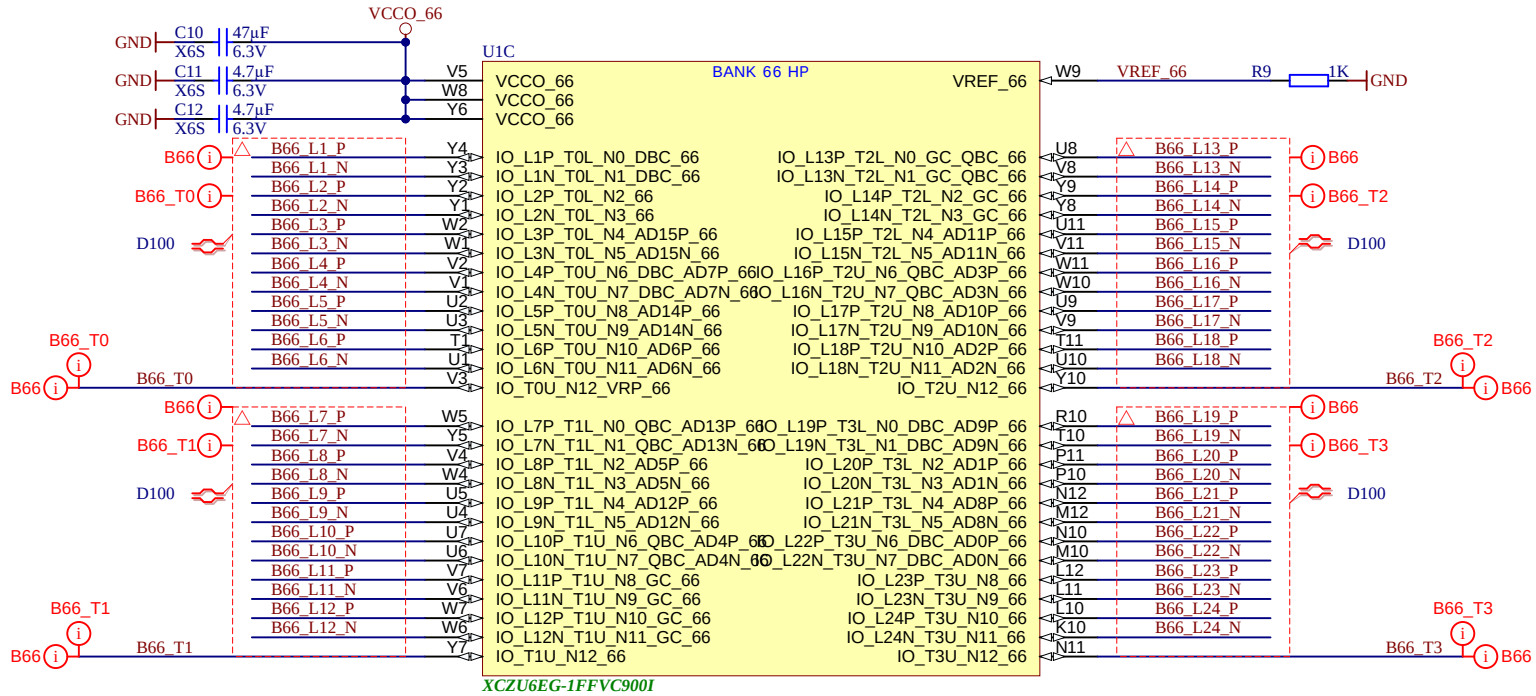
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 10 of 35
Filename: B65.SchDoc			



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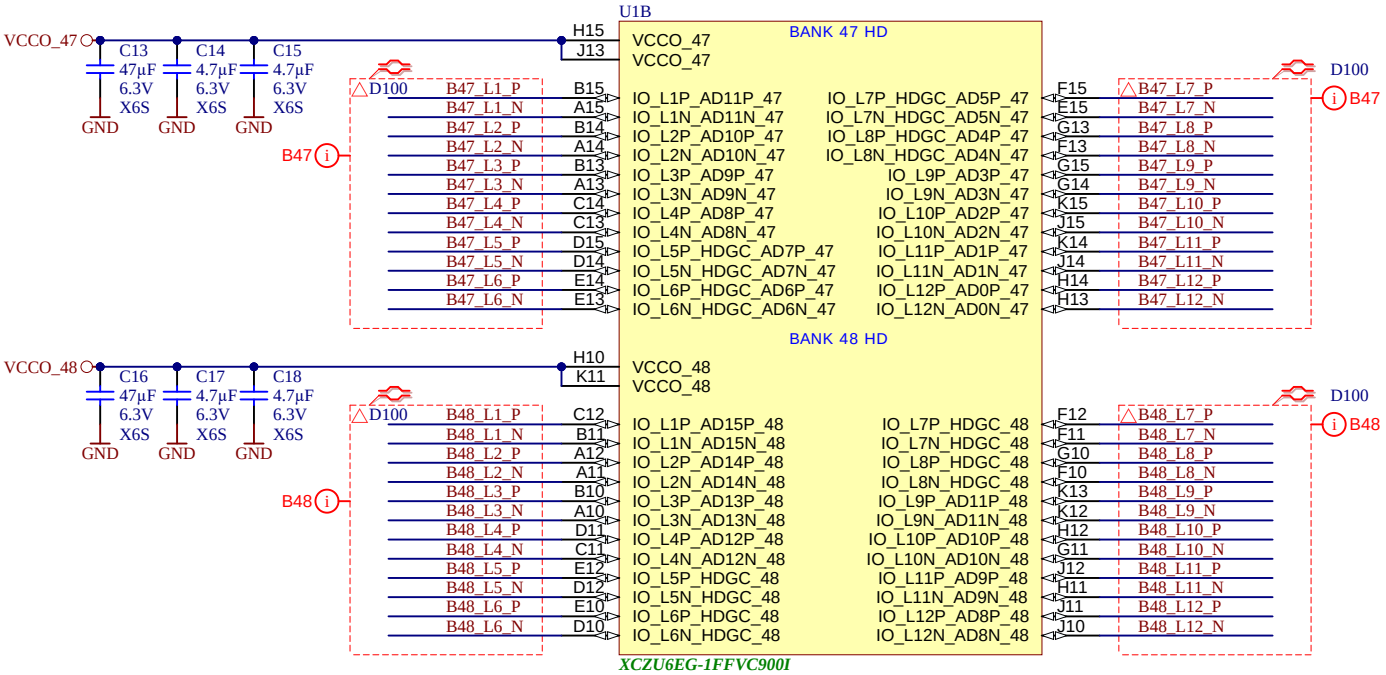
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 11 of 35
Filename: B66.SchDoc			



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Title: TE0861 – B_HD		
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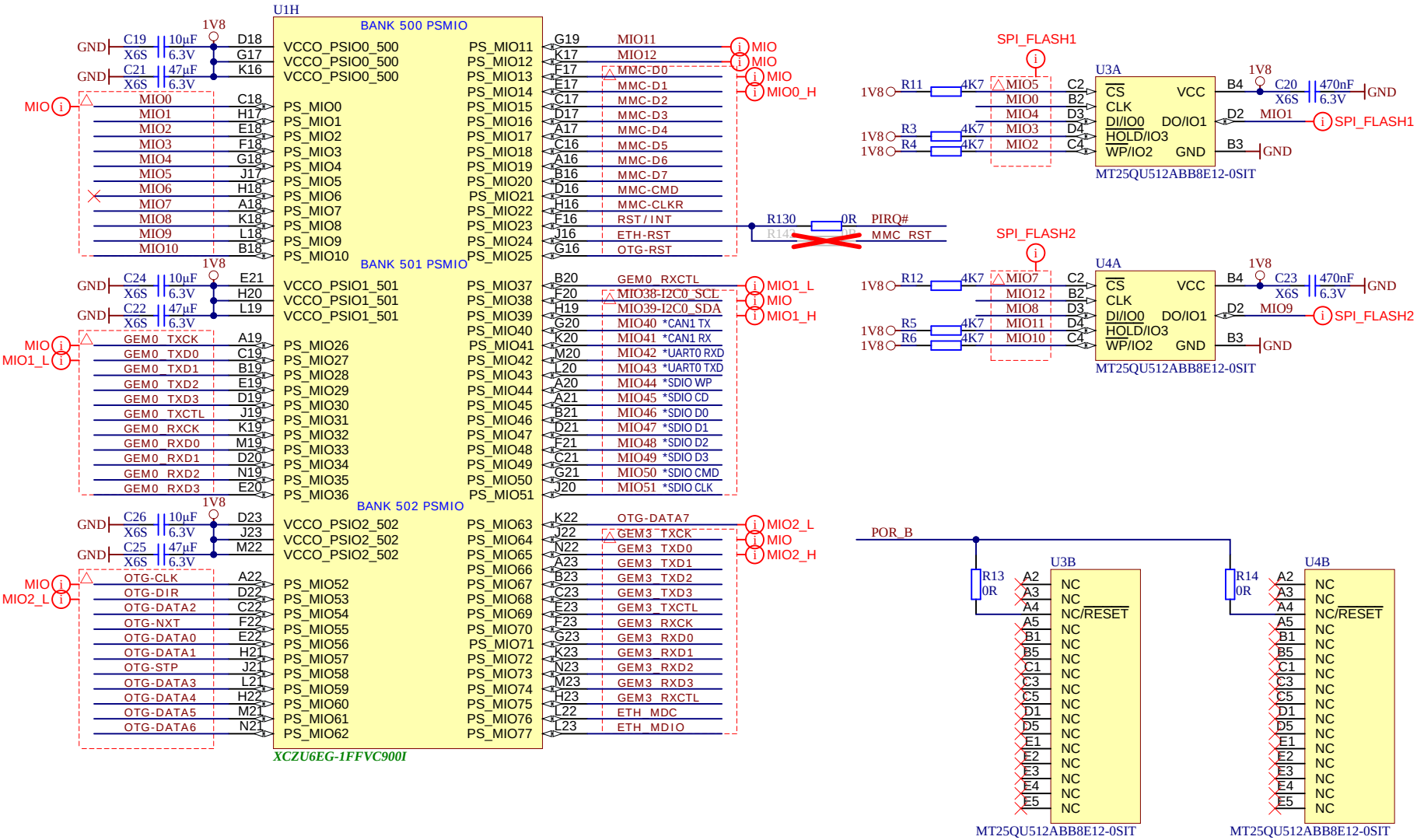
Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 12 of 35
Filename: B_HD.SchDoc		



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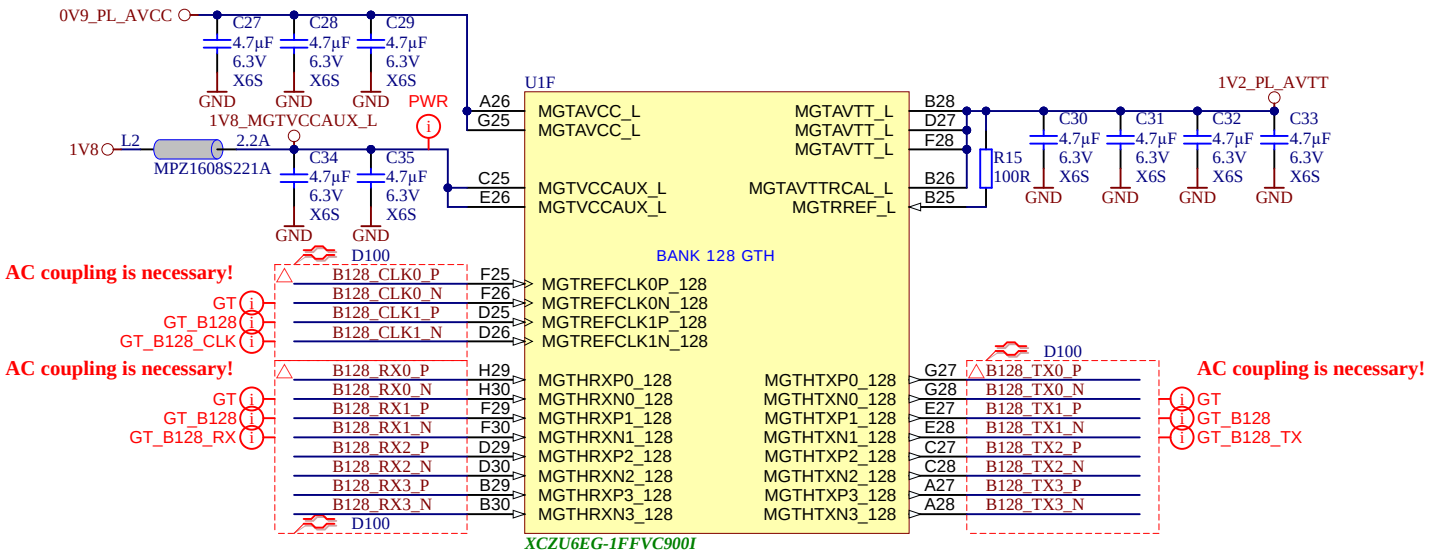
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 13 of 35
Filename: B_MIO.SchDoc			



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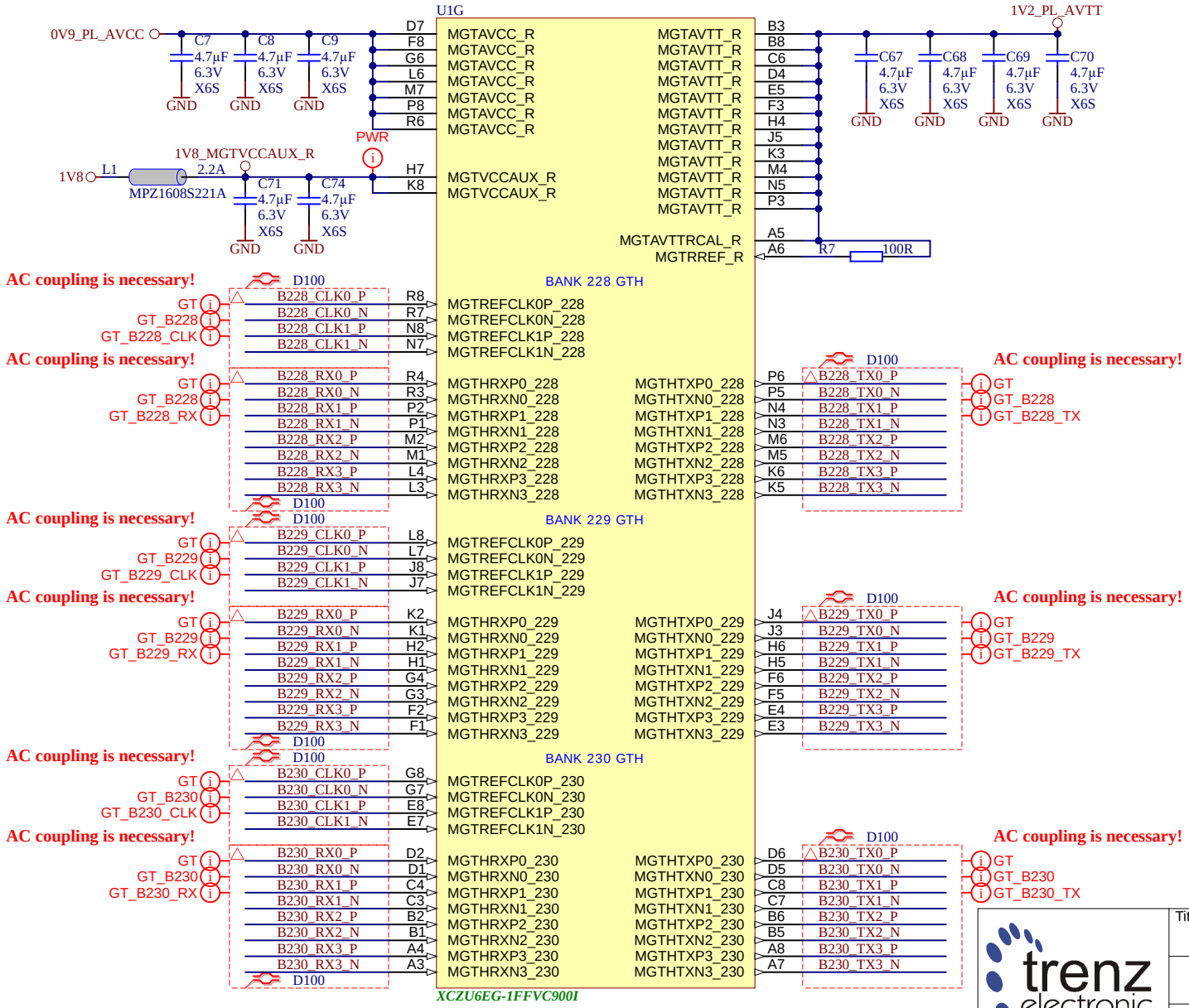
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 14 of 35
Filename: B_GT_L.SchDoc			



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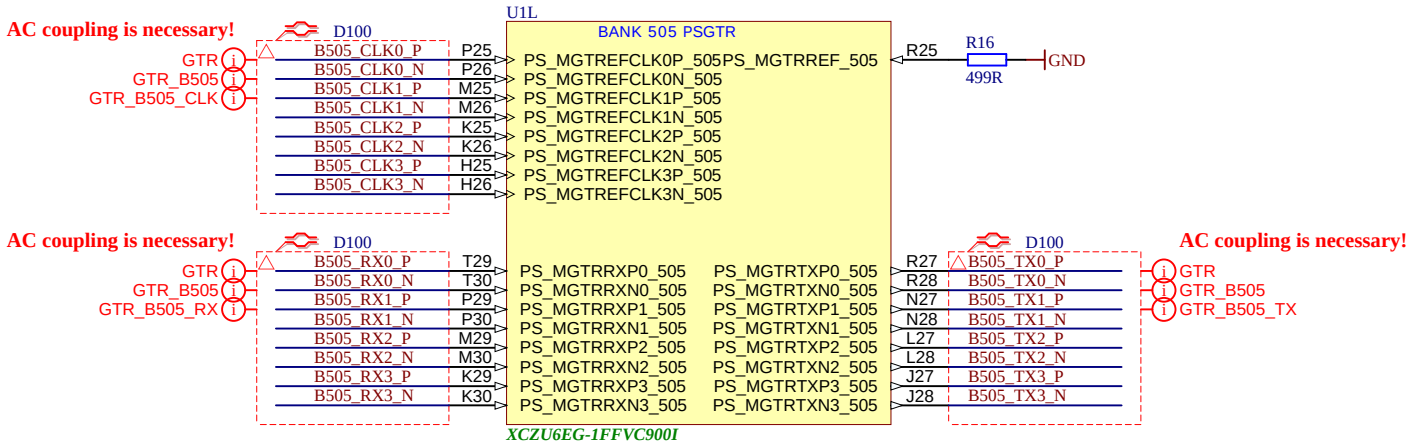
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 15 of 35
Filename: B_GT_R.SchDoc			



trenz electronic	Title: TE0861 – B_PS_GT		
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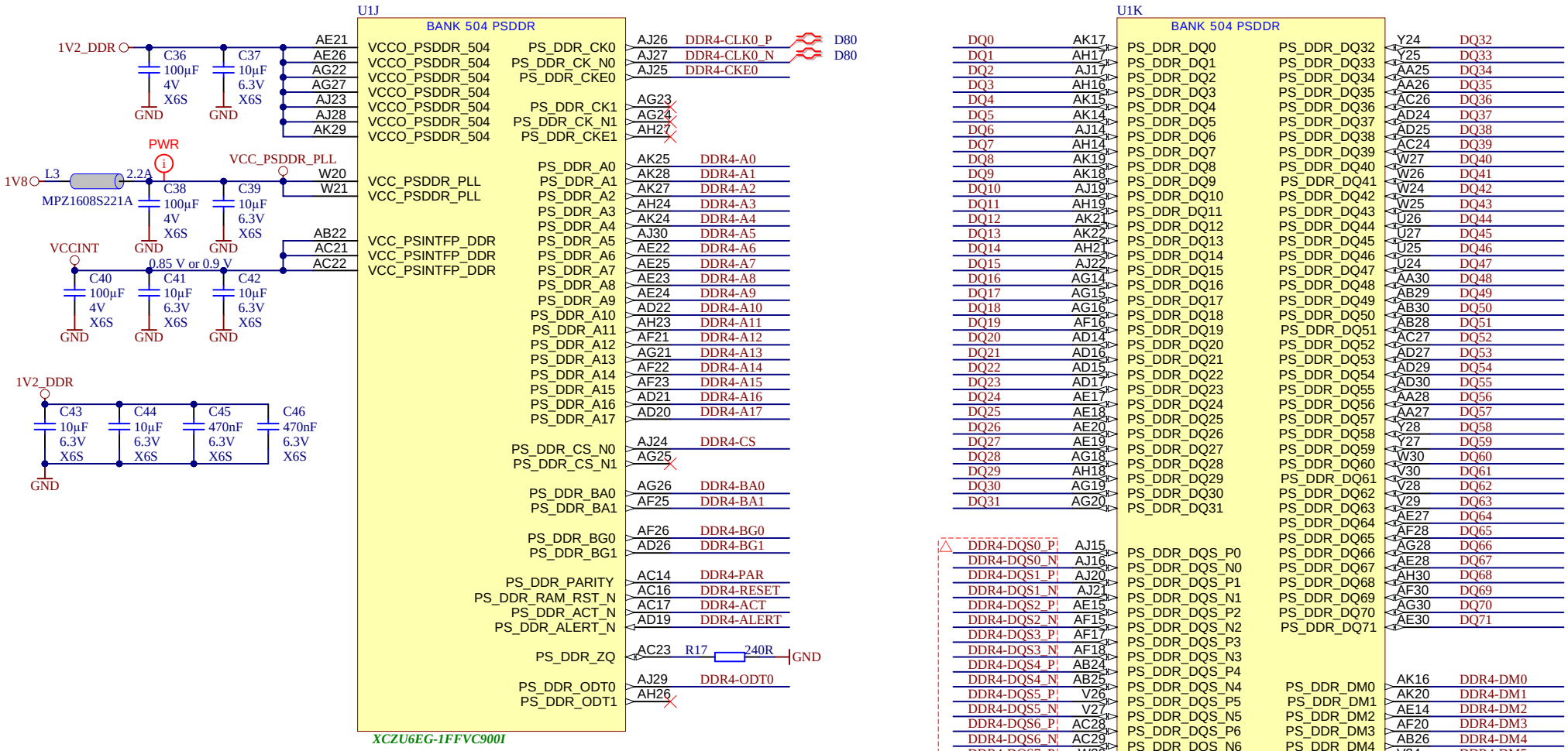
	Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 16 of 35
	Filename: B_PS_GT.SchDoc		



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Title: TE0861 – PS_DDR		
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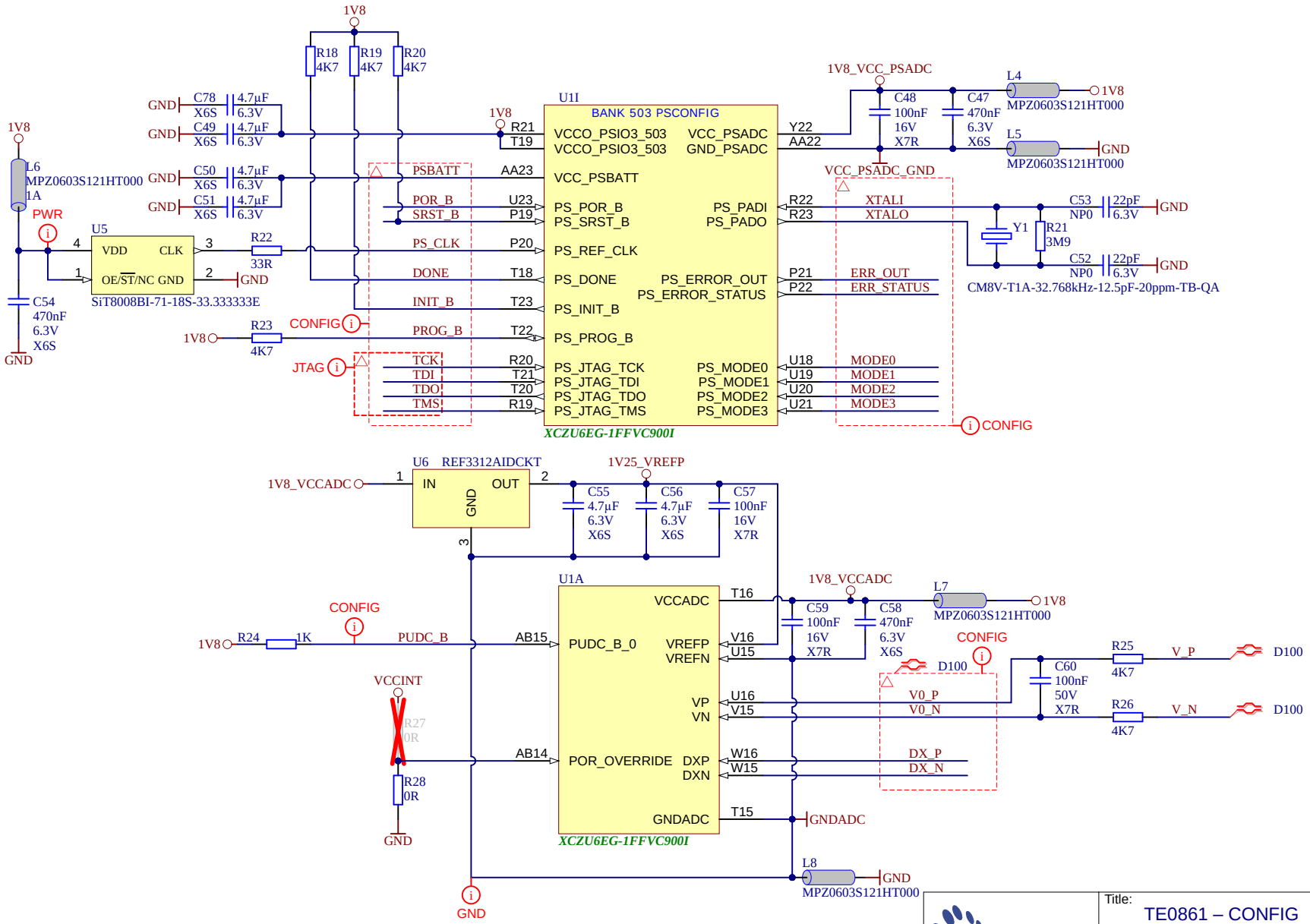
Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 17 of 35
Filename: PS_DDR.SchDoc		



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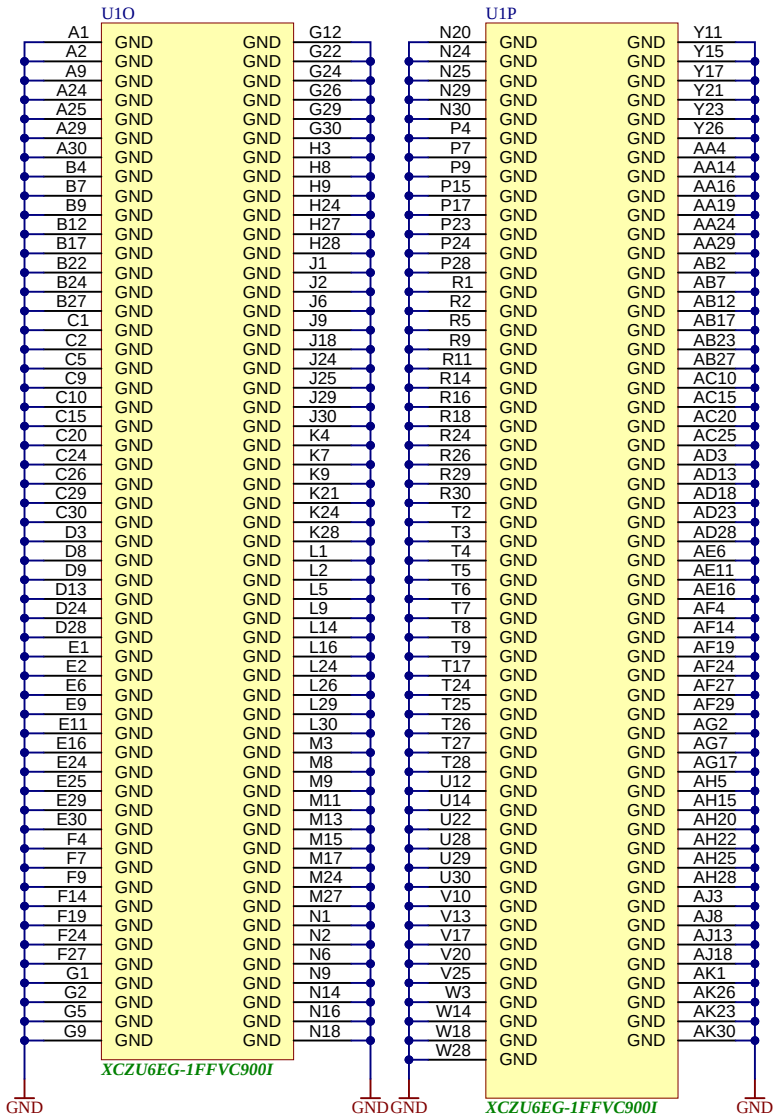
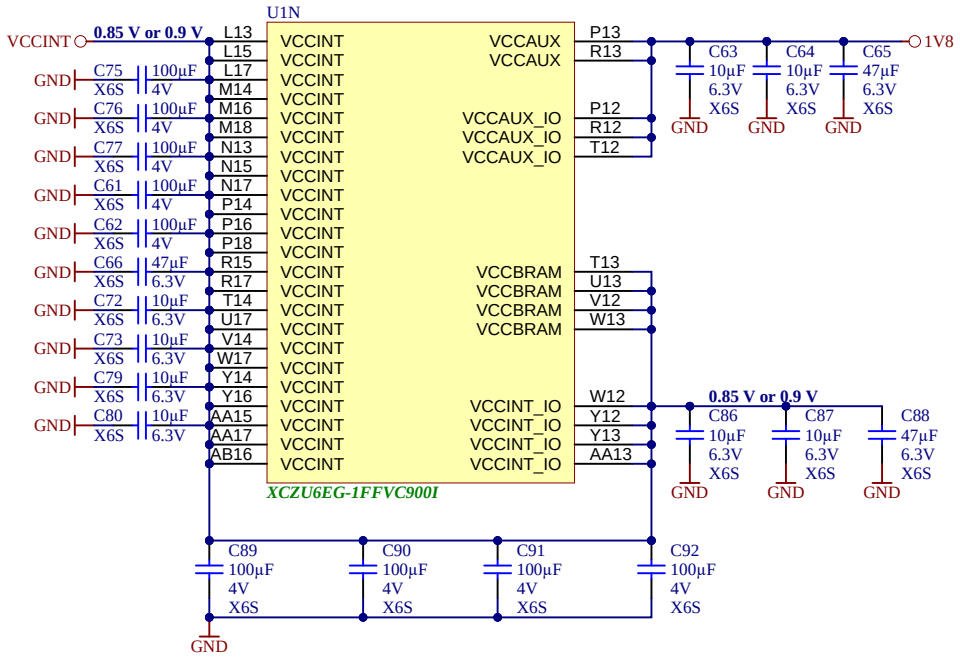
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 18 of 35
Filename: CONFIG.SchDoc			





Title: TE0861 – ZU_POWER			
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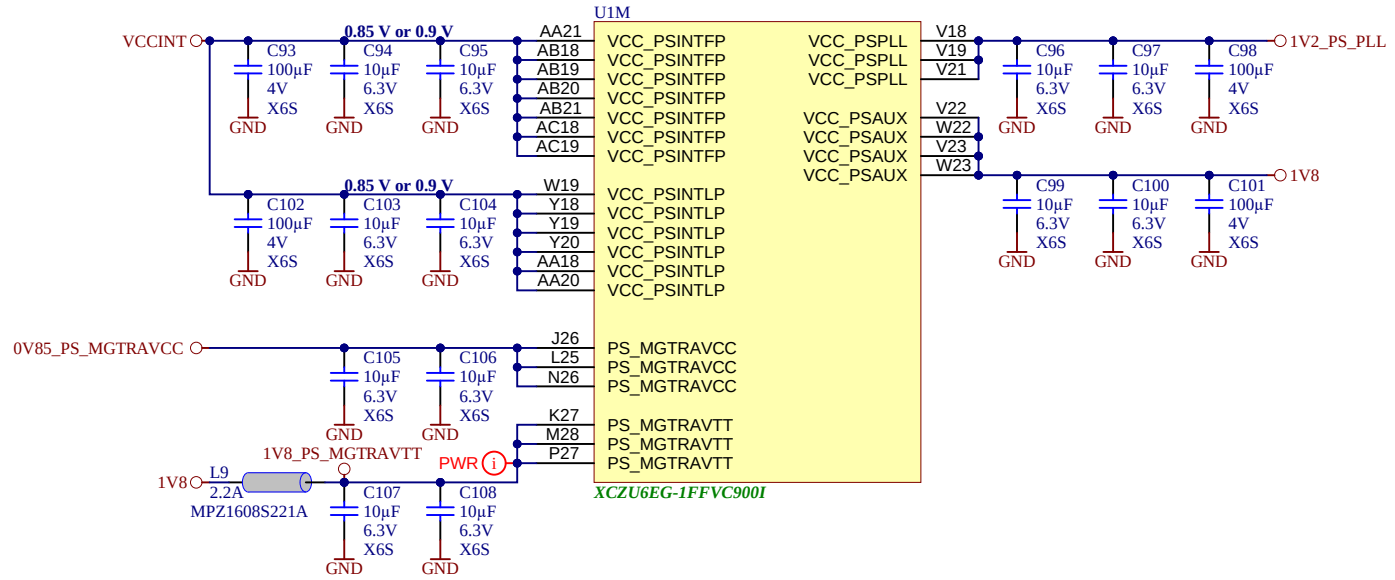
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 19 of 35
Filename: ZU_POWER.SchDoc			



trenz electronic	Title: TE0861 – ZU_PS_POWER		
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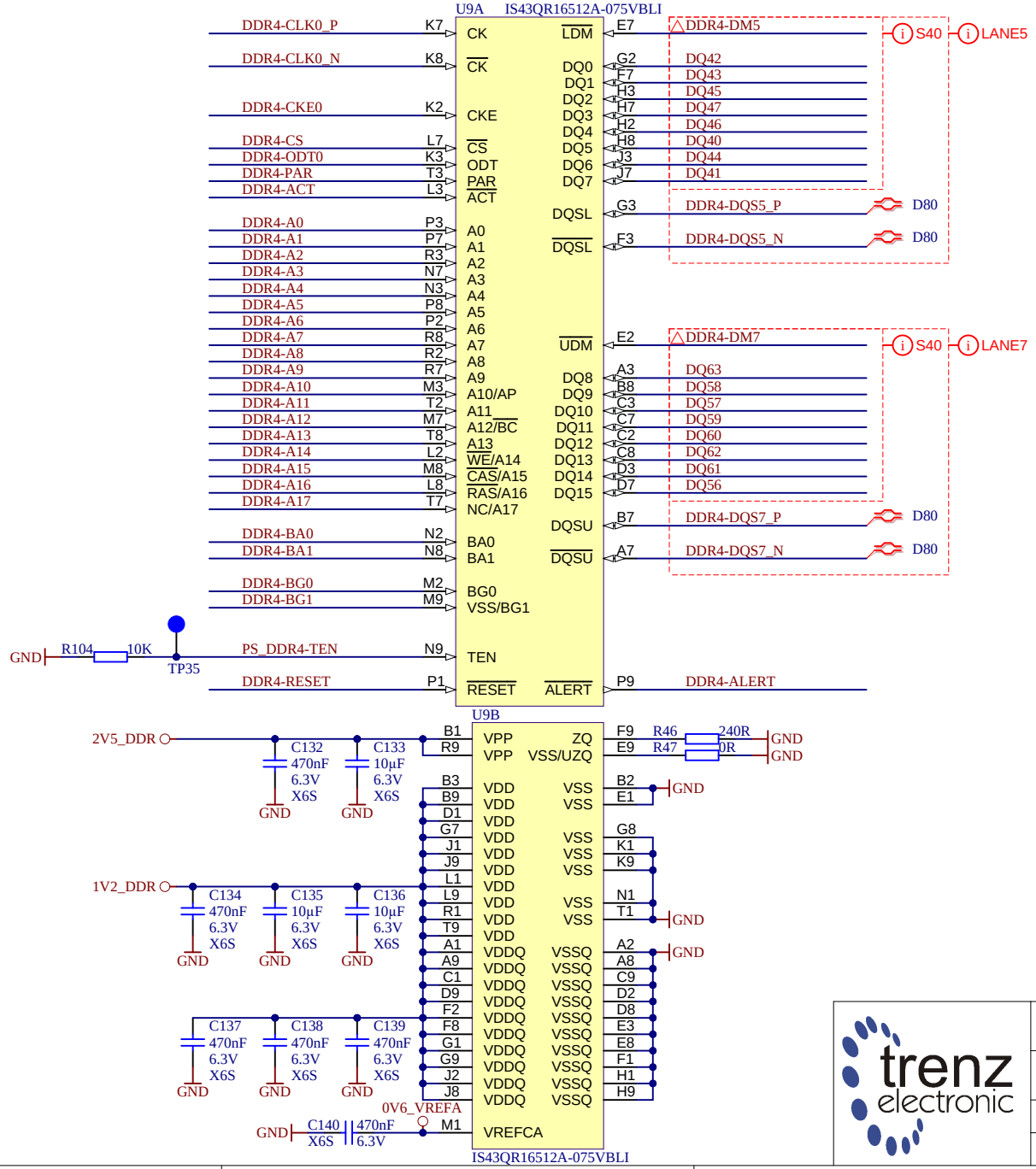
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 20 of 35
Filename: ZU_PS_POWER.SchDoc			



Title: TE0861 – DDR4-RAM_1			
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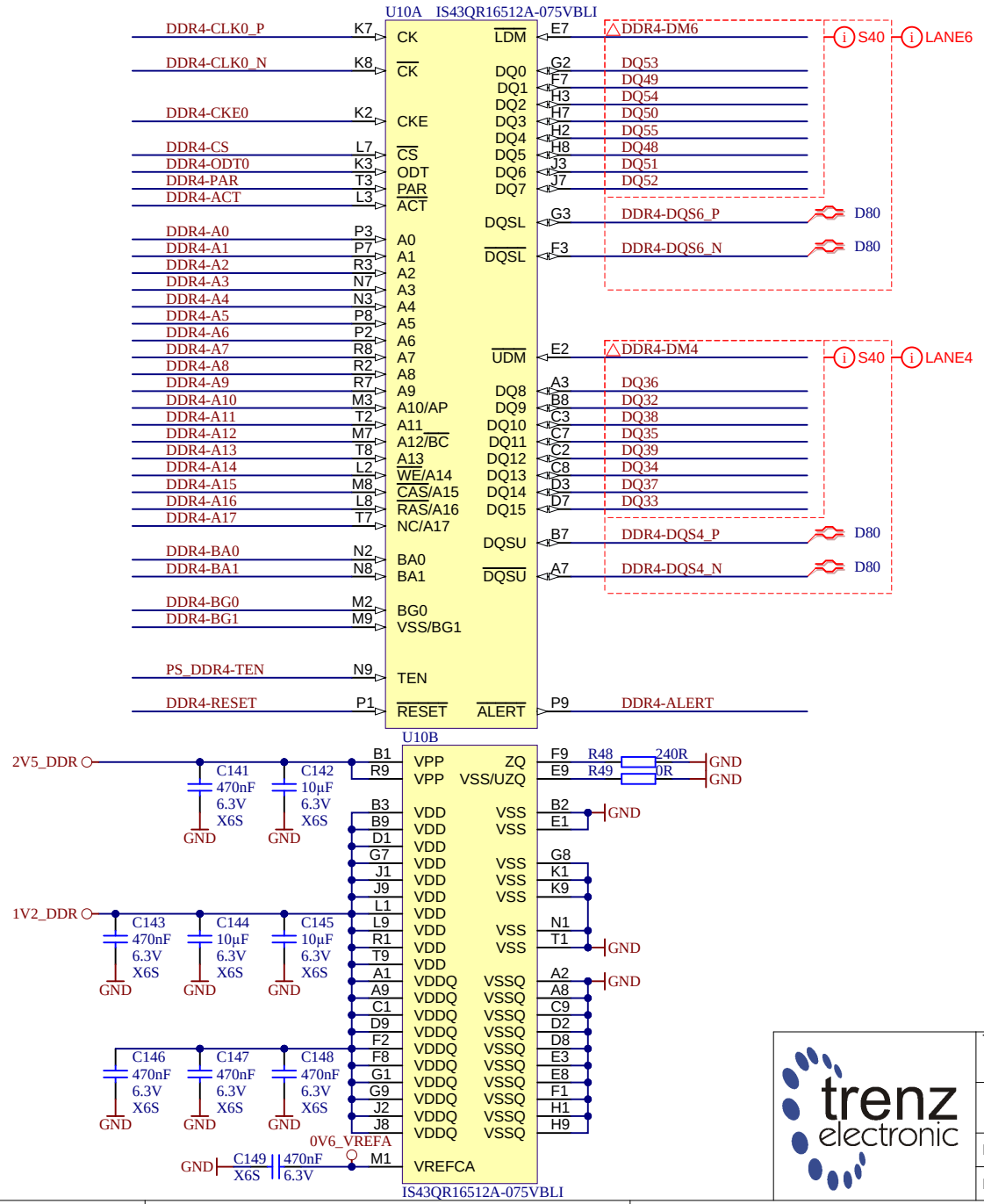
Date: 17.12.2025	Copyright: Trenz Electronic GmbH		Page 21 of 35
Filename: DDR4-RAM_1.SchDoc			



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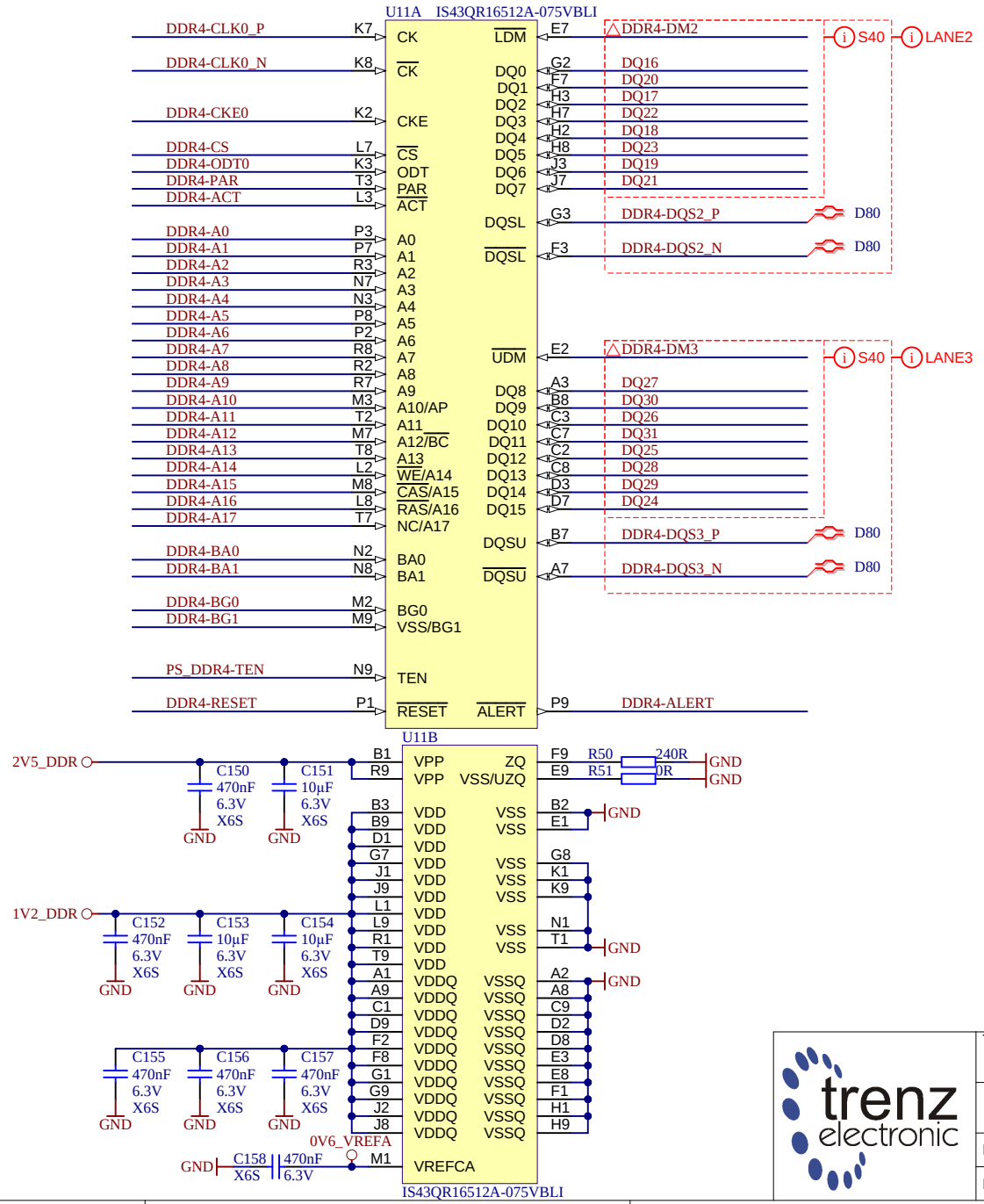
Filename: DDR4-RAM_2.SchDoc			



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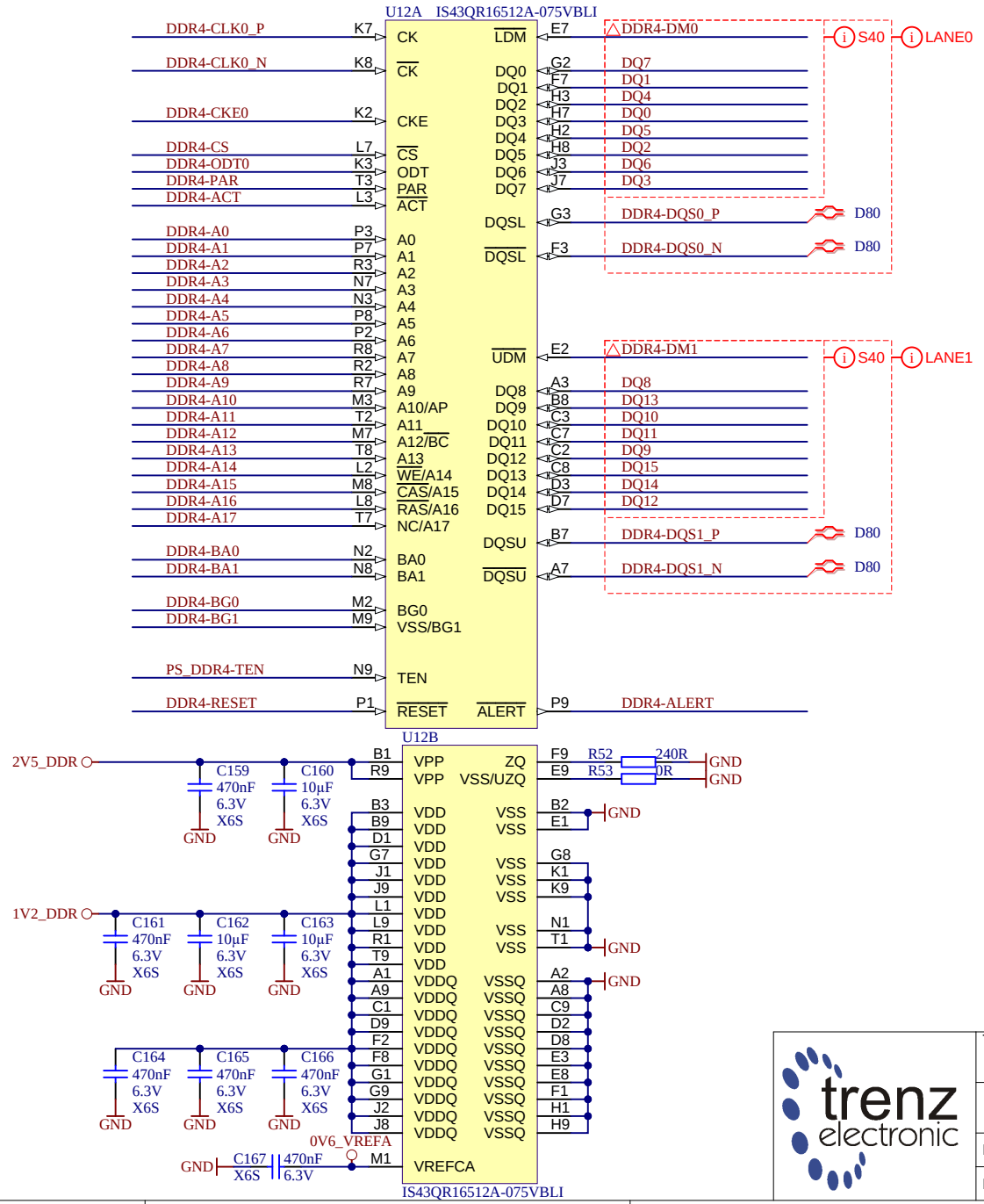
Date: 17.12.2025	Copyright: Trenz Electronic GmbH		Page 23 of 35
Filename: DDR4-RAM_3.SchDoc			



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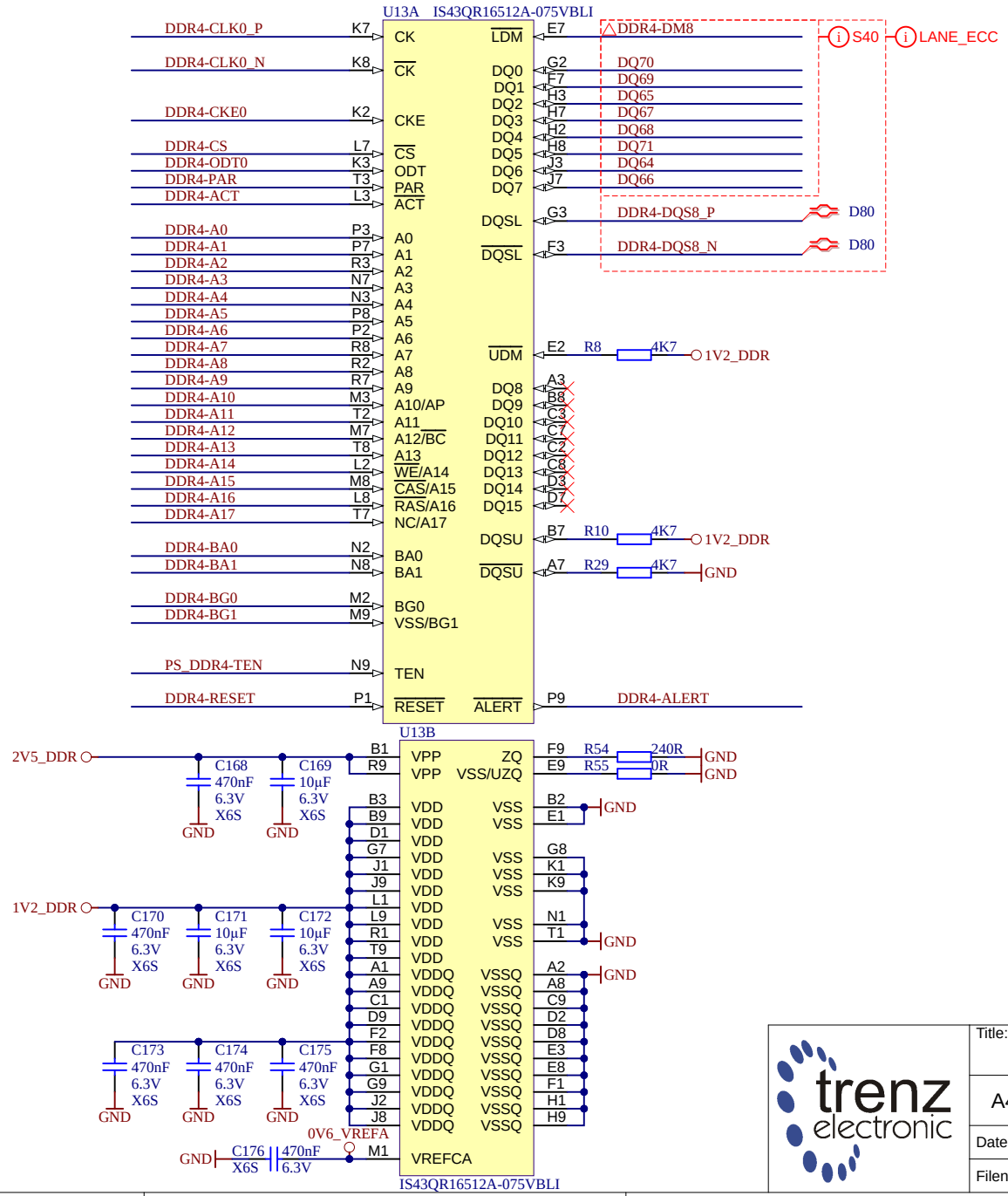
Date: 17.12.2025	Copyright: Trenz Electronic GmbH		Page 24 of 35
Filename: DDR4-RAM_4.SchDoc			



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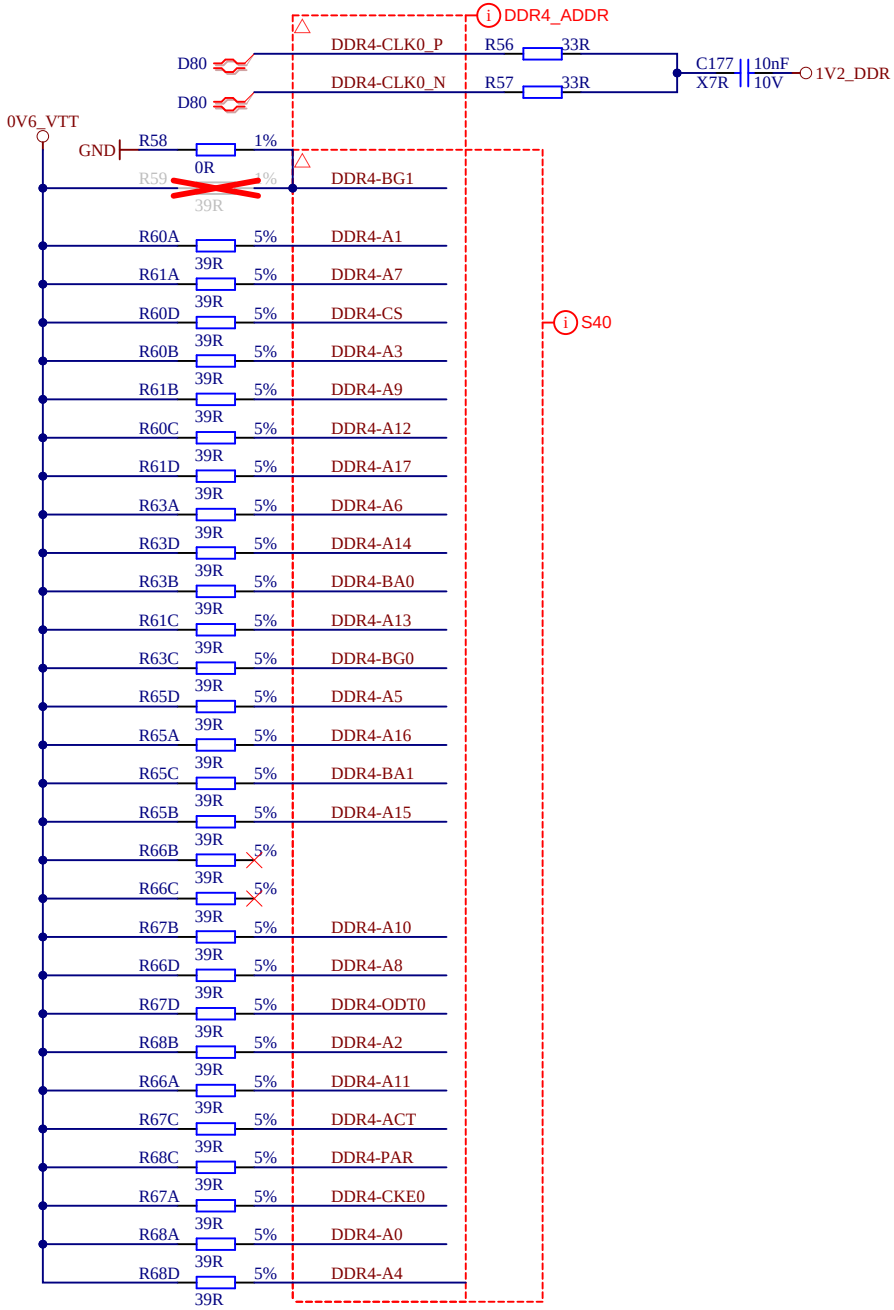
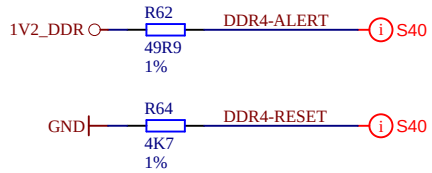
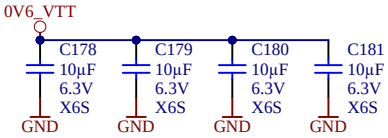
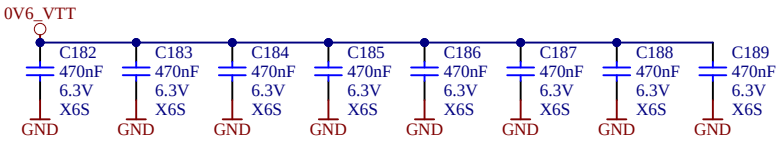
Date: 17.12.2025	Copyright: Trenz Electronic GmbH		Page 25 of 35
Filename: DDR4-RAM_5.SchDoc			









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Title: TE0861 – DDR4-TERM

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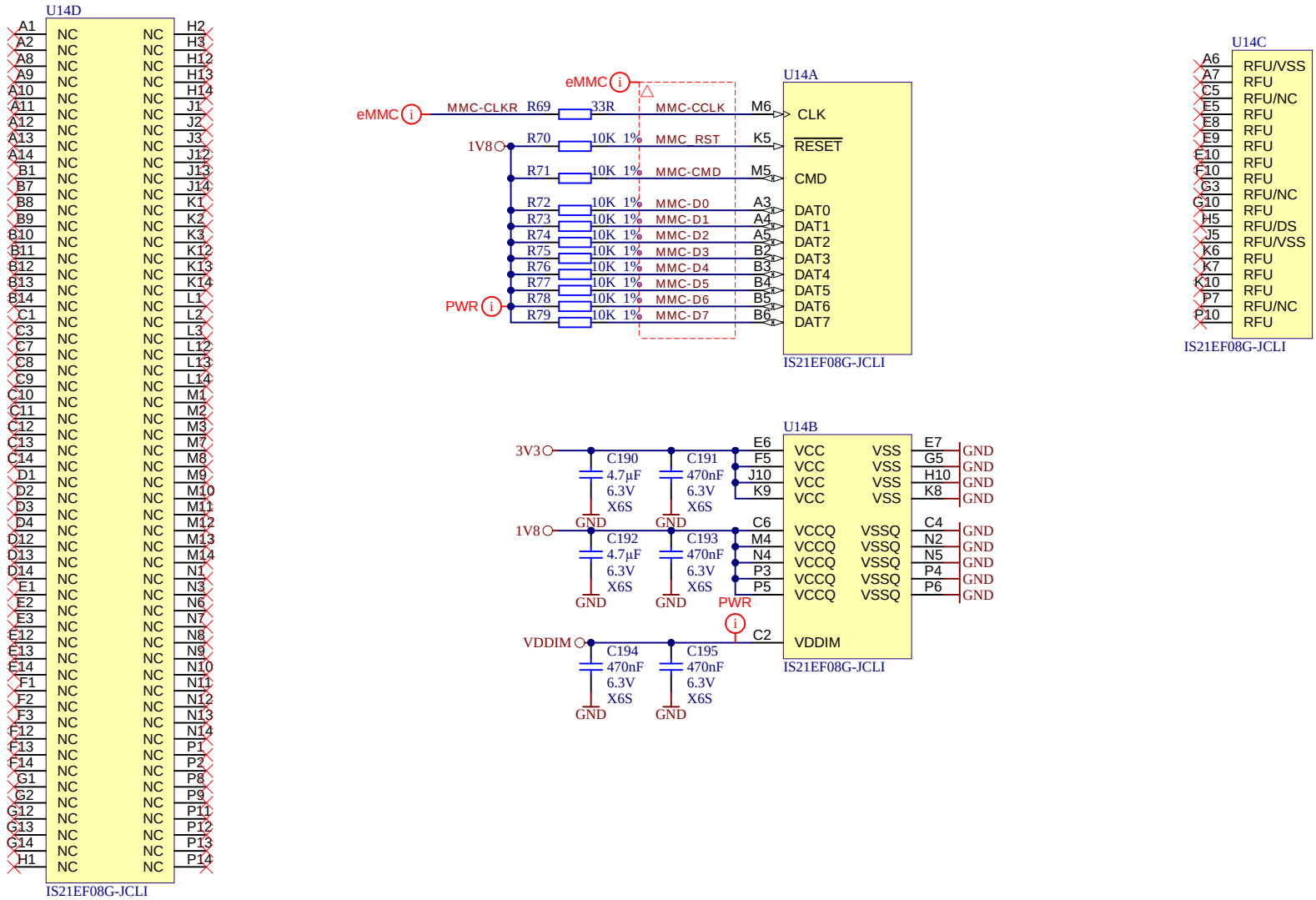
Date: 20.11.2025	Copyright: Trenz Electronic GmbH	Page 26 of 35
Filename: DDR4-TERM.SchDoc		



Title: TE0861 – eMMC			
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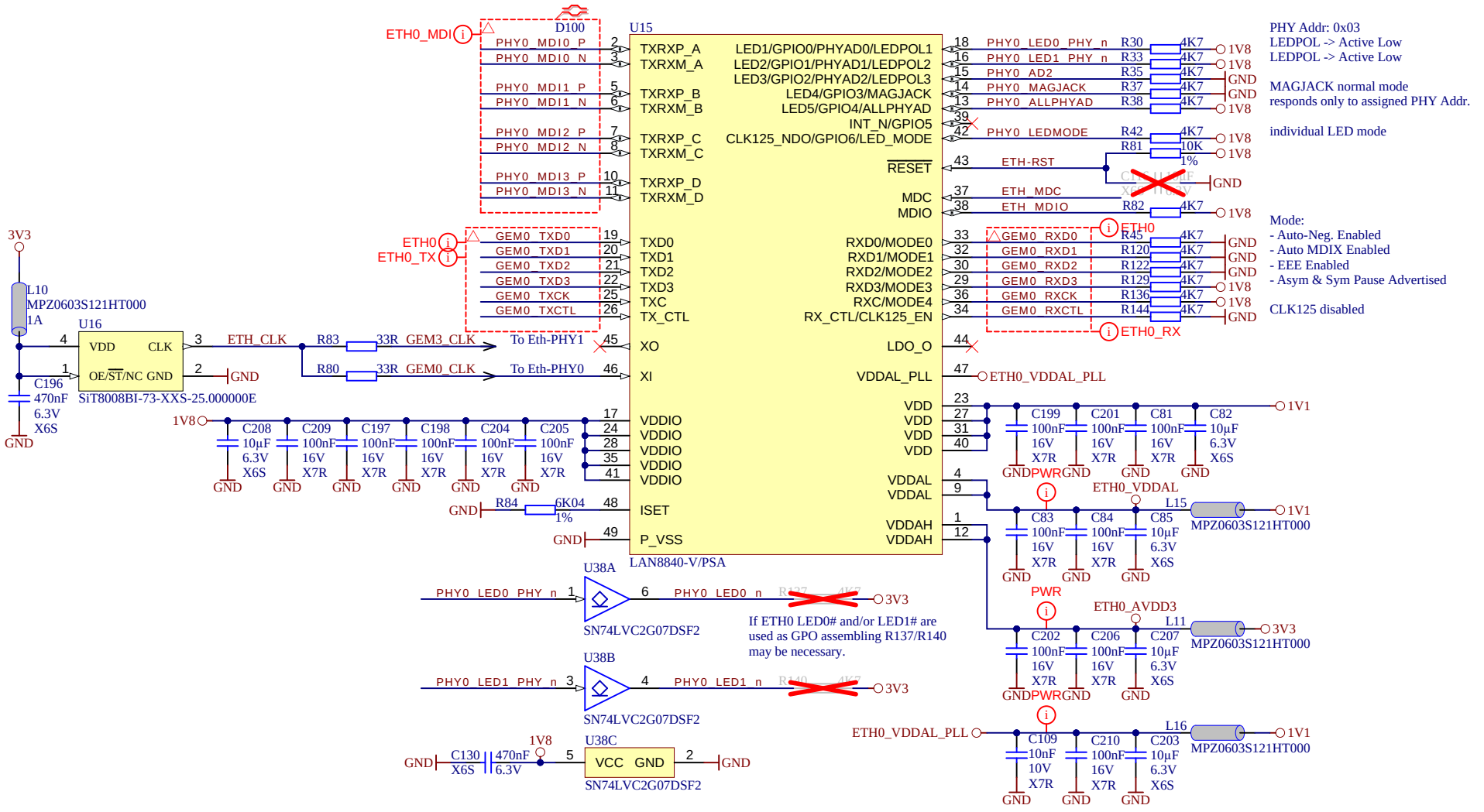
Date: 20.11.2025	Copyright: Trenz Electronic GmbH		Page 27 of 35
Filename: eMMC.SchDoc			


U15
LAN8840-V/PSA
PHY Addr: 0x03
LEDPOL -> Active Low
LEDPOL -> Active Low
MAGJACK normal mode
responds only to assigned PHY Addr.
individual LED mode
Mode:
- Auto-Neg. Enabled
- Auto MDIX Enabled
- EEE Enabled
- Asym & Sym Pause Advertised
CLK125 disabled
If ETH0 LED0# and/or LED1# are used as GPO assembling R137/R140 may be necessary.
EEPROM for MAC
Slave address: 1010000
SN74LVC2G07DSF2
24AA025E48T-I/OT
SiT8008BI-73-XXS-25.000000E
MPZ0603S121HT000
Title: TE0861 – ETH0-PHY
A4
Number: TE0861 6BI61QA
Rev. 01
Date: 20.11.2025
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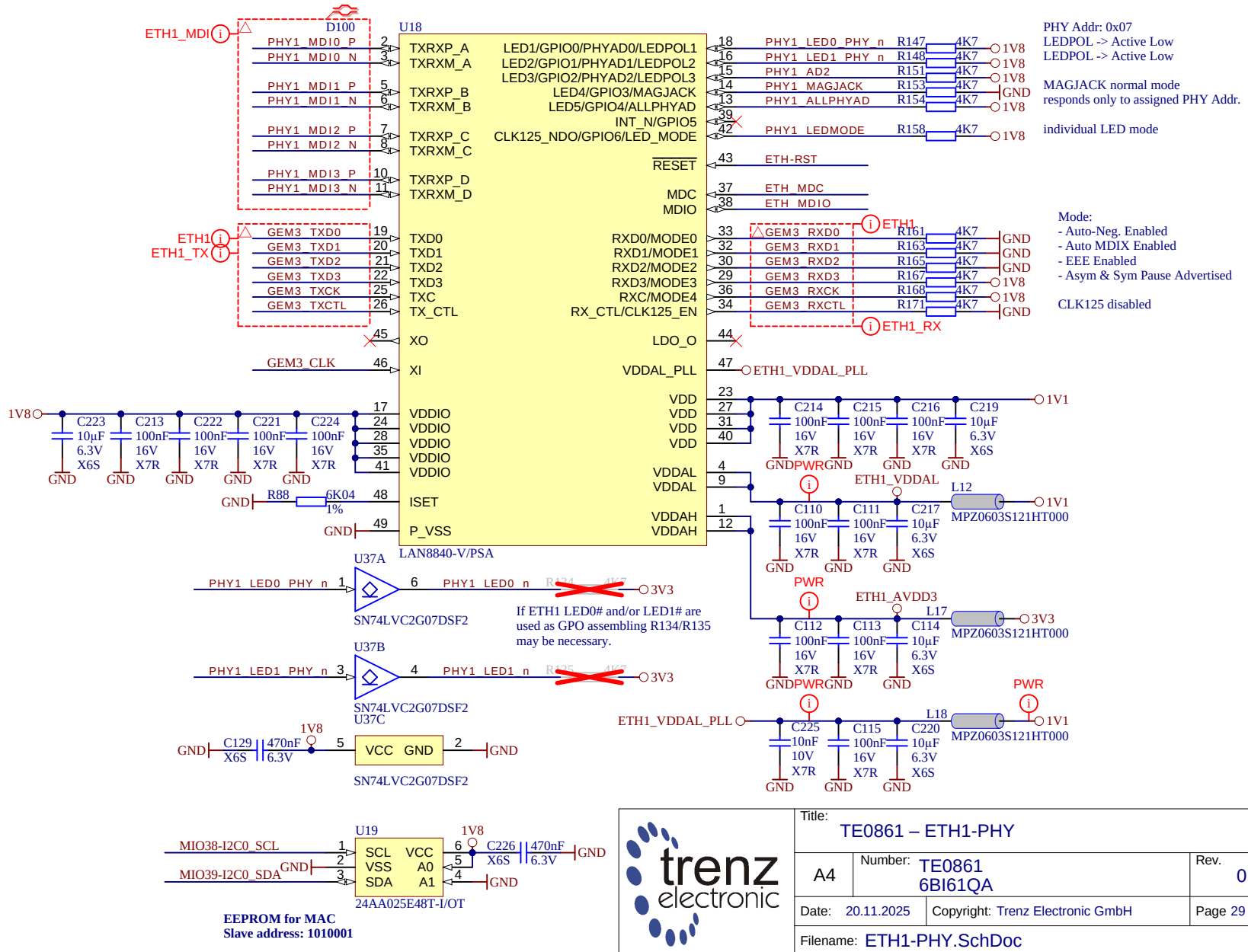
Filename: ETH0-PHY.SchDoc


ETH1_MDI
D100
U18
PHY1_MDI0_P
PHY1_MDI0_N
PHY1_MDI1_P
PHY1_MDI1_N
PHY1_MDI2_P
PHY1_MDI2_N
PHY1_MDI3_P
PHY1_MDI3_N
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
LED1/GPIO0/PHYAD0/LEDPOL1
LED2/GPIO1/PHYAD1/LEDPOL2
LED3/GPIO2/PHYAD2/LEDPOL3
LED4/GPIO3/MAGJACK
LED5/GPIO4/ALLPHYAD
INT_N/GPIO5
CLK125_NDO/GPIO6/LED_MODE
RESET
MDC
MDIO
PHY1_LED0_PHY_n
PHY1_LED1_PHY_n
PHY1_AD2
PHY1_MAGJACK
PHY1_ALLPHYAD
PHY1_LEDMODE
R147
R148
R151
R153
R154
R158
4K7
1V8
GND
ETH-RST
ETH_MDC
ETH_MDIO
PHY Addr: 0x07
LEDPOL -> Active Low
LEDPOL -> Active Low
MAGJACK normal mode
responds only to assigned PHY Addr.
individual LED mode
ETH1
ETH1_TX
GEM3_TXD0
GEM3_TXD1
GEM3_TXD2
GEM3_TXD3
GEM3_TXCK
GEM3_TXCTL
TXD0
TXD1
TXD2
TXD3
TXC
TX_CTL
RXD0/MODE0
RXD1/MODE1
RXD2/MODE2
RXD3/MODE3
RXC/MODE4
RX_CTL/CLK125_EN
GEM3_RXD0
GEM3_RXD1
GEM3_RXD2
GEM3_RXD3
GEM3_RXCK
GEM3_RXCTL
R161
R163
R165
R167
R168
R171
ETH1_RX
Mode:
- Auto-Neg. Enabled
- Auto MDIX Enabled
- EEE Enabled
- Asym & Sym Pause Advertised
CLK125 disabled
XO
XI
GEM3_CLK
LDO_O
VDDAL_PLL
ETH1_VDDAL_PLL
VDDIO
VDD
VDDAL
VDDAH
ISET
R88
6K04
1%
P_VSS
LAN8840-V/PSA
1V8
1V1
C223
C213
C222
C221
C224
C214
C215
C216
C219
C110
C111
C217
C112
C113
C114
C225
C115
C220
C129
10µF
100nF
10nF
470nF
6.3V
16V
10V
X6S
X7R
PWR
ETH1_VDDAL
ETH1_AVDD3
L12
L17
L18
MPZ0603S121HT000
3V3
U37A
U37B
U37C
SN74LVC2G07DSF2
VCC
GND
If ETH1 LED0# and/or LED1# are used as GPO assembling R134/R135 may be necessary.
U19
MIO38-I2C0_SCL
MIO39-I2C0_SDA
SCL
SDA
VSS
VCC
A0
A1
C226
24AA025E48T-I/OT
EEPROM for MAC
Slave address: 1010001
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Title:
TE0861 – ETH1-PHY
A4
Number:
TE0861
6BI61QA
Rev.
01
Date:
20.11.2025
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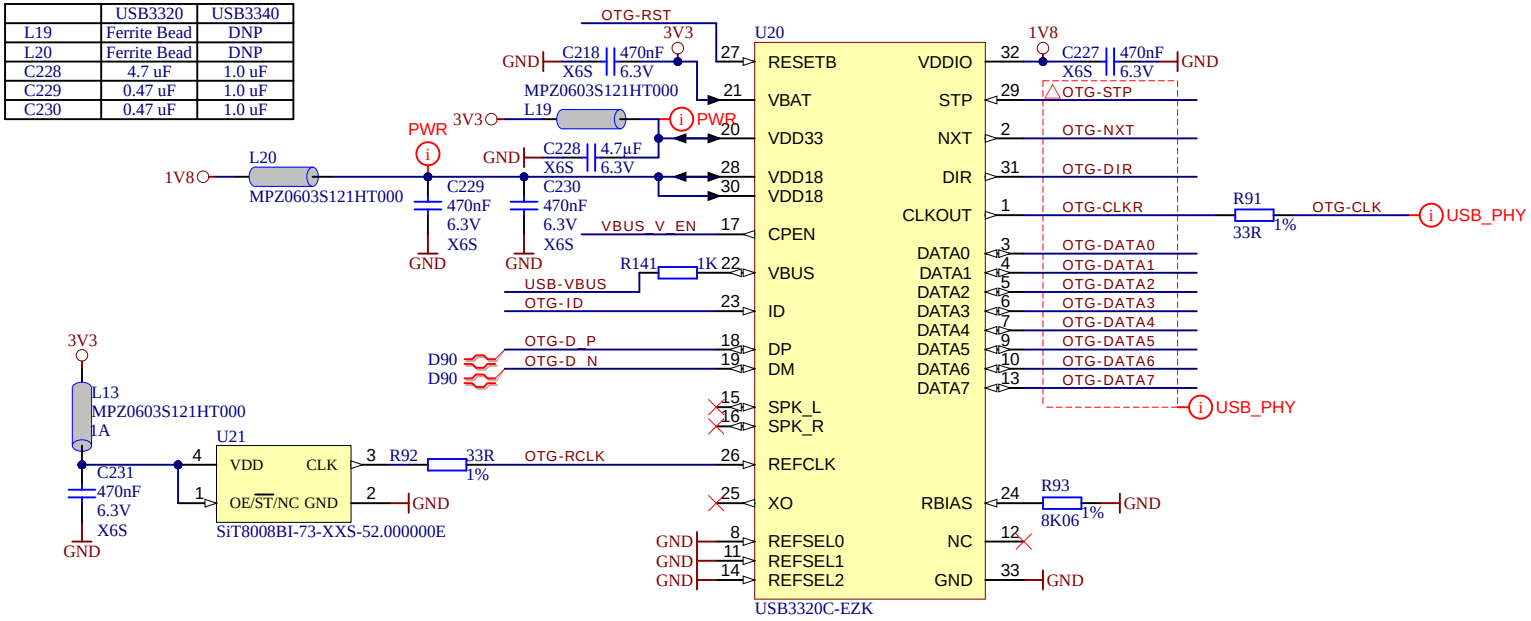
ETH1-PHY.SchDoc



	USB3320	USB3340
L19	Ferrite Bead	DNP
L20	Ferrite Bead	DNP
C228	4.7 uF	1.0 uF
C229	0.47 uF	1.0 uF
C230	0.47 uF	1.0 uF

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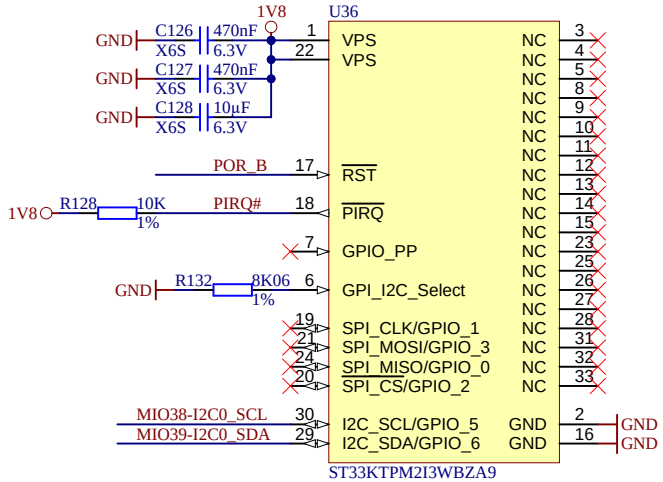

TPM
Slave address: 0101110

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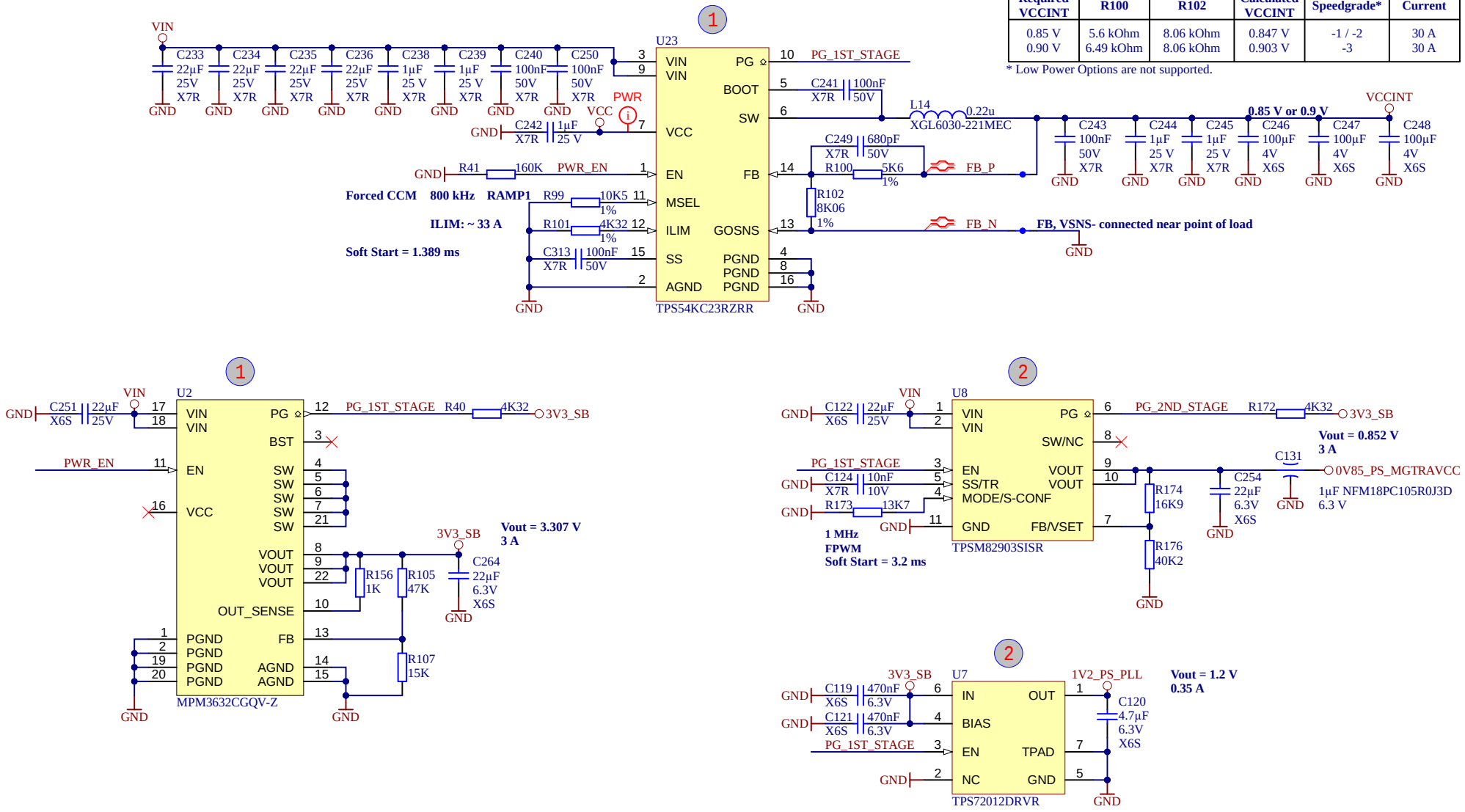

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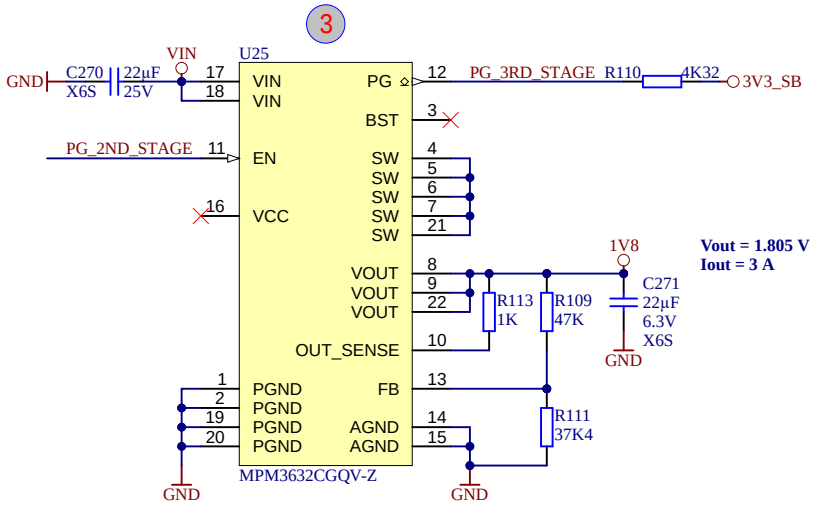

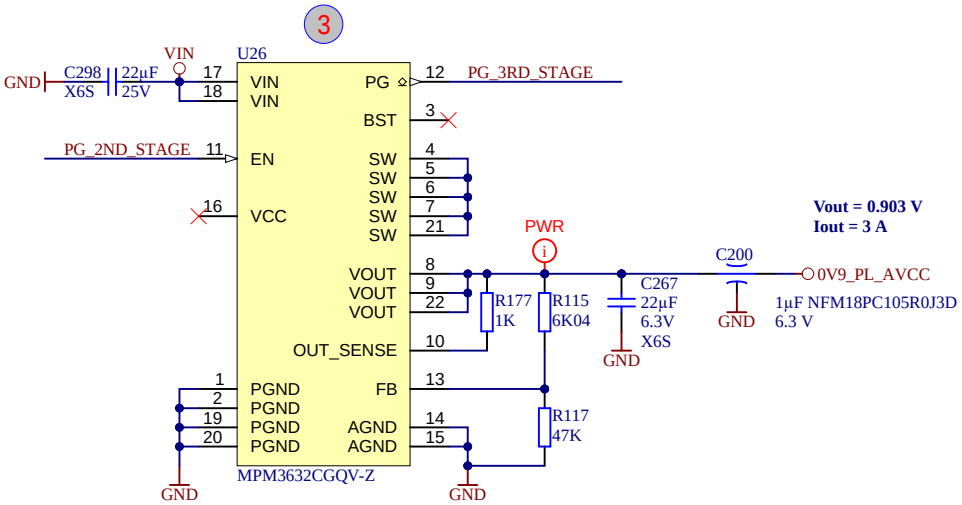

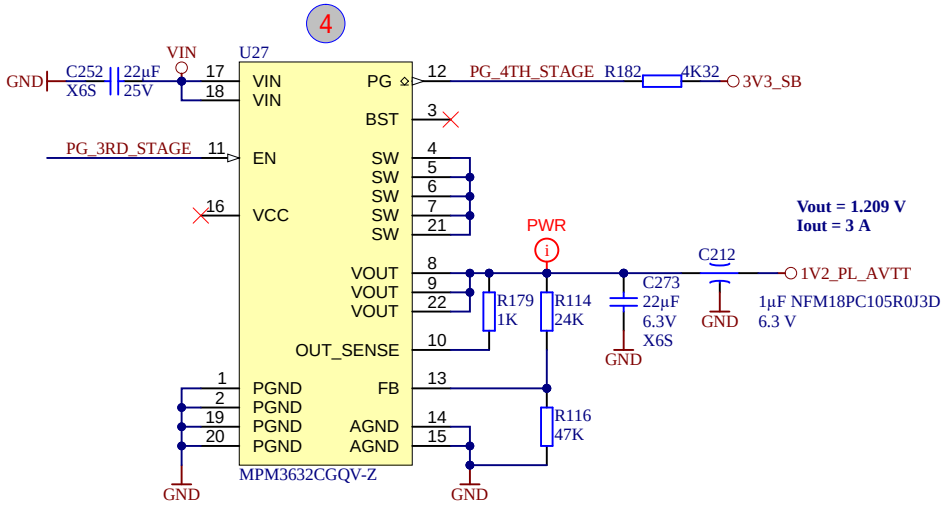

trenz electronic	Title: TE0861 – POWER 2		
	A4	Number: TE0861 6BI61QA	Rev. 01
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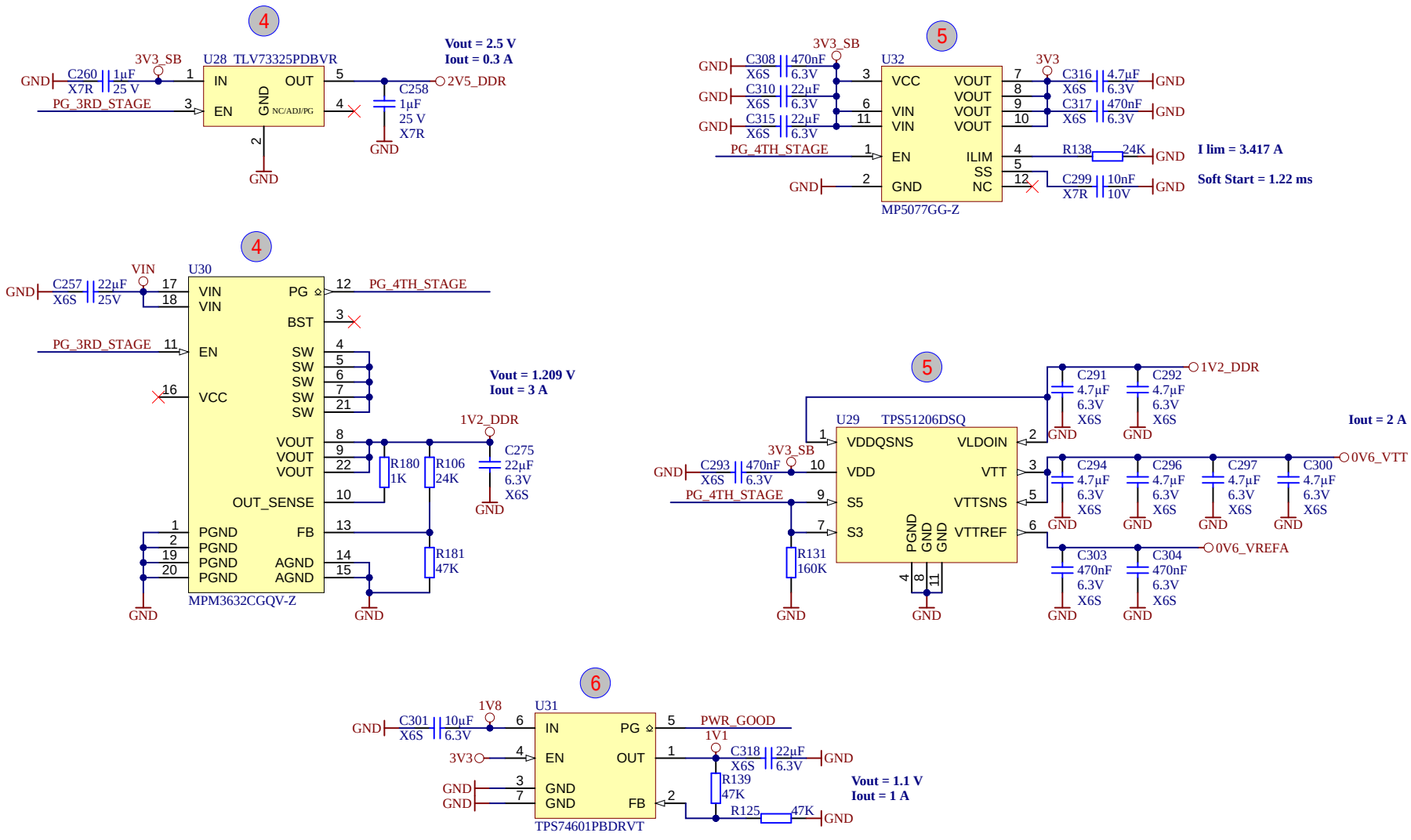
4
3V3_SB
U28 TLV73325PDBVR
C260 1µF 25 V X7R
PG_3RD_STAGE
IN
EN
GND
OUT
NC/ADJ/PG
C258 1µF 25 V X7R
2V5_DDR
Vout = 2.5 V
Iout = 0.3 A
5
3V3_SB
U32
C308 470nF 6.3V X6S
C310 22µF 6.3V X6S
C315 22µF 6.3V X6S
PG_4TH_STAGE
VCC
VIN
EN
GND
VOUT
ILIM
SS
NC
MP5077GG-Z
3V3
C316 4.7µF 6.3V X6S
C317 470nF 6.3V X6S
R138 24K
C299 10nF 10V X7R
I lim = 3.417 A
Soft Start = 1.22 ms
4
VIN
U30
C257 22µF 25V X6S
PG_3RD_STAGE
PG_4TH_STAGE
BST
SW
VCC
VOUT
OUT_SENSE
PGND
FB
AGND
MPM3632CGQV-Z
R180 1K
R106 24K
C275 22µF 6.3V X6S
R181 47K
1V2_DDR
Vout = 1.209 V
Iout = 3 A
5
U29 TPS51206DSQ
VDDQSNS
VDD
S5
S3
VLDOIN
VTT
VTTSNS
VTTREF
PGND
C293 470nF 6.3V X6S
R131 160K
C291 4.7µF 6.3V X6S
C292 4.7µF 6.3V X6S
1V2_DDR
C294 4.7µF 6.3V X6S
C296 4.7µF 6.3V X6S
C297 4.7µF 6.3V X6S
C300 4.7µF 6.3V X6S
0V6_VTT
C303 470nF 6.3V X6S
C304 470nF 6.3V X6S
0V6_VREFA
Iout = 2 A
6
1V8
U31
C301 10µF 6.3V X6S
3V3
IN
EN
GND
PG
OUT
FB
PWR_GOOD
1V1
C318 22µF 6.3V X6S
R139 47K
R125 47K
TPS74601PBDRVT
Vout = 1.1 V
Iout = 1 A
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Title: TE0861 – POWER 3
A4
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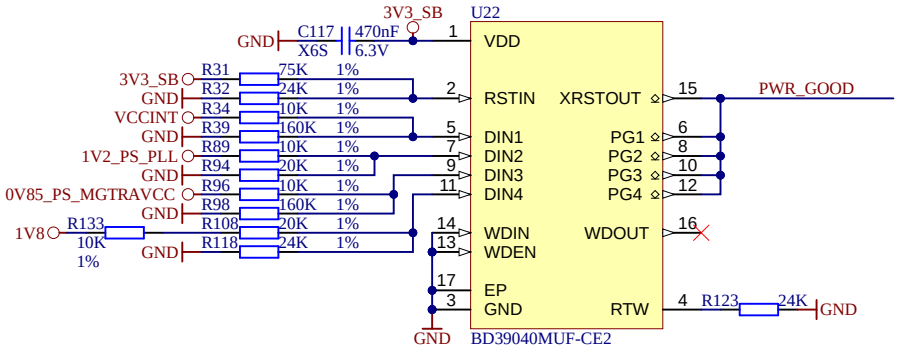
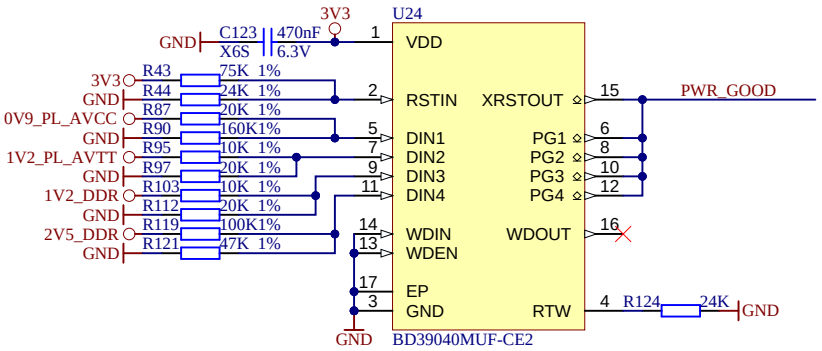
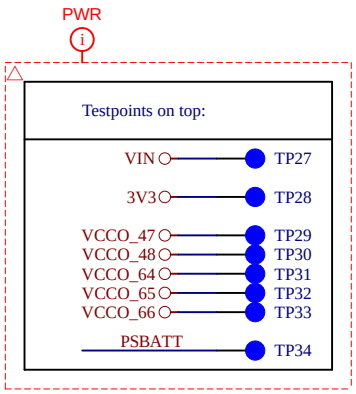
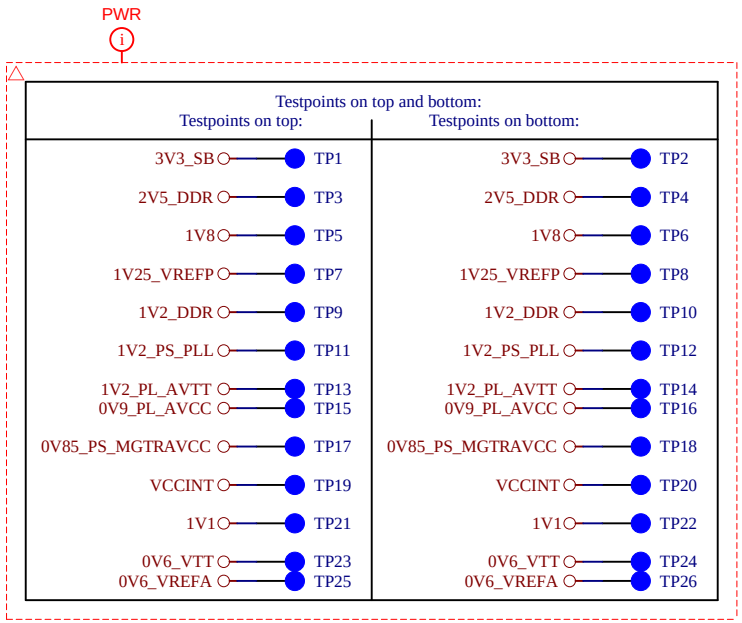
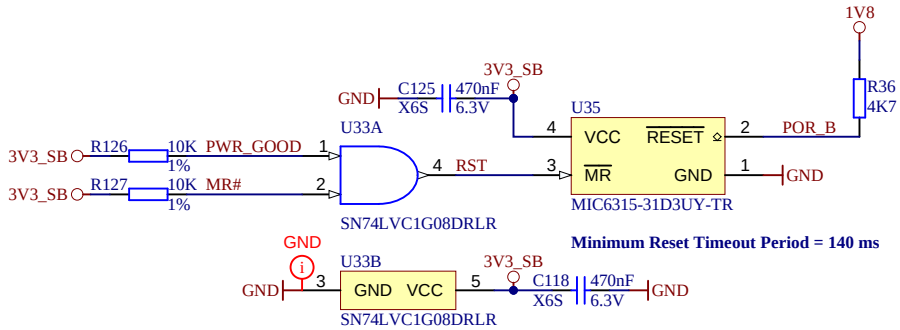




VCCINT	R34	R39
0.85 V	10 kOhm	160 kOhm
0.90 V	20 kOhm	160 kOhm







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