



## TE0835 CPLD

Revision v.29

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## 4 Overview

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Firmware for RFSoc module CPLD with designator U31: LCMX02-640HC

### 4.1 Feature Summary

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- Firmware
- Power Management
- JTAG routing
- Boot Mode
- User IO
- LED

### 4.2 Firmware Revision and supported PCB Revision

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See Document Change History

## 5 Product Specification

### 5.1 Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
PWR_STATUS	out	36	1.8V_CPLD	Output for Status-LED (After successful configuration of FPGA is connected automatically with FPGA_IO0)
MODE0	out	35	1.8V_CPLD	ZynqMP boot mode pin 0
PG_VCCRF	in	34	1.8V_CPLD	Power Good input from PWR_PRE
SRST_B	out	33	1.8V_CPLD	FPGA external system reset / <b>currently_not_used</b>
PROG_B	out	32	1.8V_CPLD	FPGA reset PL configuration logic / <b>currently_not_used</b>
PG_GR2	in	31	1.8V_CPLD	Power control input from PWR_PS and PWR_DDR
MIO28_UART1_TX	out	29	1.8V_CPLD	UART Transmission pin / <b>currently_not_used</b>
MIO28_UART1_RX	in	28	1.8V_CPLD	UART Receive pin / <b>currently_not_used</b>
FPGA_IO0	out	27	1.8V_CPLD	FPGA GPIO / User LED
FPGA_IO1	inout	26	1.8V_CPLD	FPGA GPIO / User dip switch interface
EN_PS_PL	out	14	3.3V_CPLD	Power enable for PWR_CORE , PWR_PS and PWR_GT

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
EN_GR1	out	15	3.3V_CPLD	Power enable for PWR_GT and PWR_PS
EN_RF_ADC	out	16	3.3V_CPLD	Power enable for PWR_ADC
PG_RF_DAC	in	17	3.3V_CPLD	Power control input from PWR_DAC
EN_VCCRF	out	18	3.3V_CPLD	Power enable for PWR_PRE
EN_GR2	out	19	3.3V_CPLD	Power enable for PWR_DDR , PWR_GT and PWR_PS
PG_PS_PL	in	20	3.3V_CPLD	power control input from PWR_CORE , PWR_GT and PWR_PS
PG_GR1	in	21	3.3V_CPLD	Power control input from PWR_GT and PWR_PS
PG_RF_ADC	in	23	3.3V_CPLD	Power control input from PWR_ADC
EN_RF_DAC	out	24	3.3V_CPLD	Power enable for PWR_DAC
MODE2	out	2	1.8V_CPLD	ZynqMP boot mode pin 2
MODE1	out	3	1.8V_CPLD	ZynqMP boot mode pin 1
POR_B	out	4	1.8V_CPLD	Power-On reset signal
MODE3	out	5	1.8V_CPLD	ZynqMP boot mode pin 3
INIT_B	in	7	1.8V_CPLD	FPGA PL initialization activity and configuration error signal / <b>currently_not_used</b>
F_TDI	out	8	1.8V_CPLD	JTAG ZynqMP

<b>Name / opt. VHD Name</b>	<b>Direction</b>	<b>Pin</b>	<b>Bank Power</b>	<b>Description</b>
F_TMS	out	9	1.8V_CPLD	JTAG ZynqMP
F_TCK	out	10	1.8V_CPLD	JTAG ZynqMP
F_TDO	in	11	1.8V_CPLD	JTAG ZynqMP
DONE	in	12	1.8V_CPLD	FPGA PL configuration done indicator
JTAG_TDO	out	48	3.3V_CPLD	JTAG_B2B
JTAG_TDI	in	47	3.3V_CPLD	JTAG_B2B
JTAG_TCK	in	45	3.3V_CPLD	JTAG_B2B
JTAG_TMS	in	44	3.3V_CPLD	JTAG_B2B
CPLD_IO0	in	43	3.3V_CPLD	BOOT Mode input pin 0
CPLD_IO1	in	42	3.3V_CPLD	BOOT Mode input pin 1
CPLD_JTAGEN	in	41	3.3V_CPLD	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
CPLD_IO2	in	40	3.3V_CPLD	CPLD IO to B2B / Used as dip switch interface on the carrier board (After successful configuration of FPGA is connected automatically with FPGA_IO1)
CPLD_IO3	out	38	3.3V_CPLD	CPLD IO to B2B/ Used as power good, can be used to enable carrier periphery power
RESETN	in	37	3.3V_CPLD	Reset pin (Active low)

## 5.2 Functional Description

### 5.2.1 JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on B2B. In the carrier board TEB0835 can be activated this pin with S1-4 dip switch.

CPLD_JTAGEN (B2B J1-30)	S1-4 on TEB0835 Carrier Board	Description
0	OFF	FPGA access
1	ON	CPLD access

### 5.2.2 Power

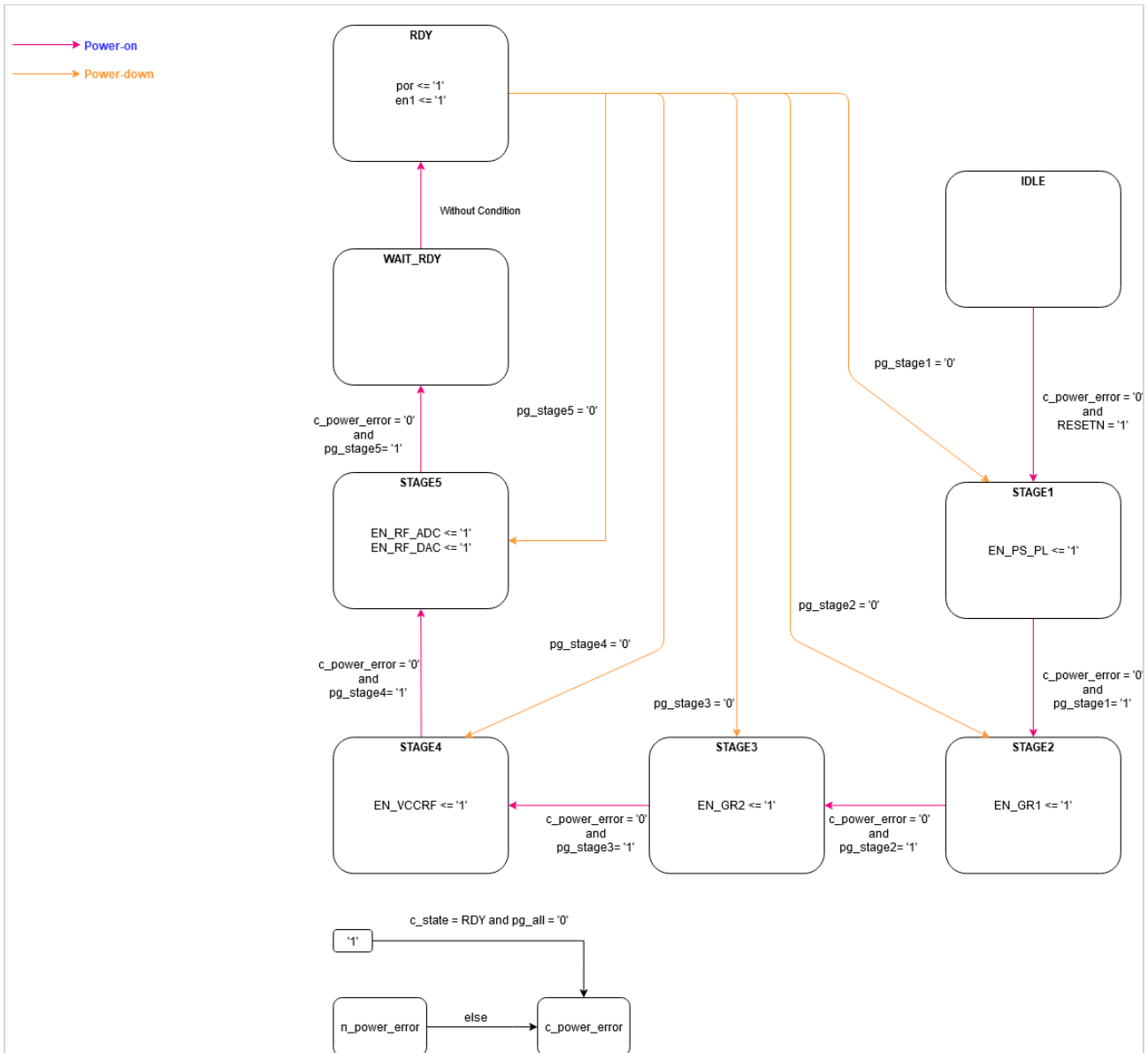
In this module the CPLD is responsible for controlling the power of the module. There are different power regulators or DC/DC converters whose outputs can be controlled by an enable signal. At the same time the outputs can also be monitored by power-good signals.

Enable Signal	Power Good Signal	Schematic page	Net	Domain	Regulator/ DC-DC Converter	in/out Voltage
EN_PS_PL	PG_PS_PL	PWR_CORE PWR_PS PWR_GT	VCCINT, VCINT_IO, VCCBRAM PSINTLP/ PSINTFP,PSIN TFP_DDR MGTAVCC	PL PS_LP/ PS_FP GTH	LTM4662EY LTM4644EY TPS82085	5V/ 0.835V 5V/ 0.85V 5V/ 0.9V
EN_GR1	PG_GR1	PWR_PS PWR_GT PWR_GT	PSAUX,PSADC, PSIO/ VCCAUX,VCCA UX_IO/ PS_DDR_PLL PSMGTRAVCC/ MGTVCCAUX	PS_LP/ PS_FP PS_FP/ P/ GTH	TPS82085 EP53A7LQI EN6347QI	5V/ 1.8V 5V/ 0.85V 5V/ 1.2V

Enable Signal	Power Good Signal	Schematic page	Net	Domain	Regulator/ DC-DC Converter	in/out Voltage
			PSPLL/ MGTAVTT	PS_L P/ GTH		
EN_GR2	PG_GR2	PWR_PS PWR_GT PWR_DDR PWR_DDR	VCC_B88_HD PS_MGTRAVTT DDR_2V5 DDR_1V2	PS_LP PS_FP DDR DDR	TPS82085 EP53A7H QI TPS82085 TPS82085	5V/ 3.3V 5V/ 1.8V 5V/ 2.5V 5V/ 1.2V
EN_VCCRF	PG_VCCRF	PWR_PRE	VCCINT_AMS, APRE_1V15, APRE_3V3	ADC and DAC	LTM4644E Y	5V/ 0.8534 V,1.15 V,3.3V
EN_RF_ADC	PG_RF_ADC	PWR_ADC PWR_ADC	ADC_AVCC ADC_AVCCAUX	ADC ADC	TPS74401 TPS74401	1.15V/ 0.925 V 3.3V/ 1.8V
EN_RF_DAC	PG_RF_DAC	PWR_DAC PWR_DAC PWR_DAC	DAC_AVCC DAC_AVCCAUX DAC_AVTT	DAC DAC DAC	TPS74801 TPS74801 TPS74801	5V/ 0.925 V 5V/ 1.8V 5V/ 2.5V

### 5.2.3 Power-on Sequencing

According to the Xilinx instructions the power regulator or DC-DC converter must be switched on or off in a certain order. This is called power-on or power-off sequencing. To implement power-on sequencing correctly, a state machine must be running there. In the following you can see the State Machine Diagram.



Stage	Control	Voltage Domains	Signal Monitoring to change stage
IDLE	---	---	RESETN
STAGE1	EN_PS_PL enabled (High)	0.853V, 0.85V, 0.9V	PG_PS_PL
STAGE2	EN_GR1 enabled (High)	1.8V, 0.85V, 1.2V	PG_GR1
STAGE3	EN_GR2 enabled (High)	3.3V, 1.8V	PG_GR2

Stage	Control	Voltage Domains	Signal Monitoring to change stage
STAGE4	EN_VCCRF enabled (High)	0.8534V, 1.158V, 3.3V	PG_VCCRF
STAGE5	EN_RF_ADC enabled (High) EN_RF_DAC enabled (High)	0.925V, 1.8V 0.925V, 1.8V, 2.5V	PG_RF_ADC PG_RF_DAC
WAIT_RDY	---	---	---
RDY	por enabled (High) en1 enabled (High) if DONE is High.	---	pg_all

- pg\_all <= PG\_PS\_PL & PG\_GR1 & PG\_GR2 & PG\_VCCRF & PG\_RF\_ADC & PG\_RF\_DAC
- If por is high then POR\_B (power-on reset signal) will be deactivated.

## 5.2.4

### LED

States	Blink Sequence	Comment
IDLE	oooooooooooooooooooo oo*	Power Sequencing can not start. RESETN is active.
Stage 1	oooooooooooooooooooo *o*	The correct voltage in one of the following nets are failed: VCCINT, VCINT_IO, VCCBRAM, PSINTLP, PSINTFP, PSINTFP_DDR, MGTAVCC
Stage 2	oooooooooooooooooooo*o* o*	The correct voltage in one of the following nets are failed: PSAUX, PSADC, PSIO, VCCAUX, VCCAUX_IO, PS_DDR_PLL, PSMGTRAVCC, MGTVCCAUX, PSPLL, MGTAVTT

States	Blink Sequence	Comment
Stage 3	oooooooooooo*o*o* o*	The correct voltage in one of the following nets are failed: VCC_B88_HD, PS_MGTRAVTT, DDR_2V5 , DDR_1V2
Stage 4	oooooooooooo*o*o*o* o*	The correct voltage in one of the following nets are failed: VCCINT_AMS, APRE_1V15, APRE_3V3
Stage 5	oooooooo*o*o*o*o* o*	The correct voltage in one of the following nets are failed: ADC_AVCC, ADC_AVCCAUX, DAC_AVCC, DAC_AVCCAUX, DAC_AVTT
WAIT_RDY / RDY and DONE='0'	ooooooo*o*o*o*o*o* o*	Power is ok. But the FPGA is not yet configured.
pg_all = '0'	ooooo*o*o*o*o*o*o* *	An unknown error has occurred. The power supply must be switched off.
USR (RDY and DONE='1')	User defined	Power is ok and the FPGA is configured successfully. LED can be controlled by user, when Power is OK and FPGA part is programmed (DONE signal is high)

- The period for every blink (\*o) is 0.5sec.

### 5.2.5 User IO

- FPGA\_IO1 (AE16 of RFSoc) is connected with CPLD\_IO2 (S1-3 Dip switch on the carrier board) when the FPGA is programmed correctly otherwise this pin is high impedance. After configuration of the FPGA can user use this pin as input.
- FPGA\_IO0 (AE18 of RFSOC) is connected with LED on the RFSoc module (D1) if the FPGA is programmed completely otherwise this LED (D1) blinks according to the state of the power-on sequencing. After configuration of the FPGA can be controlled this LED (D1) by user.

If the FPGA correctly programmed (DONE signal is high) and the power-on sequencing state is RDY then the User IOs can be shown in the following table:

Function	Interface	Schematic	FPGA Pin	Note
USER signal	B2B (J1-32)	FPGA_IO1	AE16	source by TEB0835 Dip Switch S1-3, in case FPGA is programmed

Function	Interface	Schematic	FPGA Pin	Note
LED (D1)	--	FPGA_IO0	AE18	controls LED, in case FPGA is programmed

## 5.2.6 Boot Mode

Boot Modes can be selected via B2B Pin Mode.

B2B Pin J1-28 (CPLD IO1)	B2B Pin J1-26 (CPLD IO0)	Boot Mode
0	0	Boot from PS JTAG
0	1	Boot from QSPI
1	1	Boot from SD Card

## 6 Appx. A: Change History and Legal Notices

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### 6.1 Revision Changes


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- REV00 to REV01
  - transfer verilog to vhdl
  - power stagemachine, add power down cyclus on error state
  - bugfix: Power Good(CPLD\_IO3) depends now on module power sequencing
  - LED status changed
  - LED controllable by USR after power up
  - CPLD\_IO2 connected to FPGA IO (can be controlled by user)
  - constrains and buffer changes for JTAG

### 6.2 Document Change History

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To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
 2020-11-02	<a href="#">v.29</a>	REV01	REV02, REV01	<a href="#">Mohsen Chamanbaz</a> <sup>1</sup>	<ul style="list-style-type: none"> <li>• REV01 release (firmware release 2020-10-27)</li> </ul>
2020-08-18	v.4	REV00	REV01	Ivan Girshchenko / Mohsen Chamanbaz	<ul style="list-style-type: none"> <li>• REV00 release (firmware release 2019-12-18)</li> </ul>
	All			<a href="#">Mohsen Chamanbaz</a> <sup>2</sup>	

### 6.3 Legal Notices

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### 6.4 Data Privacy

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

<sup>1</sup> <https://wiki.trenz-electronic.de/display/~M.Chamanbaz>

<sup>2</sup> <https://wiki.trenz-electronic.de/display/~M.Chamanbaz>

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## 6.10 REACH, RoHS and WEEE

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<sup>3</sup> <http://guidance.echa.europa.eu/>

[Candidate List](#)<sup>4</sup> are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#)<sup>5</sup>.

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07

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<sup>4</sup> <https://echa.europa.eu/candidate-list-table>

<sup>5</sup> <http://www.echa.europa.eu/>