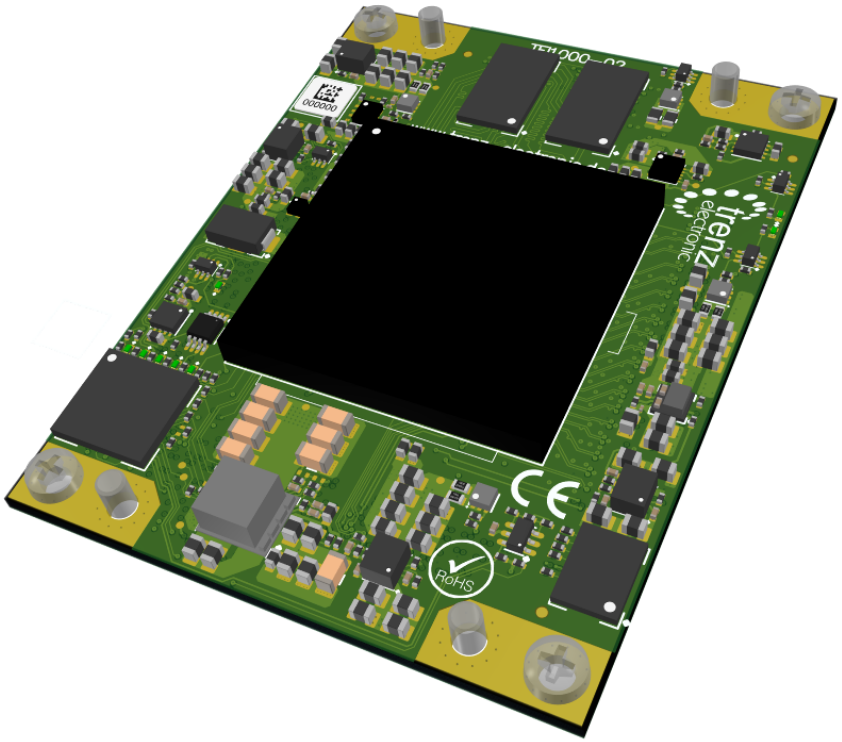

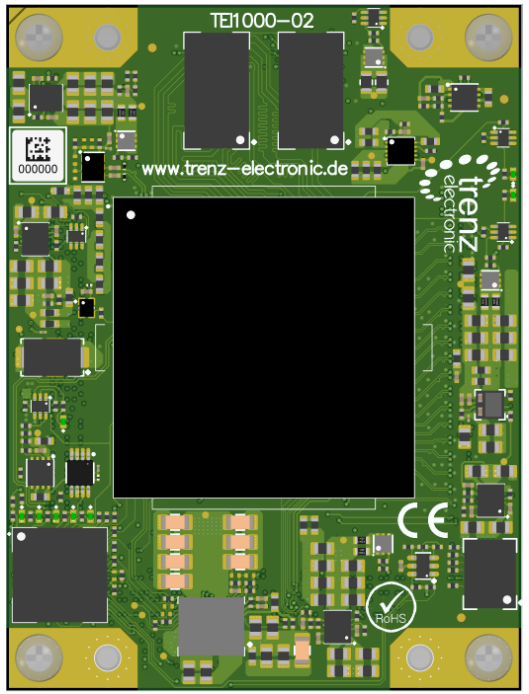

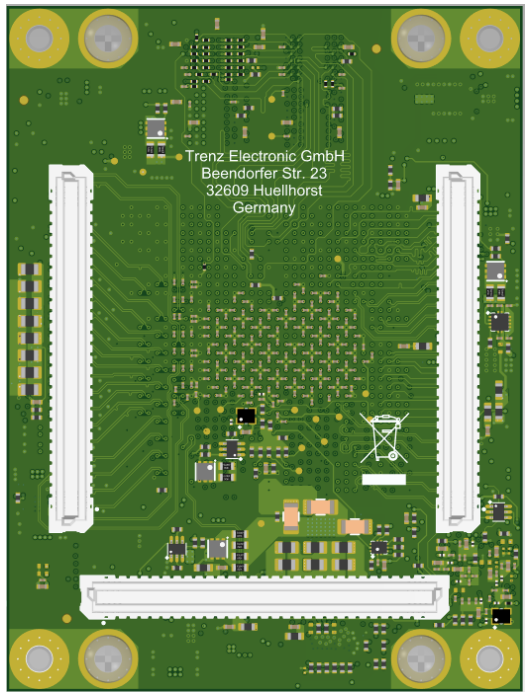

Regarding the usage of our schematics and alike documentation for Trenz module TEI1000.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TEI1000 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TEI1000		
	A4	Number: TEI1000 AGI11-A	Rev. 02
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	Filename: Legal Notices Modules.SchDoc		

3V3D_perm

MAX10
(10M08SAU169I7G)

Vin PG ← TLV6700

To S10 → nConfig
From S10 ← nStatus

Sequ. group1

Sequ. group 3, 4 → To Carrier
Sequ. group 3, 4 ← From Carrier

Sequ. group 5

Sequ. group 2

VCCIO_REQ → To Carrier
VCCIO_PG ← From Carrier
MAX10_PG → To Carrier

FS1525 (EN, PG) → VCCPLLDIG_HPS, VCC, VCCP, VCCL_HPS
0.850V-0.910V
20A

TDM3885 (EN, PG) → VCCERAM, VCCPLLDIG_SDM
0.890V-0.911V
3.4A

TDM3885 (EN, PG) → VCCR_GXB, VCCT_GXB
1.013V-1.047V0.890V-0.911V
>4A

MP5077 (EN, PG) → S10_VCCIO3C
3.225V-3.377V
1A

NCV51200 (EN, PG) → RAM_VREFCA, RAM_VTT

TDM3885 ('1', EN, PG) → 3V3D_PERM
3.225V-3.377V
?A
To Carrier

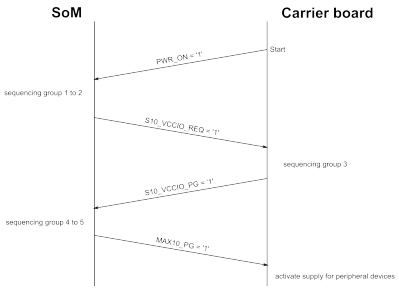
NCV8164 (EN, PG) → RAM_VPP
2.446V-2.556V
0.1A

NCV51200 (EN, PG, V_SET) → VCCFUSEWR_SDM
1.803V-1.857V
2.362V-2.449V
?A

TDM3885 (EN, PG) → RAM_VDDQ, RAM_VDD
1.179V-1.221V
0.95A

TDM3885 (EN, PG) → VCCPT, VCCBAT, VCCA_PLL, VCCPLL_SDM, VCCADC, VCCIO_SDM, VCCH_GXBL, VCCH_GXBR
1.764A - 1.837A
2.0A

ON Squencing



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Title: TEI1000 - Power Diagram		
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REV	Description	
02	- Changed pulldowns to 1K for all power sequencing groups. Corrected notes about enable thresholds of voltage regulators and load switches. - Changed value for R191-195 to 0R - Added 100pF MAX10 JTAG TCK to GND. Comp. C88 - Removed T6A from Net MAX10_nCONFIG. - Swapped R184 with R186. Upper side 150R, lower side 100R for voltage divider. - Added filtered monitoring of 1.03V power raill by MAX10. - Changed LED D1 to color green. Same like other LEDs. - Fixed group length matching issue of ADD/CMD signals between S10 and first DRAM-Chip. - Replaced RAM-RefClock oscillator (Y1) by 125MHz LVDS oscillator for SX variant and 100MHz LVDS GX variant - Replaced TDM3883 GXB regulator with TDM3885 type - Replaced VCC_CORE voltage regulator by FS1525. Used schematic from TDK User Guide as reference - Moved R180 out of connector J3 - Drew overview diagram in Altium instead of adding SVG-Image at overview sheet. - Updated overview sheet - Added 100R bleeding resistor R228 (AN 22507) from VCC_CORE rail to GND - Connected R175.2 to U20.6/U20.11 instead of net "S10_VCCIO3C". Added 0R jumper R234 (AN 22738) between "3V3D_PERM" and U20.6/U20.11. Set R175 to DNP. Set R234 to populated. - Added 0402 499R (AN 27123) pull-down resistors to TEN pins (U1A.TEN, U2A.TEN) (R229, 230). - Pin U4A.D2 (ANAIN1), U4.H4 (CLK1P), U4.H5 (CLK1N), U4.N2 (DPCLK0) and U4.L3 (CLKOUTP) connected to GND. - Replaced R227 and R224 by 4k99 (AN 22754). - Seperated AGND and PGND of U12: U12.(64-69) -> AGND, U12.(31,32,33,34,35,36,37,58,59,60,61,62,36) -> GND. Connected AGND to GND by net-tie V12 (AN 30278) under U12 in layout. Connected to AGND: R226.2 (PS-resistor), R225.2 (ADDR-resistor), R222.2 (FB-LS-resistor). - Added 4k99 pull-up (AN 22754) from VCC to ALERT-pin of FS15625 (U12.28) - Added test points to CLKOUT- and ISHRE-pin of FS1525 (U12.29, U12.20) (TP7, TP9) - Replaced R72 by 1k resistor (AN 22752). - Added note about power consumption of 3V3D_PERM-rail. - Added note about purpose of R175. - Added note about slave address and Fsw of FS1525. - Connected unused GXB receiver pins to GND. (U14.(N32, N31, M30, M29, H30, H29, F30, F29, D30, D29, B30, B29)) - Added note about supply voltage range of bank 2K. - Added 0R jumper R235 (AN 22738) between VTT and VREFB2MN0. Added 0R jumper R236 (AN 22738) between VTT and VREFB2NN0. - Added note about logic levels of PCIE_PERSTN and PCIE_WAKEN, as well as necessarily of level shifters on carrier board for these signals. - Added DNP 10k PUs (R232, R233) (AN 22750) to QSPI_R_IO3 and QSPI_R_IO2. - Added test point to voltage rails: VCC_CORE (TP18), 1V8_FLT1 (TP19), 1V8_FLT2 (TP20), VCCPLLDIG_SDM (TP21). - Added return path vias next to layer jump of diff pair DDR4-IP_CLK - Improved entries to pads of U11. - Fixed courtyard intersections where possible. - Merged GND polygons near U10. - Added additional return path vias next to layer jumps of GXB-pairs, where possible. - Added anti-pad keeptouts to GXB-related diff-pair layer jump vias. - Removed splits in reference planes for impedance controlled signals were possible.	MSt
	- Added test points to the voltage rails on the TOP side - Changed DCDC (U6) TDM3885XUMA1 (Ioutmax=4A)-> FS1606-0600-AL (Ioutmax=6A). - Added I2C connection (signals B2B_CLK & B2B_SDA) DCDC U6 to MAX10 (U4.M10 & U4.N12) , B2B connector (J3.B30 & J3.B31) - Moved Net-Tie V11(signal "EN_S10_VCCFUSEWR_SDM") from "EN5" to "EN3" - Full update Library	VT
02A 2026-06-25	- Updated the Vin power supervisor circuit (R206, R209, R210). Input power range is changed from 4.7V - 12.9V to 5.5 V - 13.69 V. - Added voltage description table (Page TEI1000)	VY

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Title: TEI1000 – Revision_Changes

A4	Number: TEI1000 AGI11-A	Rev. 02
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U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_REV_CH
Revision_Changes.SchDoc

U_Bank_1C
Bank_1C.SchDoc

U_Bank_1D
Bank_1D.SchDoc

U_Bank_1E
Bank_1E.SchDoc

U_Bank_1F
Bank_1F.SchDoc

U_Bank_2K
Bank_2K.SchDoc

U_Bank_2L
Bank_2L.SchDoc

U_Bank_2M
Bank_2M.SchDoc

RAM / RAM-CLK

U_Bank_2N
Bank_2N.SchDoc

RAM

U_Bank_3A
Bank_3A.SchDoc

U_POWER_Discharging_3
POWER_Discharging_3.SchDoc

U_POWER_Discharging_2
POWER_Discharging_2.SchDoc

U_POWER_Discharging_1
POWER_Discharging_1.SchDoc

U_POWER_Decoupling_1
POWER_Decoupling_1.SchDoc

U_POWER_Decoupling_2
POWER_Decoupling_2.SchDoc

U_POWER_Decoupling_3
POWER_Decoupling_3.SchDoc

U_POWER_Decoupling_4
POWER_Decoupling_4.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_PD
Power_Diagram.SchDoc

U_Bank_3B
Bank_3B.SchDoc

U_Bank_6A
Bank_6A.SchDoc

U_Bank_3D
Bank_3D.SchDoc

U_Bank_SDM
Bank_SDM.SchDoc

U_LN
Legal Notices Modules.SchDoc

U_POWER_Sequencing_3
POWER_Sequencing_3.SchDoc

U_POWER_Sequencing_1
POWER_Sequencing_1.SchDoc

U_POWER_Sequencing_2
POWER_Sequencing_2

U_POWER_1
POWER_1.SchDoc

U_POWER_Decoupling_4
Power_Sequencing_filtering.SchDoc

U_POWER_2
POWER_2.SchDoc

U_POWER_3
POWER_3.SchDoc

U_POWER_4
POWER_4.SchDoc

U_Misc
Misc.SchDoc

U_Bank_3C
Bank_3C.SchDoc

U_Bank_HPS
Bank_HPS.SchDoc

U_FPGA_POWER_1
FPGA_POWER_1.SchDoc

U_FPGA_POWER_2
FPGA_POWER_2.SchDoc

H1
GND
Mount.Hole 3.2mm für Unterlegscheibe

H3
GND
Mount.Hole 3.2mm für Unterlegscheibe

H5
GND
Mount.Hole 3.2mm für Unterlegscheibe

H7
GND
Mount.Hole 3.2mm für Unterlegscheibe

H2
GND
Mount.Hole 3.2mm für Unterlegscheibe

H4
GND
Mount.Hole 3.2mm für Unterlegscheibe

H6
GND
Mount.Hole 3.2mm für Unterlegscheibe

H8
GND
Mount.Hole 3.2mm für Unterlegscheibe

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description
VIN	IN	6 - 12V	+10/- 5 %	Main power input
S10_VCCIO_B2K	IN	1.2 - 1.8V	+/- 5 %	FPGA Bank 2A power input. Connect to 1V8D or to external DCDC on carrier card.
1V8D	OUT	1.8V	+/- 3 %	SoM output voltage. Can be used to power FPGA banks or peripherals. Up to 1A
S10_VCCIO3C	OUT	3.3V	+/- 3 %	SoM output voltage. Can be used to power FPGA banks or peripherals. Up to 1A

Special notes:

PM1
FIDU-DOT - mini
PM2
FIDU-DOT - mini
PM3
FIDU-DOT - mini
PM4
FIDU-DOT - mini
PM5
FIDU-DOT - mini
PM6
FIDU-DOT - mini

UKCA
UKCA Logo on Top Overlay
UKCA-TOPOVERLAY
MECH1
TE Address Overlay
LOGO ADDRESS
LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial1
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	AGI11-A
Created by	VY
Modified by	VY
Modified at	2026-06-25
SVN Revision	19891 [Locally Modified]

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Title: TEI1000			
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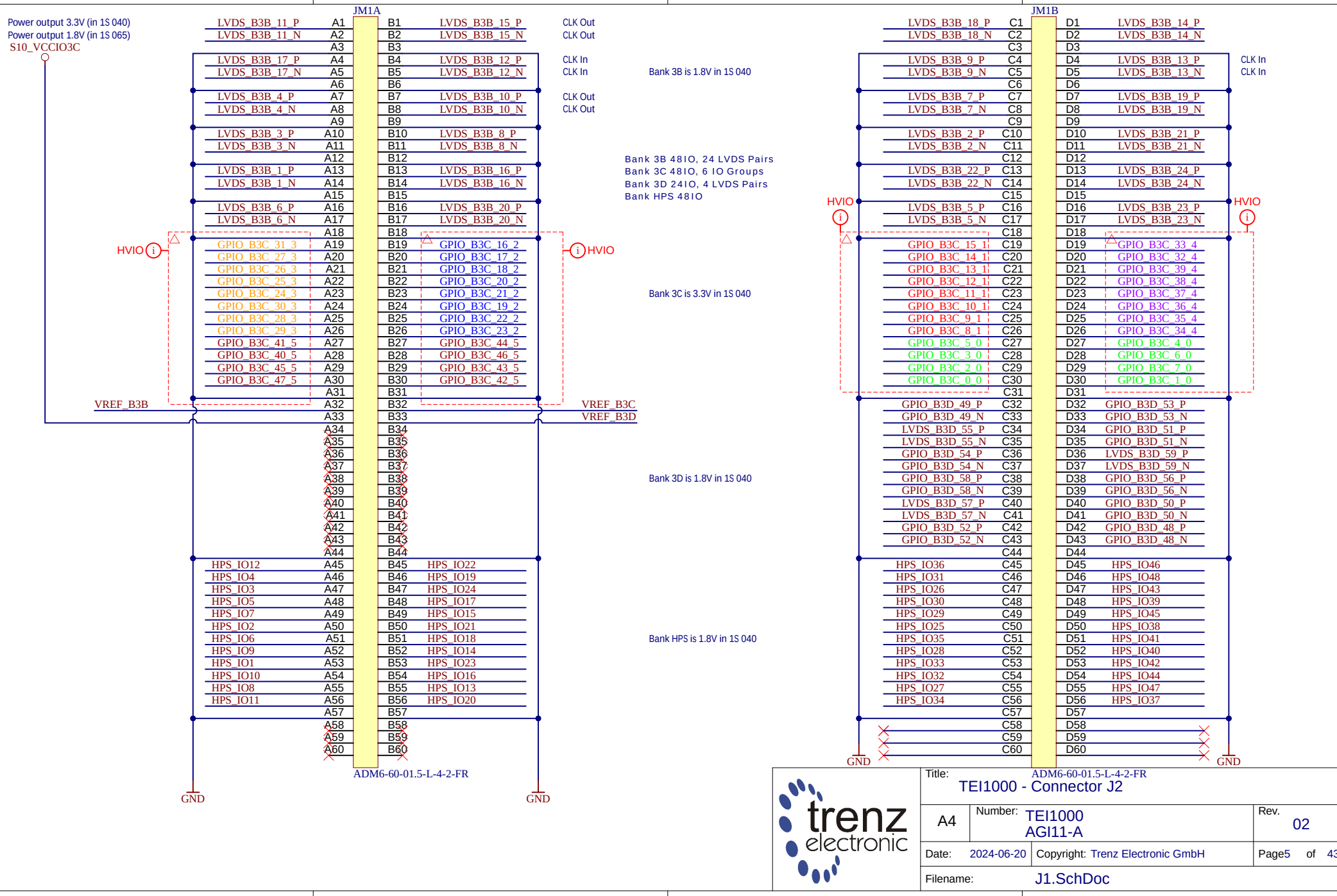
Power output 3.3V (in 1S 040)
Power output 1.8V (in 1S 065)
S10_VCCIO3C
JM1A
LVDS_B3B_11_P A1 B1 LVDS_B3B_15_P CLK Out
LVDS_B3B_11_N A2 B2 LVDS_B3B_15_N CLK Out
A3 B3
LVDS_B3B_17_P A4 B4 LVDS_B3B_12_P CLK In
LVDS_B3B_17_N A5 B5 LVDS_B3B_12_N CLK In
A6 B6
LVDS_B3B_4_P A7 B7 LVDS_B3B_10_P CLK Out
LVDS_B3B_4_N A8 B8 LVDS_B3B_10_N CLK Out
A9 B9
LVDS_B3B_3_P A10 B10 LVDS_B3B_8_P
LVDS_B3B_3_N A11 B11 LVDS_B3B_8_N
A12 B12
LVDS_B3B_1_P A13 B13 LVDS_B3B_16_P
LVDS_B3B_1_N A14 B14 LVDS_B3B_16_N
A15 B15
LVDS_B3B_6_P A16 B16 LVDS_B3B_20_P
LVDS_B3B_6_N A17 B17 LVDS_B3B_20_N
A18 B18
HVIO
GPIO_B3C_31_3 A19 B19 GPIO_B3C_16_2
GPIO_B3C_27_3 A20 B20 GPIO_B3C_17_2
GPIO_B3C_26_3 A21 B21 GPIO_B3C_18_2
GPIO_B3C_25_3 A22 B22 GPIO_B3C_20_2
GPIO_B3C_24_3 A23 B23 GPIO_B3C_21_2
GPIO_B3C_30_3 A24 B24 GPIO_B3C_19_2
GPIO_B3C_28_3 A25 B25 GPIO_B3C_22_2
GPIO_B3C_29_3 A26 B26 GPIO_B3C_23_2
GPIO_B3C_41_5 A27 B27 GPIO_B3C_44_5
GPIO_B3C_40_5 A28 B28 GPIO_B3C_46_5
GPIO_B3C_45_5 A29 B29 GPIO_B3C_43_5
GPIO_B3C_47_5 A30 B30 GPIO_B3C_42_5
A31 B31
HVIO
VREF_B3B A32 B32 VREF_B3C
A33 B33 VREF_B3D
A34 B34
A35 B35
A36 B36
A37 B37
A38 B38
A39 B39
A40 B40
A41 B41
A42 B42
A43 B43
A44 B44
HPS_IO12 A45 B45 HPS_IO22
HPS_IO4 A46 B46 HPS_IO19
HPS_IO3 A47 B47 HPS_IO24
HPS_IO5 A48 B48 HPS_IO17
HPS_IO7 A49 B49 HPS_IO15
HPS_IO2 A50 B50 HPS_IO21
HPS_IO6 A51 B51 HPS_IO18
HPS_IO9 A52 B52 HPS_IO14
HPS_IO1 A53 B53 HPS_IO23
HPS_IO10 A54 B54 HPS_IO16
HPS_IO8 A55 B55 HPS_IO13
HPS_IO11 A56 B56 HPS_IO20
A57 B57
A58 B58
A59 B59
A60 B60
ADM6-60-01.5-L-4-2-FR
GND
GND
Bank 3B is 1.8V in 1S 040
Bank 3B 48IO, 24 LVDS Pairs
Bank 3C 48IO, 6 IO Groups
Bank 3D 24IO, 4 LVDS Pairs
Bank HPS 48IO
Bank 3C is 3.3V in 1S 040
Bank 3D is 1.8V in 1S 040
Bank HPS is 1.8V in 1S 040
JM1B
LVDS_B3B_18_P C1 D1 LVDS_B3B_14_P
LVDS_B3B_18_N C2 D2 LVDS_B3B_14_N
C3 D3
LVDS_B3B_9_P C4 D4 LVDS_B3B_13_P CLK In
LVDS_B3B_9_N C5 D5 LVDS_B3B_13_N CLK In
C6 D6
LVDS_B3B_7_P C7 D7 LVDS_B3B_19_P
LVDS_B3B_7_N C8 D8 LVDS_B3B_19_N
C9 D9
LVDS_B3B_2_P C10 D10 LVDS_B3B_21_P
LVDS_B3B_2_N C11 D11 LVDS_B3B_21_N
C12 D12
LVDS_B3B_22_P C13 D13 LVDS_B3B_24_P
LVDS_B3B_22_N C14 D14 LVDS_B3B_24_N
C15 D15
HVIO
LVDS_B3B_5_P C16 D16 LVDS_B3B_23_P
LVDS_B3B_5_N C17 D17 LVDS_B3B_23_N
C18 D18
HVIO
GPIO_B3C_15_1 C19 D19 GPIO_B3C_33_4
GPIO_B3C_14_1 C20 D20 GPIO_B3C_32_4
GPIO_B3C_13_1 C21 D21 GPIO_B3C_39_4
GPIO_B3C_12_1 C22 D22 GPIO_B3C_38_4
GPIO_B3C_11_1 C23 D23 GPIO_B3C_37_4
GPIO_B3C_10_1 C24 D24 GPIO_B3C_36_4
GPIO_B3C_9_1 C25 D25 GPIO_B3C_35_4
GPIO_B3C_8_1 C26 D26 GPIO_B3C_34_4
GPIO_B3C_5_0 C27 D27 GPIO_B3C_4_0
GPIO_B3C_3_0 C28 D28 GPIO_B3C_6_0
GPIO_B3C_2_0 C29 D29 GPIO_B3C_7_0
GPIO_B3C_0_0 C30 D30 GPIO_B3C_1_0
C31 D31
GPIO_B3D_49_P C32 D32 GPIO_B3D_53_P
GPIO_B3D_49_N C33 D33 GPIO_B3D_53_N
LVDS_B3D_55_P C34 D34 GPIO_B3D_51_P
LVDS_B3D_55_N C35 D35 GPIO_B3D_51_N
GPIO_B3D_54_P C36 D36 LVDS_B3D_59_P
GPIO_B3D_54_N C37 D37 LVDS_B3D_59_N
GPIO_B3D_58_P C38 D38 GPIO_B3D_56_P
GPIO_B3D_58_N C39 D39 GPIO_B3D_56_N
LVDS_B3D_57_P C40 D40 GPIO_B3D_50_P
LVDS_B3D_57_N C41 D41 GPIO_B3D_50_N
GPIO_B3D_52_P C42 D42 GPIO_B3D_48_P
GPIO_B3D_52_N C43 D43 GPIO_B3D_48_N
C44 D44
HPS_IO36 C45 D45 HPS_IO46
HPS_IO31 C46 D46 HPS_IO48
HPS_IO26 C47 D47 HPS_IO43
HPS_IO30 C48 D48 HPS_IO39
HPS_IO29 C49 D49 HPS_IO45
HPS_IO25 C50 D50 HPS_IO38
HPS_IO35 C51 D51 HPS_IO41
HPS_IO28 C52 D52 HPS_IO40
HPS_IO33 C53 D53 HPS_IO42
HPS_IO32 C54 D54 HPS_IO44
HPS_IO27 C55 D55 HPS_IO47
HPS_IO34 C56 D56 HPS_IO37
C57 D57
C58 D58
C59 D59
C60 D60
GND
GND
ADM6-60-01.5-L-4-2-FR
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Title: TEI1000 - Connector J2
A4
Number: TEI1000 AGI11-A
Rev. 02
Date: 2024-06-20
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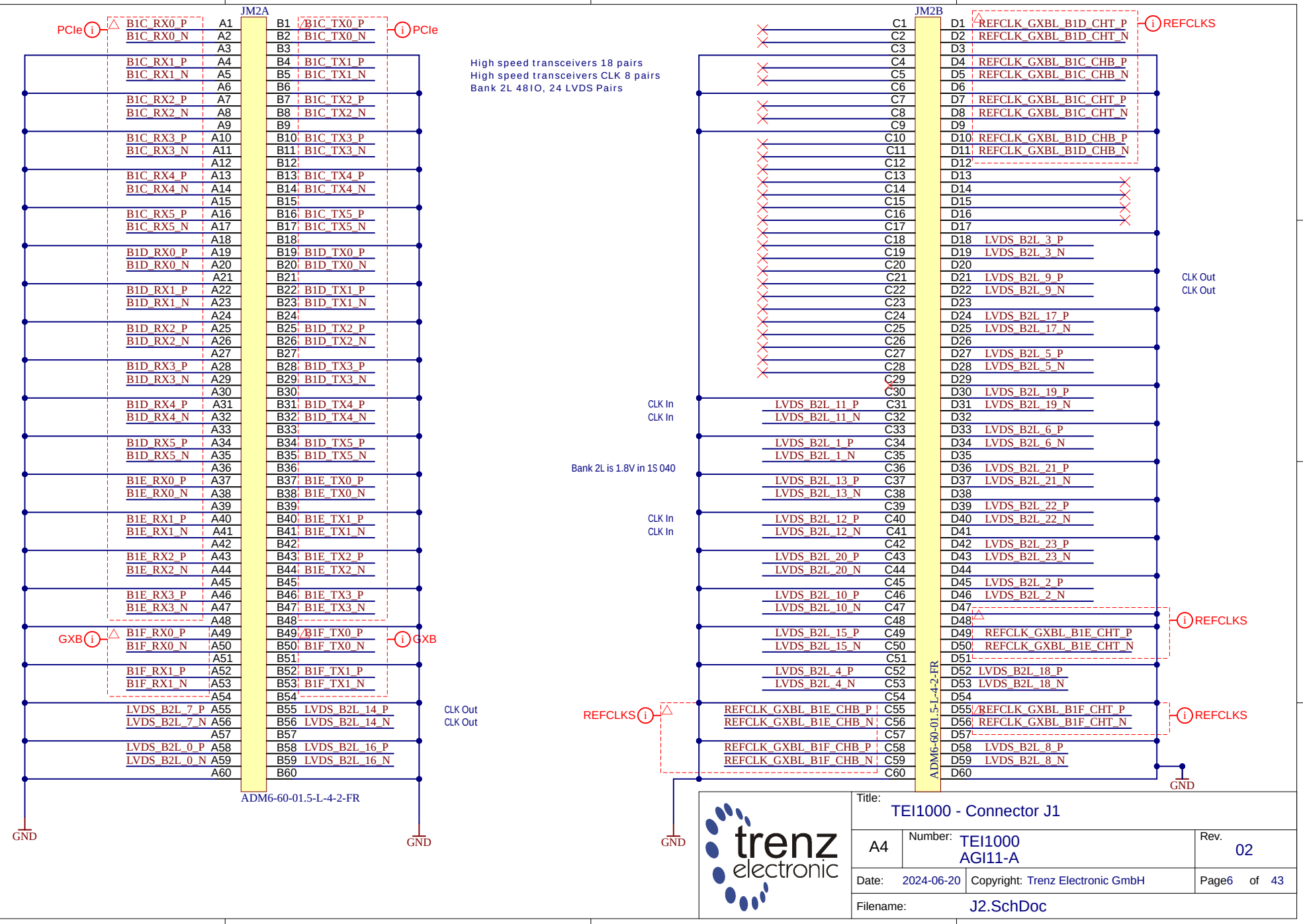
Filename: J1.SchDoc



Title: TEI1000 - Connector J1			
A4	Number: TEI1000 AGI11-A		Rev. 02
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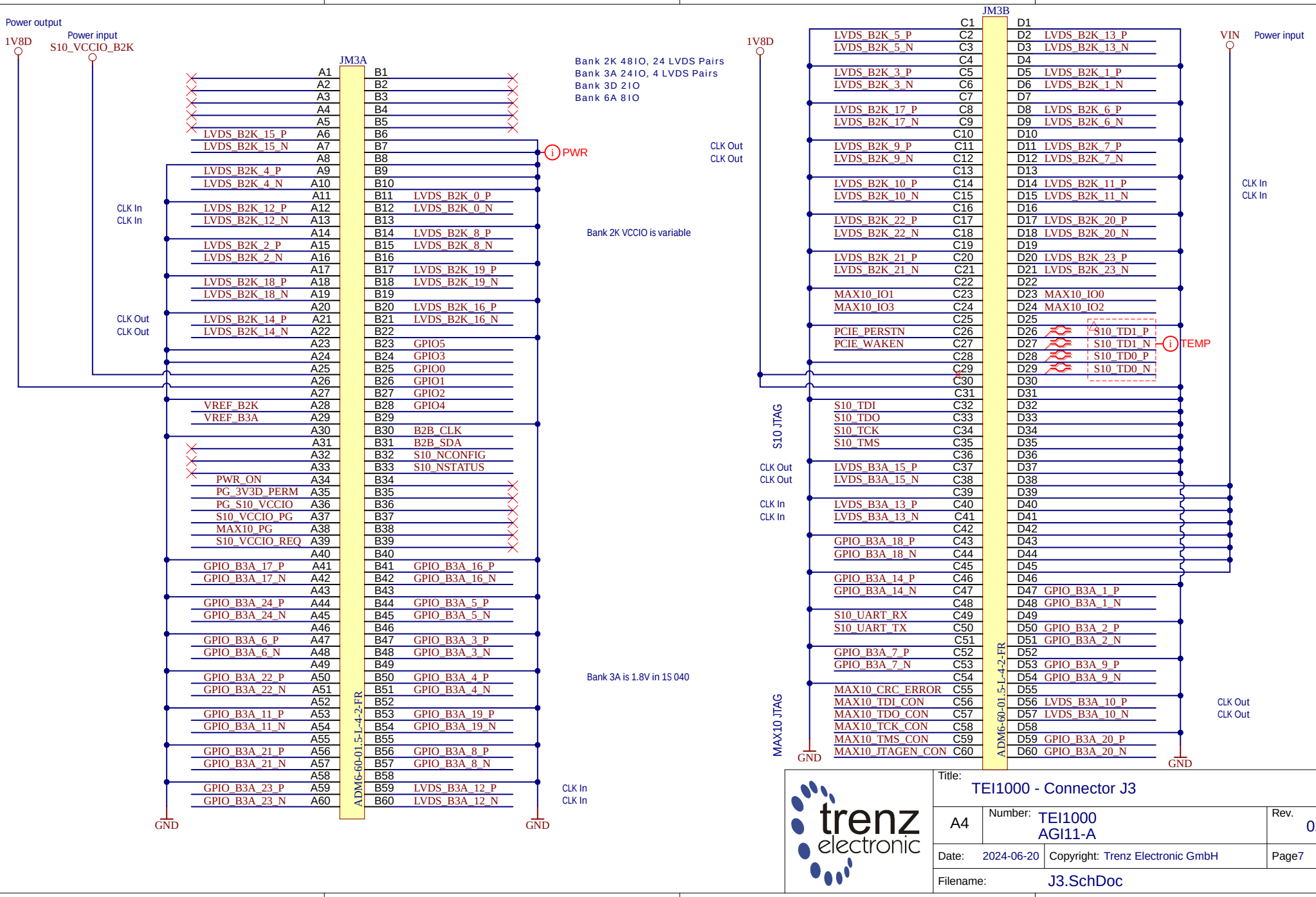
Filename: J2.SchDoc			



Title:	TEI1000 - Connector J3		
A4	Number: TEI1000 AGI11-A		Rev. 02
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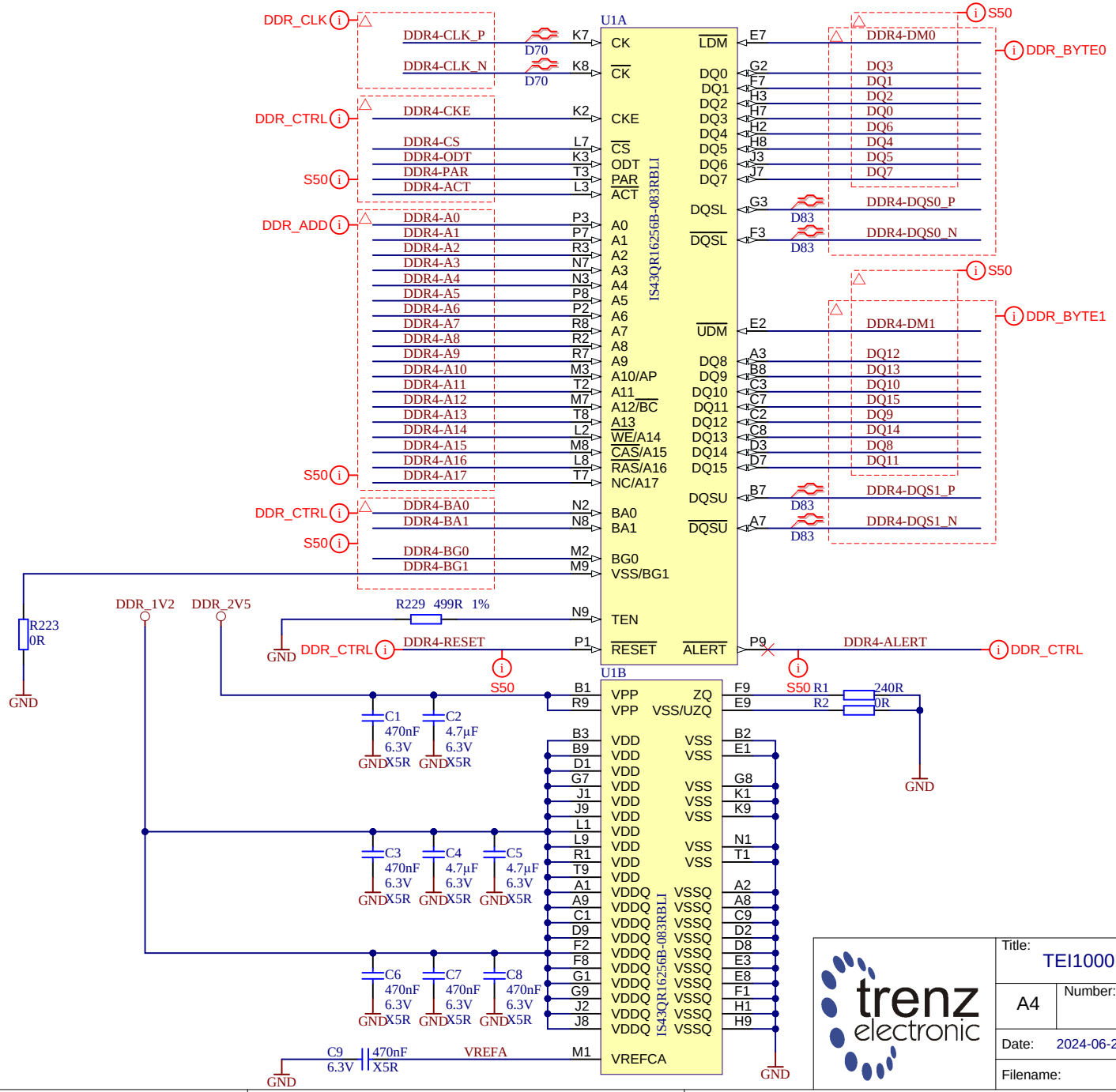

Title: TEI1000 - DDR4_1_RAM			
A4	Number: TEI1000 AGI11-A		Rev. 02
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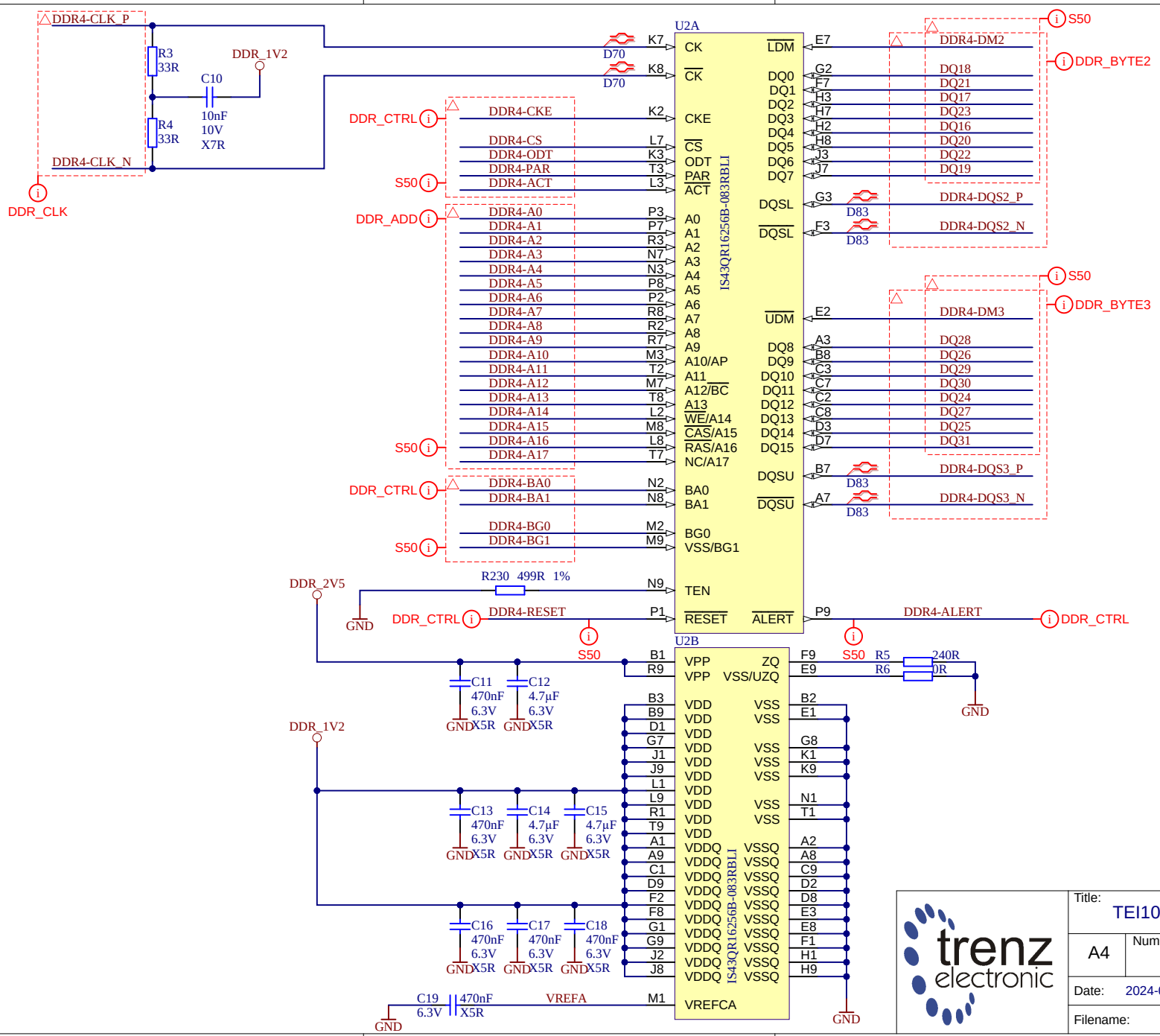
DDR4-CLK_P
DDR4-CLK_N
DDR_CLK
R3 33R
R4 33R
C10 10nF 10V X7R
DDR_1V2
U2A
IS43QR16256B-083RBLI
CK
CKE
CS
ODT
PAR
ACT
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
WE/A14
CAS/A15
RAS/A16
NC/A17
BA0
BA1
BG0
VSS/BG1
TEN
RESET
LDM
UDM
DQSL
DQSU
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
ALERT
D70
D83
DDR_CTRL
DDR4-CKE
DDR4-CS
DDR4-ODT
DDR4-PAR
DDR4-ACT
DDR_ADD
DDR4-A0
DDR4-A1
DDR4-A2
DDR4-A3
DDR4-A4
DDR4-A5
DDR4-A6
DDR4-A7
DDR4-A8
DDR4-A9
DDR4-A10
DDR4-A11
DDR4-A12
DDR4-A13
DDR4-A14
DDR4-A15
DDR4-A16
DDR4-A17
DDR4-BA0
DDR4-BA1
DDR4-BG0
DDR4-BG1
S50
DDR_BYTE2
DDR_BYTE3
DDR4-DM2
DDR4-DM3
DDR4-DQS2_P
DDR4-DQS2_N
DDR4-DQS3_P
DDR4-DQS3_N
DQ18
DQ21
DQ17
DQ23
DQ16
DQ20
DQ22
DQ19
DQ28
DQ26
DQ29
DQ30
DQ24
DQ27
DQ25
DQ31
DDR_2V5
R230 499R 1%
DDR4-RESET
DDR4-ALERT
GND
U2B
VPP
VDD
VSS
VDDQ
VSSQ
VREFCA
ZQ
VSS/UZQ
R5 240R
R6 0R
C11 470nF 6.3V X5R
C12 4.7µF 6.3V X5R
C13 470nF 6.3V X5R
C14 4.7µF 6.3V X5R
C15 4.7µF 6.3V X5R
C16 470nF 6.3V X5R
C17 470nF 6.3V X5R
C18 470nF 6.3V X5R
C19 470nF 6.3V X5R
VREFA
trenz electronic
Title: TEI1000 - DDR4_2_RAM
A4
Number: TEI1000 AGI11-A
Rev. 02
Date: 2024-06-20
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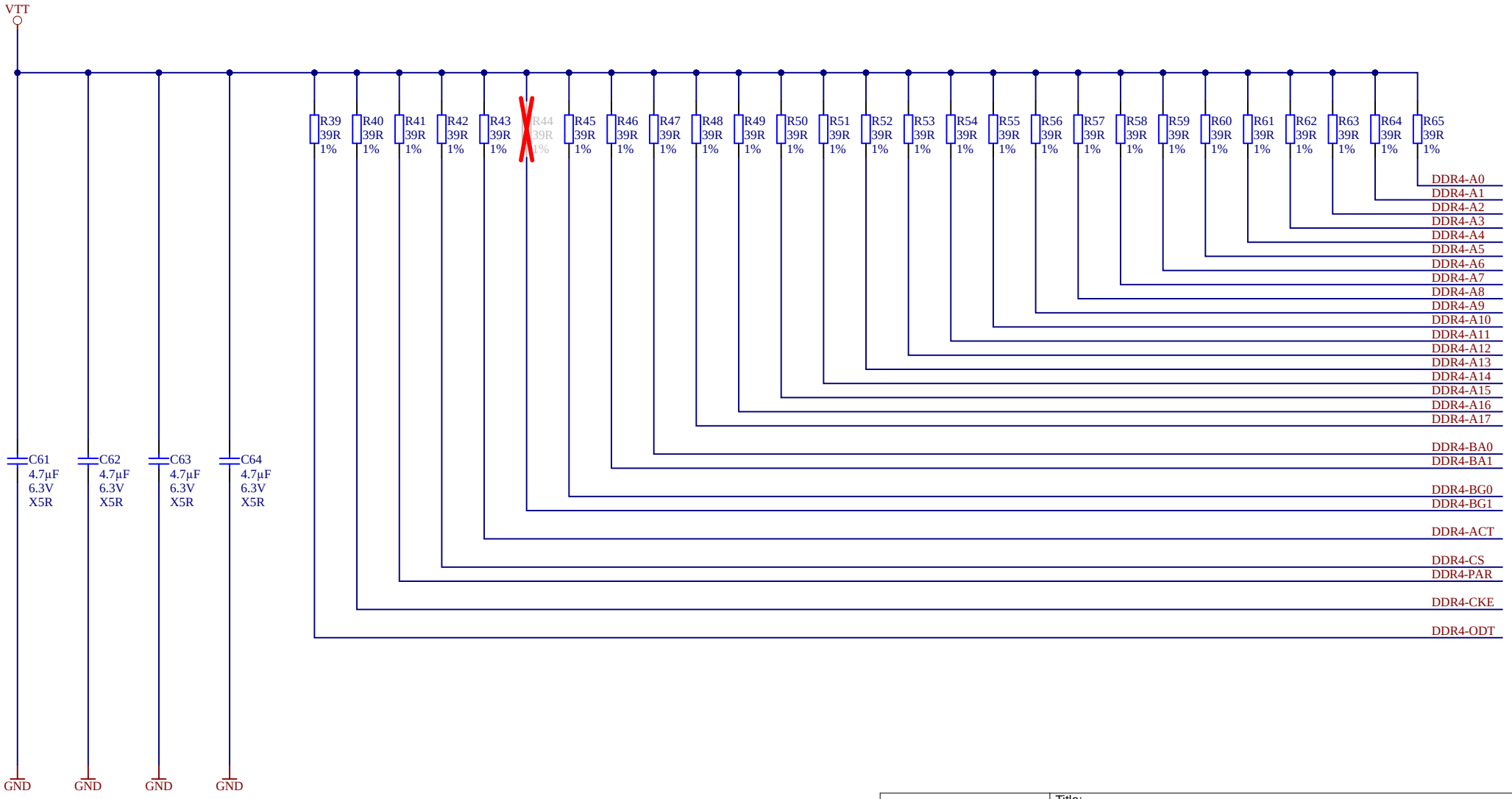
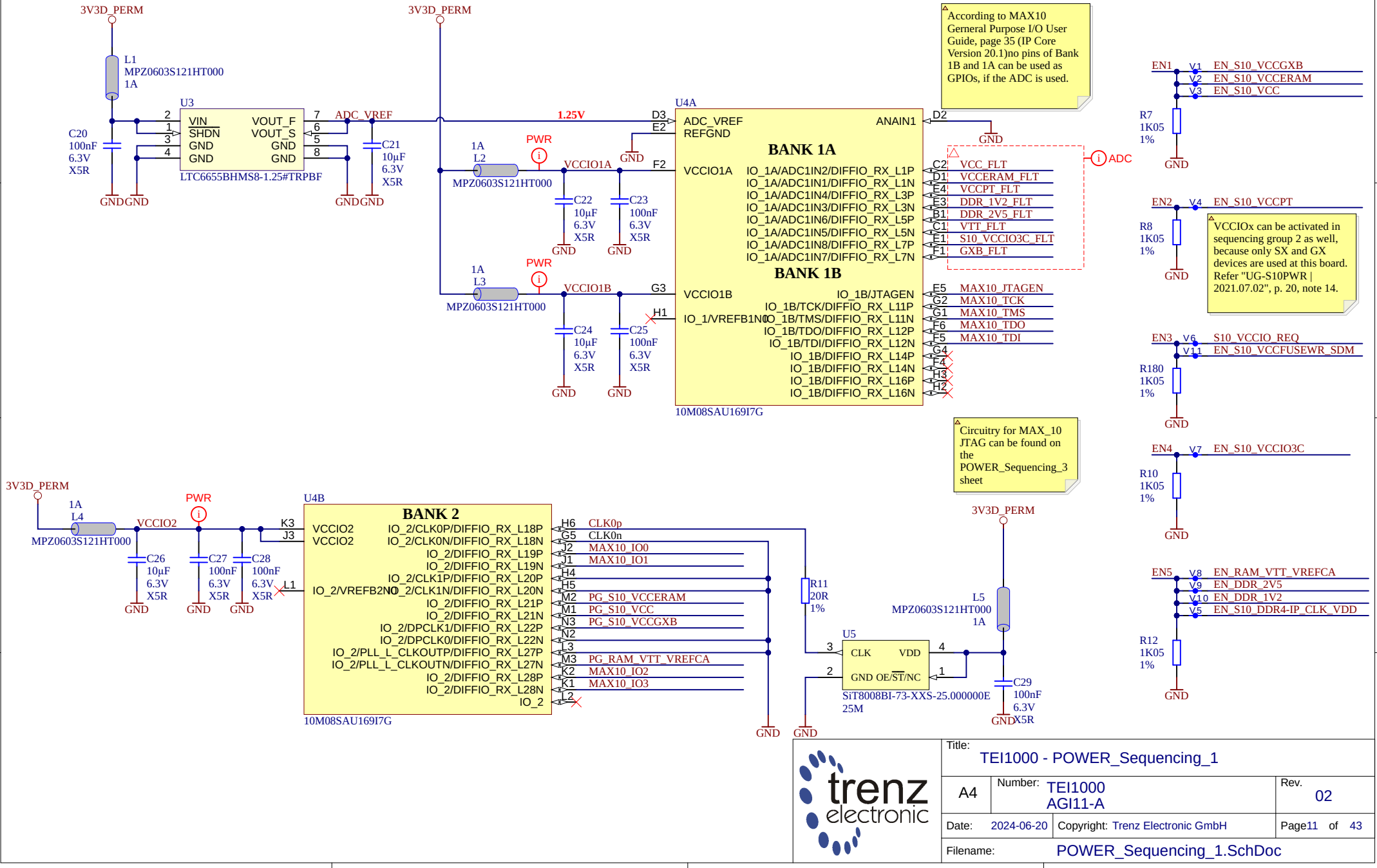
Page9 of 43
Filename: DDR4-RAM_2.SchDoc



trenz electronic	Title: TEI1000 - DDR4_TERM		
	A4	Number: TEI1000 AGI11-A	Rev. 02
	Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page10 of 43
	Filename: DDR4-TERM.SchDoc		


3V3D_PERM
L1
MPZ0603S121HT000
1A
U3
VIN
SHDN
GND
GND
VOUT_F
VOUT_S
GND
GND
ADC_VREF
LTC6655BHMS8-1.25#TRPBF
C20
100nF
6.3V
X5R
C21
10µF
6.3V
X5R
1.25V
U4A
ADC_VREF
REFGND
ANAIN1
BANK 1A
VCCIO1A
IO_1A/ADC1IN2/DIFFIO_RX_L1P
IO_1A/ADC1IN1/DIFFIO_RX_L1N
IO_1A/ADC1IN4/DIFFIO_RX_L3P
IO_1A/ADC1IN3/DIFFIO_RX_L3N
IO_1A/ADC1IN6/DIFFIO_RX_L5P
IO_1A/ADC1IN5/DIFFIO_RX_L5N
IO_1A/ADC1IN8/DIFFIO_RX_L7P
IO_1A/ADC1IN7/DIFFIO_RX_L7N
BANK 1B
VCCIO1B
IO_1B/JTAGEN
IO_1B/TCK/DIFFIO_RX_L11P
IO_1B/TMS/DIFFIO_RX_L11N
IO_1B/TDO/DIFFIO_RX_L12P
IO_1B/TDI/DIFFIO_RX_L12N
IO_1B/DIFFIO_RX_L14P
IO_1B/DIFFIO_RX_L14N
IO_1B/DIFFIO_RX_L16P
IO_1B/DIFFIO_RX_L16N
IO_1/VREFB1N0
10M08SAU169I7G
1A
L2
MPZ0603S121HT000
PWR
VCCIO1A
C22
10µF
6.3V
X5R
C23
100nF
6.3V
X5R
1A
L3
MPZ0603S121HT000
PWR
VCCIO1B
C24
10µF
6.3V
X5R
C25
100nF
6.3V
X5R
According to MAX10 Gerneral Purpose I/O User Guide, page 35 (IP Core Version 20.1)no pins of Bank 1B and 1A can be used as GPIOs, if the ADC is used.
ADC
VCC_FLT
VCCERAM_FLT
VCCPT_FLT
DDR_1V2_FLT
DDR_2V5_FLT
VTT_FLT
S10_VCCIO3C_FLT
GXB_FLT
MAX10_JTAGEN
MAX10_TCK
MAX10_TMS
MAX10_TDO
MAX10_TDI
Circuitry for MAX_10 JTAG can be found on the POWER_Sequencing_3 sheet
EN1
EN_S10_VCCGXB
EN_S10_VCCERAM
EN_S10_VCC
R7
1K05
1%
EN2
EN_S10_VCCPT
R8
1K05
1%
VCCIOx can be activated in sequencing group 2 as well, because only SX and GX devices are used at this board. Refer "UG-S10PWR | 2021.07.02", p. 20, note 14.
EN3
S10_VCCIO_REQ
EN_S10_VCCFUSEWR_SDM
R180
1K05
1%
EN4
EN_S10_VCCIO3C
R10
1K05
1%
EN5
EN_RAM_VTT_VREFCA
EN_DDR_2V5
EN_DDR_1V2
EN_S10_DDR4-IP_CLK_VDD
R12
1K05
1%
3V3D_PERM
1A
L4
MPZ0603S121HT000
PWR
VCCIO2
C26
10µF
6.3V
X5R
C27
100nF
6.3V
X5R
C28
100nF
6.3V
X5R
L1
U4B
BANK 2
VCCIO2
VCCIO2
IO_2/CLK0P/DIFFIO_RX_L18P
IO_2/CLK0N/DIFFIO_RX_L18N
IO_2/DIFFIO_RX_L19P
IO_2/DIFFIO_RX_L19N
IO_2/CLK1P/DIFFIO_RX_L20P
IO_2/CLK1N/DIFFIO_RX_L20N
IO_2/DIFFIO_RX_L21P
IO_2/DIFFIO_RX_L21N
IO_2/DPCLK1/DIFFIO_RX_L22P
IO_2/DPCLK0/DIFFIO_RX_L22N
IO_2/PLL_L_CLKOUTP/DIFFIO_RX_L27P
IO_2/PLL_L_CLKOUTN/DIFFIO_RX_L27N
IO_2/DIFFIO_RX_L28P
IO_2/DIFFIO_RX_L28N
IO_2
IO_2/VREFB2N0
10M08SAU169I7G
CLK0p
CLK0n
MAX10_IO0
MAX10_IO1
PG_S10_VCCERAM
PG_S10_VCC
PG_S10_VCCGXB
PG_RAM_VTT_VREFCA
MAX10_IO2
MAX10_IO3
R11
20R
1%
U5
CLK
VDD
GND
OE/ST/NC
SiT8008BI-73-XXS-25.000000E
25M
3V3D_PERM
L5
MPZ0603S121HT000
1A
C29
100nF
6.3V
X5R
GND
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A4
Number: TEI1000 AGI11-A
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Date: 2024-06-20
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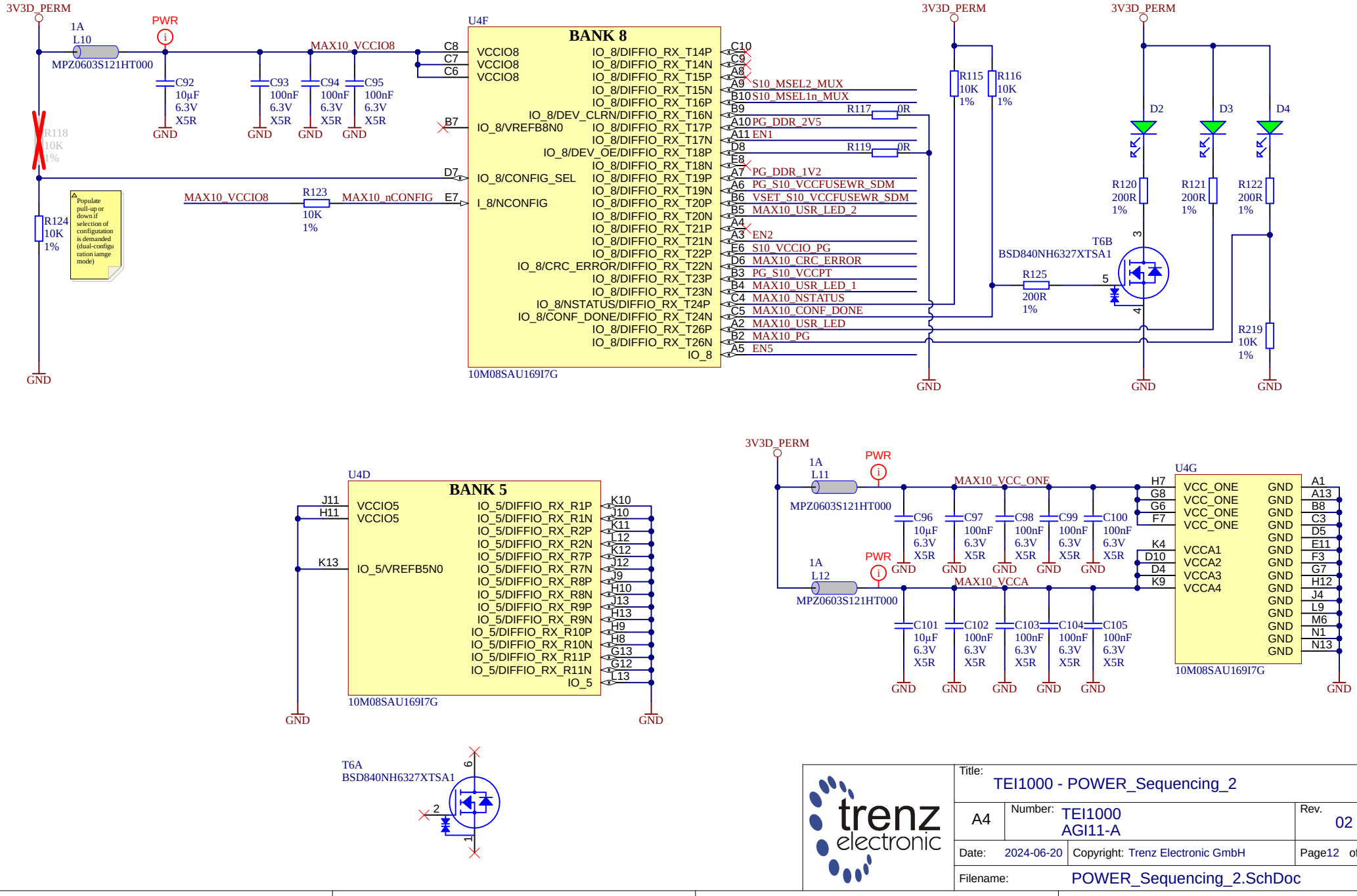
Filename: POWER_Sequencing_1.SchDoc


3V3D_PERM
1A
L10
MPZ0603S121HT000
PWR
C92
10µF
6.3V
X5R
GND
C93
100nF
6.3V
X5R
C94
100nF
6.3V
X5R
C95
100nF
6.3V
X5R
MAX10_VCCIO8
R118
10K
1%
R124
10K
1%
Populate pull-up or down if selection of configuration is demanded (dual-configu ration iamge mode)
U4F
BANK 8
VCCIO8
VCCIO8
VCCIO8
IO_8/VREFB8N0
IO_8/CONFIG_SEL
I_8/NCONFIG
IO_8/DEV_CLRN/DIFFIO_RX_T16N
IO_8/DEV_OE/DIFFIO_RX_T18P
IO_8/CRC_ERROR/DIFFIO_RX_T22N
IO_8/NSTATUS/DIFFIO_RX_T24P
IO_8/CONF_DONE/DIFFIO_RX_T24N
IO_8
S10_MSEL2_MUX
S10_MSEL1n_MUX
PG_DDR_2V5
EN1
PG_DDR_1V2
PG_S10_VCCFUSEWR_SDM
VSET_S10_VCCFUSEWR_SDM
MAX10_USR_LED_2
EN2
S10_VCCIO_PG
MAX10_CRC_ERROR
PG_S10_VCCPT
MAX10_USR_LED_1
MAX10_NSTATUS
MAX10_CONF_DONE
MAX10_USR_LED
MAX10_PG
EN5
10M08SAU169I7G
MAX10_nCONFIG
R123
10K
1%
R117
0R
R119
0R
R115
10K
1%
R116
10K
1%
R125
200R
1%
T6B
BSD840NH6327XTSA1
D2
D3
D4
R120
200R
1%
R121
200R
1%
R122
200R
1%
R219
10K
1%
U4D
BANK 5
VCCIO5
VCCIO5
IO_5/VREFB5N0
IO_5
10M08SAU169I7G
T6A
BSD840NH6327XTSA1
3V3D_PERM
1A
L11
MPZ0603S121HT000
PWR
1A
L12
MPZ0603S121HT000
MAX10_VCC_ONE
MAX10_VCCA
C96
10µF
6.3V
X5R
C97
100nF
6.3V
X5R
C98
100nF
6.3V
X5R
C99
100nF
6.3V
X5R
C100
100nF
6.3V
X5R
C101
10µF
6.3V
X5R
C102
100nF
6.3V
X5R
C103
100nF
6.3V
X5R
C104
100nF
6.3V
X5R
C105
100nF
6.3V
X5R
U4G
VCC_ONE
VCCA1
VCCA2
VCCA3
VCCA4
GND
10M08SAU169I7G
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Title: TEI1000 - POWER_Sequencing_2
A4
Number: TEI1000 AGI11-A
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Date: 2024-06-20
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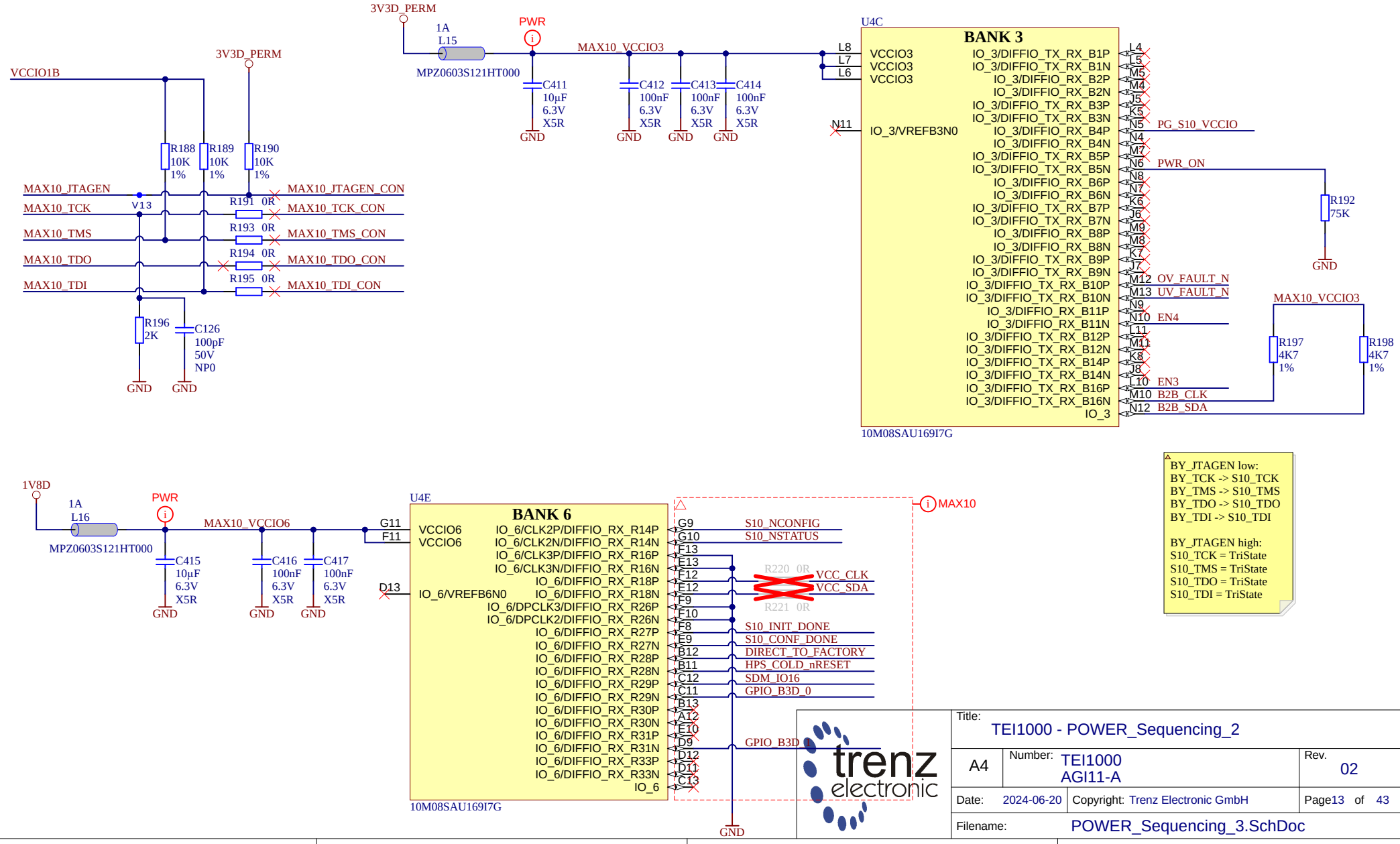
Filename: POWER_Sequencing_2.SchDoc


3V3D_PERM
1A
L15
MPZ0603S121HT000
PWR
MAX10_VCCIO3
C411
10µF
6.3V
X5R
C412
100nF
6.3V
X5R
C413
100nF
6.3V
X5R
C414
100nF
6.3V
X5R
GND
U4C
BANK 3
VCCIO3
IO_3/VREFB3N0
IO_3/DIFFIO_TX_RX_B1P
IO_3/DIFFIO_TX_RX_B1N
IO_3/DIFFIO_RX_B2P
IO_3/DIFFIO_RX_B2N
IO_3/DIFFIO_TX_RX_B3P
IO_3/DIFFIO_TX_RX_B3N
IO_3/DIFFIO_RX_B4P
IO_3/DIFFIO_RX_B4N
IO_3/DIFFIO_TX_RX_B5P
IO_3/DIFFIO_TX_RX_B5N
IO_3/DIFFIO_RX_B6P
IO_3/DIFFIO_RX_B6N
IO_3/DIFFIO_TX_RX_B7P
IO_3/DIFFIO_TX_RX_B7N
IO_3/DIFFIO_RX_B8P
IO_3/DIFFIO_RX_B8N
IO_3/DIFFIO_TX_RX_B9P
IO_3/DIFFIO_TX_RX_B9N
IO_3/DIFFIO_TX_RX_B10P
IO_3/DIFFIO_TX_RX_B10N
IO_3/DIFFIO_RX_B11P
IO_3/DIFFIO_RX_B11N
IO_3/DIFFIO_TX_RX_B12P
IO_3/DIFFIO_TX_RX_B12N
IO_3/DIFFIO_TX_RX_B14P
IO_3/DIFFIO_TX_RX_B14N
IO_3/DIFFIO_TX_RX_B16P
IO_3/DIFFIO_TX_RX_B16N
IO_3
10M08SAU169I7G
PG_S10_VCCIO
PWR_ON
OV_FAULT_N
UV_FAULT_N
EN4
EN3
B2B_CLK
B2B_SDA
R192
75K
MAX10_VCCIO3
R197
4K7
1%
R198
4K7
1%
VCCIO1B
3V3D_PERM
R188
10K
1%
R189
10K
1%
R190
10K
1%
MAX10_JTAGEN
MAX10_TCK
MAX10_TMS
MAX10_TDO
MAX10_TDI
V13
R191 0R
R193 0R
R194 0R
R195 0R
MAX10_JTAGEN_CON
MAX10_TCK_CON
MAX10_TMS_CON
MAX10_TDO_CON
MAX10_TDI_CON
R196
2K
C126
100pF
50V
NP0
1V8D
1A
L16
MPZ0603S121HT000
PWR
MAX10_VCCIO6
C415
10µF
6.3V
X5R
C416
100nF
6.3V
X5R
C417
100nF
6.3V
X5R
U4E
BANK 6
VCCIO6
IO_6/VREFB6N0
IO_6/CLK2P/DIFFIO_RX_R14P
IO_6/CLK2N/DIFFIO_RX_R14N
IO_6/CLK3P/DIFFIO_RX_R16P
IO_6/CLK3N/DIFFIO_RX_R16N
IO_6/DIFFIO_RX_R18P
IO_6/DIFFIO_RX_R18N
IO_6/DPCLK3/DIFFIO_RX_R26P
IO_6/DPCLK2/DIFFIO_RX_R26N
IO_6/DIFFIO_RX_R27P
IO_6/DIFFIO_RX_R27N
IO_6/DIFFIO_RX_R28P
IO_6/DIFFIO_RX_R28N
IO_6/DIFFIO_RX_R29P
IO_6/DIFFIO_RX_R29N
IO_6/DIFFIO_RX_R30P
IO_6/DIFFIO_RX_R30N
IO_6/DIFFIO_RX_R31P
IO_6/DIFFIO_RX_R31N
IO_6/DIFFIO_RX_R33P
IO_6/DIFFIO_RX_R33N
IO_6
10M08SAU169I7G
S10_NCONFIG
S10_NSTATUS
S10_INIT_DONE
S10_CONF_DONE
DIRECT_TO_FACTORY
HPS_COLD_nRESET
SDM_IO16
GPIO_B3D_0
GPIO_B3D
R220 0R
R221 0R
VCC_CLK
VCC_SDA
MAX10
BY_JTAGEN low:
BY_TCK -> S10_TCK
BY_TMS -> S10_TMS
BY_TDO -> S10_TDO
BY_TDI -> S10_TDI
BY_JTAGEN high:
S10_TCK = TriState
S10_TMS = TriState
S10_TDO = TriState
S10_TDI = TriState
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Title: TEI1000 - POWER_Sequencing_2
A4
Number: TEI1000 AGI11-A
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Date: 2024-06-20
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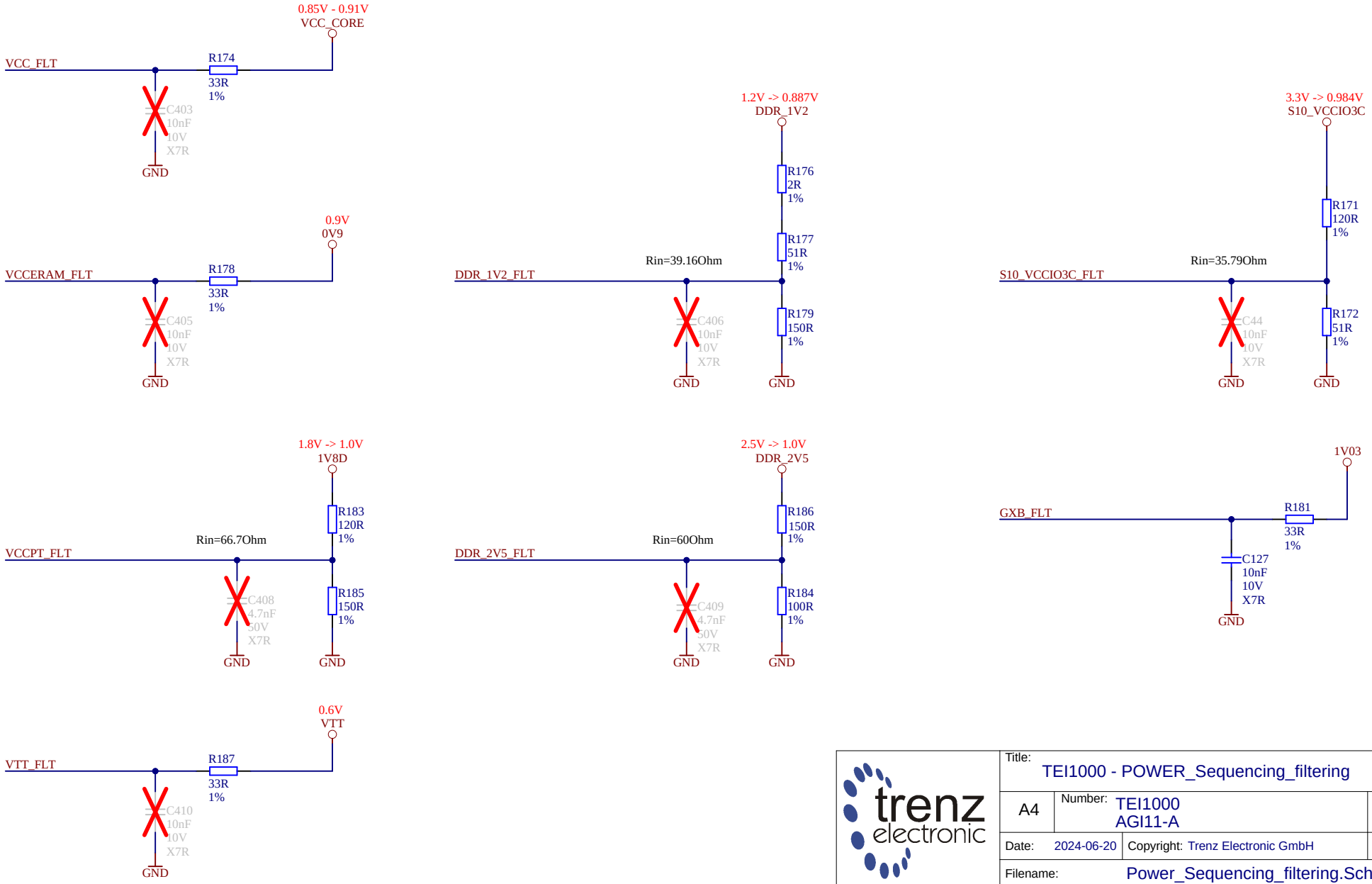
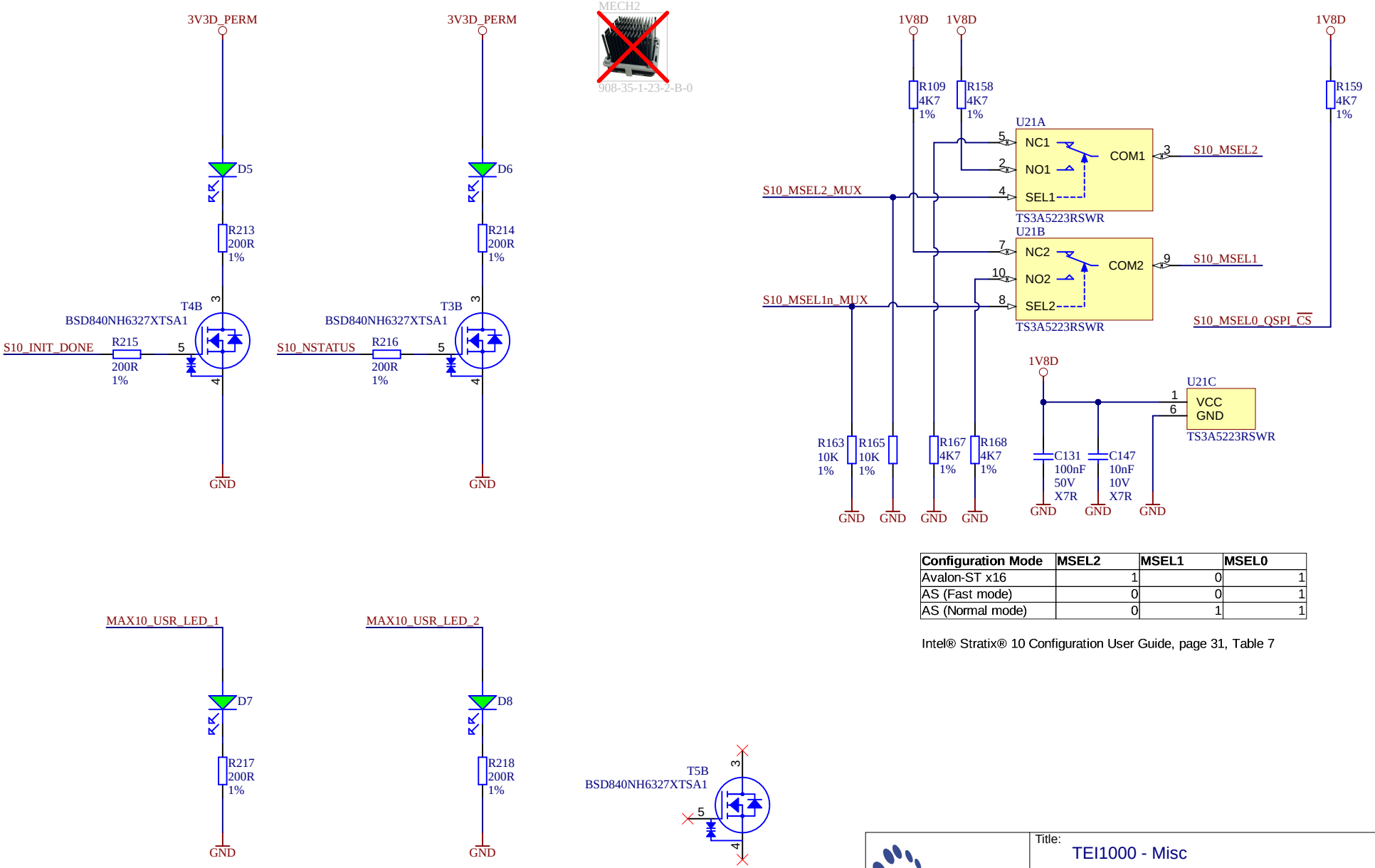
Filename: POWER_Sequencing_3.SchDoc



trenz electronic	Title: TEI1000 - POWER_Sequencing_filtering		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page14 of 43
Filename: Power_Sequencing_filtering.SchDoc			



Configuration Mode	MSEL2	MSEL1	MSEL0
Avalon-ST x16	1	0	1
AS (Fast mode)	0	0	1
AS (Normal mode)	0	1	1

Intel® Stratix® 10 Configuration User Guide, page 31, Table 7

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Title: TEI1000 - Misc		
A4	Number: TEI1000 AGI11-A	Rev. 02
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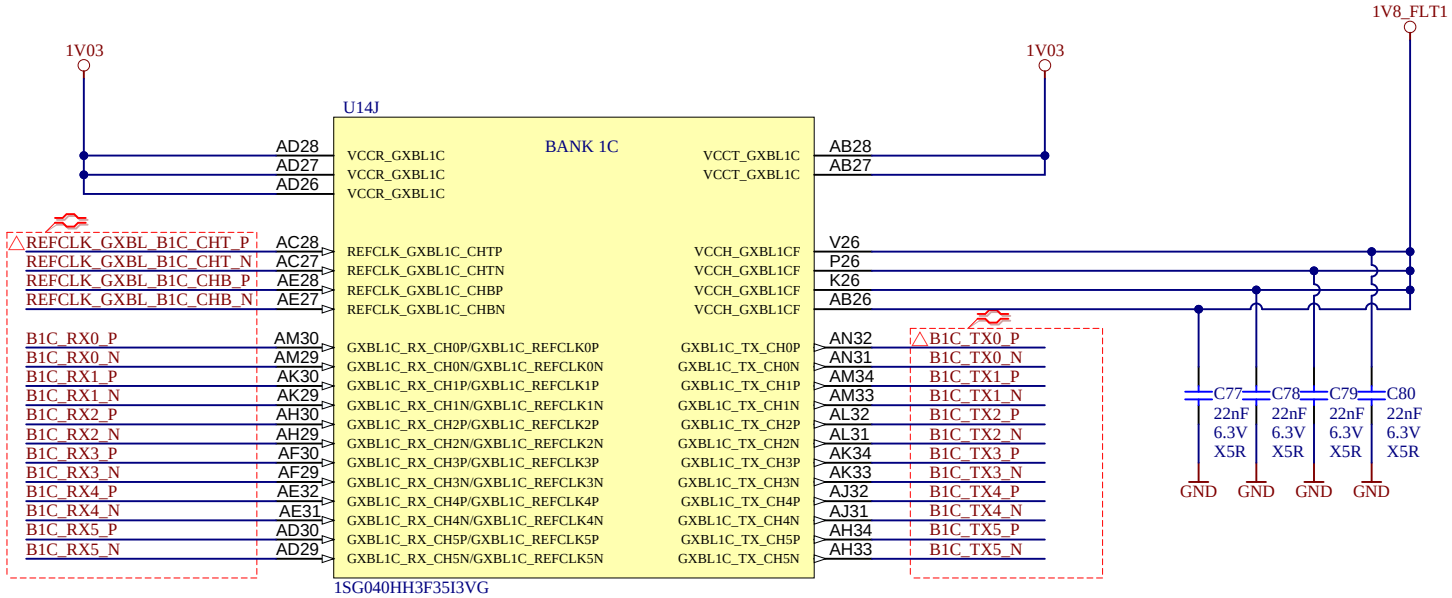
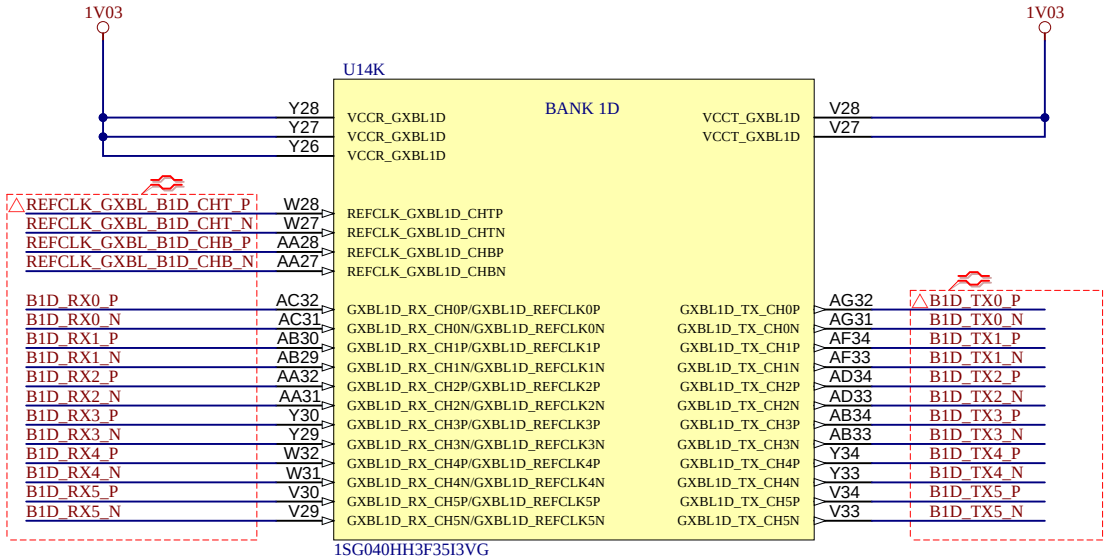
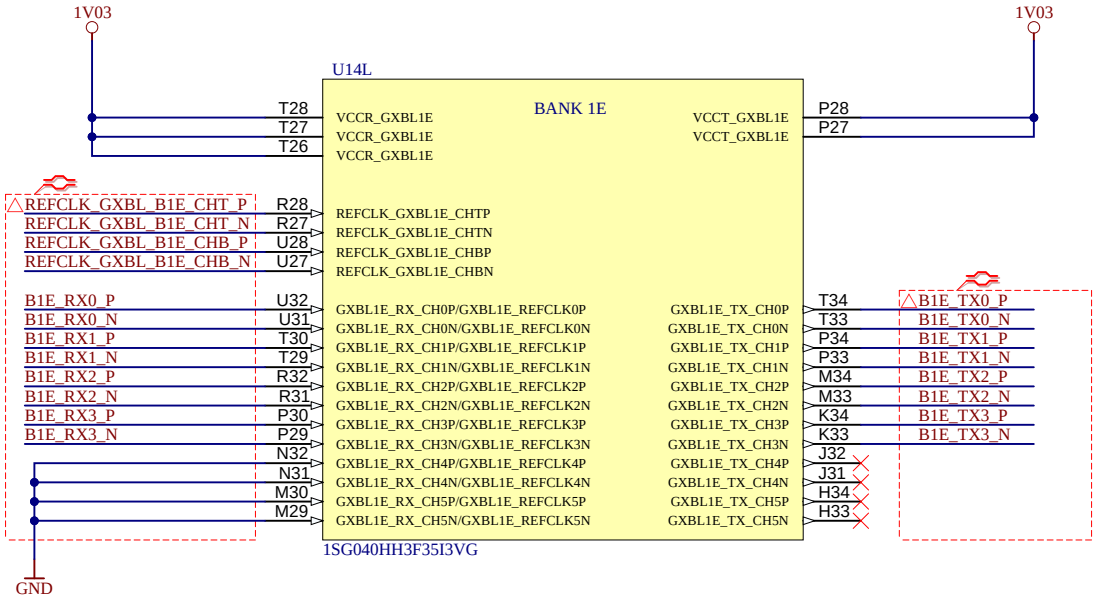
Filename: Misc.SchDoc		



trenz electronic	Title: TEI1000 - B1C		
	A4	Number: TEI1000 AGI11-A	Rev. 02
	Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page16 of 43
	Filename: Bank_1C.SchDoc		



trenz electronic	Title: TEI1000 - B1D		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page17 of 43
Filename: Bank_1D.SchDoc			



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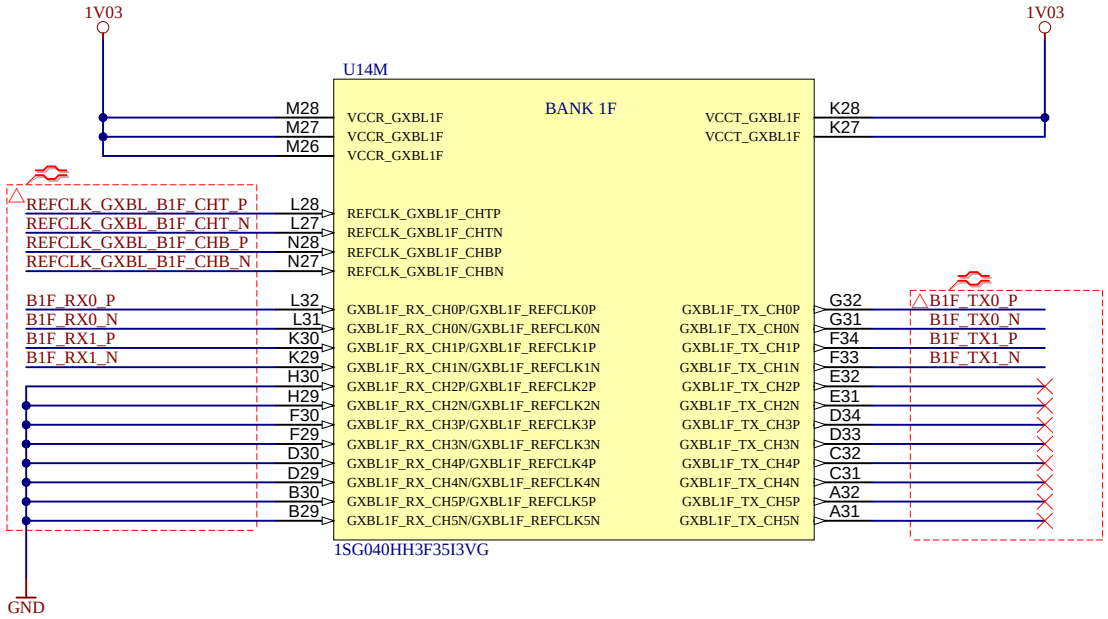
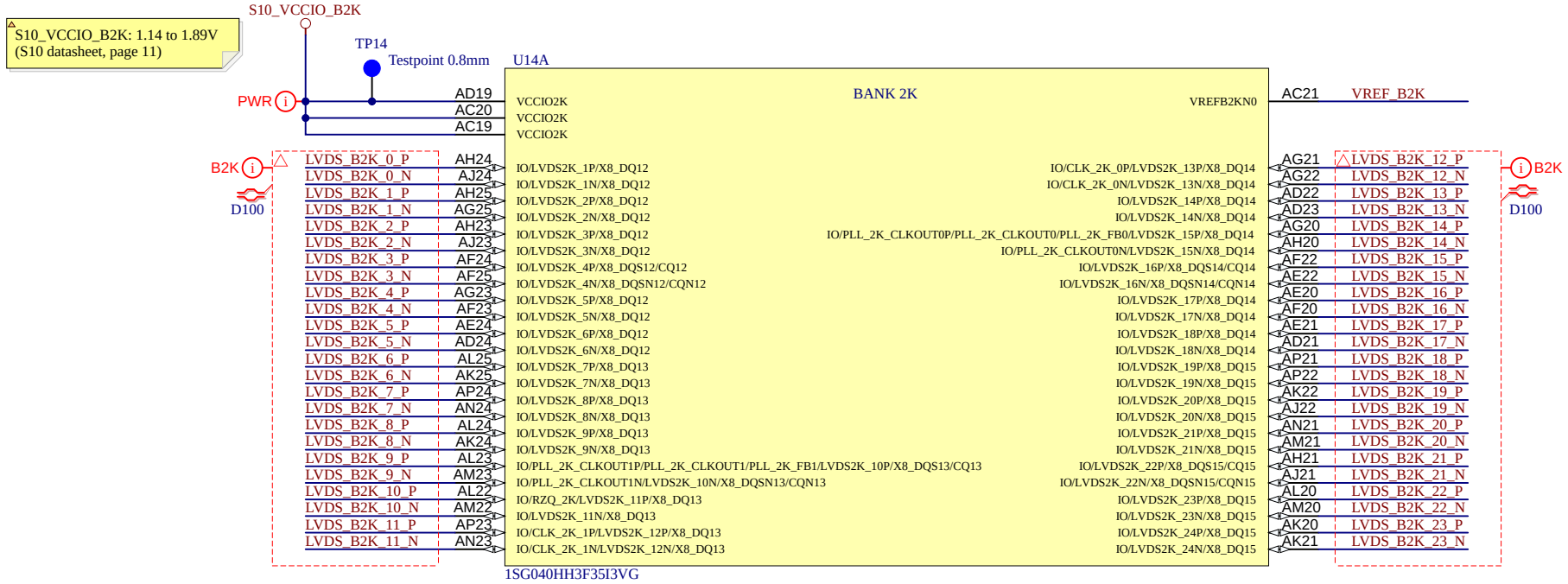
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page18 of 43
Filename: Bank_1E.SchDoc			



trenz electronic	Title: TEI1000 - B1F		
	A4	Number: TEI1000 AGI11-A	Rev. 02
	Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page19 of 43
	Filename: Bank_1F.SchDoc		



trenz electronic	Title: TEI1000 - B2K		
A4	Number: TEI1000 AGI11-A		Rev. 02
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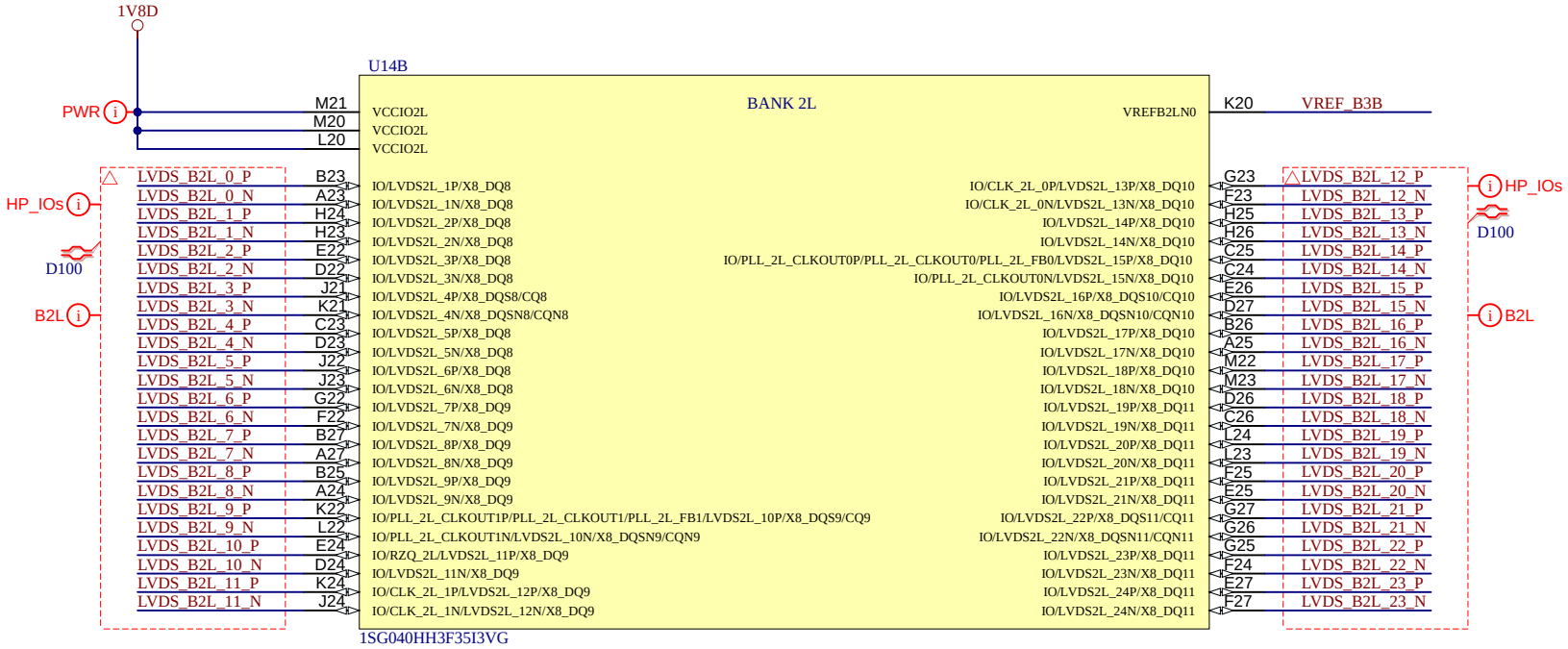
Filename: Bank_2K.SchDoc			



trenz electronic	Title: TEI1000 - B2L		
A4	Number: TEI1000 AGI11-A		Rev. 02
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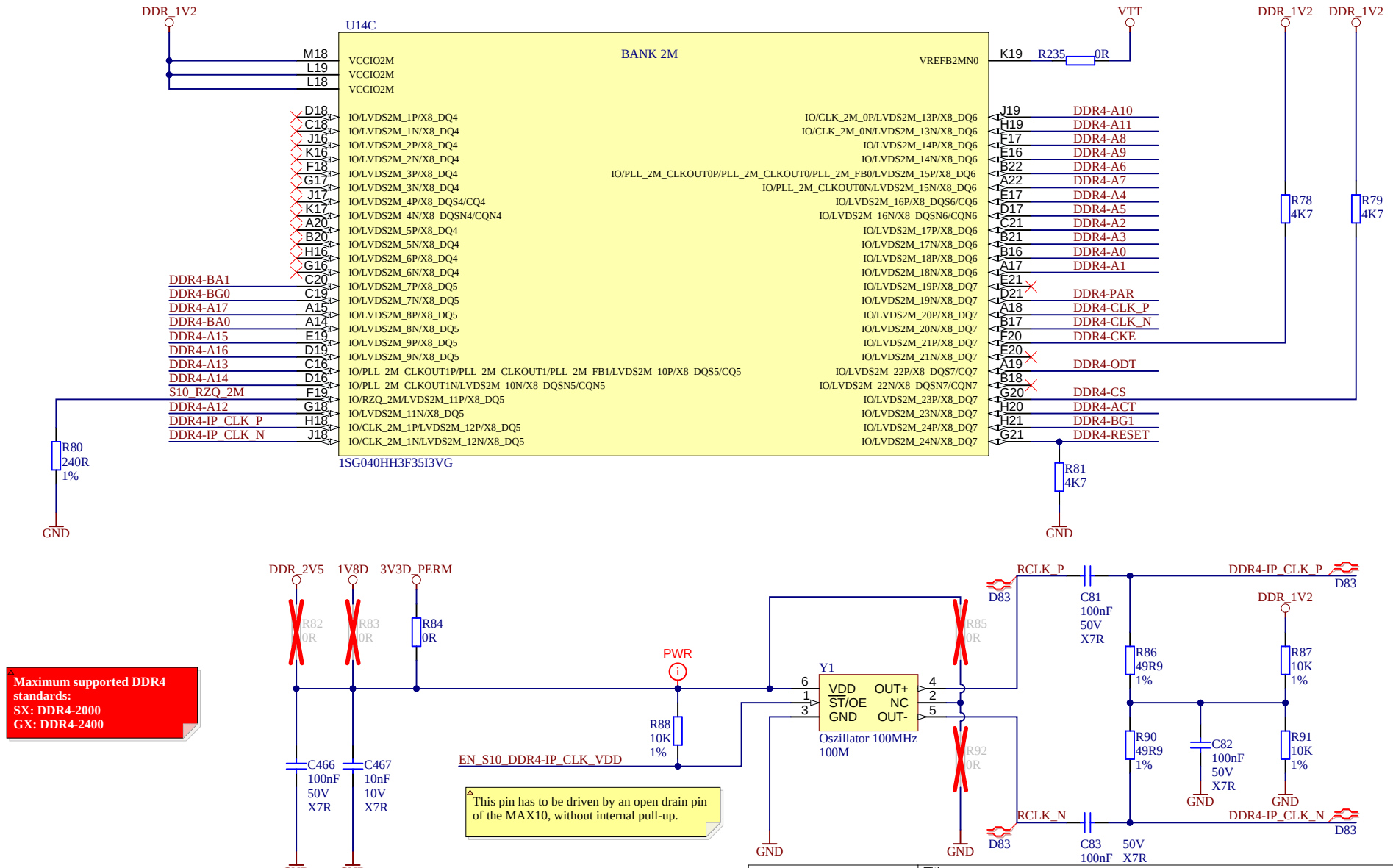
U14C
BANK 2M
1SG040HH3F35I3VG
DDR_1V2
VTT
R235 0R
R78 4K7
R79 4K7
R80 240R 1%
R81 4K7
GND
DDR_2V5
1V8D
3V3D_PERM
R82 0R
R83 0R
R84 0R
PWR
R88 10K 1%
EN_S10_DDR4-IP_CLK_VDD
Y1
VDD
ST/OE
GND
OUT+
NC
OUT-
Oszillator 100MHz
100M
R85 0R
R92 0R
C466 100nF 50V X7R
C467 10nF 10V X7R
C81 100nF 50V X7R
C82 100nF 50V X7R
C83 100nF 50V X7R
R86 49R9 1%
R87 10K 1%
R90 49R9 1%
R91 10K 1%
RCLK_P
RCLK_N
D83
DDR4-IP_CLK_P
DDR4-IP_CLK_N
Maximum supported DDR4 standards:
SX: DDR4-2000
GX: DDR4-2400
This pin has to be driven by an open drain pin of the MAX10, without internal pull-up.
VCCIO2M
VREFB2MN0
IO/LVDS2M_1P/X8_DQ4
IO/LVDS2M_1N/X8_DQ4
IO/LVDS2M_2P/X8_DQ4
IO/LVDS2M_2N/X8_DQ4
IO/LVDS2M_3P/X8_DQ4
IO/LVDS2M_3N/X8_DQ4
IO/LVDS2M_4P/X8_DQS4/CQ4
IO/LVDS2M_4N/X8_DQSN4/CQN4
IO/LVDS2M_5P/X8_DQ4
IO/LVDS2M_5N/X8_DQ4
IO/LVDS2M_6P/X8_DQ4
IO/LVDS2M_6N/X8_DQ4
IO/LVDS2M_7P/X8_DQ5
IO/LVDS2M_7N/X8_DQ5
IO/LVDS2M_8P/X8_DQ5
IO/LVDS2M_8N/X8_DQ5
IO/LVDS2M_9P/X8_DQ5
IO/LVDS2M_9N/X8_DQ5
IO/PLL_2M_CLKOUT1P/PLL_2M_CLKOUT1/PLL_2M_FB1/LVDS2M_10P/X8_DQS5/CQ5
IO/PLL_2M_CLKOUT1N/LVDS2M_10N/X8_DQSN5/CQN5
IO/RZQ_2M/LVDS2M_11P/X8_DQ5
IO/LVDS2M_11N/X8_DQ5
IO/CLK_2M_1P/LVDS2M_12P/X8_DQ5
IO/CLK_2M_1N/LVDS2M_12N/X8_DQ5
IO/CLK_2M_0P/LVDS2M_13P/X8_DQ6
IO/CLK_2M_0N/LVDS2M_13N/X8_DQ6
IO/LVDS2M_14P/X8_DQ6
IO/LVDS2M_14N/X8_DQ6
IO/PLL_2M_CLKOUT0P/PLL_2M_CLKOUT0/PLL_2M_FB0/LVDS2M_15P/X8_DQ6
IO/PLL_2M_CLKOUT0N/LVDS2M_15N/X8_DQ6
IO/LVDS2M_16P/X8_DQS6/CQ6
IO/LVDS2M_16N/X8_DQSN6/CQN6
IO/LVDS2M_17P/X8_DQ6
IO/LVDS2M_17N/X8_DQ6
IO/LVDS2M_18P/X8_DQ6
IO/LVDS2M_18N/X8_DQ6
IO/LVDS2M_19P/X8_DQ7
IO/LVDS2M_19N/X8_DQ7
IO/LVDS2M_20P/X8_DQ7
IO/LVDS2M_20N/X8_DQ7
IO/LVDS2M_21P/X8_DQ7
IO/LVDS2M_21N/X8_DQ7
IO/LVDS2M_22P/X8_DQS7/CQ7
IO/LVDS2M_22N/X8_DQSN7/CQN7
IO/LVDS2M_23P/X8_DQ7
IO/LVDS2M_23N/X8_DQ7
IO/LVDS2M_24P/X8_DQ7
IO/LVDS2M_24N/X8_DQ7
DDR4-A10
DDR4-A11
DDR4-A8
DDR4-A9
DDR4-A6
DDR4-A7
DDR4-A4
DDR4-A5
DDR4-A2
DDR4-A3
DDR4-A0
DDR4-A1
DDR4-PAR
DDR4-CLK_P
DDR4-CLK_N
DDR4-CKE
DDR4-ODT
DDR4-CS
DDR4-ACT
DDR4-BG1
DDR4-RESET
DDR4-BA1
DDR4-BG0
DDR4-A17
DDR4-BA0
DDR4-A15
DDR4-A16
DDR4-A13
DDR4-A14
S10_RZQ_2M
DDR4-A12
DDR4-IP_CLK_P
DDR4-IP_CLK_N
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Title: TEI1000 - 2M
A4
Number: TEI1000 AGI11-A
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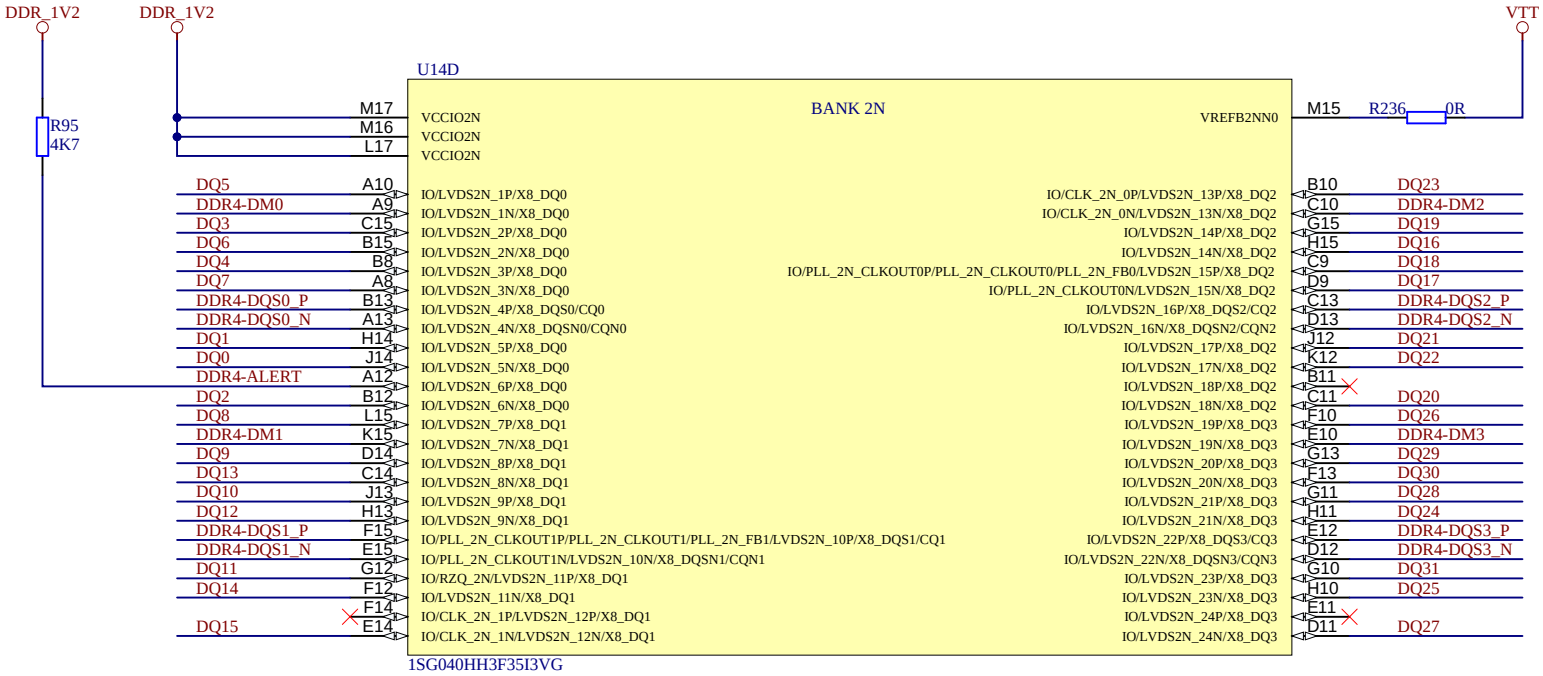
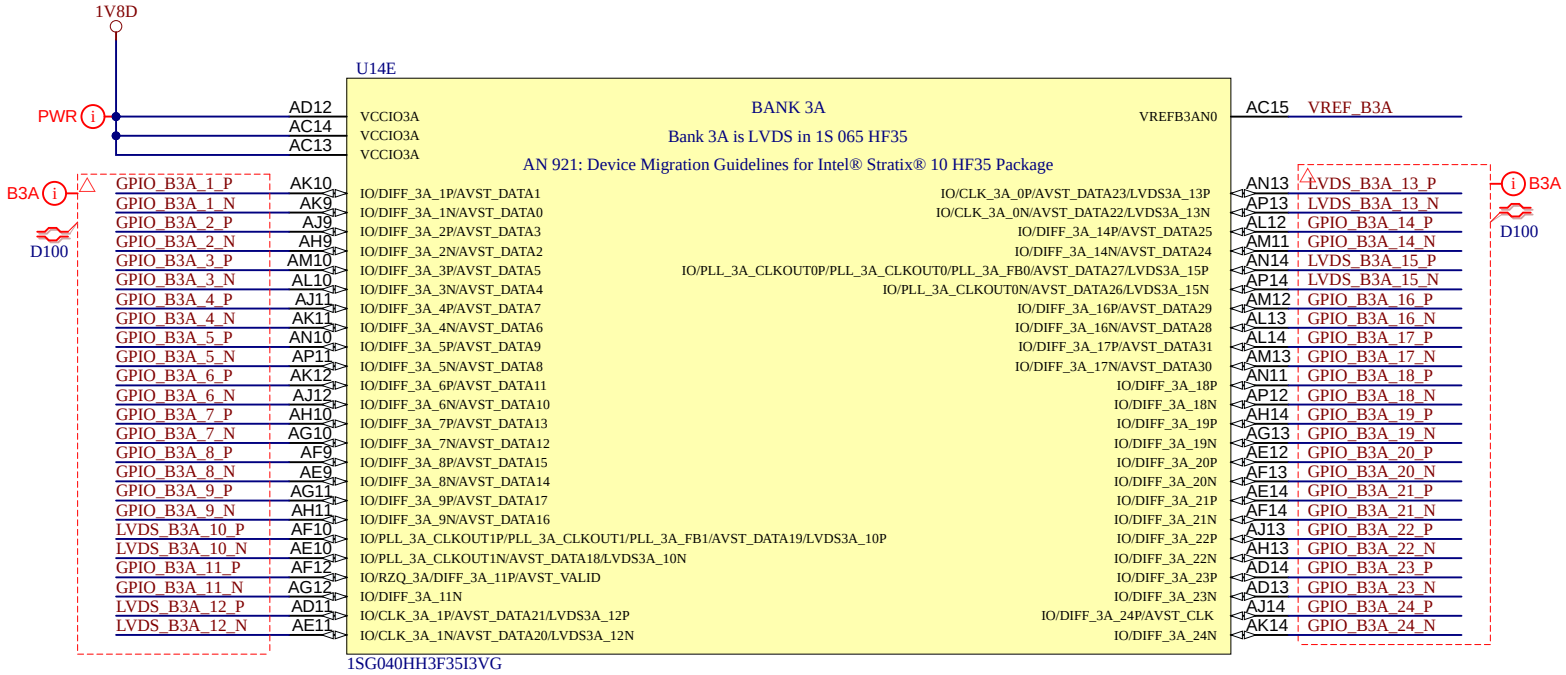
Filename: Bank_2M.SchDoc



Title: TEI1000 - B2N			
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page 23 of 43
Filename: Bank_2N.SchDoc			



When I/O bank 3A is used for AVST x16 or AVST x32 configuration mode, you must connect the VCCIO3A power supply to the VCCIO_SDM power supply for proper device functionality.
(Intel® Stratix® 10 Device Family Pin Connection Guidelines, p. 20)

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Title: TEI1000 - B3A		
A4	Number: TEI1000 AGI11-A	Rev. 02
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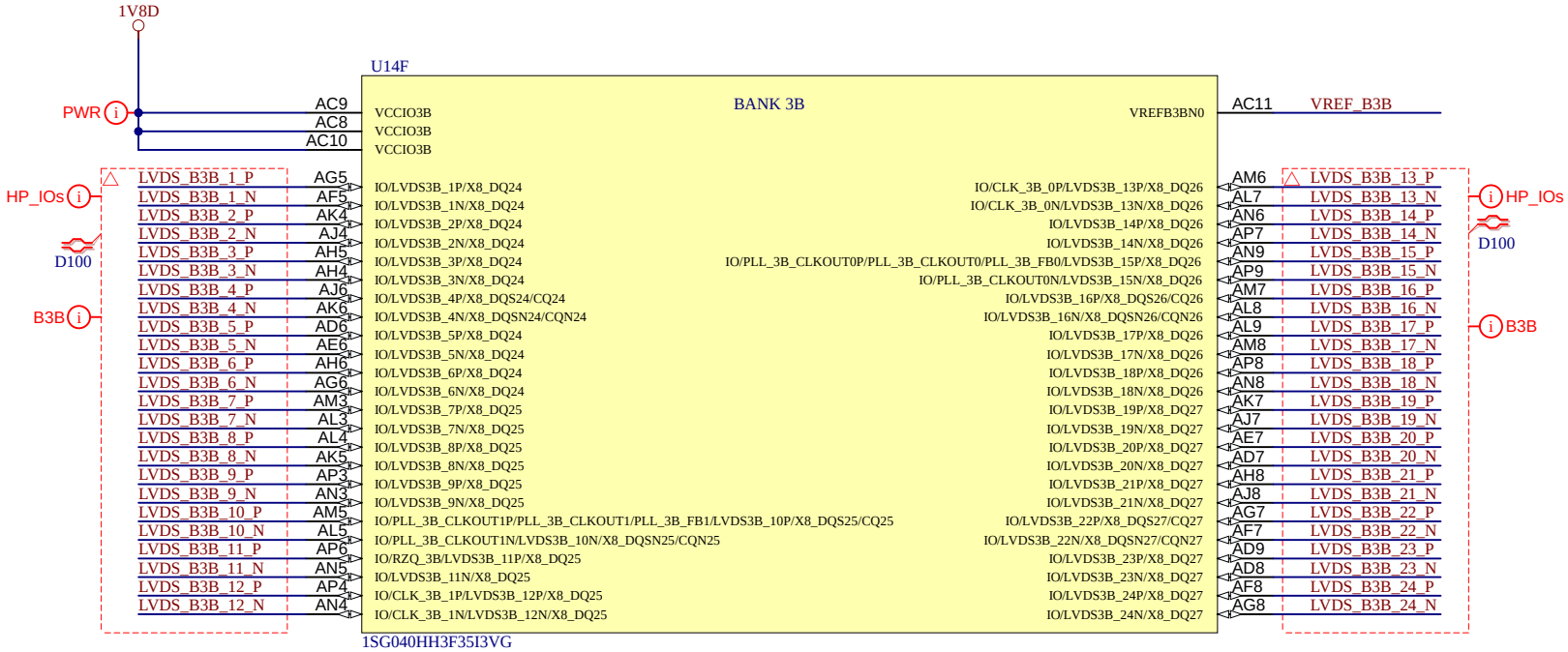
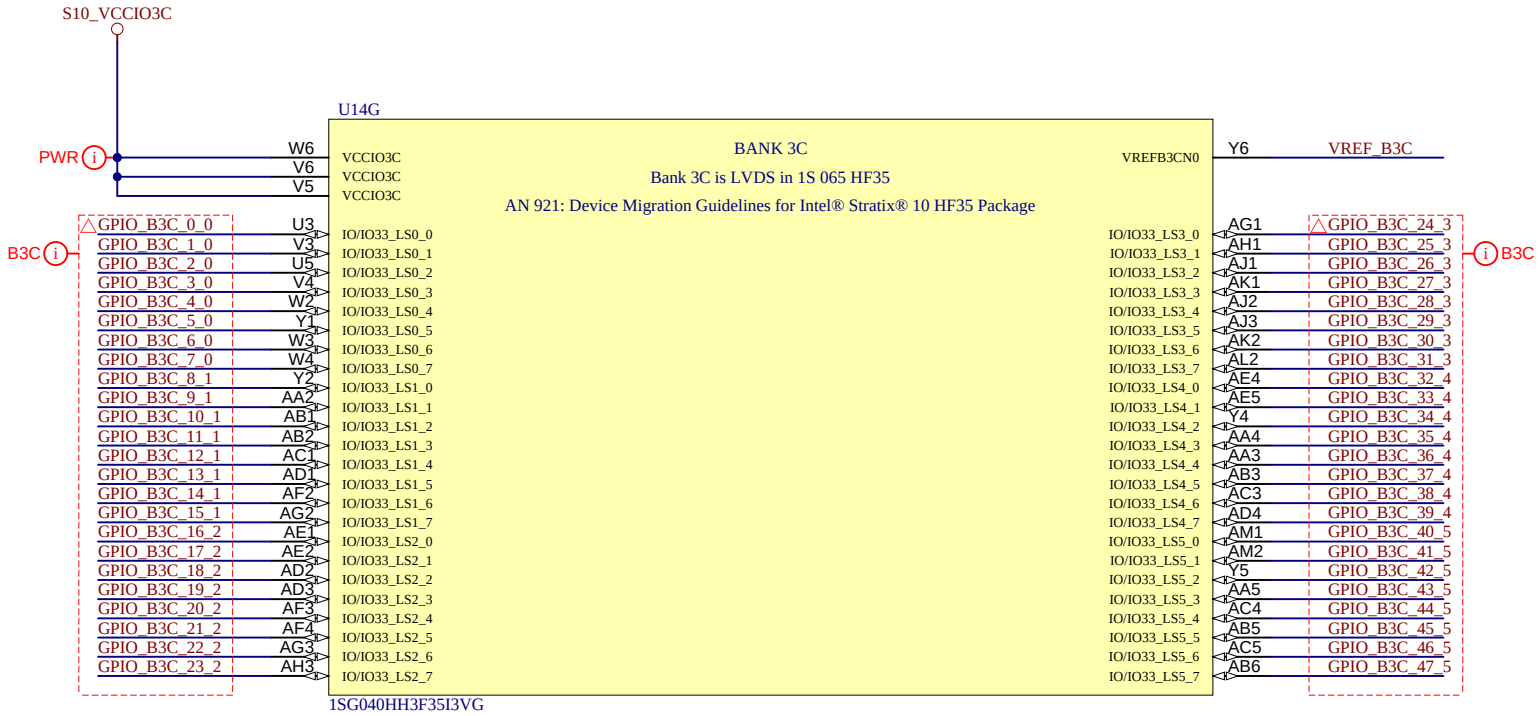
Filename: Bank_3A.SchDoc		



trenz electronic	Title: TEI1000 - B3B		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page25 of 43
Filename: Bank_3B.SchDoc			



48x high voltage I/Os

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Title: TEI1000 - B3C		
A4	Number: TEI1000 AGI11-A	Rev. 02
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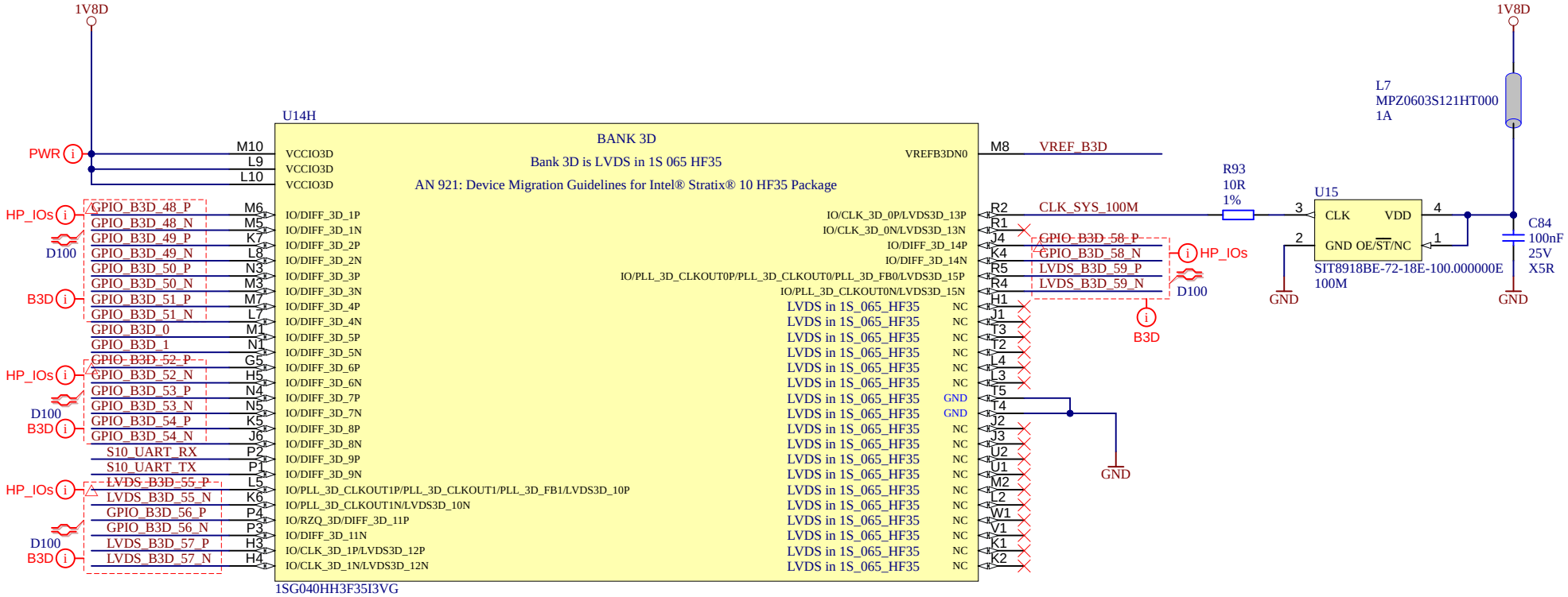
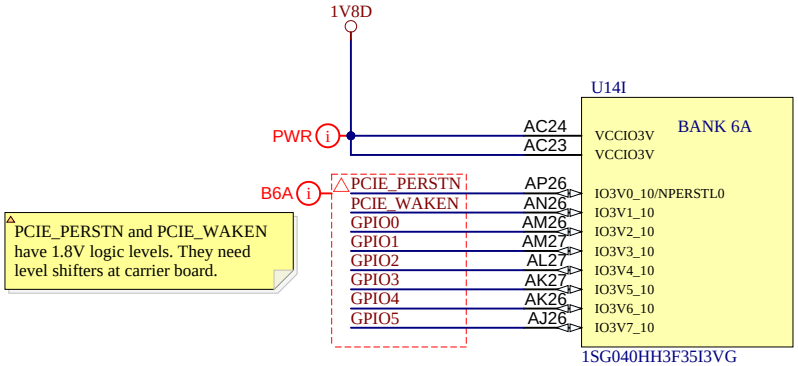
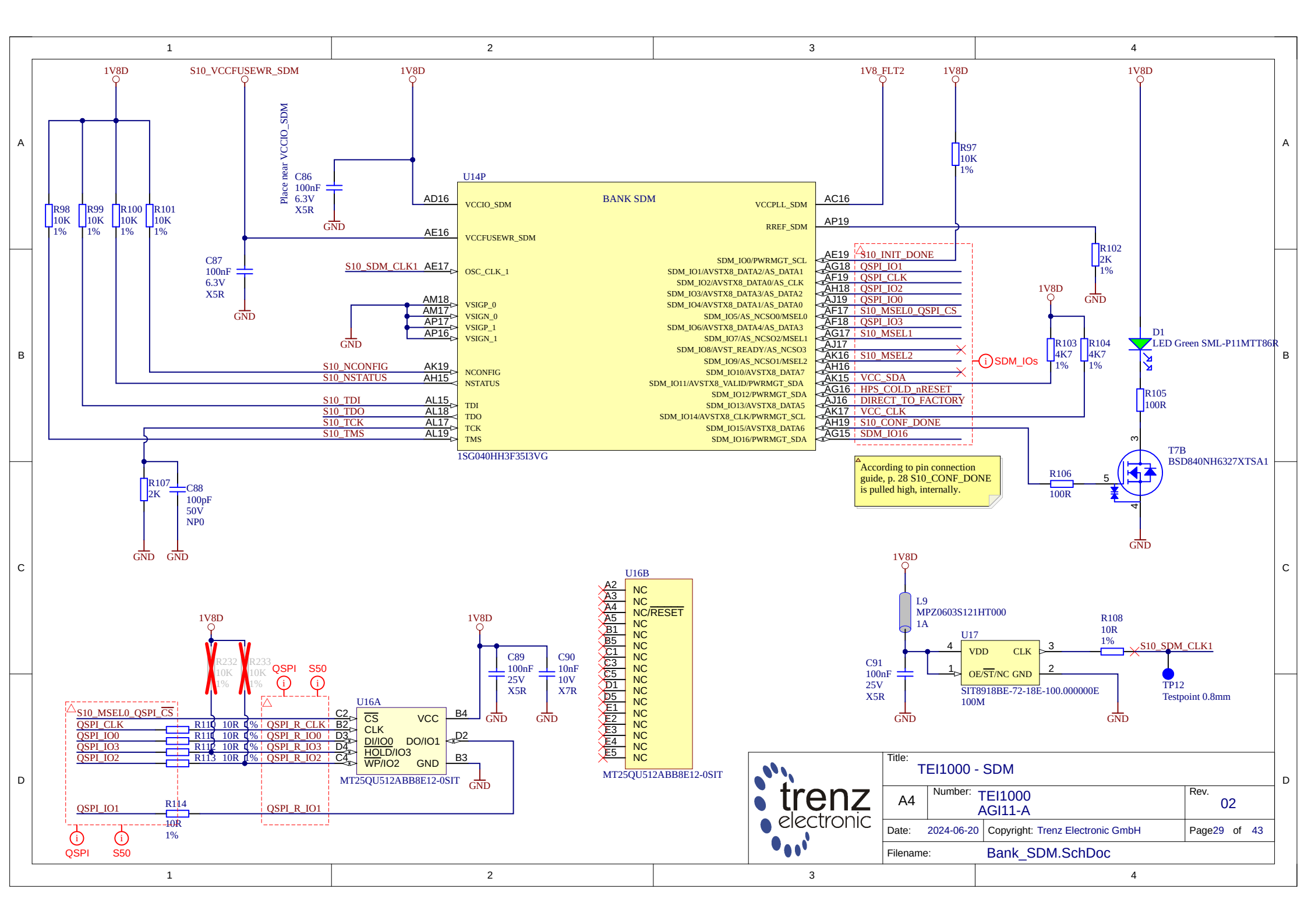
Filename: Bank_3C.SchDoc		



trenz electronic	Title: TEI1000 - B3D		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page27 of 43
Filename: Bank_3D.SchDoc			



trenz electronic	Title: TEI1000 - B6A		
	A4	Number: TEI1000 AGI11-A	Rev. 02
	Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page28 of 43
	Filename: Bank_6A.SchDoc		


1V8D
S10_VCCFUSEWR_SDM
1V8D
1V8_FLT2
1V8D
1V8D
Place near VCCIO_SDM
C86
100nF
6.3V
X5R
GND
U14P
BANK SDM
AD16
VCCIO_SDM
AC16
VCCPLL_SDM
R97
10K
1%
AP19
RREF_SDM
AE16
VCCFUSEWR_SDM
R98
10K
1%
R99
10K
1%
R100
10K
1%
R101
10K
1%
C87
100nF
6.3V
X5R
S10_SDM_CLK1
AE17
OSC_CLK_1
AM18
AM17
AP17
AP16
VSIGP_0
VSIGN_0
VSIGP_1
VSIGN_1
GND
R102
2K
1%
1V8D
R103
4K7
1%
R104
4K7
1%
D1
LED Green SML-P11MTT86R
R105
100R
S10_NCONFIG
S10_NSTATUS
AK19
AH15
NCONFIG
NSTATUS
S10_TDI
S10_TDO
S10_TCK
S10_TMS
AL15
AL18
AL17
AL19
TDI
TDO
TCK
TMS
SDM_IO0/PWRMGT_SCL
SDM_IO1/AVSTX8_DATA2/AS_DATA1
SDM_IO2/AVSTX8_DATA0/AS_CLK
SDM_IO3/AVSTX8_DATA3/AS_DATA2
SDM_IO4/AVSTX8_DATA1/AS_DATA0
SDM_IO5/AS_NCSO0/MSEL0
SDM_IO6/AVSTX8_DATA4/AS_DATA3
SDM_IO7/AS_NCSO2/MSEL1
SDM_IO8/AVST_READY/AS_NCSO3
SDM_IO9/AS_NCSO1/MSEL2
SDM_IO10/AVSTX8_DATA7
SDM_IO11/AVSTX8_VALID/PWRMGT_SDA
SDM_IO12/PWRMGT_SDA
SDM_IO13/AVSTX8_DATA5
SDM_IO14/AVSTX8_CLK/PWRMGT_SCL
SDM_IO15/AVSTX8_DATA6
SDM_IO16/PWRMGT_SDA
AE19 S10_INIT_DONE
AG18 QSPI_IO1
AF19 QSPI_CLK
AH18 QSPI_IO2
AJ19 QSPI_IO0
AF17 S10_MSEL0_QSPI_CS
AF18 QSPI_IO3
AG17 S10_MSEL1
AJ17
AK16 S10_MSEL2
AH16
AK15 VCC_SDA
AG16 HPS_COLD_nRESET
AJ16 DIRECT_TO_FACTORY
AK17 VCC_CLK
AH19 S10_CONF_DONE
AG15 SDM_IO16
SDM_IOs
1SG040HH3F35I3VG
According to pin connection guide, p. 28 S10_CONF_DONE is pulled high, internally.
R106
100R
T7B
BSD840NH6327XTSA1
R107
2K
C88
100pF
50V
NP0
GND
GND
U16B
NC
NC/RESET
MT25QU512ABB8E12-0SIT
1V8D
L9
MPZ0603S121HT000
1A
U17
VDD
CLK
OE/ST/NC
GND
SIT8918BE-72-18E-100.000000E
100M
R108
10R
1%
S10_SDM_CLK1
TP12
Testpoint 0.8mm
C91
100nF
25V
X5R
R232
10K
1%
R233
10K
1%
QSPI
S50
1V8D
C89
100nF
25V
X5R
C90
10nF
10V
X7R
U16A
CS
CLK
DI/IO0
HOLD/IO3
WP/IO2
VCC
DO/IO1
GND
MT25QU512ABB8E12-0SIT
S10_MSEL0_QSPI_CS
QSPI_CLK
QSPI_IO0
QSPI_IO3
QSPI_IO2
R110
R111
R112
R113
10R
1%
QSPI_R_CLK
QSPI_R_IO0
QSPI_R_IO3
QSPI_R_IO2
R114
10R
1%
QSPI_IO1
QSPI_R_IO1
QSPI
S50
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Title: TEI1000 - SDM
A4
Number: TEI1000 AGI11-A
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Filename: Bank_SDM.SchDoc


1V8D
U14N
M11
M12
VCCPT *
VCCPT *
BANK HPS
*** HPS only available for SX devices ***
Legend:
* HPS_VCCIO in SX device
** HPS_VCCL in SX device
*** HPS_VCCPLLDIG in SX device
**** HPS_VCCPLL in SX device
** VCC
** VCC
** VCC
** VCC
** VCC
*** VCC
**** VCCA_PLL
M13
L12
L13
L14
K14
J11
K11
VCC_CORE
1V8_FLT1
HPS_IOs
S50
EMAC0
HPS_IO1 C5
HPS_IO2 D4
HPS_IO3 C8
HPS_IO4 C4
HPS_IO5 D1
HPS_IO6 C1
HPS_IO7 D3
HPS_IO8 B3
HPS_IO9 C3
HPS_IO10 B2
HPS_IO11 B6
HPS_IO12 D6
HPS_IO13 A4
HPS_IO14 B5
HPS_IO15 D2
HPS_IO16 A5
HPS_IO17 D7
HPS_IO18 B7
HPS_IO19 G6
HPS_IO20 A3
HPS_IO21 C6
HPS_IO22 G2
HPS_IO23 A7
HPS_IO24 G8
NC
1SG040HH3F35I3VG
At SoCs with -V suffix:
According to A10 Datasheet, page 17, note (33): "VCCL_HPS and VCCPLLDIG_HPS may be connected to the PMBus voltage regulator" -> S10_VCC regulator
VCCPLL_HPS: 0.71V - 1.89V -> S10_VCCIO regulator
VCCIO_HPS: 1.71 - 1.89V
S50
HPS_IOs
U14O
BANK HPS
*** HPS only available for SX devices ***
EMAC1
EMAC2
HPS_IO25 F5
HPS_IO26 G7
HPS_IO27 E4
HPS_IO28 F3
HPS_IO29 G1
HPS_IO30 F9
HPS_IO31 H6
HPS_IO32 E1
HPS_IO33 F8
HPS_IO34 E7
HPS_IO35 F4
HPS_IO36 H9
HPS_IO37 D8
HPS_IO38 F2
HPS_IO39 J9
HPS_IO40 E2
HPS_IO41 F7
HPS_IO42 E5
HPS_IO43 J7
HPS_IO44 E6
HPS_IO45 G3
HPS_IO46 K9
HPS_IO47 E9
HPS_IO48 K10
NC
1SG040HH3F35I3VG
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Title: TEI1000 - HPS
A4
Number: TEI1000 AGI11-A
Rev. 02
Date: 2024-06-20
Copyright: Trenz Electronic GmbH
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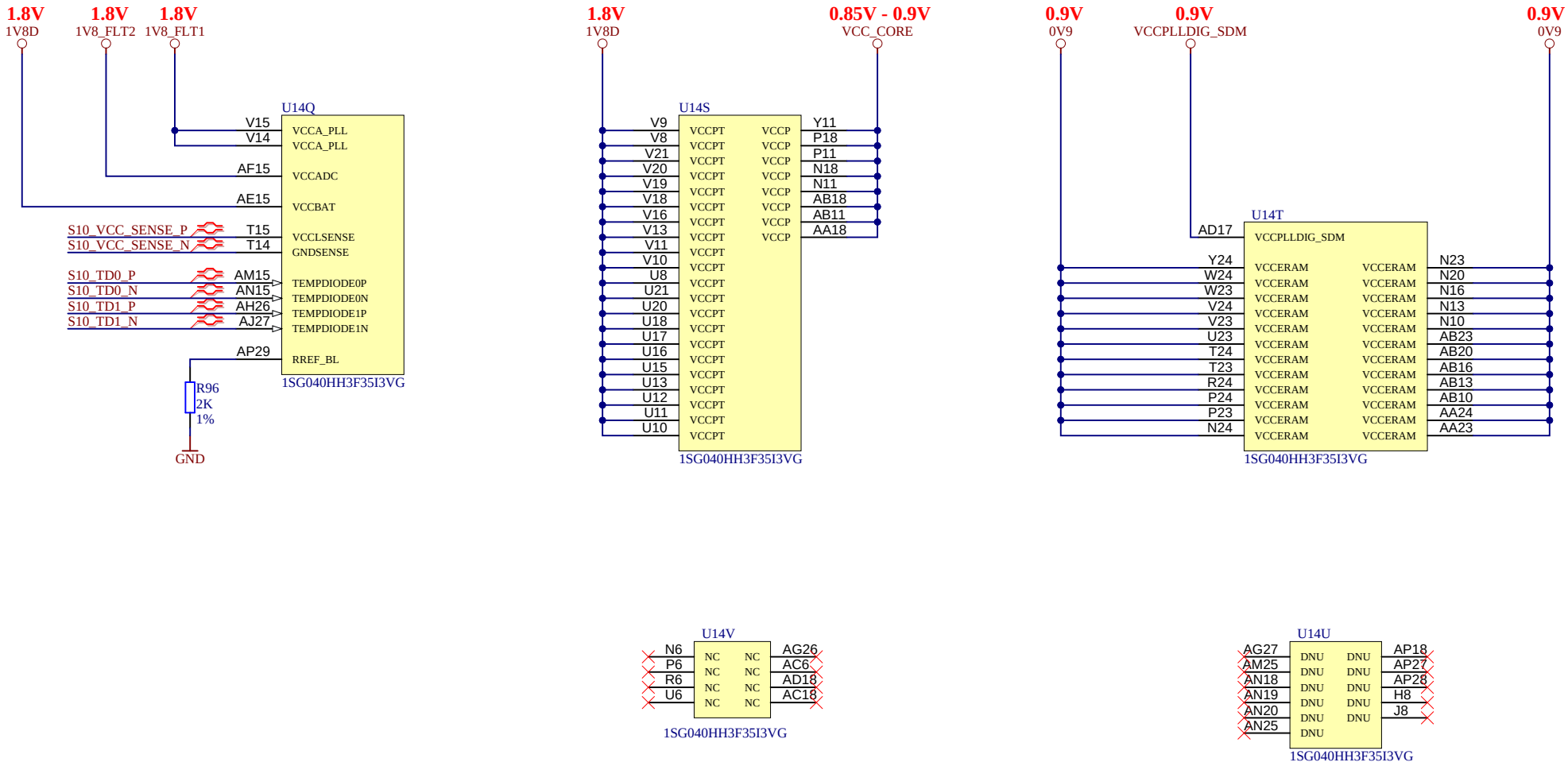
Filename: Bank_HPS.SchDoc



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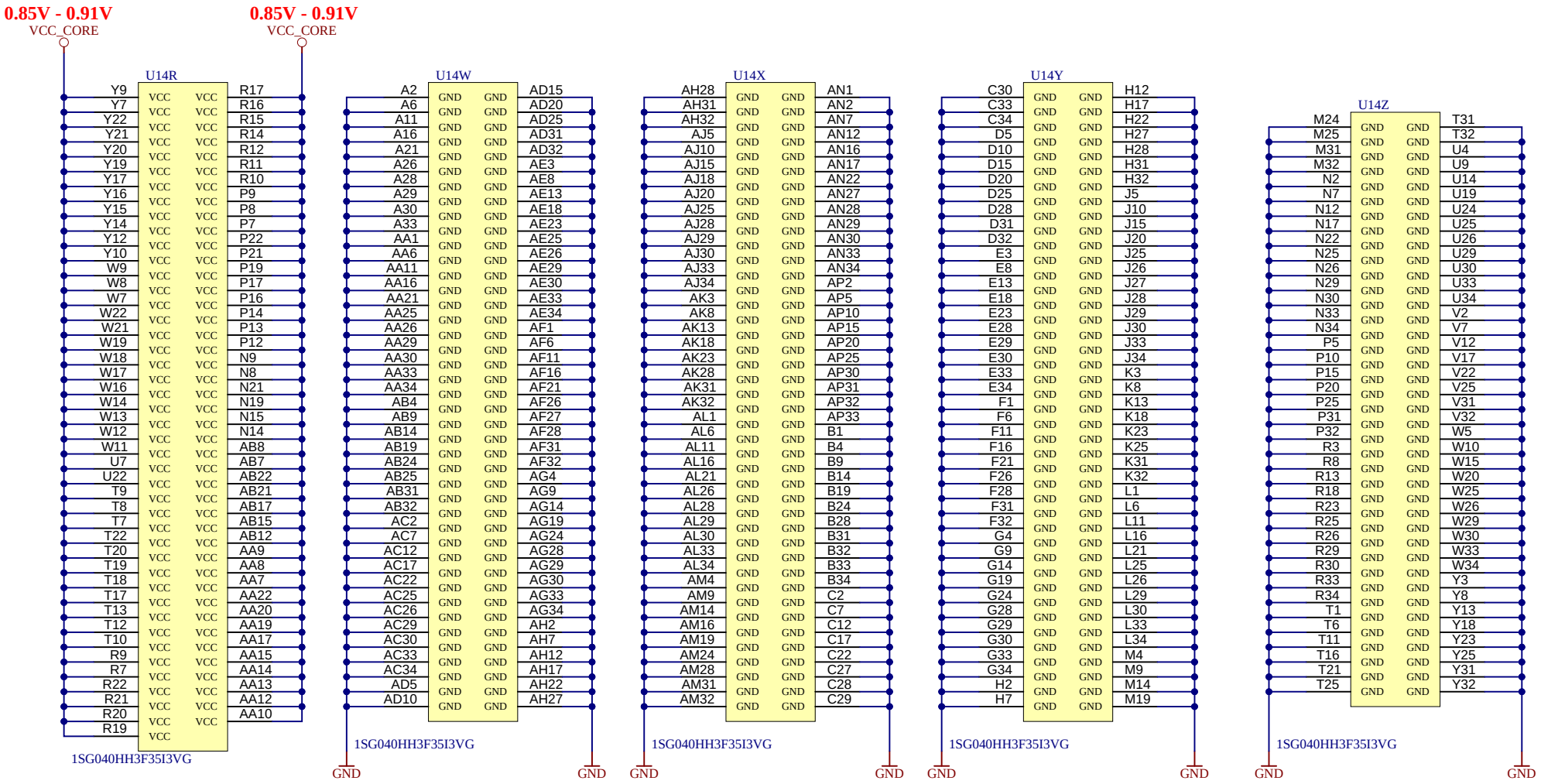
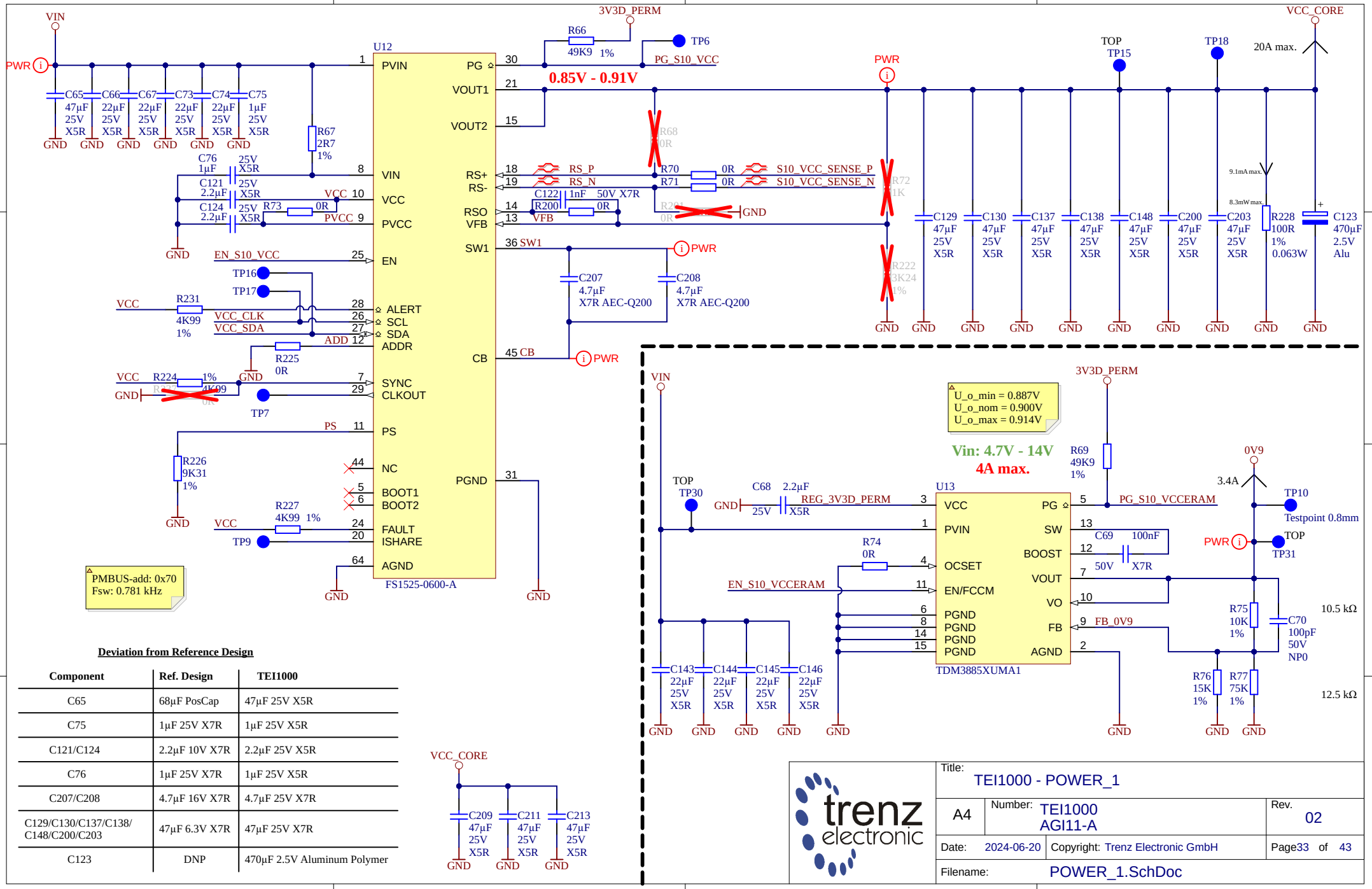
Title: TEI1000 - FPGA_POWER_1		
A4	Number: TEI1000 AGI11-A	Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page31 of 43
Filename: FPGA_POWER_1.SchDoc		



Title: TEI1000 - FPGA_POWER_2			
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page32 of 43
Filename: FPGA_POWER_2.SchDoc			



Deviation from Reference Design

Component	Ref. Design	TEI1000
C65	68µF PosCap	47µF 25V X5R
C75	1µF 25V X7R	1µF 25V X5R
C121/C124	2.2µF 10V X7R	2.2µF 25V X5R
C76	1µF 25V X7R	1µF 25V X5R
C207/C208	4.7µF 16V X7R	4.7µF 25V X7R
C129/C130/C137/C138/ C148/C200/C203	47µF 6.3V X7R	47µF 25V X7R
C123	DNP	470µF 2.5V Aluminum Polymer

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Title: TEI1000 - POWER_1		
A4	Number: TEI1000 AGI11-A	Rev. 02
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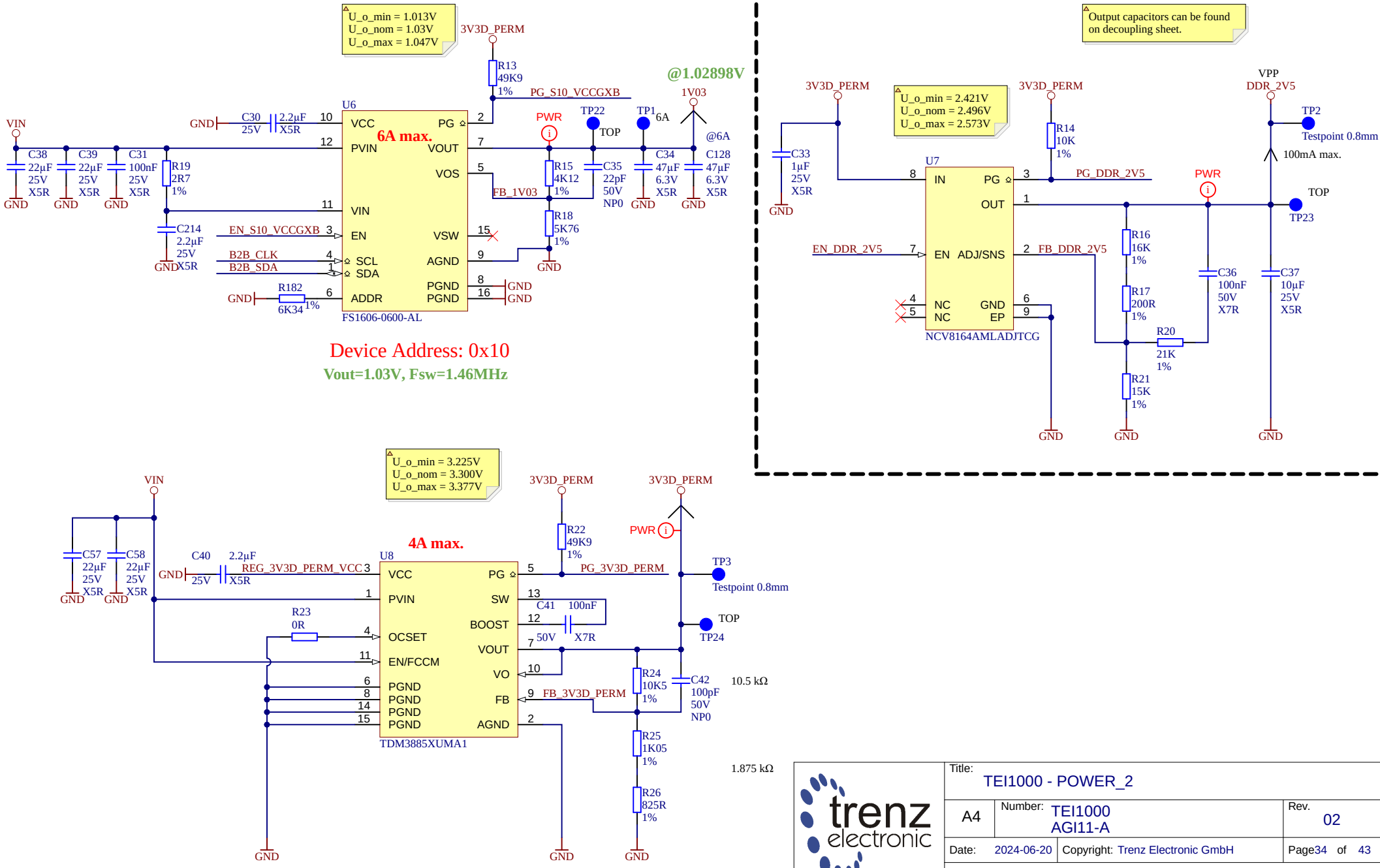
Filename: POWER_1.SchDoc		


U_o_min = 1.013V
U_o_nom = 1.03V
U_o_max = 1.047V
3V3D_PERM
@1.02898V
U6
6A max.
FS1606-0600-AL
VIN
GND
PWR
TOP
1V03
@6A
PG_S10_VCCGXB
FB_1V03
EN_S10_VCCGXB
B2B_CLK
B2B_SDA
Device Address: 0x10
Vout=1.03V, Fsw=1.46MHz
Output capacitors can be found on decoupling sheet.
U_o_min = 2.421V
U_o_nom = 2.496V
U_o_max = 2.573V
U7
NCV8164AMLADJTCG
VPP
DDR_2V5
PG_DDR_2V5
EN_DDR_2V5
FB_DDR_2V5
Testpoint 0.8mm
100mA max.
U_o_min = 3.225V
U_o_nom = 3.300V
U_o_max = 3.377V
4A max.
U8
TDM3885XUMA1
REG_3V3D_PERM_VCC
PG_3V3D_PERM
FB_3V3D_PERM
10.5 kΩ
1.875 kΩ
Title: TEI1000 - POWER_2
A4
Number: TEI1000 AGI11-A
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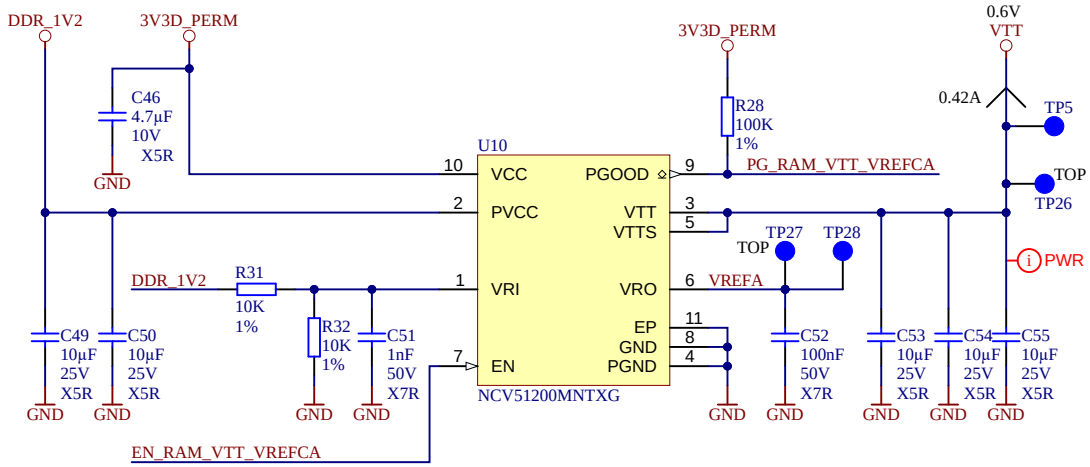
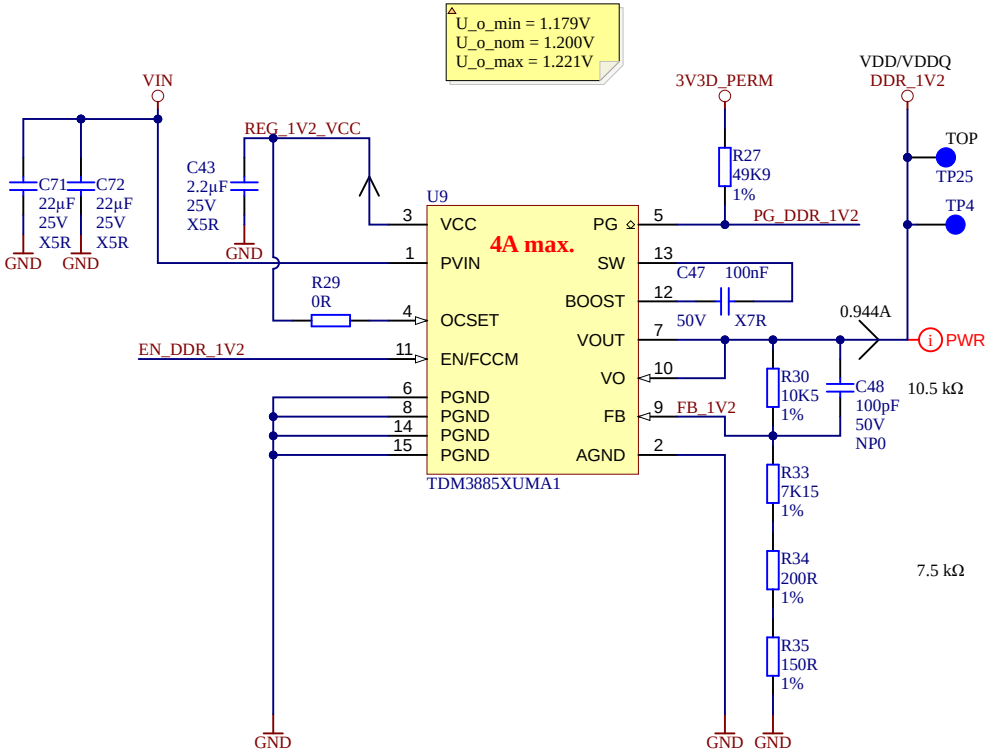
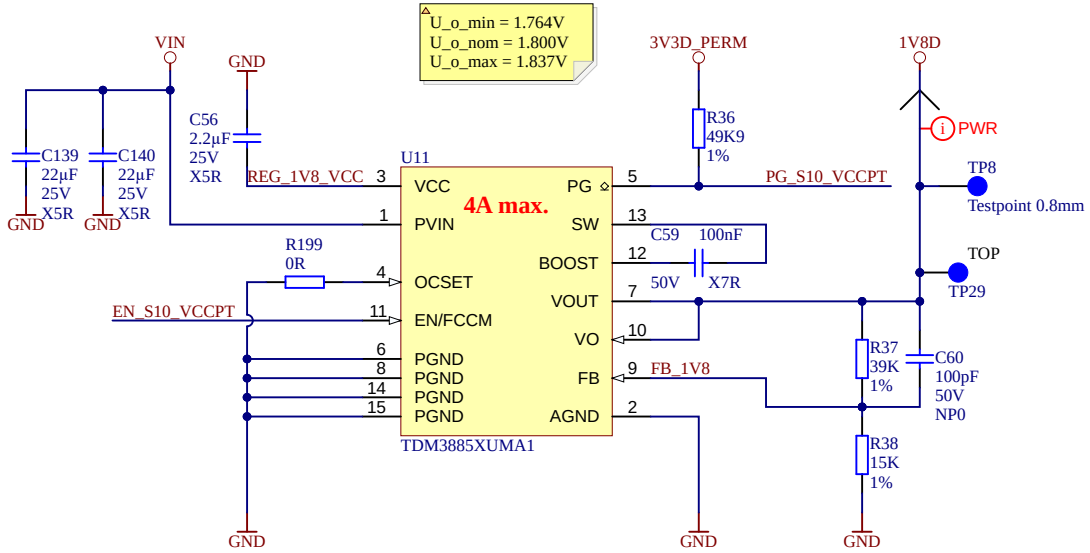
Filename: POWER_2.SchDoc







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Title: TEI1000 - POWER_3			
A4	Number: TEI1000 AGI11-A		Rev. 02
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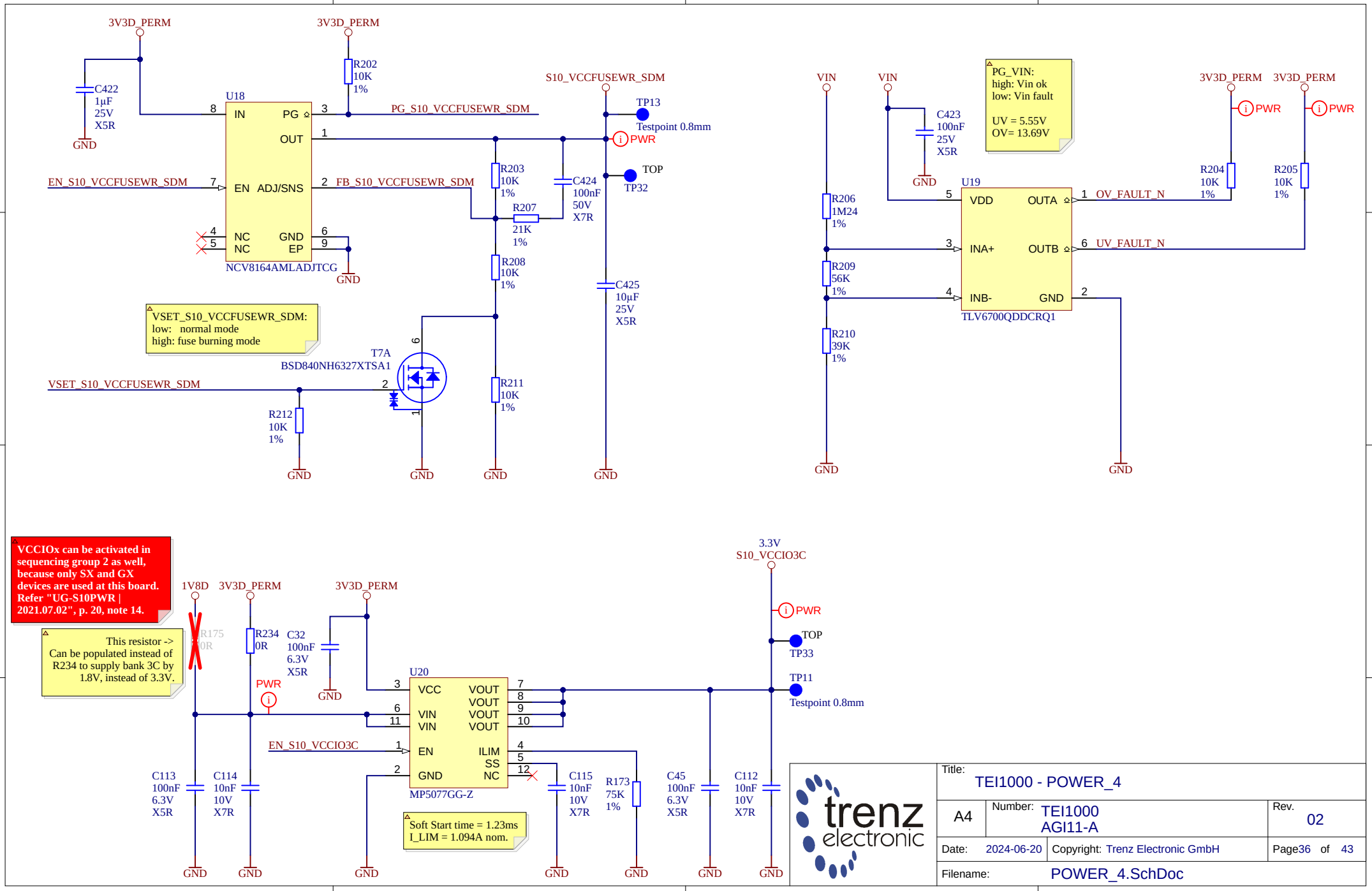
3V3D_PERM
C422
1µF
25V
X5R
GND
U18
IN
PG
OUT
NC
NC
GND
EP
NCV8164AMLADJTCG
R202
10K
1%
PG_S10_VCCFUSEWR_SDM
EN_S10_VCCFUSEWR_SDM
EN
ADJ/SNS
FB_S10_VCCFUSEWR_SDM
S10_VCCFUSEWR_SDM
TP13
Testpoint 0.8mm
PWR
TOP
TP32
R203
10K
1%
R207
21K
1%
C424
100nF
50V
X7R
C425
10µF
25V
X5R
R208
10K
1%
R211
10K
1%
VSET_S10_VCCFUSEWR_SDM:
low: normal mode
high: fuse burning mode
T7A
BSD840NH6327XTSA1
VSET_S10_VCCFUSEWR_SDM
R212
10K
1%
VIN
C423
100nF
25V
X5R
PG_VIN:
high: Vin ok
low: Vin fault
UV = 5.55V
OV= 13.69V
R206
1M24
1%
R209
56K
1%
R210
39K
1%
U19
VDD
OUTA
INA+
OUTB
INB-
GND
TLV6700QDDCRQ1
OV_FAULT_N
UV_FAULT_N
R204
10K
1%
R205
10K
1%
VCCIOx can be activated in sequencing group 2 as well, because only SX and GX devices are used at this board. Refer "UG-S10PWR | 2021.07.02", p. 20, note 14.
This resistor -> Can be populated instead of R234 to supply bank 3C by 1.8V, instead of 3.3V.
1V8D
R175
0R
R234
0R
C32
100nF
6.3V
X5R
3.3V
S10_VCCIO3C
TP33
TP11
Testpoint 0.8mm
U20
VCC
VIN
VIN
EN
GND
VOUT
VOUT
VOUT
VOUT
ILIM
SS
NC
MP5077GG-Z
EN_S10_VCCIO3C
C113
100nF
6.3V
X5R
C114
10nF
10V
X7R
C115
10nF
10V
X7R
R173
75K
1%
C45
100nF
6.3V
X5R
C112
10nF
10V
X7R
Soft Start time = 1.23ms
I_LIM = 1.094A nom.
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Title: TEI1000 - POWER_4
A4
Number: TEI1000 AGI11-A
Rev. 02
Date: 2024-06-20
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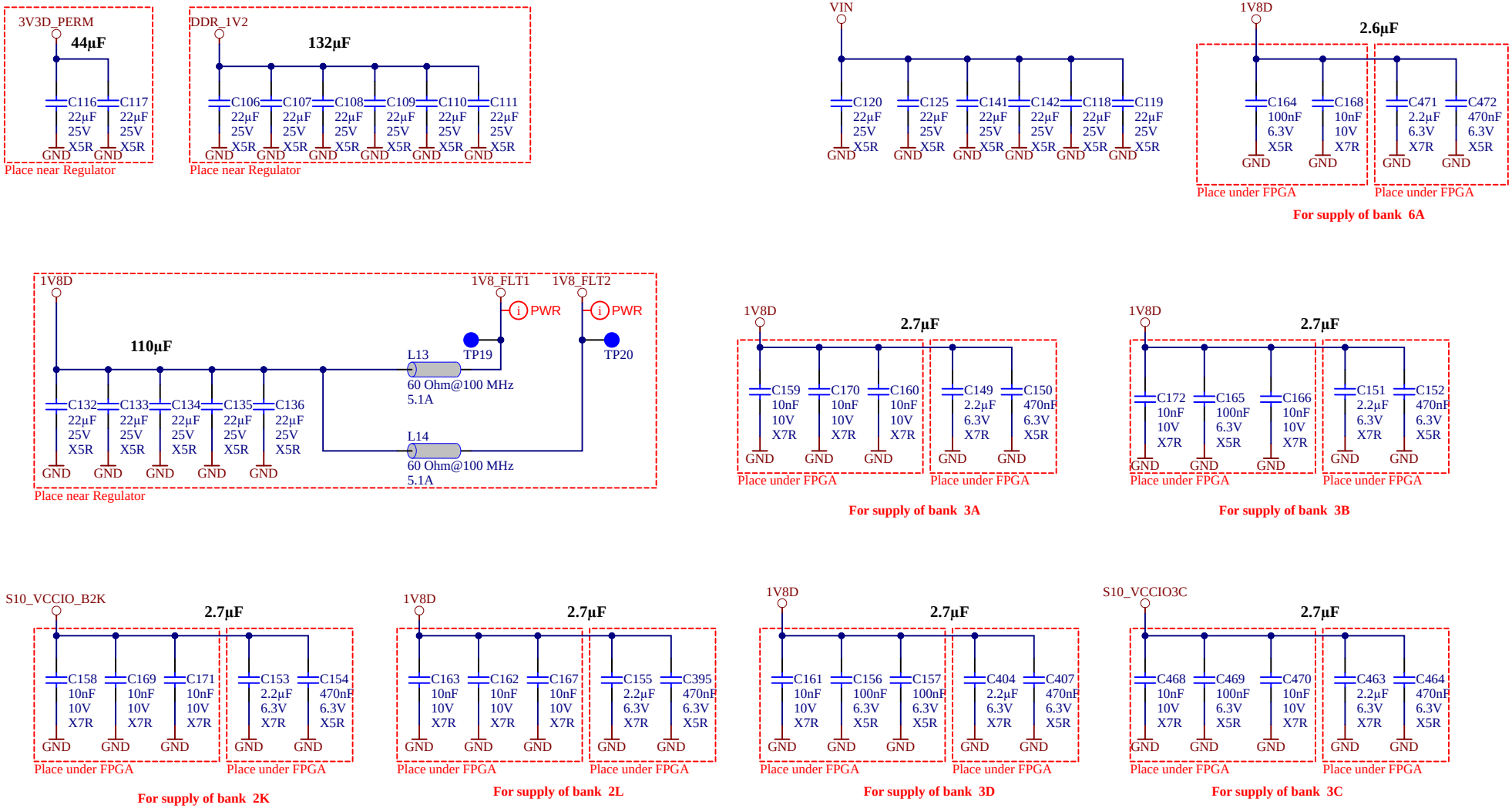
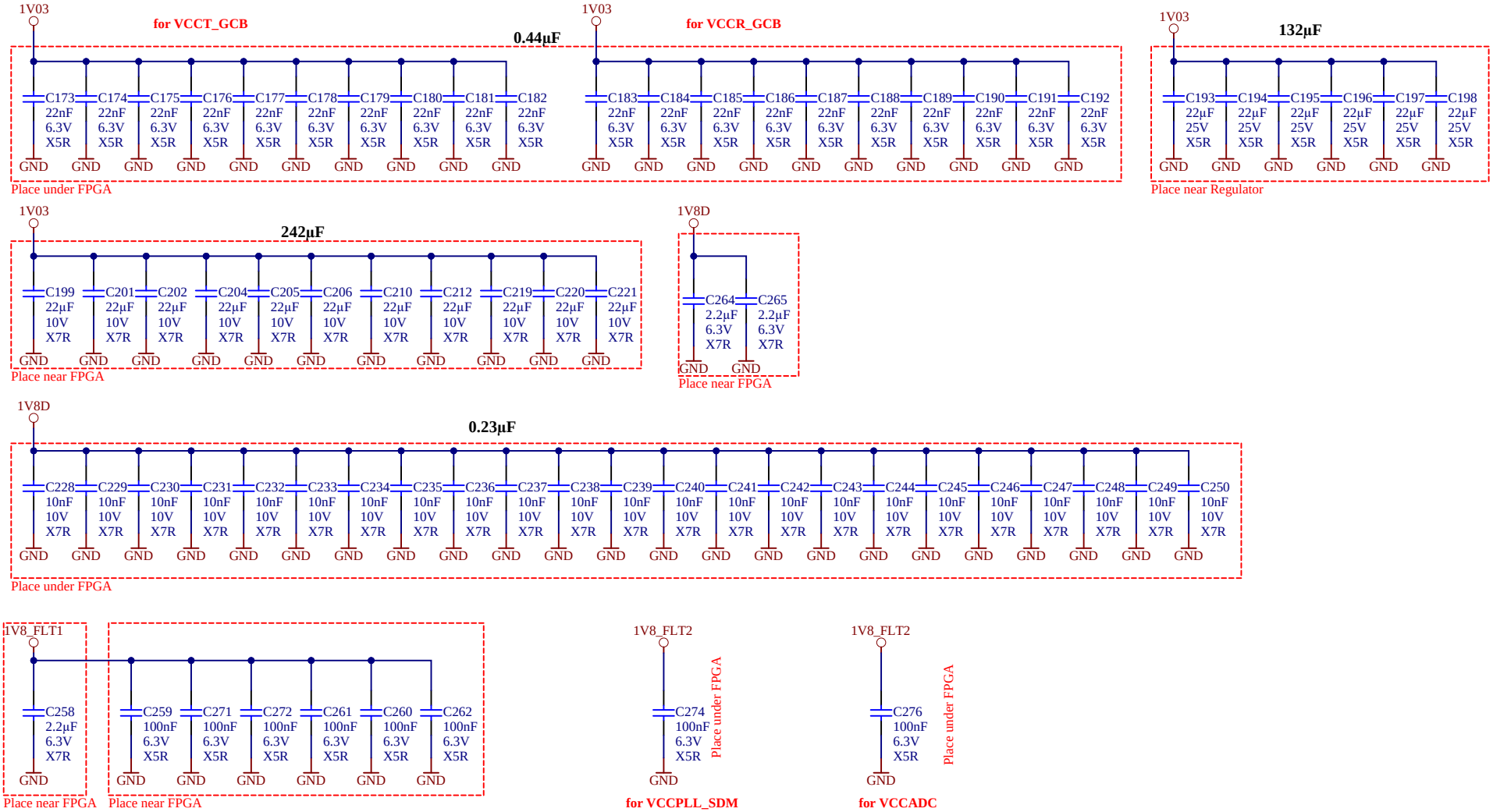
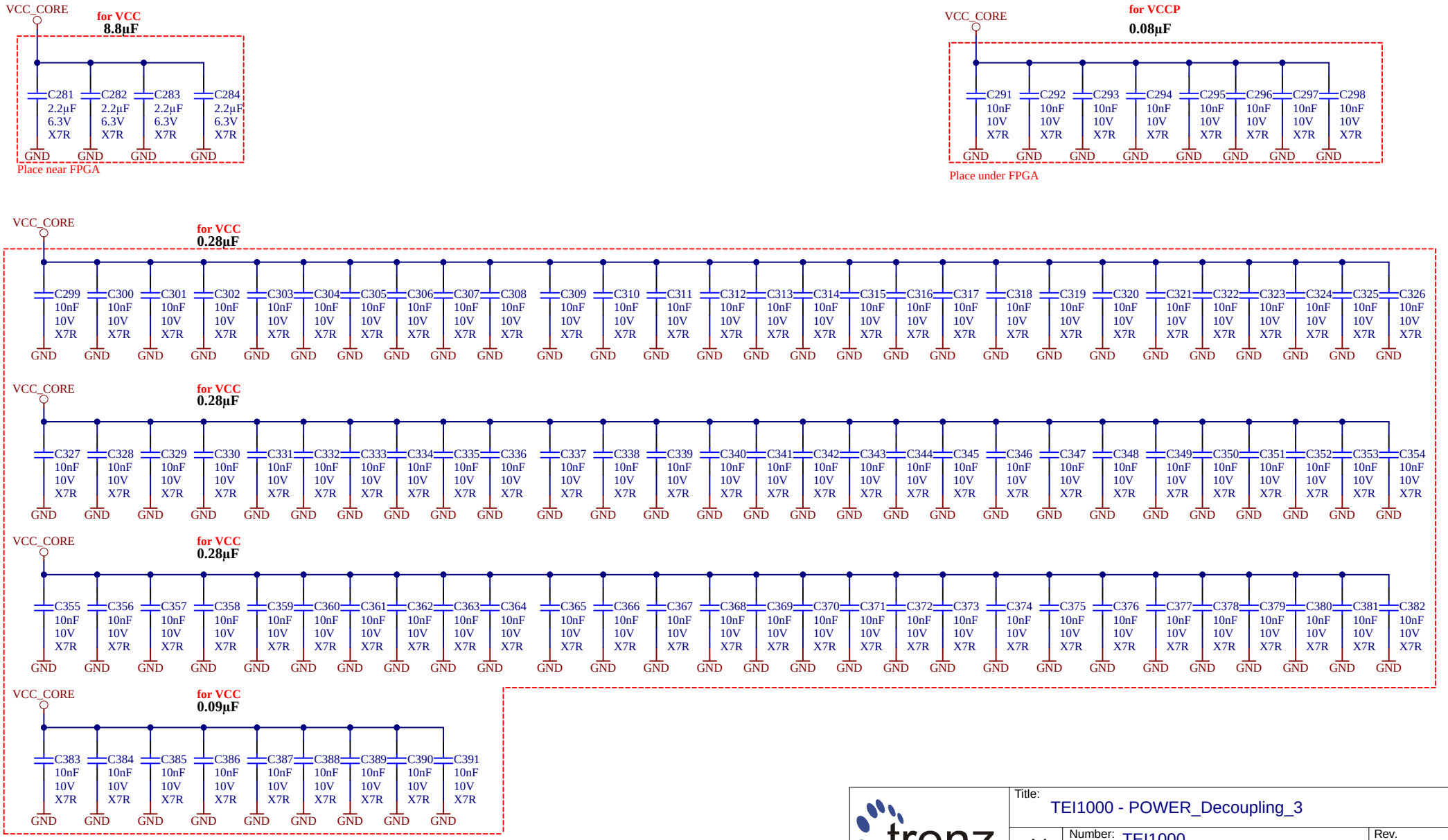
Filename: POWER_4.SchDoc



Title: TEI1000 - POWER_Decoupling_1			
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page37 of 43
Filename: POWER_Decoupling_1.SchDoc			



trenz electronic	Title: TEI1000 - POWER_Decoupling_2		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page38 of 43
Filename: POWER_Decoupling_2.SchDoc			



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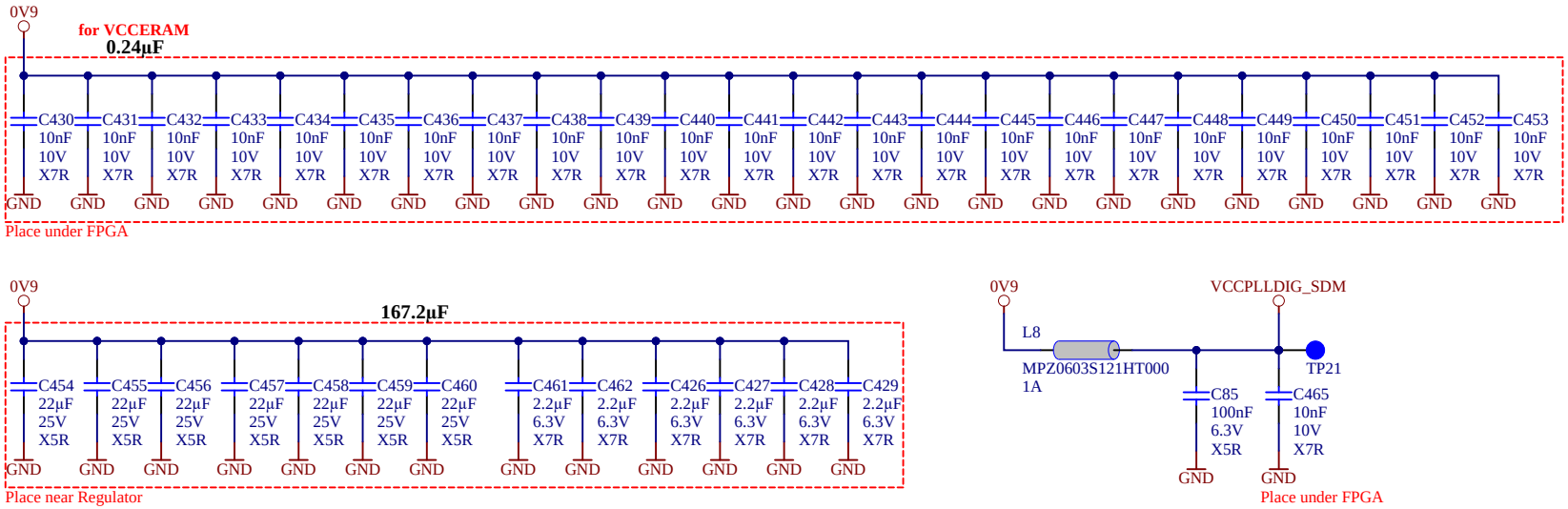
Title: TEI1000 - POWER_Decoupling_3		
A4	Number: TEI1000 AGI11-A	Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH	Page39 of 43
Filename: POWER_Decoupling_3.SchDoc		



trenz electronic	Title: TEI1000 - POWER_Decoupling_3		
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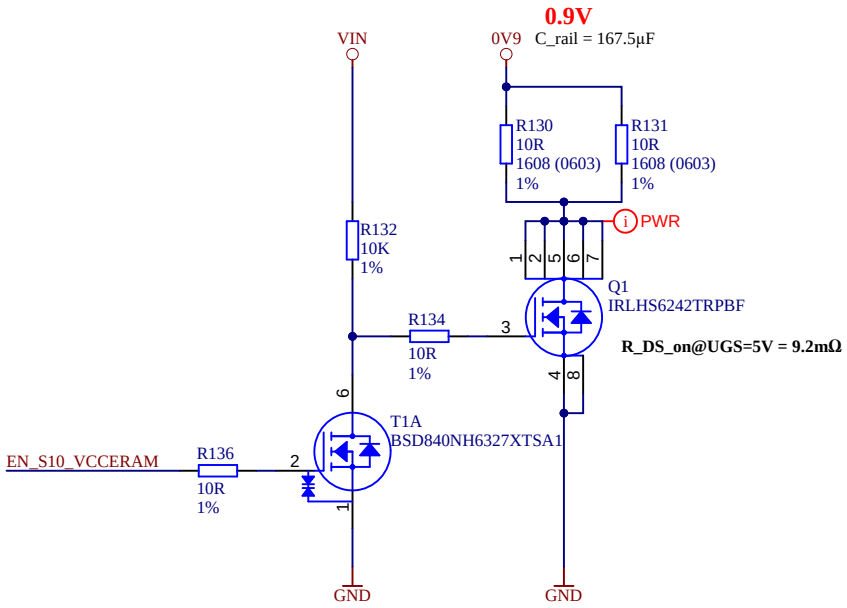
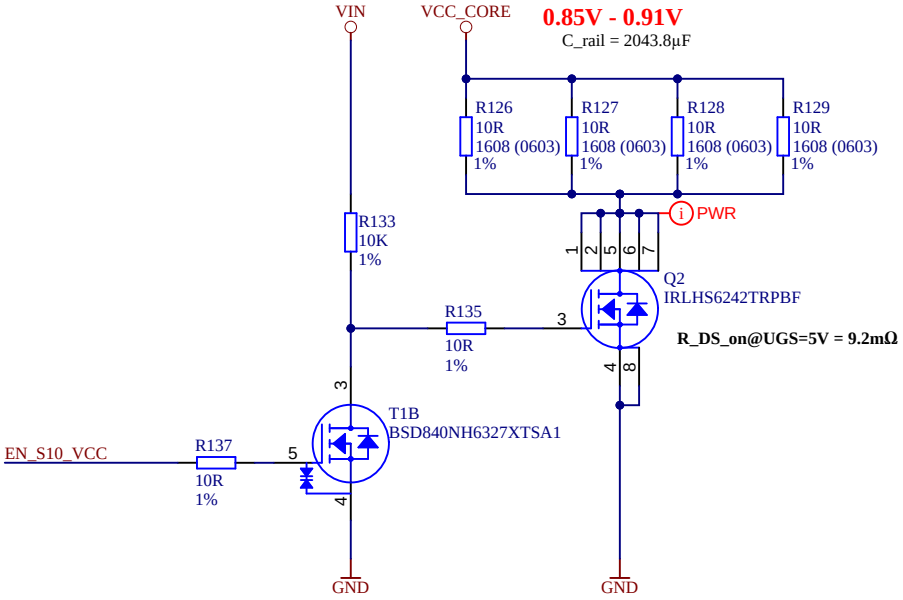
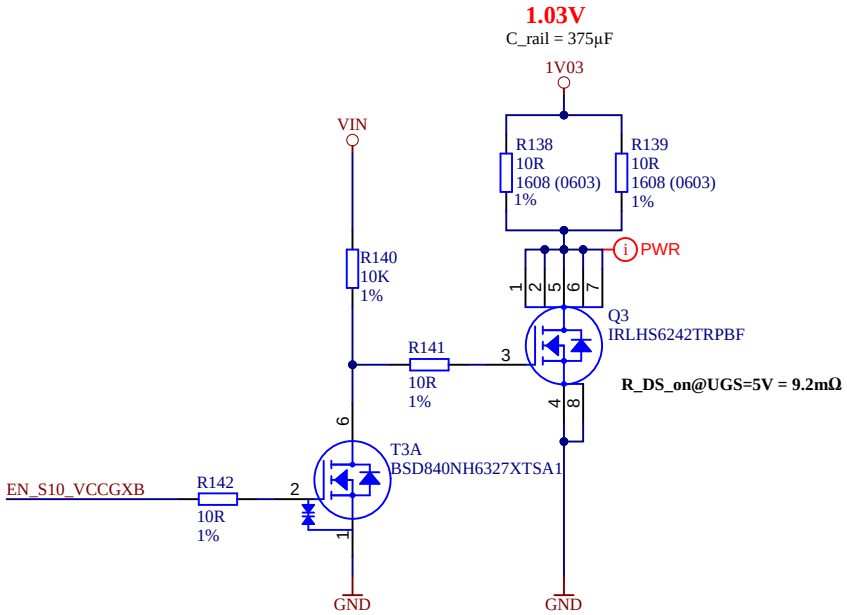
Filename: POWER_Decoupling_4.SchDoc			







Pull-downs of enable signals can be found on POWER_1 / POWER_2 sheet

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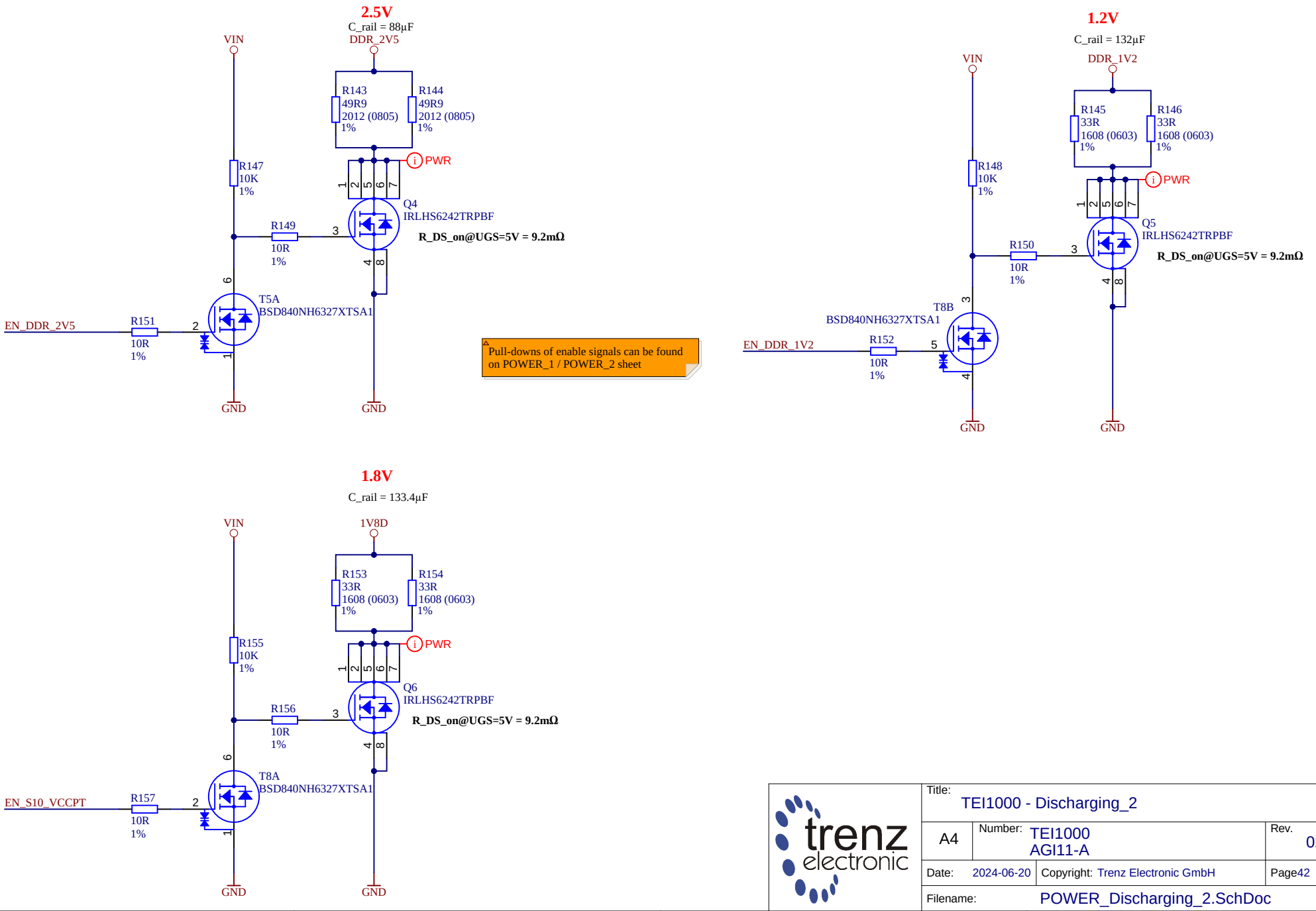
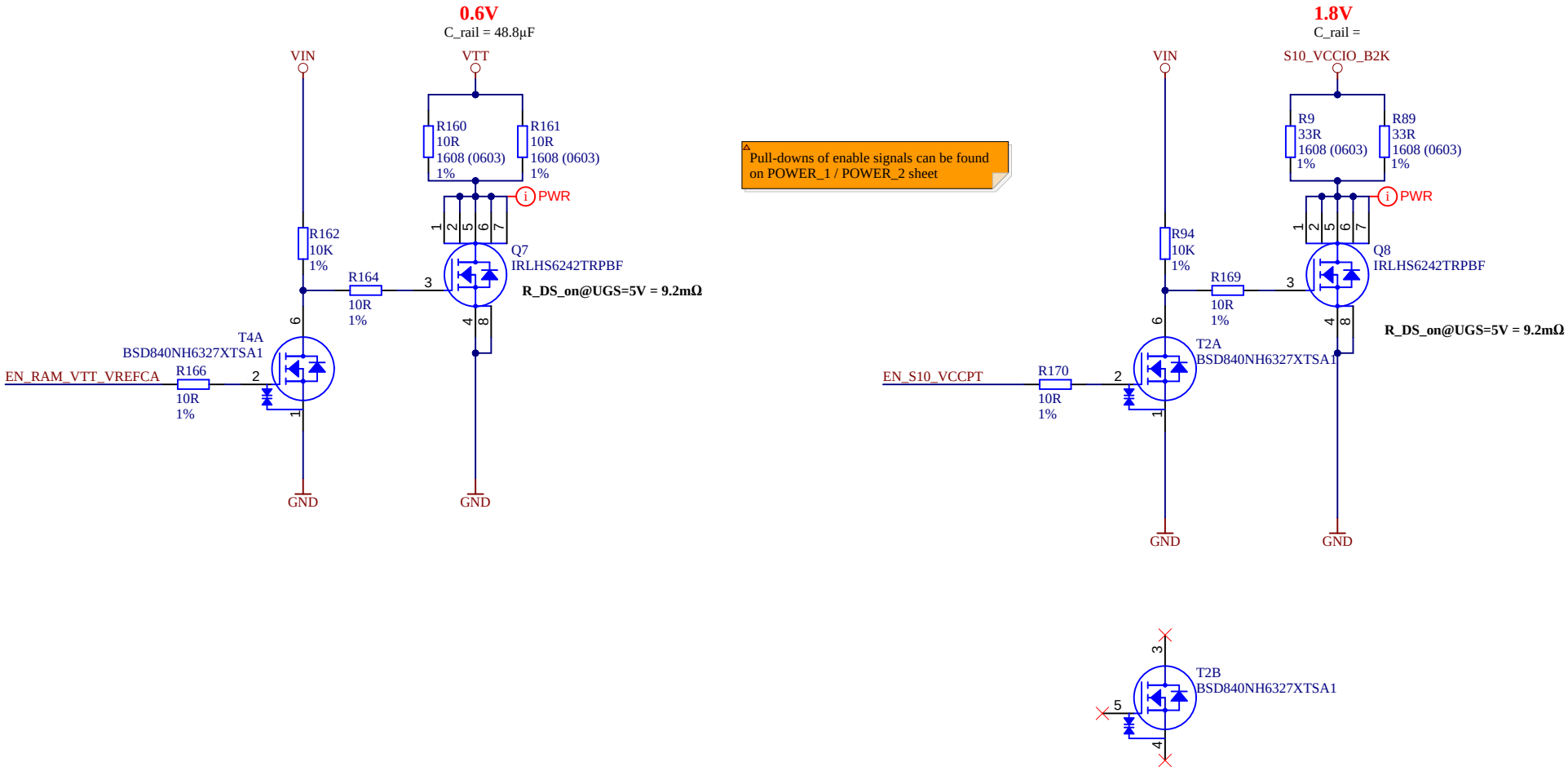


Title: TEI1000 - Discharging_2			
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page 42 of 43
Filename: POWER_Discharging_2.SchDoc			



trenz electronic	Title: TEI1000 - Discharging_3		
A4	Number: TEI1000 AGI11-A		Rev. 02
Date: 2024-06-20	Copyright: Trenz Electronic GmbH		Page43 of 43
Filename: POWER_Discharging_3.SchDoc			