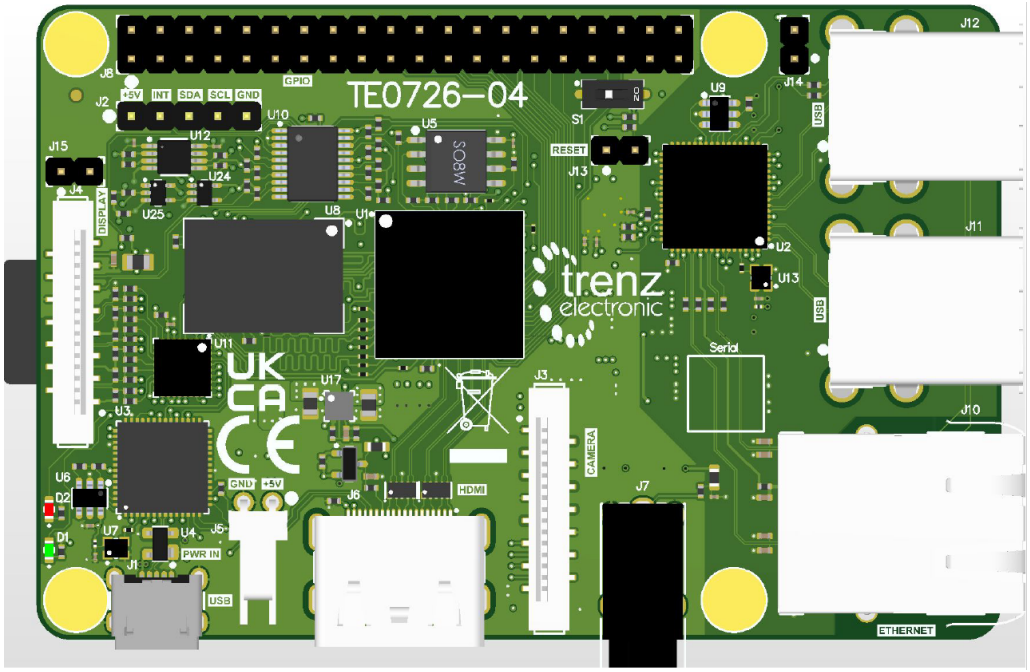

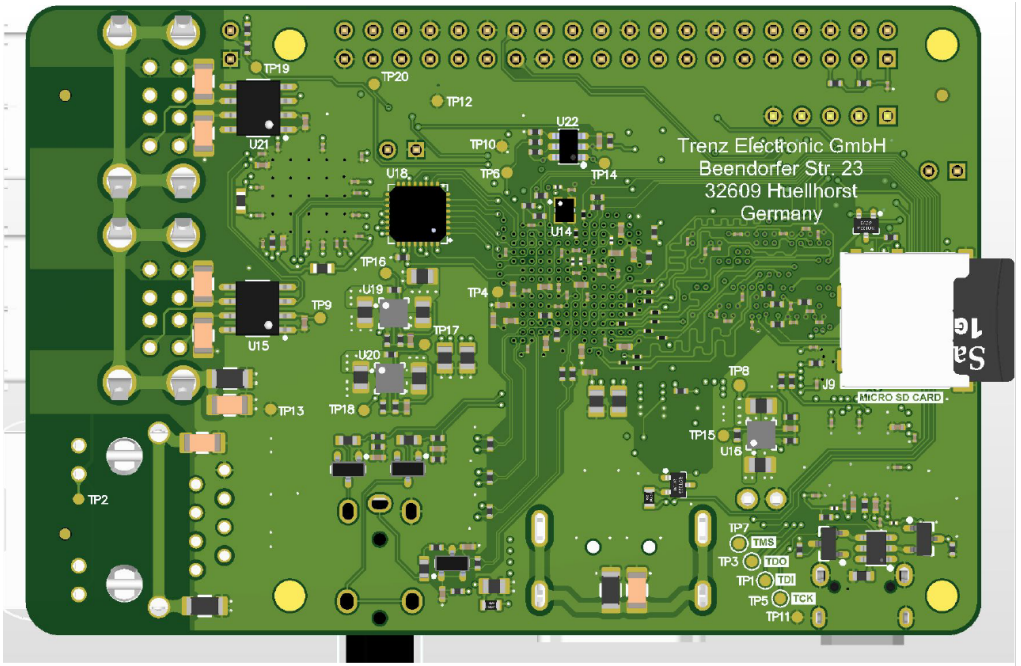

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: Legal Notices Modules	
A4	Number: TE0726 41C98-A	Rev. 04
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Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02	1. CSI CLK line moved to MRCC pin, CSI lanes swap -> DONE 2. CSI camera GPIO moved to MIO GPIO -> DONE 3. RPi GPIO 14,15 moved from MIO to PL -> DONE 4. add C for SD Card VCC (required by SD spec) 47uF ->DONE 5. add C for RPi camera - prevent voltage drop at camera init - 47uF ? or R + 47uf ->DONE 6. fix MODE pin strapping -> DONE 7. LED change 0603 (cheaper) -> DONE 8. add POWER connector 2 pin -> DONE (2pin 2.54mm) 9. change HDMI ESD to ESD+EMI -> DONE (replaced on EMI4192) 10. fix HDMI HPD and backpower? how? -> fix reset 11. DSI find solution for LS mode 12. fix XADC power caps -> DONE 13. change LPDRR2 ->> DDR3L -> DONE	
-03	1. make variants: a) default with DDR3L 128Mb; b) TE0726-03M with DDR3L 512Mb; c) TE0726-03L with DDR3L 128Mb, without usb's, eth_phy, connectors usb, RJ-45, CSI,DSI,HDMI, jack 3.5mm -> done 2. replace FTDI on 56pins package -> done 3. move LED's as raspberry pi 3 -> done 4. replace POWER connector on right angle connector -> done (not fitted) 5. make corect conection PUDC pin -> done 6. optimize BOM, replace on cheaper components -> done (replace HDMI, DSI/CSI connector, USB stacked connectors, RJ-45, power connector)	
-03a	1. VBUS Resistor R94 replaced by 10k ohm (was 12k1)	VY (08.04.2019)
-04	1. EOL components U16, U17 , U19, U20 (EN5311QI) were replaced by MPM3834CGPA; 2. Added MIC bias power L12, C114 , R151 (Page 16); 3. Added Legal notices (Page 1); 4. Added power diagram (Page 4); 5. Added S1 switch and R152 for "JTAG only mode" enable (Page 8); 6. The signals were renamed: - SPI-DQ0/M0 ---> SPI-DQ0/M3, - SPI-DQ3/M3 ---> SPI-DQ3/M0 according to AMD Table 6-4 (Page 8); 7. ECC function has been added for U8 (Page 11); 7.1 Added I2C level shifter U12 for DDR3 ECC function (Page 11); 7.2 Added Buffers U24, U25 to match the level of signals (Page 6); 7.3. Added Diode D7, resistors R155, R160. 8. EOL components L1, L2, L3, L4, L6, L7, L9, L10 BKP0603HS121-T replaced by MPZ0603S121HT000. 9. EOL components D8, D9 SP5001-04TTG replaced by EMI8042MUTAG. 10. Resistors R80-R82 replaced by 10k ohm (was 1k43). 11. Added Testpoints TP15 - TP20. 12. The type of testpoints TP1 - TP14 was updated. Diameter changed from 0.8 mm to 1 mm. 13. CEC function is not supported. L11 was removed. C127, D5, R140, R42 are DNP. 14. Power-up sequencing was updated for new DC-DC supplies. 15. Capacitors C29, C32, C33 replaced by 470nF (was 100nF).	VG (06.10.2023)
-04a	1. Removed Digilent licence (MISC1).	ED (16.06.2025)

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Title: Revision_Changes			
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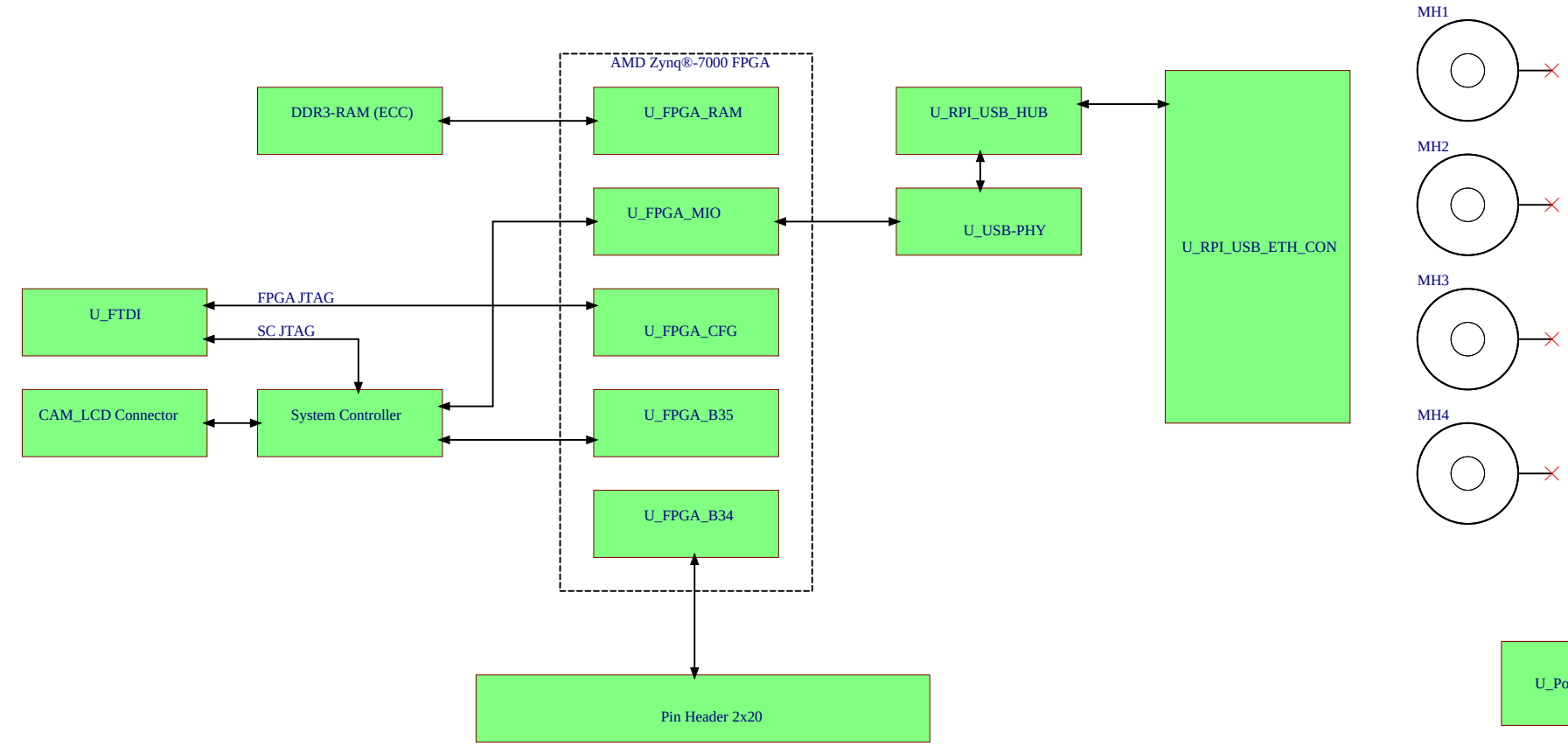

MECH1

TE Address Overlay

LOGO ADDRESS

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

LOGO1

TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

PM1 PM2 PM3

PM4 PM5 PM6

Serial

Serial

Serialnumber 6,3 x 6.3mm

Drawn by	VG
Checked by	IG
Assembly variant	41C98-A
Created by	OT
Modified by	2025-02-13
Modified at	OT

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Title: Overview

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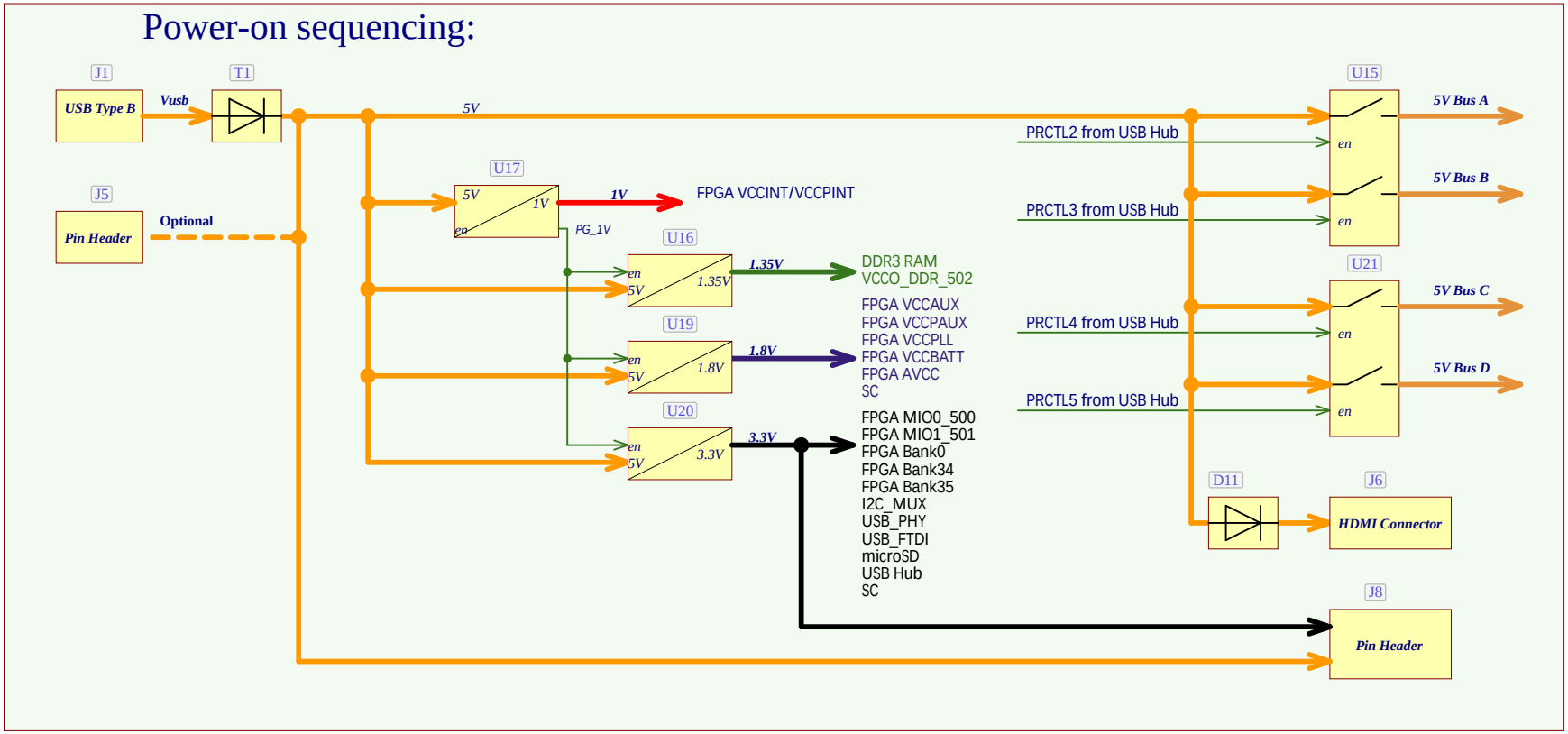
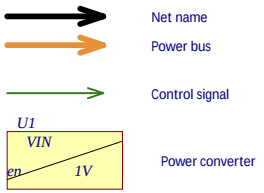
Power-on sequencing:



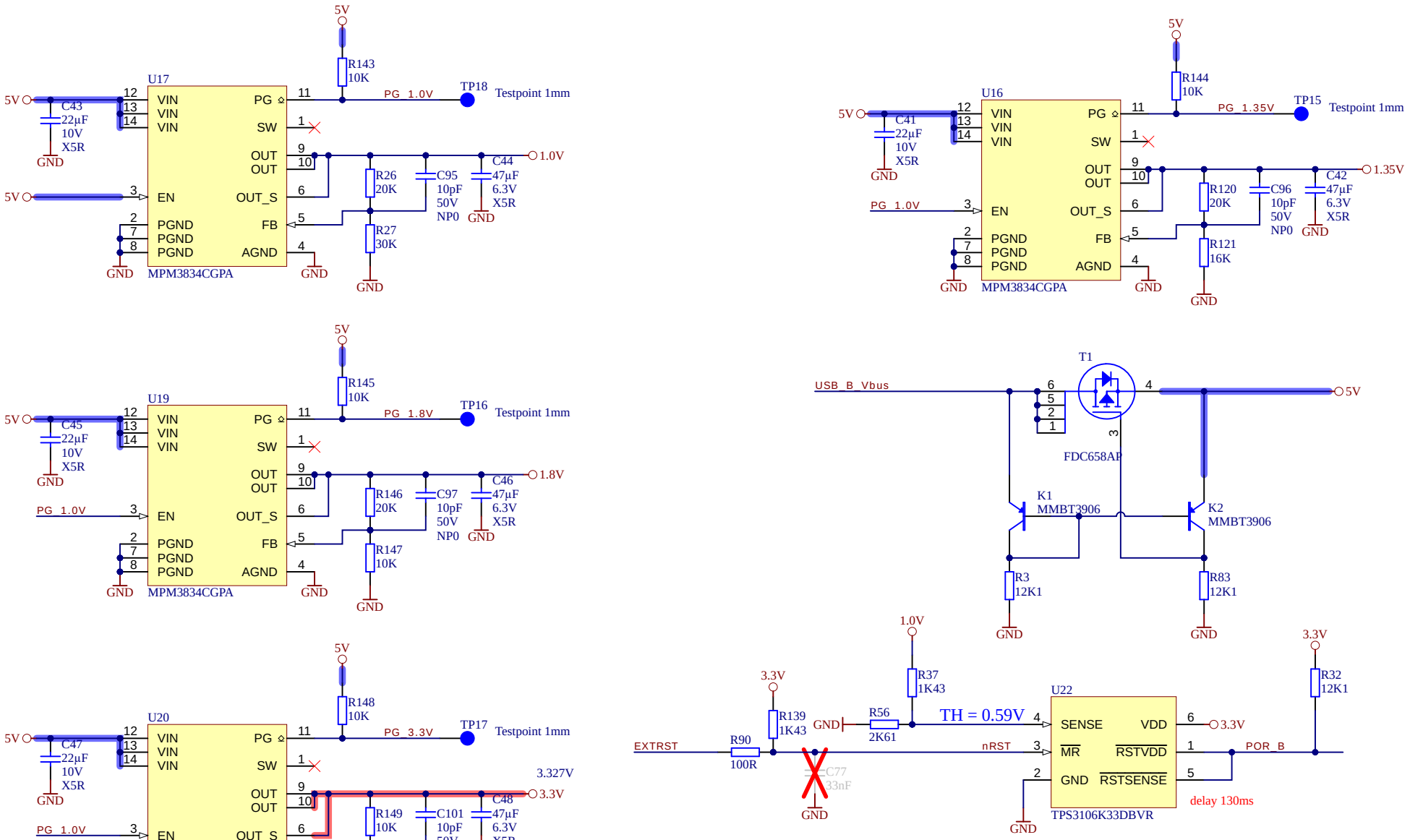
Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V	OUT	5V	+/-5%	Micromodule Power	-
USB_B_Vbus	IN	5V	+/-5%	Micromodule Power	-
3.3V	OUT	3.3V	+/-3%	Micromodule Power	-



U_PowerSupply
PowerSupply.SchDoc

trenz electronic	Title: Power_Diagram		
A4	Number: TE0726 41C98-A		Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page4 of 18
Filename: Power_Diagram.SchDoc			



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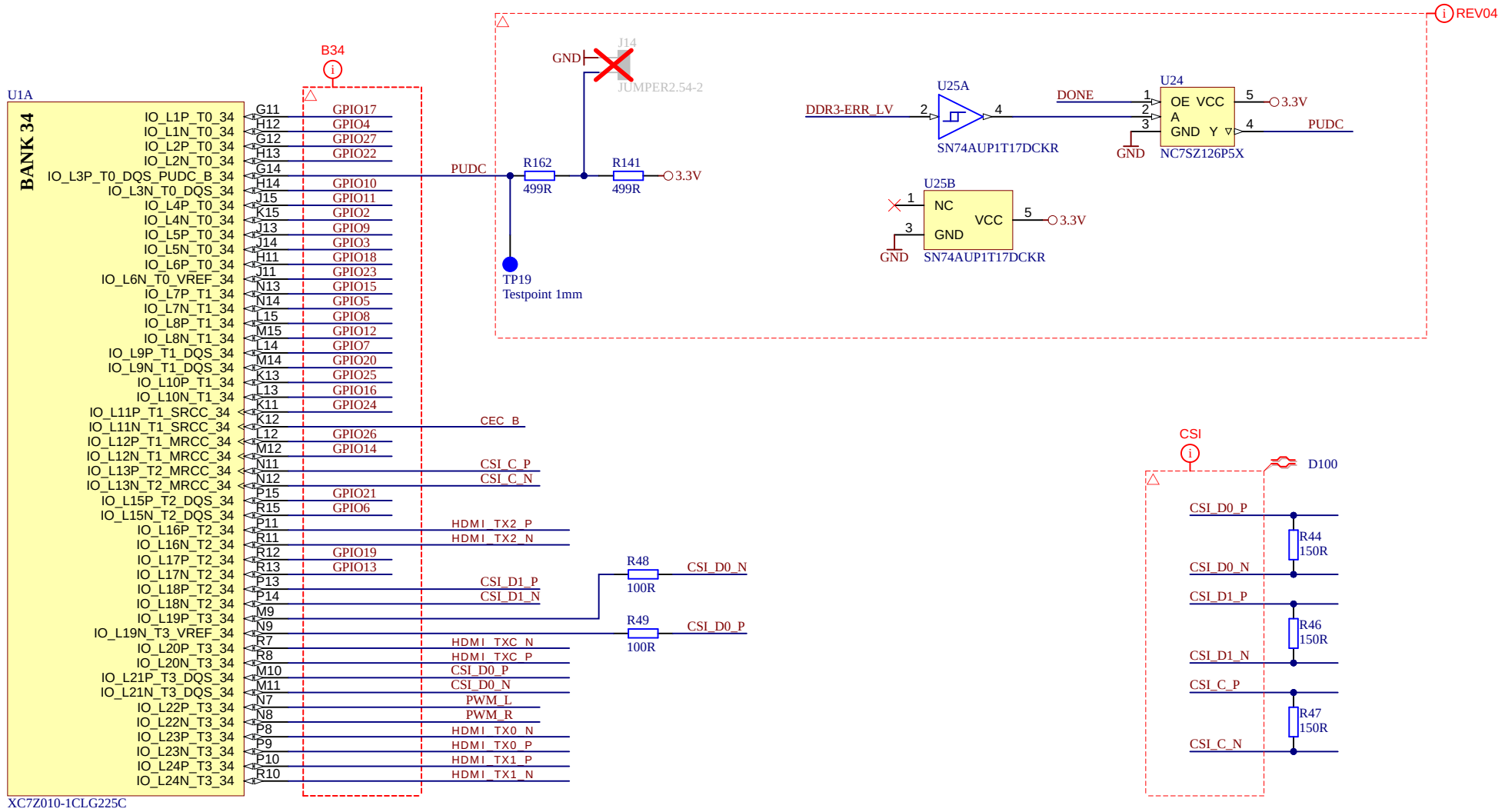
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 5 of 18
Filename: PowerSupply.SchDoc			



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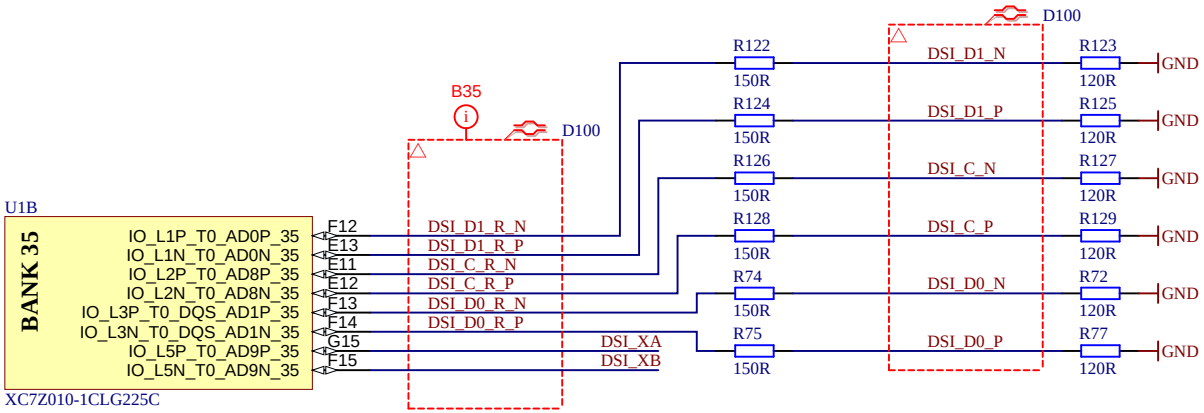
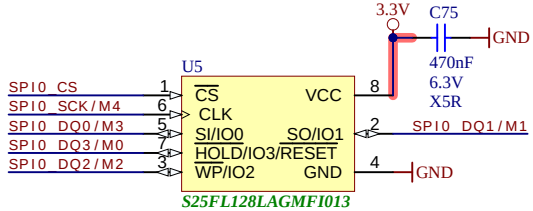
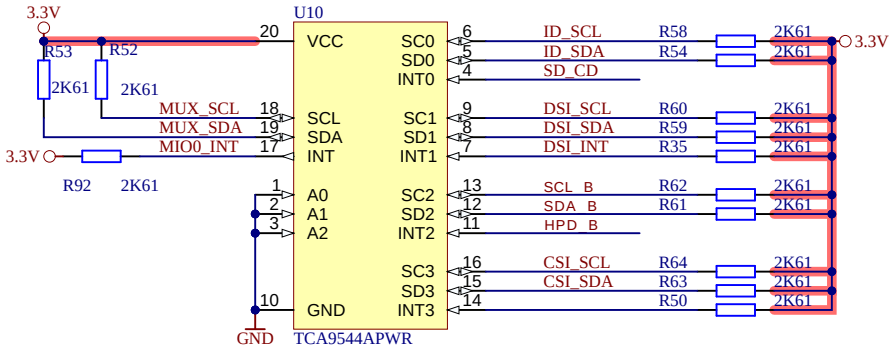
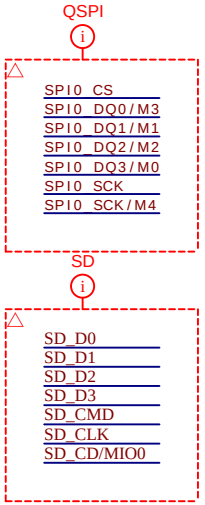
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page6 of 18
Filename: FPGA_B34.SchDoc			

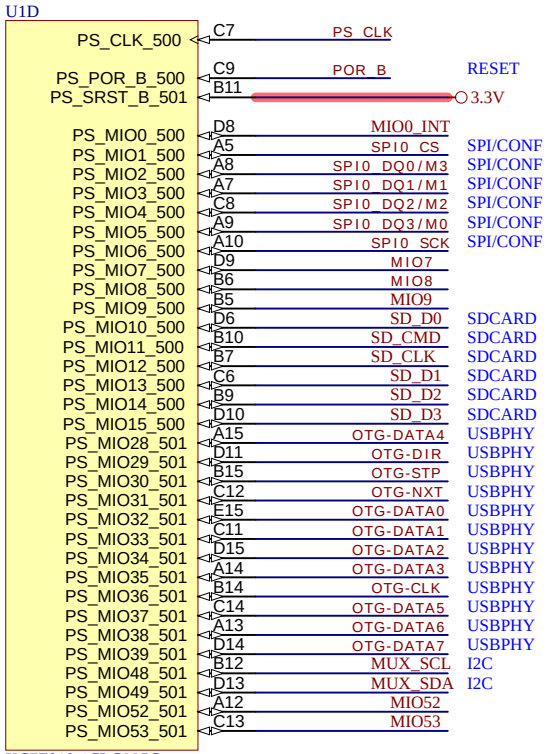


trenz electronic	Title: FPGA B35		
A4	Number: TE0726 41C98-A		Rev. 04
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page7 of 18
Filename: FPGA_B35.SchDoc			









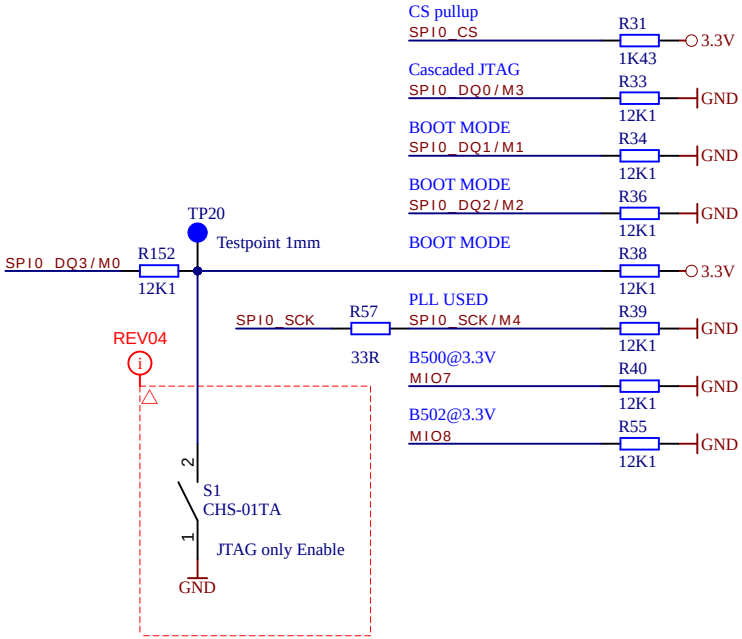


Table 6-4: **Boot Mode MIO Strapping Pins**

Pin-signal / Mode	MIO[8] VMODE[1]	MIO[7] VMODE[0]	MIO[6] BOOT_MODE[4]	MIO[5] BOOT_MODE[0]	MIO[4] BOOT_MODE[2]	MIO[3] BOOT_MODE[1]	MIO[2] BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common[1]			0	0	0		JTAG Chain Routing[2]
NOR Boot[3]			0	0	1		0: Cascade mode
NAND			0	1	0		1: Independent mode
Quad-SPI[3]			1	0	0		
SD Card			1	1	0		

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Title: FPGA MIO		
A4	Number: TE0726 41C98-A	Rev. 04
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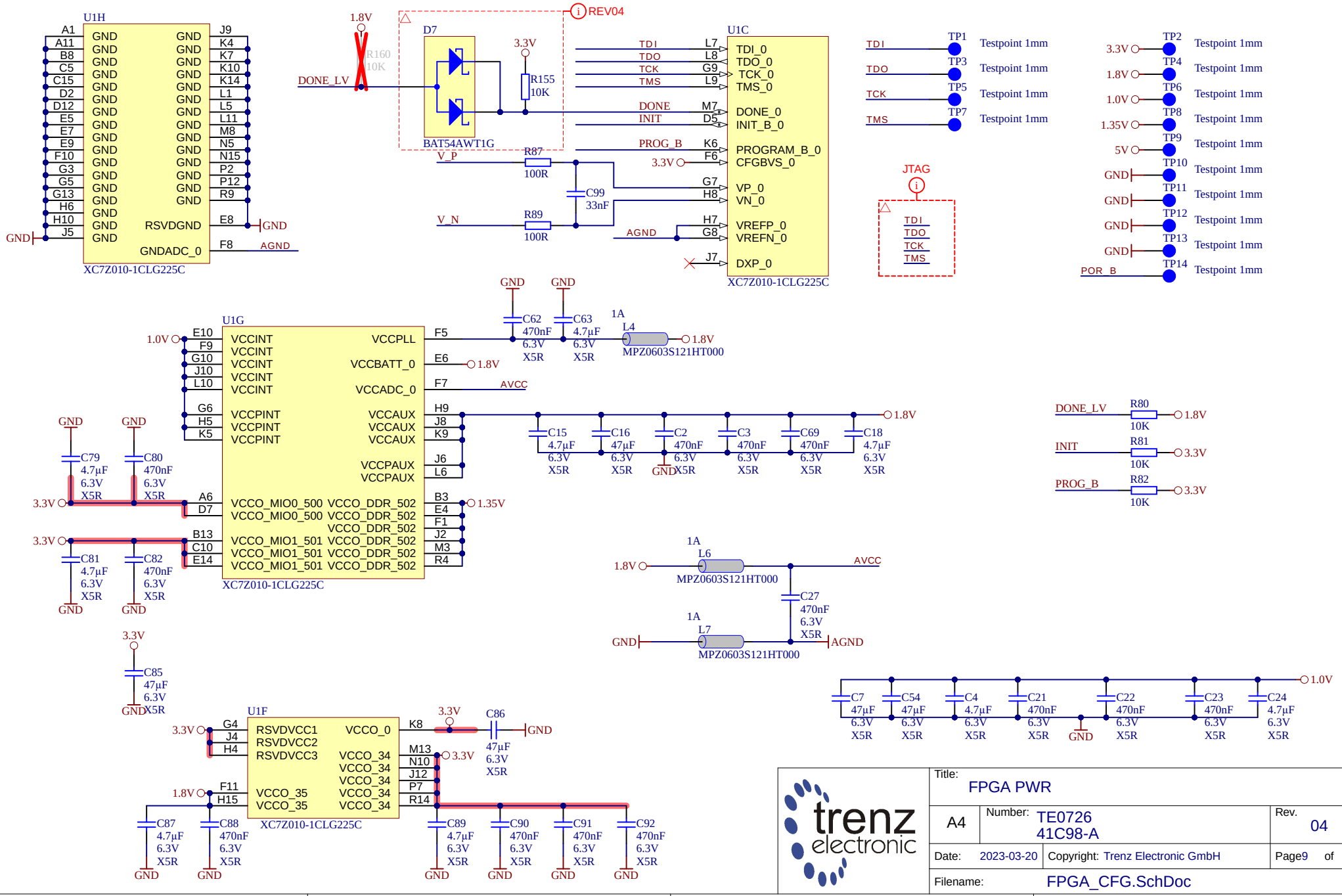
U1H
XC7Z010-1CLG225C
R160 10K
DONE_LV
1.8V
D7
BAT54AWT1G
3.3V
R155 10K
REV04
U1C
TDI
TDO
TCK
TMS
DONE
INIT
PROG_B
V_P
V_N
AGND
R87 100R
R89 100R
C99 33nF
TDI_0
TDO_0
TCK_0
TMS_0
DONE_0
INIT_B_0
PROGRAM_B_0
CFGBVS_0
VP_0
VN_0
VREFP_0
VREFN_0
DXP_0
JTAG
TP1 Testpoint 1mm
TP2 Testpoint 1mm
TP3 Testpoint 1mm
TP4 Testpoint 1mm
TP5 Testpoint 1mm
TP6 Testpoint 1mm
TP7 Testpoint 1mm
TP8 Testpoint 1mm
TP9 Testpoint 1mm
TP10 Testpoint 1mm
TP11 Testpoint 1mm
TP12 Testpoint 1mm
TP13 Testpoint 1mm
TP14 Testpoint 1mm
POR_B
U1G
XC7Z010-1CLG225C
1.0V
VCCINT
VCCPLL
VCCBATT_0
VCCADC_0
VCCPINT
VCCAUX
VCCPAUX
VCCO_MIO0_500
VCCO_MIO1_501
VCCO_DDR_502
C62 470nF 6.3V X5R
C63 4.7µF 6.3V X5R
L4 MPZ0603S121HT000
1A
AVCC
C15 4.7µF 6.3V X5R
C16 47µF 6.3V X5R
C2 470nF 6.3V X5R
C3 470nF 6.3V X5R
C69 470nF 6.3V X5R
C18 4.7µF 6.3V X5R
C79 4.7µF 6.3V X5R
C80 470nF 6.3V X5R
C81 4.7µF 6.3V X5R
C82 470nF 6.3V X5R
1.35V
R80 10K
R81 10K
R82 10K
L6 MPZ0603S121HT000
L7 MPZ0603S121HT000
C27 470nF 6.3V X5R
C85 47µF 6.3V X5R
U1F
RSVDVCC1
RSVDVCC2
RSVDVCC3
VCCO_0
VCCO_34
VCCO_35
C86 47µF 6.3V X5R
C87 4.7µF 6.3V X5R
C88 470nF 6.3V X5R
C89 4.7µF 6.3V X5R
C90 470nF 6.3V X5R
C91 470nF 6.3V X5R
C92 470nF 6.3V X5R
C7 47µF 6.3V X5R
C54 47µF 6.3V X5R
C4 4.7µF 6.3V X5R
C21 470nF 6.3V X5R
C22 470nF 6.3V X5R
C23 470nF 6.3V X5R
C24 4.7µF 6.3V X5R
GND
AGND
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Title: FPGA PWR
A4
Number: TE0726 41C98-A
Rev. 04
Date: 2023-03-20
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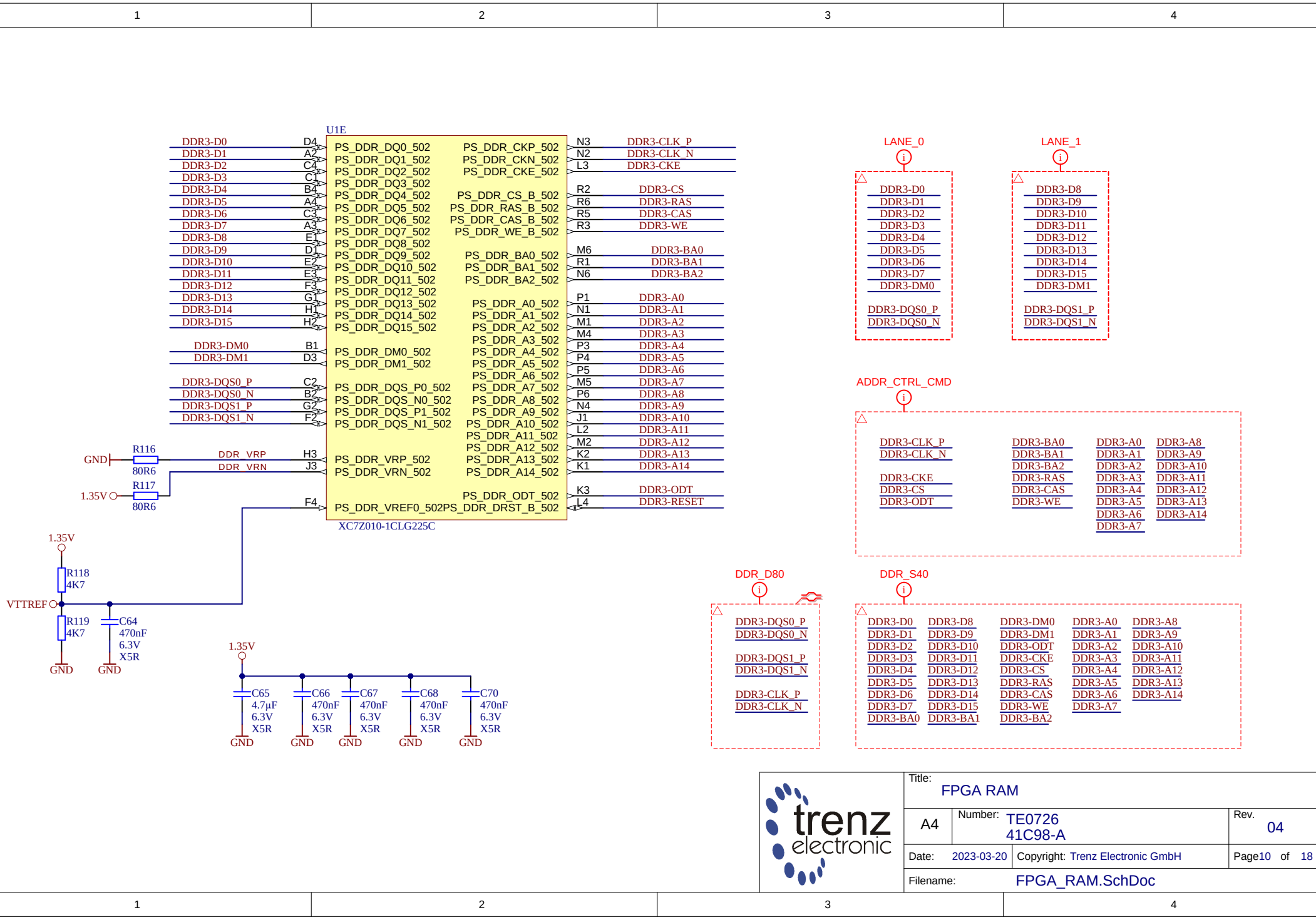
Filename: FPGA_CFG.SchDoc



Title: FPGA RAM			
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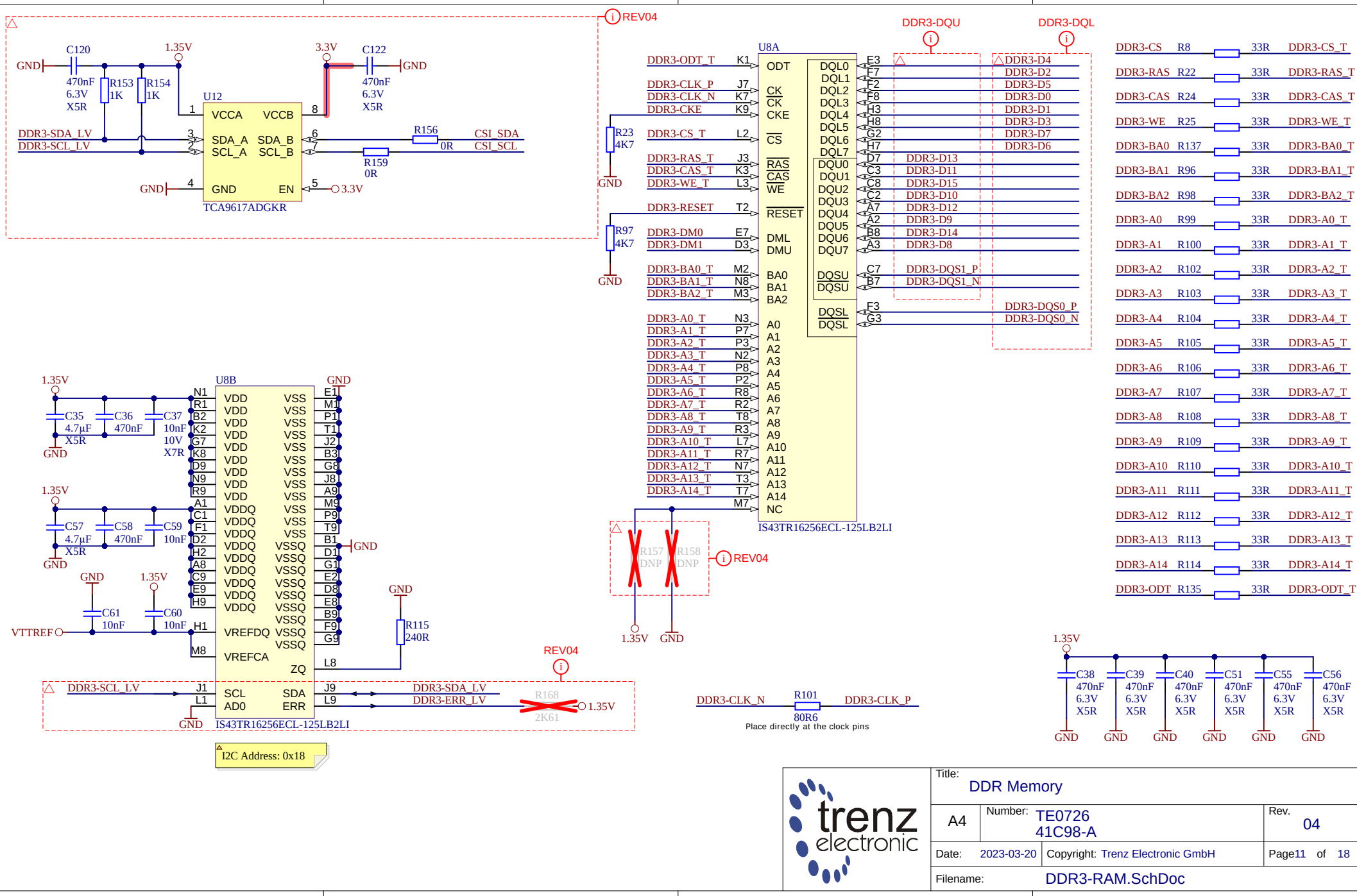
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page10 of 18
Filename: FPGA_RAM.SchDoc			



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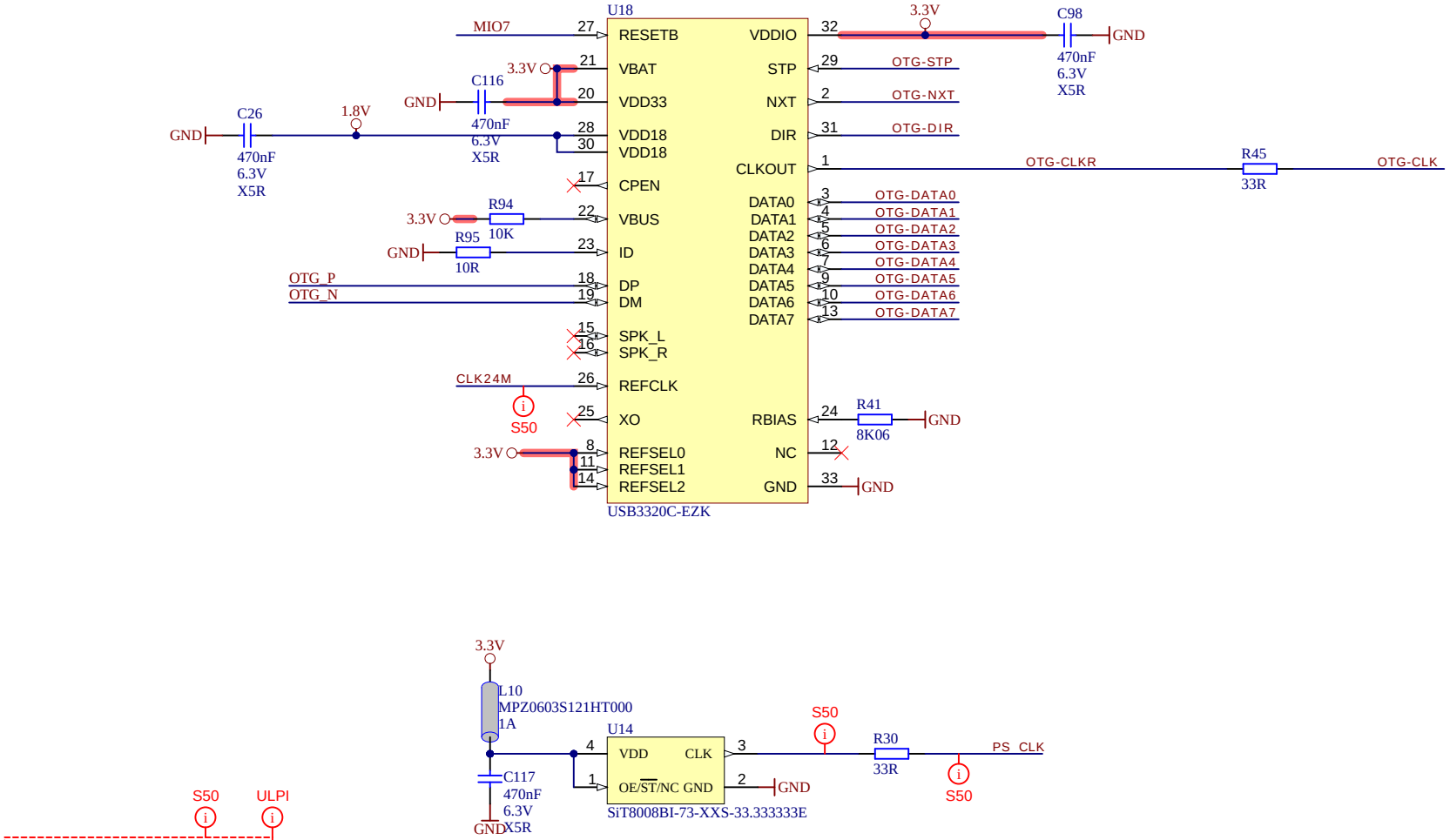
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page11 of 18
Filename: DDR3-RAM.SchDoc			



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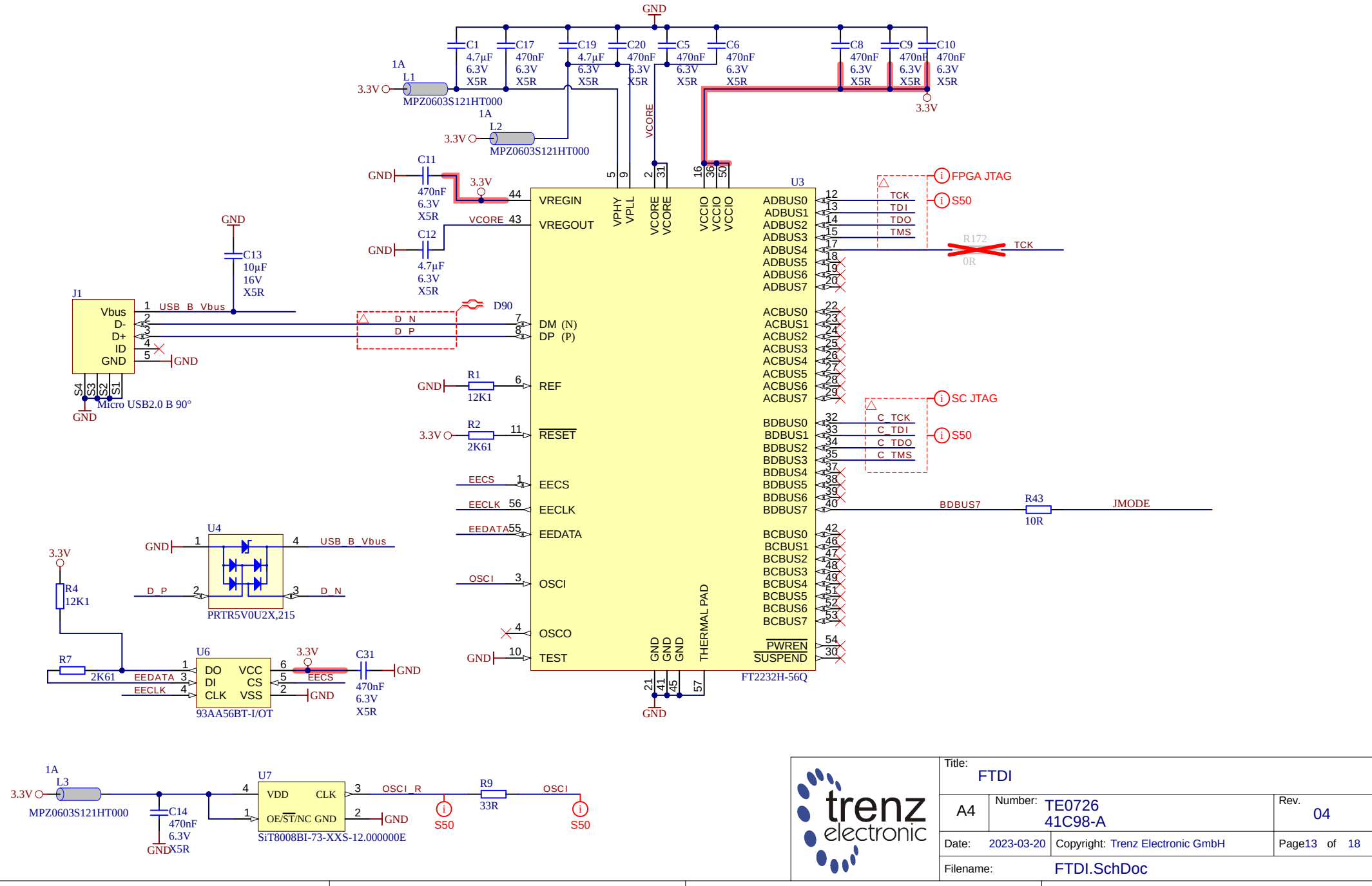
Date: 2023-03-20	Copyright: Trenz Electronic GmbH		Page12 of 18
Filename: USB-PHY.SchDoc			



trenz electronic	Title: FTDI		
	A4	Number: TE0726 41C98-A	Rev. 04
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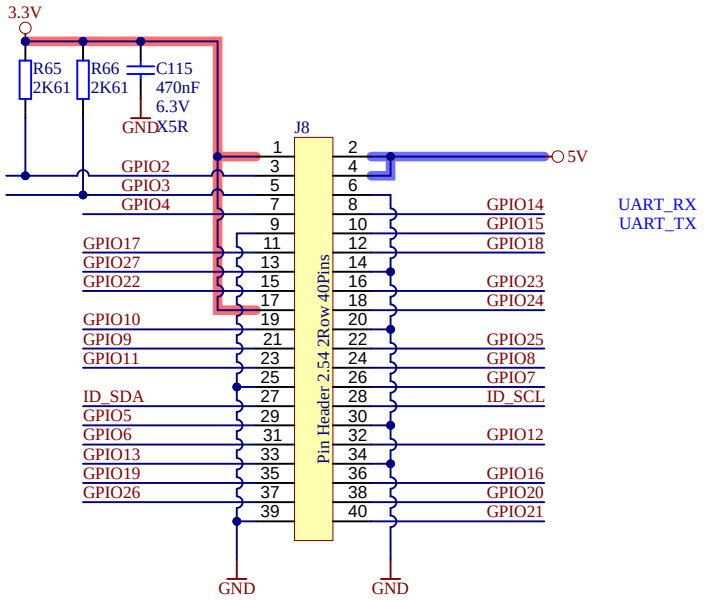
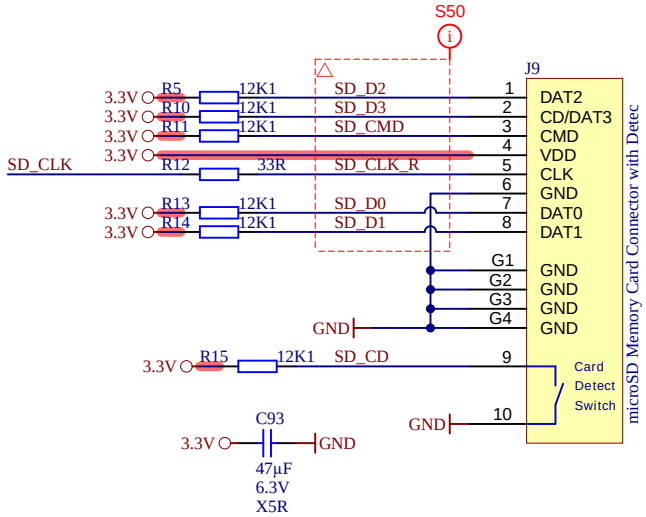
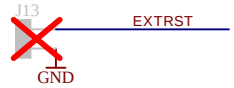
	Filename: FTDI.SchDoc		







JUMPER2.54-2

trenz electronic	Title: Connectors		
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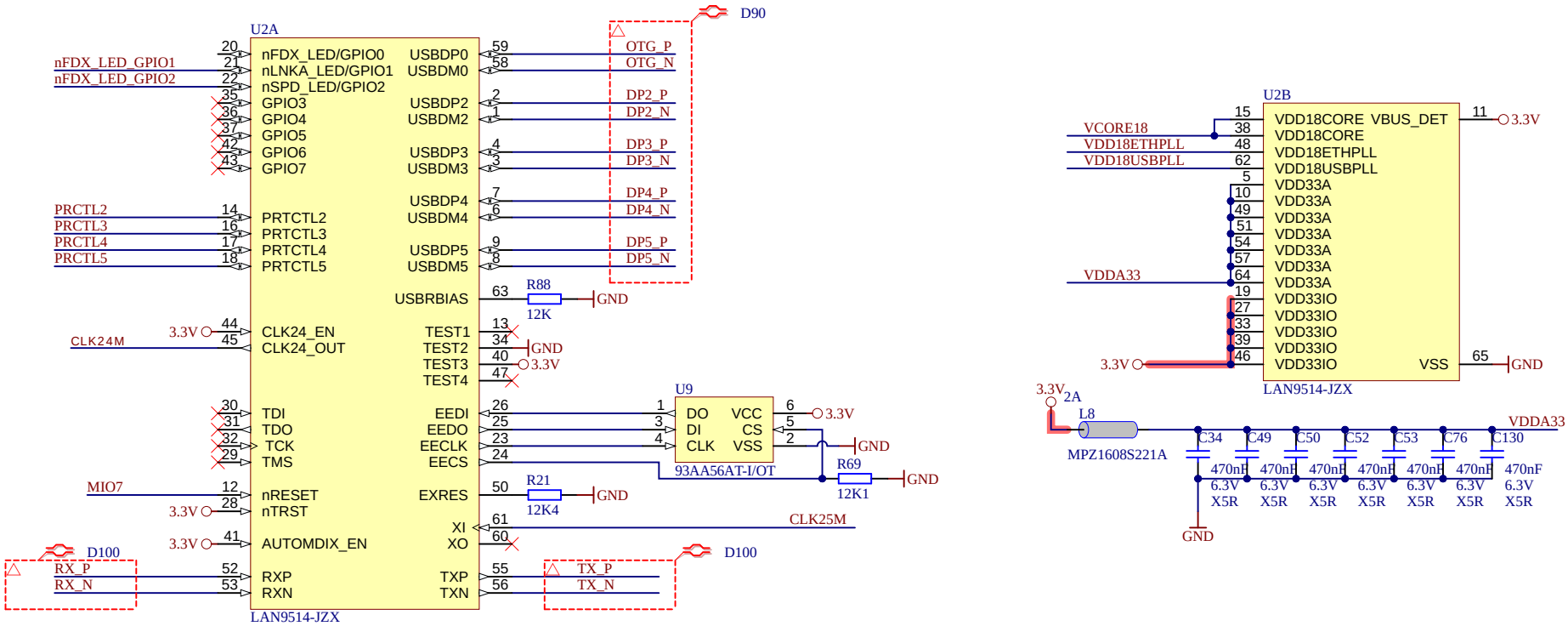
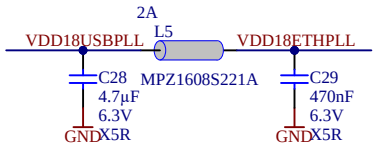
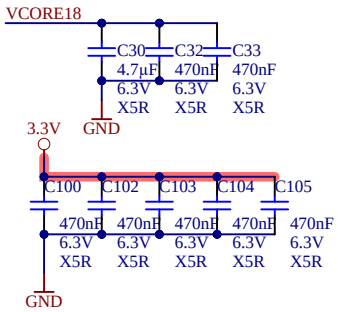
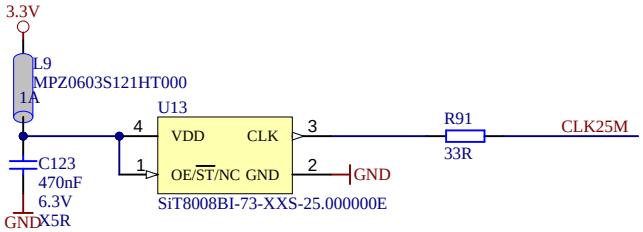
Filename: RPi-Headers.SchDoc			









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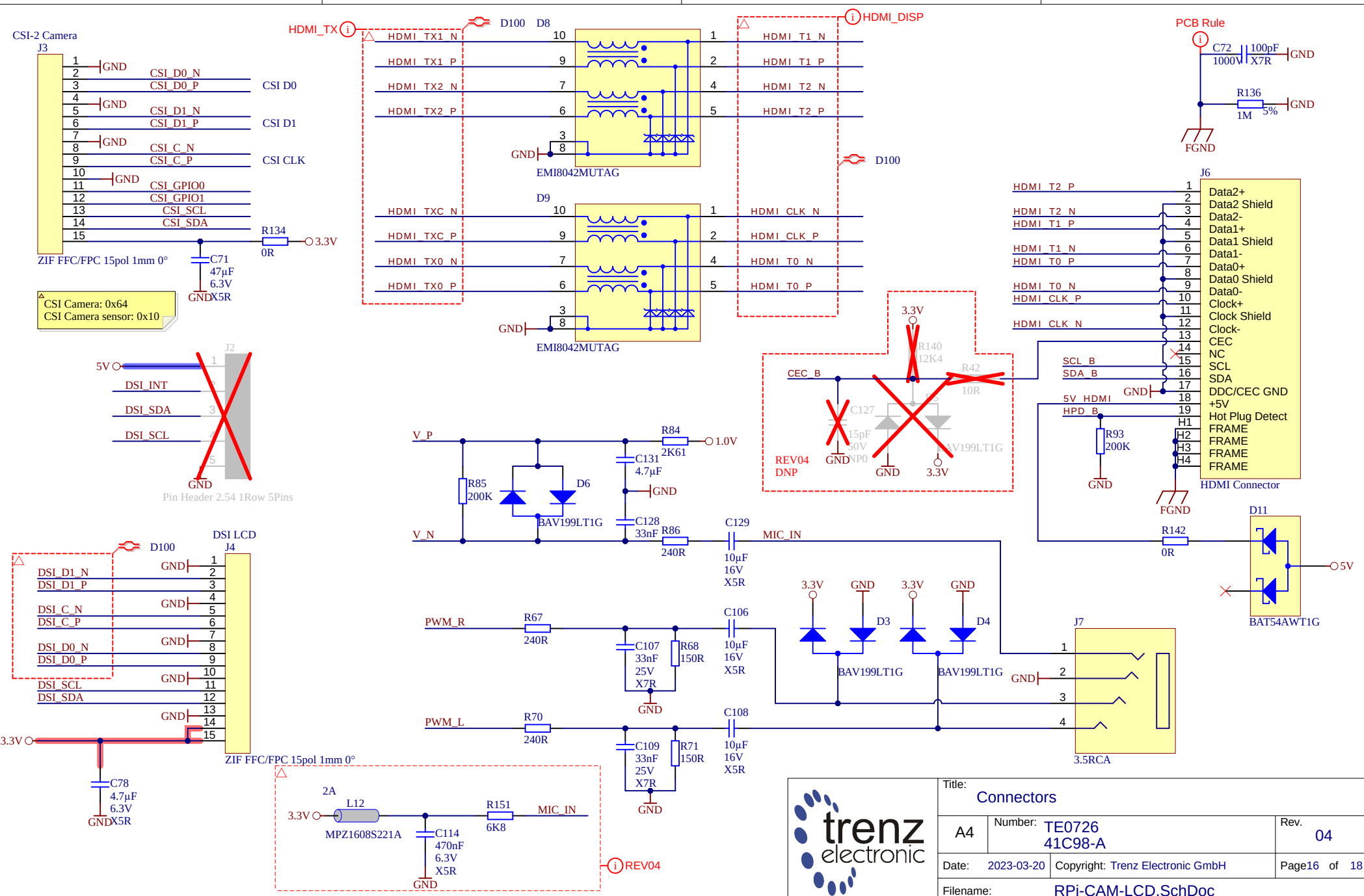
Filename: RPi-USB-HUB.SchDoc			


CSI-2 Camera
J3
CSI_D0_N
CSI_D0_P
CSI D0
CSI_D1_N
CSI_D1_P
CSI D1
CSI_C_N
CSI_C_P
CSI CLK
CSI_GPIO0
CSI_GPIO1
CSI_SCL
CSI_SDA
R134
0R
3.3V
C71
47µF
6.3V
X5R
ZIF FFC/FPC 15pol 1mm 0°
CSI Camera: 0x64
CSI Camera sensor: 0x10
HDMI_TX
D100
D8
HDMI_TX1_N
HDMI_TX1_P
HDMI_TX2_N
HDMI_TX2_P
EMI8042MUTAG
D9
HDMI_TXC_N
HDMI_TXC_P
HDMI_TX0_N
HDMI_TX0_P
HDMI_DISP
HDMI_T1_N
HDMI_T1_P
HDMI_T2_N
HDMI_T2_P
HDMI_CLK_N
HDMI_CLK_P
HDMI_T0_N
HDMI_T0_P
PCB Rule
C72
1000V
100pF
X7R
R136
1M
5%
FGND
J6
Data2+
Data2 Shield
Data2-
Data1+
Data1 Shield
Data1-
Data0+
Data0 Shield
Data0-
Clock+
Clock Shield
Clock-
CEC
NC
SCL
SDA
DDC/CEC GND
+5V
Hot Plug Detect
FRAME
HDMI Connector
SCL_B
SDA_B
5V_HDMI
HPD_B
R93
200K
J2
5V
DSI_INT
DSI_SDA
DSI_SCL
Pin Header 2.54 1Row 5Pins
CEC_B
R140
12K4
R42
10R
C127
15pF
50V
NP0
BAV199LT1G
REV04
DNP
V_P
V_N
R84
2K61
1.0V
C131
4.7µF
R85
200K
D6
C128
33nF
R86
240R
C129
10µF
16V
X5R
MIC_IN
R142
0R
D11
5V
BAT54AWT1G
DSI LCD
J4
DSI_D1_N
DSI_D1_P
DSI_C_N
DSI_C_P
DSI_D0_N
DSI_D0_P
DSI_SCL
DSI_SDA
ZIF FFC/FPC 15pol 1mm 0°
C78
4.7µF
6.3V
X5R
PWM_R
PWM_L
R67
240R
R70
240R
C106
C107
33nF
25V
X7R
R68
150R
C108
C109
33nF
25V
X7R
R71
150R
10µF
16V
X5R
D3
D4
BAV199LT1G
J7
3.5RCA
2A
L12
MPZ1608S221A
R151
6K8
C114
470nF
6.3V
X5R
REV04
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electronic
Title:
Connectors
A4
Number:
TE0726
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Filename:
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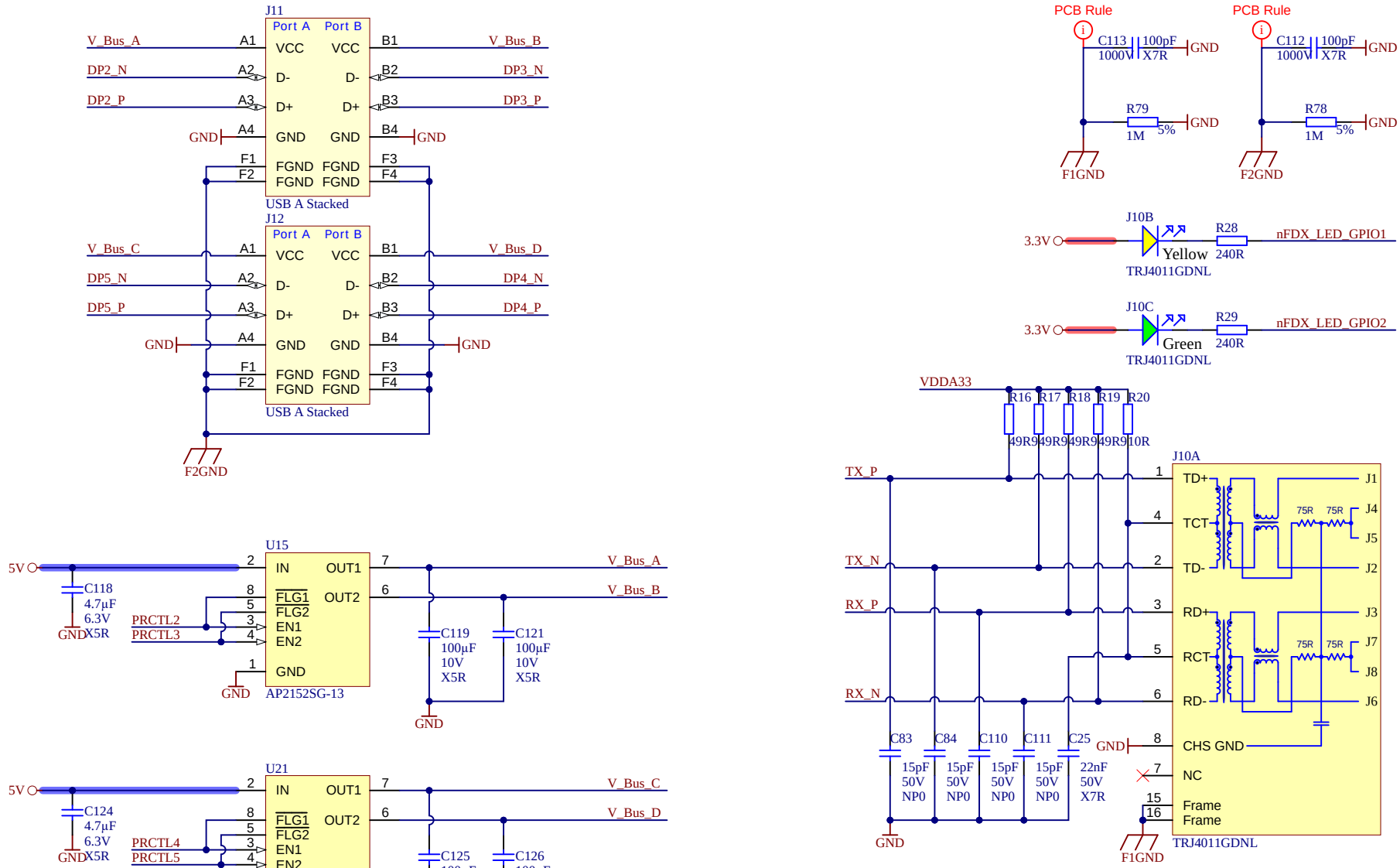

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Title: USB ETHERNET			
A4	Number: TE0726 41C98-A		Rev. 04
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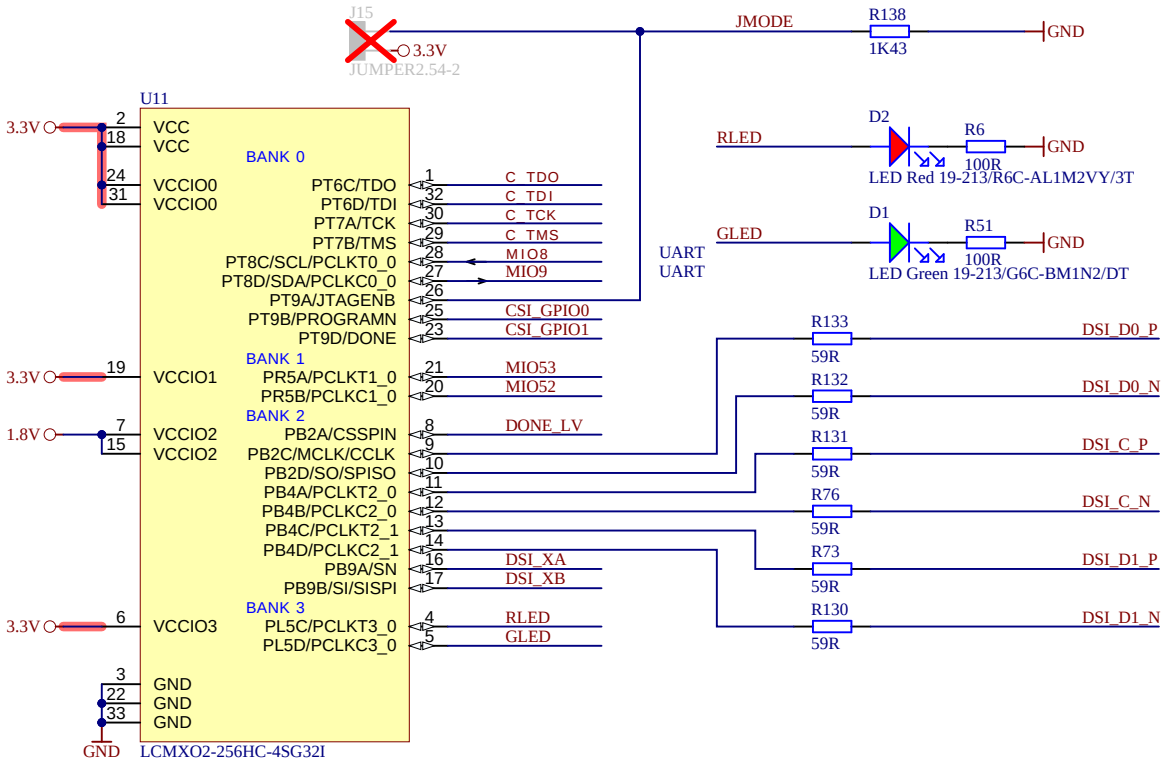
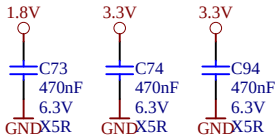
Filename: PRi-USB-ETH-CON.SchDoc			





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