

Supported Voltage Ranges:

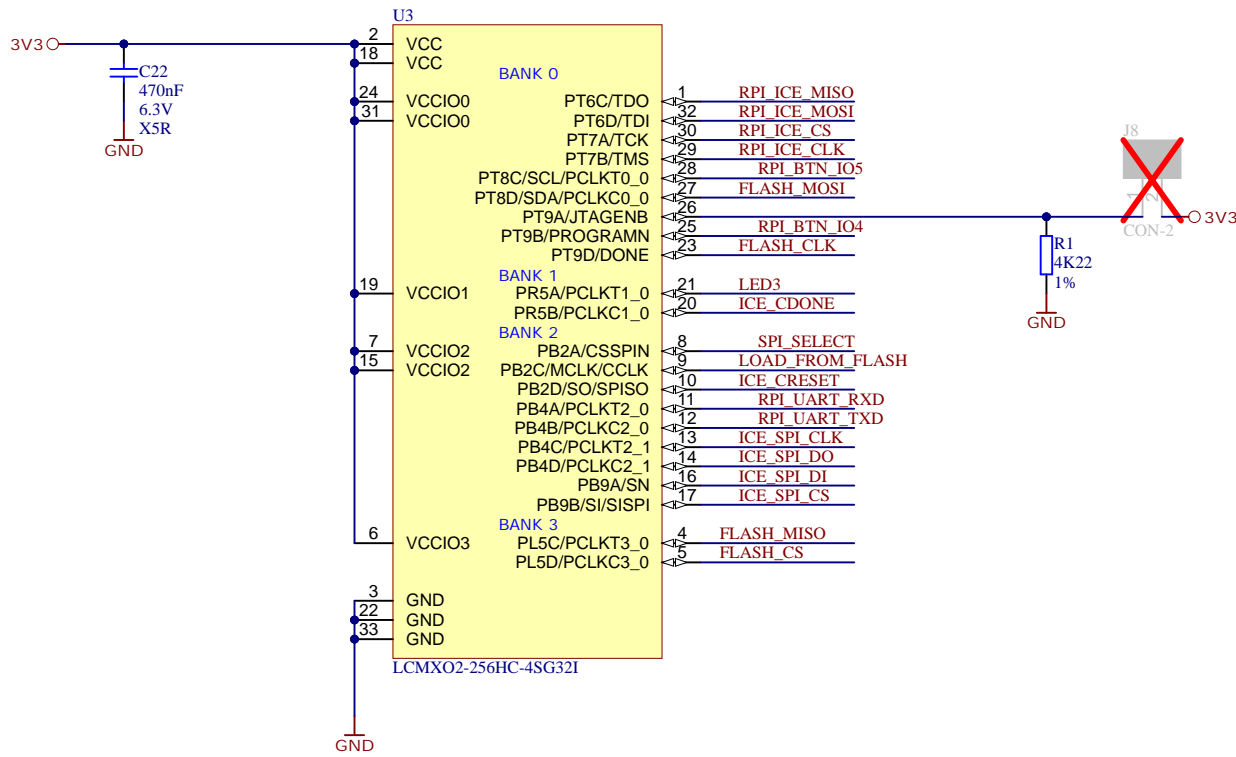
Power Rail	Direction	Range	Tolerance	Description	Note
5V0	IN	5.0 V	+/- 3 %	Input Power	From RPi HAT
3V3	OUT	3.3 V	+/- 3 %	Module Power	Power for Chips and Connectors

Legend:

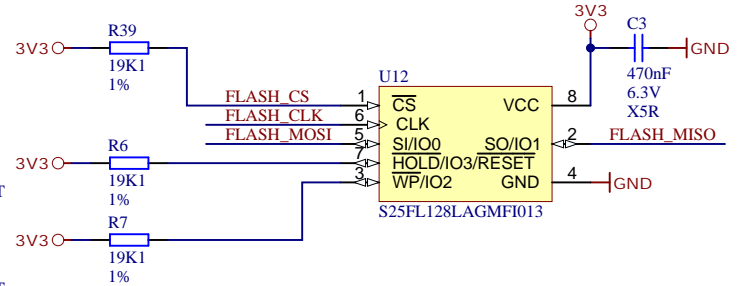
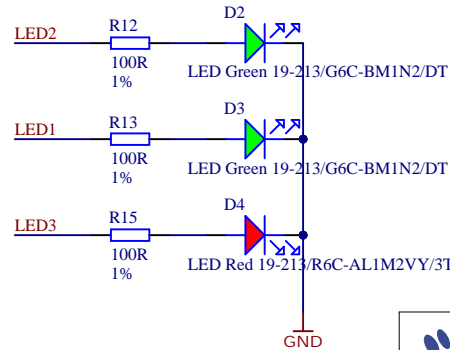
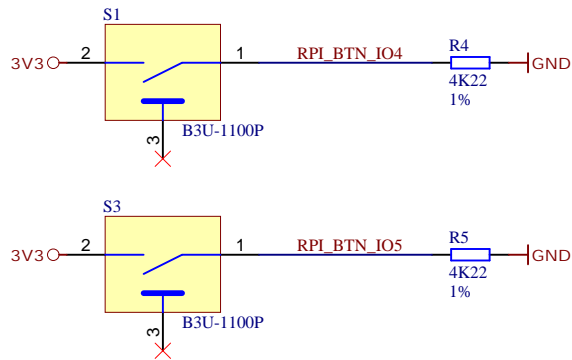
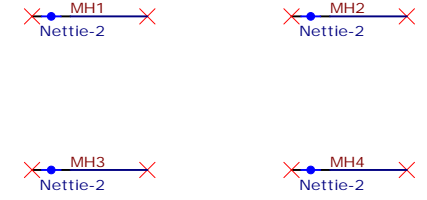
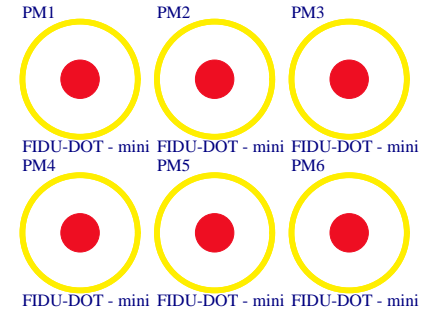
- Connectors
- LED Interface
- On-board Components
- Misc
- PWR FPGA
- Revision changes
- Legal notices



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Serial
Serialnumber 6,3 x 6.3mm



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A

A

B

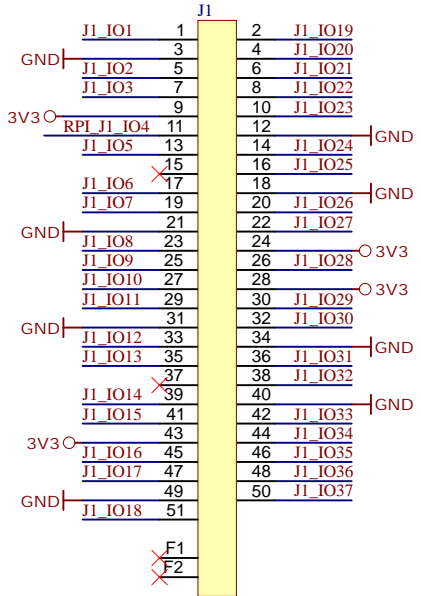
B

C

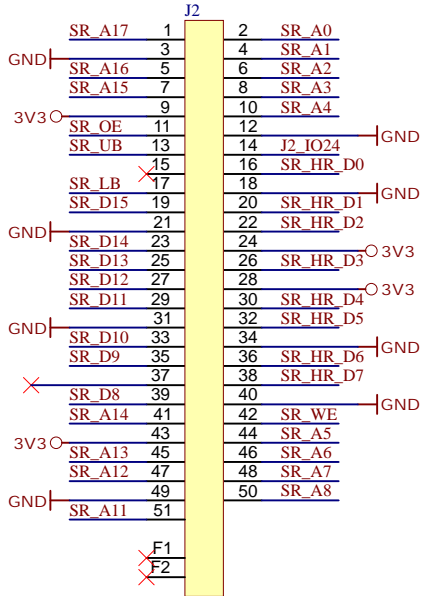
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D

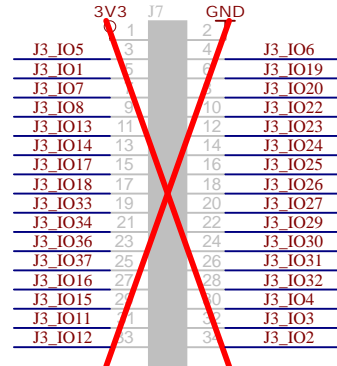
D



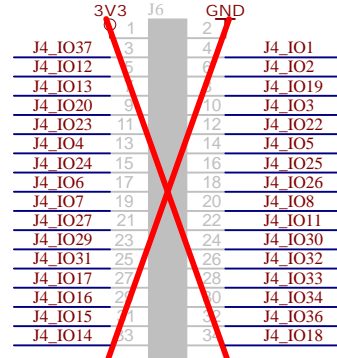
FPC 51pol. 0,3mm 90°



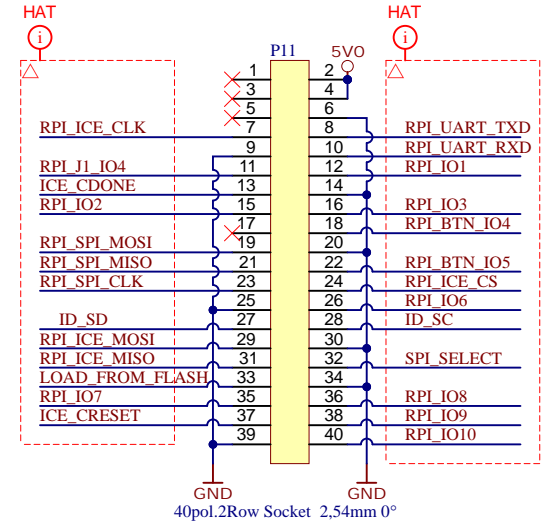
FPC 51pol. 0,3mm 90°



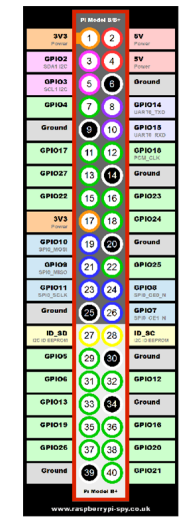
WANNE2,54-34 GERÄDE



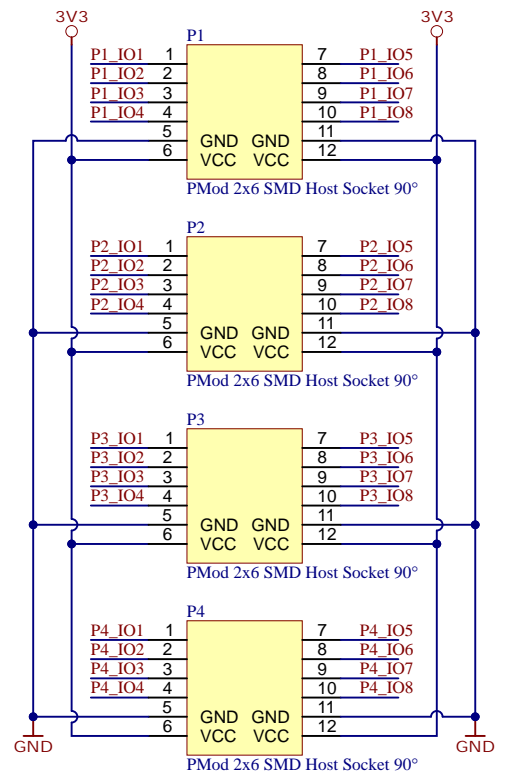
WANNE2,54-34 GERÄDE




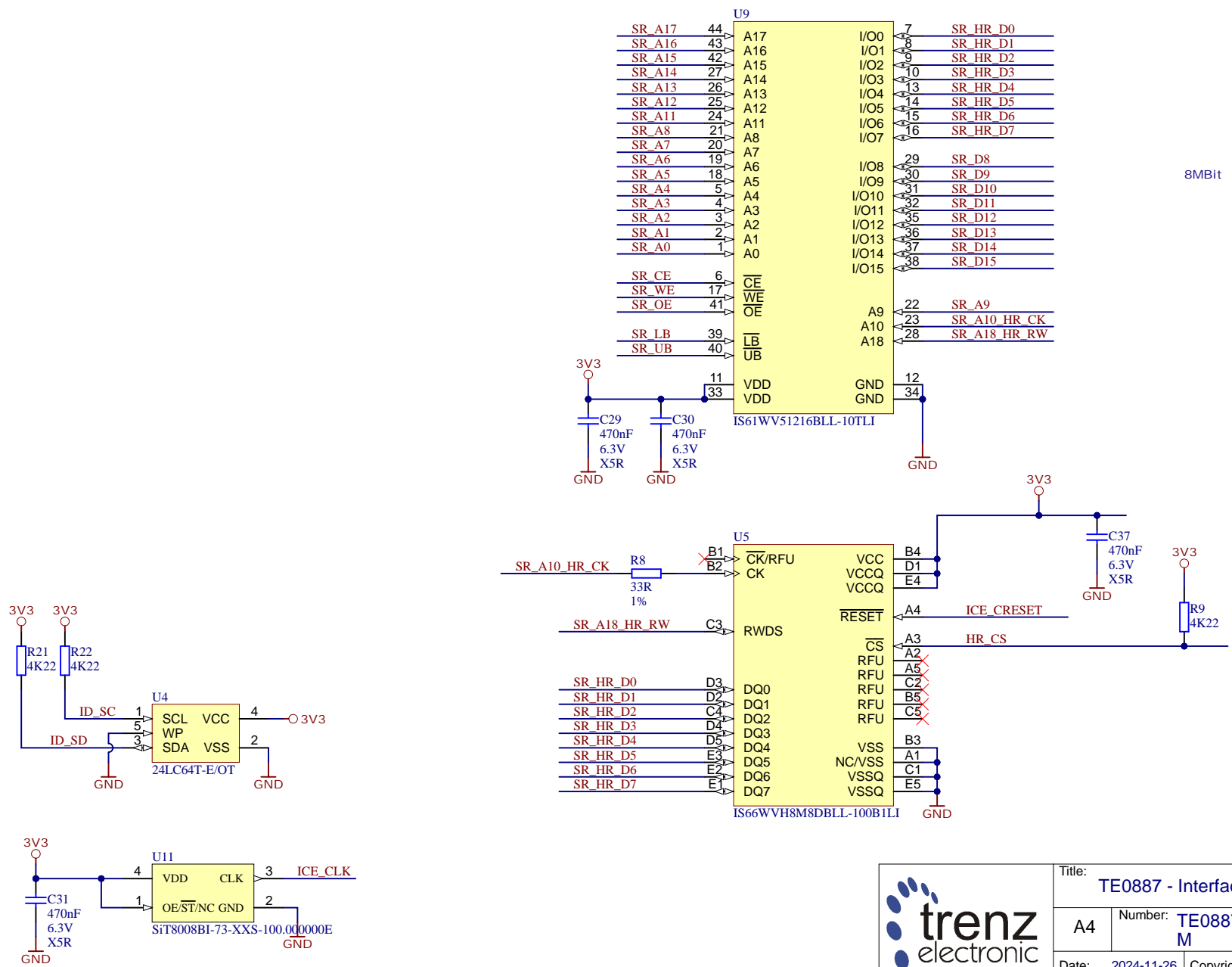
40pol.2Row Socket 2,54mm 0°



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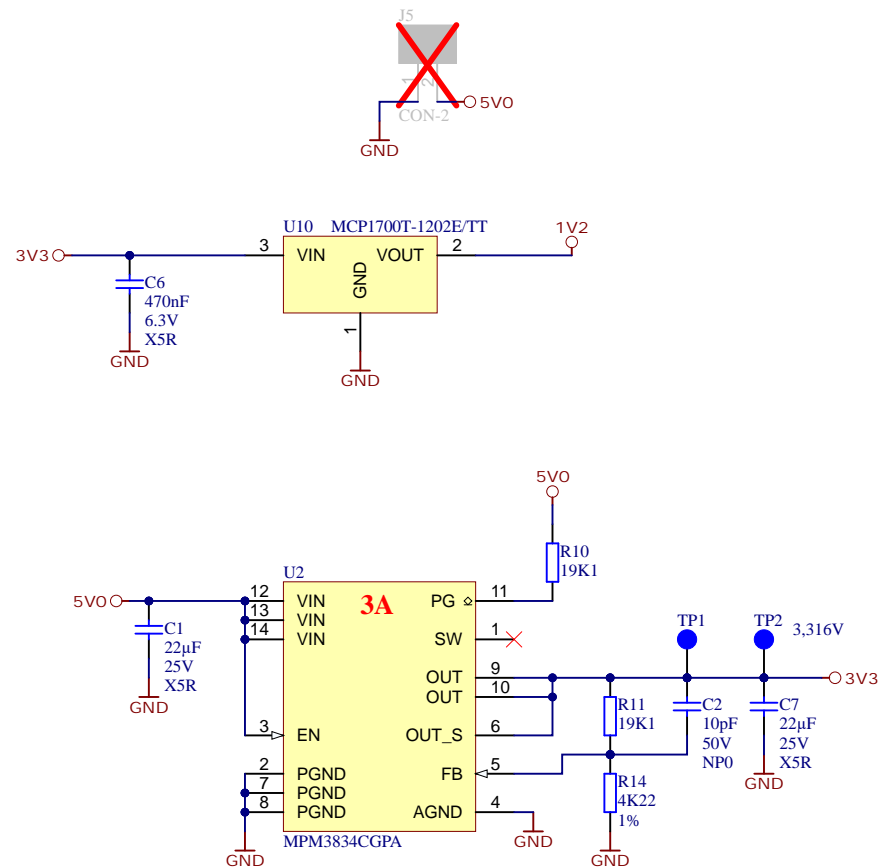
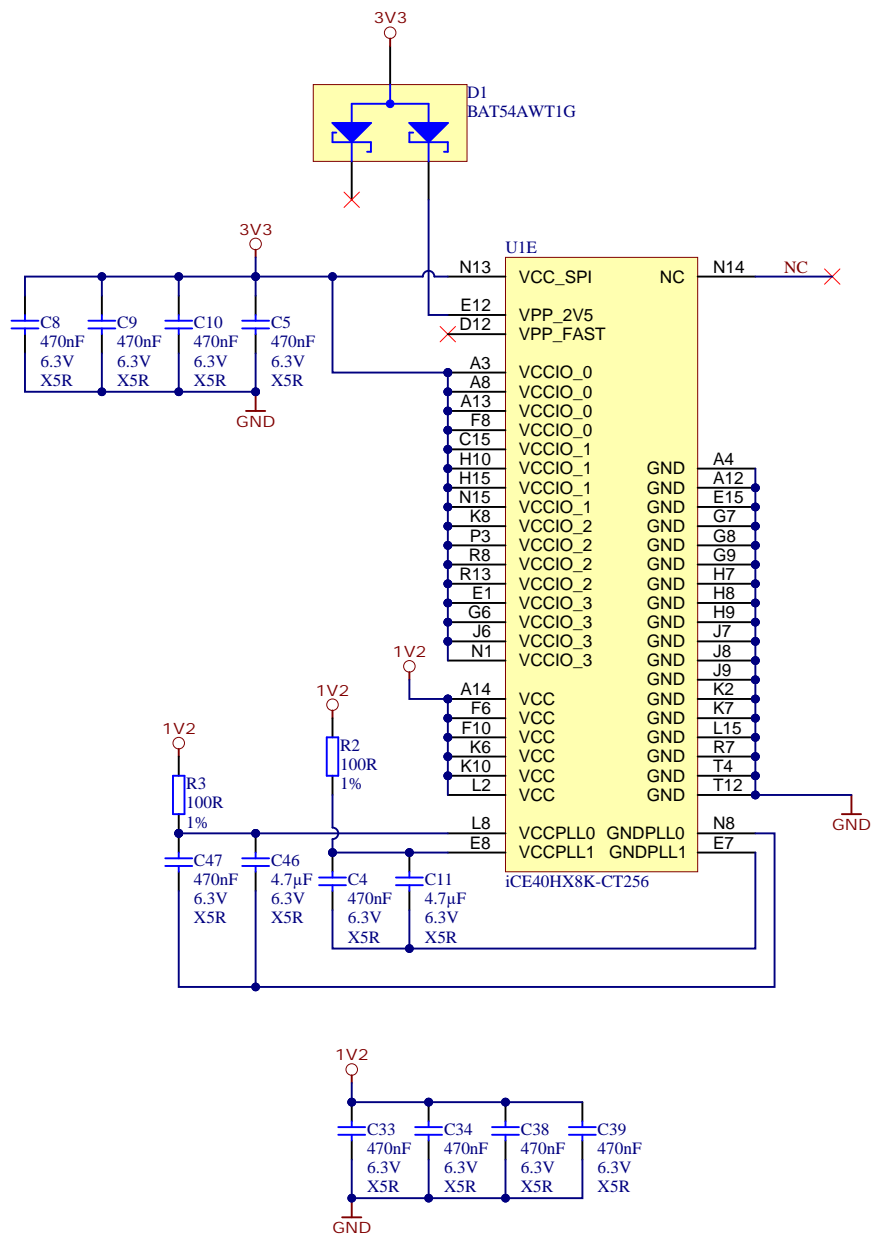
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SRAM on the WEB
 8MBit [IS61WV51216BLL-10TLI](http://www.trenz-electronic.com/Products/IS61WV51216BLL-10TLI)




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	Title: TE0887 - Power		
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REV	Description	
-01	Initial revision	IG
-02	See old project files	IG
-03	<ol style="list-style-type: none"> 1. PCB: changed position of connectors J1-J4. J1, J3: ΔY -0.8mm; J2, J4: ΔY -0.9mm 2. U12 HOLD and WP inputs connected to 3.3V via 10 kOm pull-up resistor. 3. PCB: jumper J8 (CPLD JTAG_EN) moved between P3 - P4 4. Added series R8 to IO87 (Hyper RAM CK input) 5. Added pull-up resistor R9 (Hyper RAM CS input) 6. P1 and P2 are interchanged 7. Added PMOD and pin headers labels 8. Renamed nets 9. U5 HyperFlash replaced by HyperRAM 	IG
-04	<ol style="list-style-type: none"> 1. Changed U2 from EN5311QI (EOL) to MPM3834CGPA-Z. 2. Updated nomenclature of power nets (3.3V -> 3V3 etc.) 3. Changed LEDs (D2, D3, D4) to newer versions. 4. Changed U12 from S25FL127 to S25FL128. 5. Changed U5 from S27KL0641 to IS66WVH8M8. 6. Changed R1, R4, R5, R21 and R22 from 3k3 to 4k22. 7. Changed R6, R7, R20 and R39 from 10k to 19k1. 8. Added 19K1 pull-up to ICE_CRESET and ICE_SPI_CS (R16, R17) 9. Added three 470 nF capacitors (C8,C9,C10) to 3V3 under U1 10. Added Pull-up resistor R9 to net HR_CS. 	LH

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Drawn by: LH			

