

TEB0911 TRM

Revision v.188

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4 Overview

The Trenz Electronic TEB0911 UltraRack+ board has as its heart an AMD Zynq UltraScale+ MPSoC with a DDR4-SDRAM SODIMM socket for RAM, 2 QSPI flashes and an e.MMC Flash memory for configuration and operation. Further an MMC SD card and a M.2 SSD socket are provided. Power for multiple domains is provided by switch-mode power supplies for all on-board voltages.

The SoCs pins are exposed to 6 FMC HPC connectors, so that 22x MGT Lanes and 236x single ended or 118 differential pairs are available. The board is further equipped with gigabit ethernet via RJ45 and two SFP+ connectors, a DisplayPort and two USB 3.0 type A connectors.
A System Controller is on-board for control and management. It provides a CAN bus port and interfaces multiple buttons, DIP switches and status LEDs to the system.

The board is equipped with two TE0790 programming adapters with access to the SoC, system controller and all FMC HPC connectors.

Refer to https://trenz.org/teb0911-info for current online available documentation.

4.1 Key Features

- **SoC**
  - AMD Zynq UltraScale+ MPSoC [1)]: XCZU6EG / XCZU9EG / XCZU15EG
  - Speedgrade [1)]: -1 / -2 / -3
  - Temperature Range [1)]: E / I
  - Package [1)]: B1156
- **RAM/Storage**
  - 1x DDR4 SDRAM SODIMM socket (64 bit width)
  - 2x QSPI Flash 512 Mbit (with XiP support) [2)]
  - e.MMC 8 GByte [2)]
  - M.2 M key socket
  - MMC SD card socket
  - 1x EEPROM 128 kbit for USB 3.2 hub configuration
  - 1x EEPROM 128 kbit
  - 3x EEPROM 2 kbit with unique EUI-48 ™ / MAC address
- **On Board**
  - 10/100/1000 BASE-T/X ethernet transceiver
  - USB 3.2 hub with ESD protection
  - USB 2.0 transceiver
  - CAN transceiver with ESD protection
  - 2x I2C switches
  - Programmable clock generators for FMC HPC
  - Programmable clock generators for M.2 and SoC PS GTR bank
  - Clocking sources for:
    - USB 3.2 hub and USB 2.0 transceiver
    - Ethernet PHY
    - Both CLK generators - 2x oscillators and 1x crystal
    - SoC programming system
    - Optional:
      - Oscillator for SoC MGT bank 505
      - Oscillator for System controller
- **Interface**
  - 2x TE0790 programming adapters with JTAG/UART/IO to USB 2.0 bridge
  - FMC HPC / ANSI/VITA 57.4 compliant FMC+:
    - IO: 236x SE / 118x DIFF

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        - MGT: 22x GTH (RX/TX)
        - JTAG and I2C for each connector
        - Control signals, trigger and Clocks
        - PWM fan header 12 V (optional 5 V) for each connector
    - 2x SFP+ connector
    - RJ45 mag-jack with 2x LEDs
    - 2x USB 3.0 type A sockets
    - DisplayPort - AUX channel with ESD protection
    - CAN with termination options
    - I2C header for PLL/CLK generator configuration
    - 3x PWM fans 12 V for SoC and system cooling
    - LEDs:
        - SoC status - 1x red
        - RJ45 ethernet status - 1x green and 1x green/yellow
        - SFP+ slot status - 2x green and 2x red
        - USB 3.2 hub status - 1x green
        - 4x user - 1x red and 3x green
    - Buttons: 2x reset, 1x user definable
    - DIP switches:
        - 4x user definable
        - 2x SoC boot mode and 2x system
- **Power**
    - 24 V Single Rail Power Supply - 5x pin Würth WE series
    - Supply protection - Over and under voltage, Reverse polarity and fuse (4 A)
    - Multi domain power options for periphery and SoC supply
    - Backup battery - Coin Cell 1220, 3 V/Lithium
- **Dimension**
    - 234.0 mm x 406.0 mm
- **Notes**

[1)] Available as assembly variant or upon request.

[2)] Other sizes/devices, which are pin/package-compatible, upon request.

4.2 Block Diagram

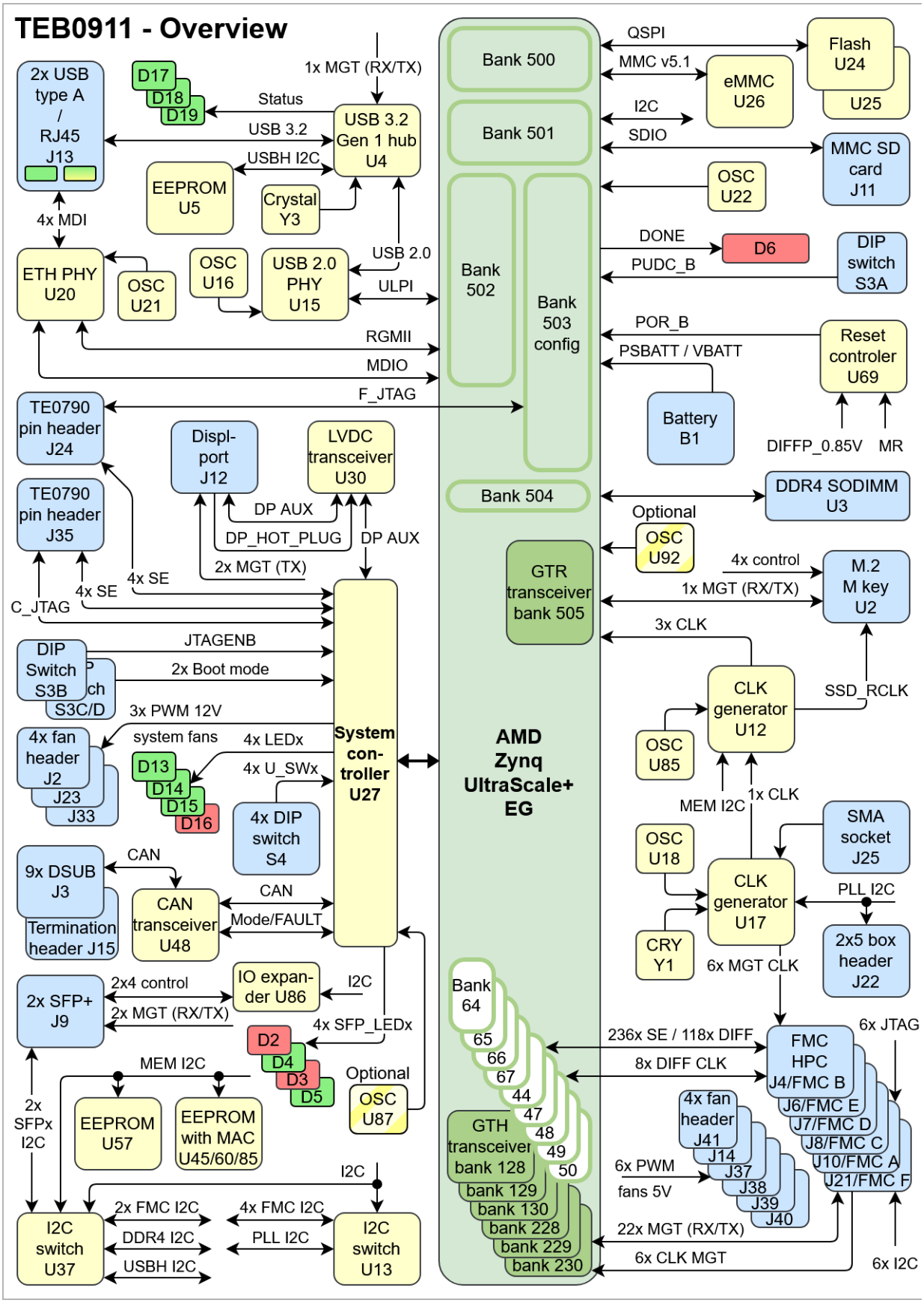
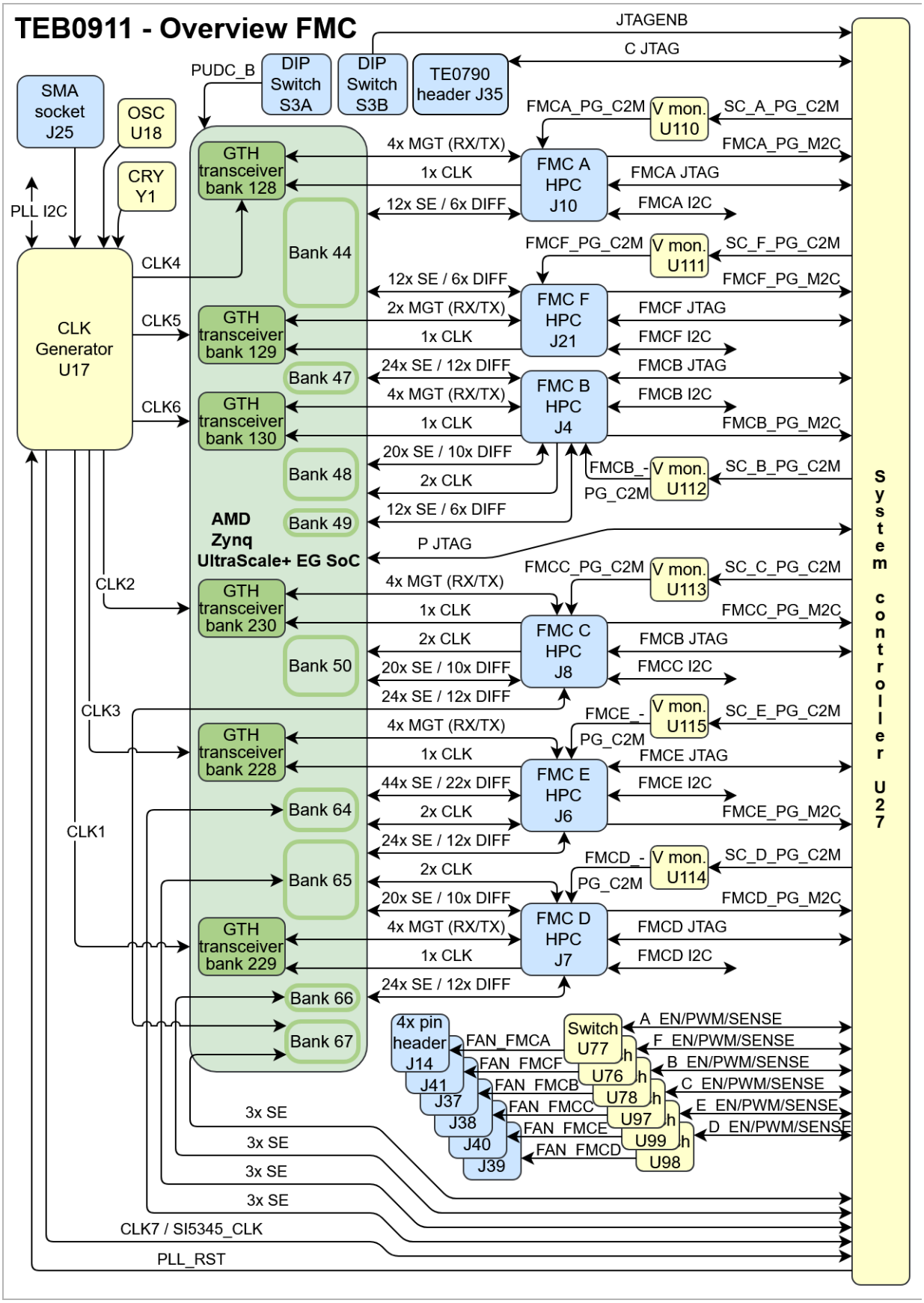
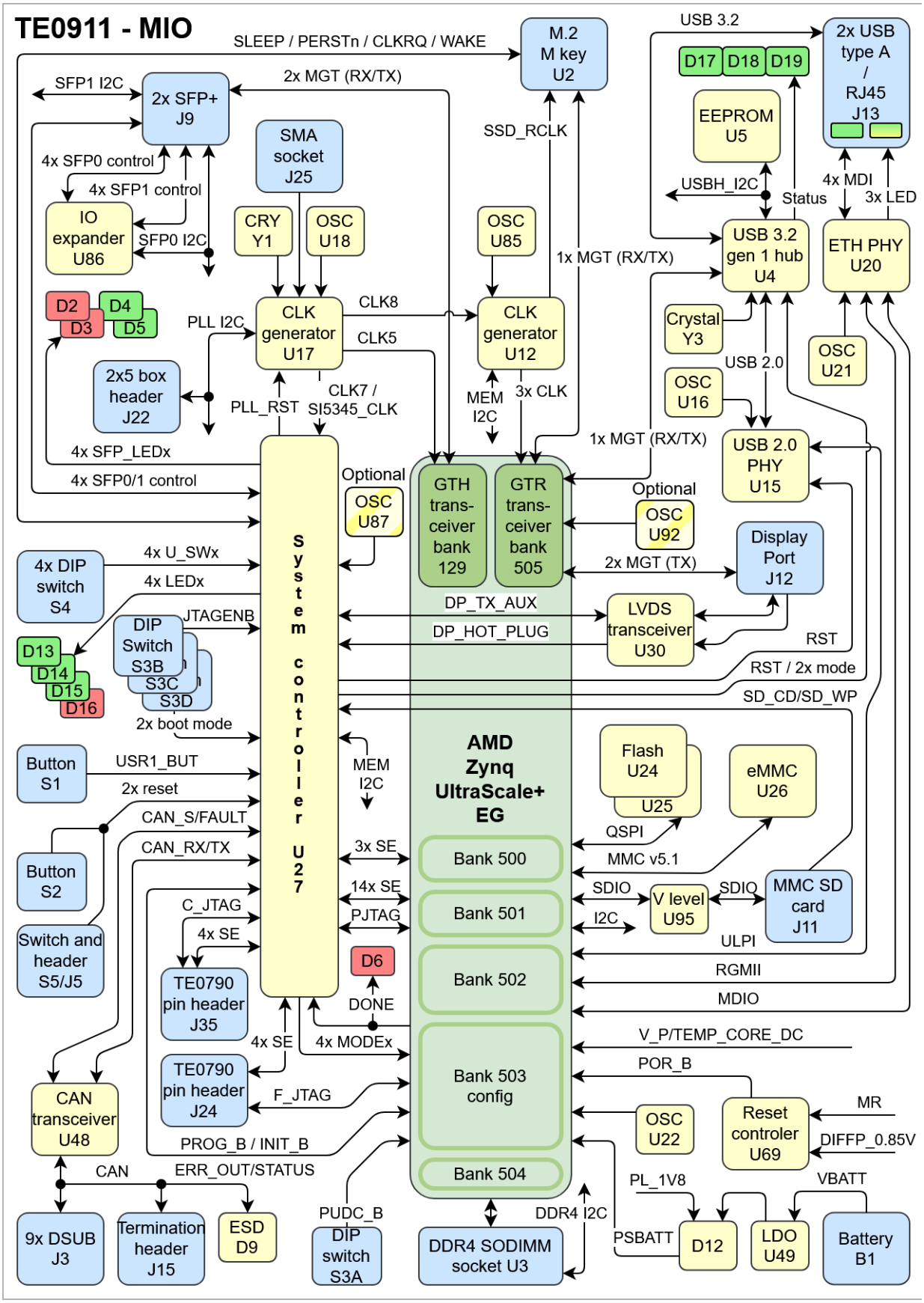
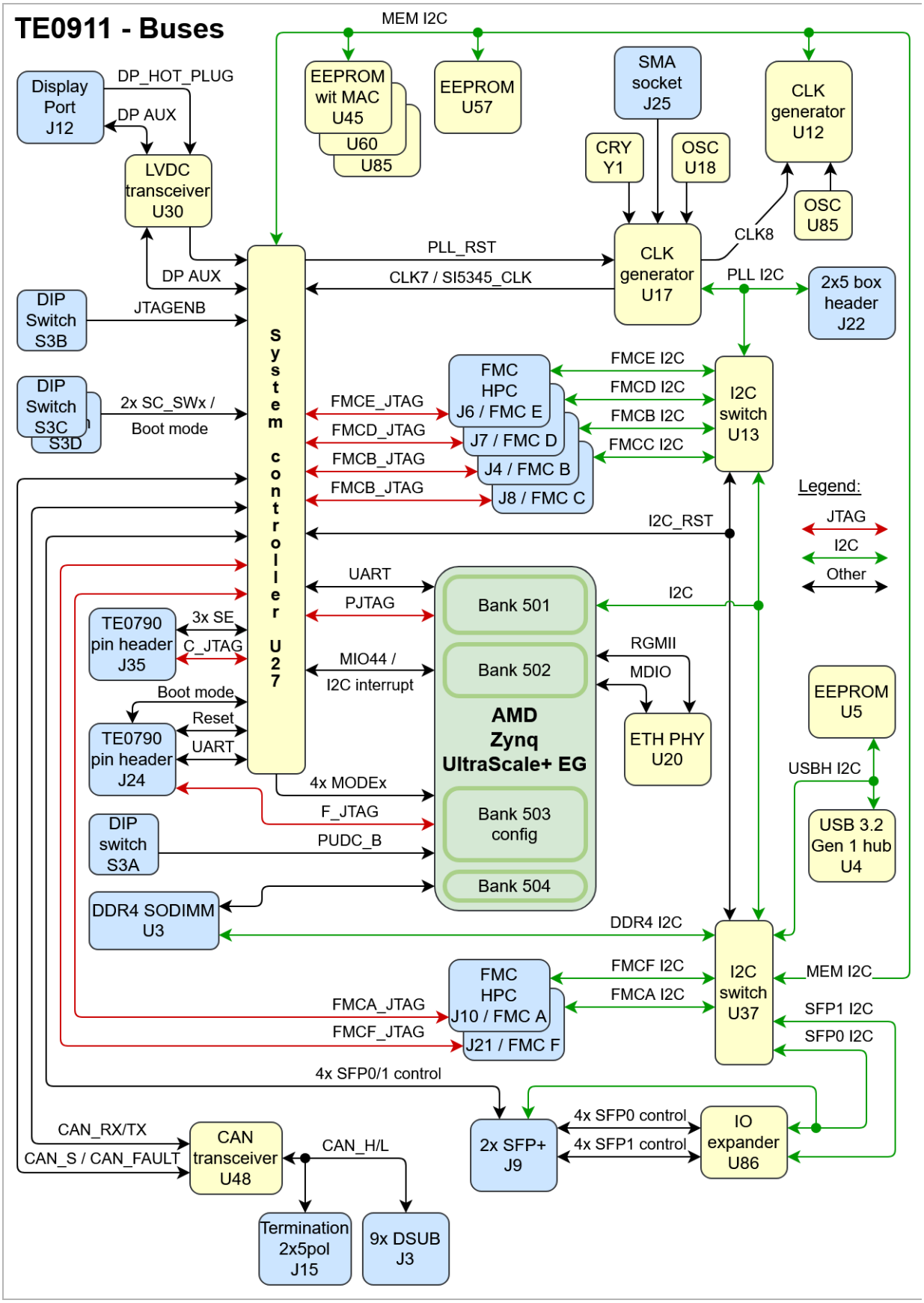


Figure 1: TEB0911 block diagram


TEB0911 - Overview FMC
JTAGENB
C JTAG
PUDC_B
DIP Switch S3A
DIP Switch S3B
TE0790 header J35
SMA socket J25
OSC U18
CRY Y1
PLL I2C
CLK Generator U17
CLK4
CLK5
CLK6
CLK2
CLK3
CLK1
GTH transceiver bank 128
GTH transceiver bank 129
GTH transceiver bank 130
GTH transceiver bank 230
GTH transceiver bank 228
GTH transceiver bank 229
Bank 44
Bank 47
Bank 48
Bank 49
Bank 50
Bank 64
Bank 65
Bank 66
Bank 67
AMD Zynq UltraScale+ EG SoC
FMC A HPC J10
FMC F HPC J21
FMC B HPC J4
FMC C HPC J8
FMC E HPC J6
FMC D HPC J7
FMCA_PG_C2M
V mon. U110
SC_A_PG_C2M
FMCA_PG_M2C
FMCA JTAG
FMCA I2C
FMCF_PG_C2M
V mon. U111
SC_F_PG_C2M
FMCF_PG_M2C
FMCF JTAG
FMCF I2C
FMCB JTAG
FMCB I2C
FMCB_PG_M2C
FMCB_PG_C2M
V mon. U112
SC_B_PG_C2M
P JTAG
FMCC_PG_C2M
V mon. U113
SC_C_PG_C2M
FMCC_PG_M2C
FMCB JTAG
FMCC I2C
FMCE_PG_C2M
V mon. U115
SC_E_PG_C2M
FMCE JTAG
FMCE I2C
FMCE_PG_M2C
FMCD_PG_C2M
V mon. U114
SC_D_PG_C2M
FMCD_PG_M2C
FMCD JTAG
FMCD I2C
4x MGT (RX/TX)
1x CLK
12x SE / 6x DIFF
2x MGT (RX/TX)
24x SE / 12x DIFF
20x SE / 10x DIFF
2x CLK
44x SE / 22x DIFF
4x pin header J14
J41
J37
J38
J40
J39
FAN_FMCA
FAN_FMCF
FAN_FMCB
FAN_FMCC
FAN_FMCE
FAN_FMCD
Switch U77
U76
U78
U97
U99
U98
A_EN/PWM/SENSE
F_EN/PWM/SENSE
B_EN/PWM/SENSE
C_EN/PWM/SENSE
E_EN/PWM/SENSE
D_EN/PWM/SENSE
3x SE
CLK7 / SI5345_CLK
PLL_RST
System controller U27



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TE0911 - Buses
MEM I2C
Display Port J12
DP_HOT_PLUG
DP AUX
LVDC transceiver U30
EEPROM wit MAC U45
U60
U85
EEPROM U57
SMA socket J25
CRY Y1
OSC U18
CLK generator U12
OSC U85
CLK8
PLL_RST
CLK7 / SI5345_CLK
CLK generator U17
PLL I2C
2x5 box header J22
DP AUX
DIP Switch S3B
JTAGENB
DIP Switch S3C
S3D
2x SC_SWx / Boot mode
System controller U27
FMCE_JTAG
FMCD_JTAG
FMCB_JTAG
FMCB_JTAG
FMC HPC J6 / FMC E
J7 / FMC D
J4 / FMC B
J8 / FMC C
FMCE I2C
FMCD I2C
FMCB I2C
FMCC I2C
I2C switch U13
Legend:
JTAG
I2C
Other
I2C_RST
UART
PJTAG
MIO44 / I2C interrupt
Bank 501
Bank 502
AMD Zynq UltraScale+ EG
Bank 503 config
Bank 504
I2C
RGMII
MDIO
ETH PHY U20
EEPROM U5
USBH I2C
USB 3.2 Gen 1 hub U4
TE0790 pin header J35
3x SE
C_JTAG
Boot mode
Reset
UART
TE0790 pin header J24
4x MODEx
F_JTAG
PUDC_B
DIP switch S3A
DDR4 SODIMM U3
DDR4 I2C
FMCF I2C
FMCA I2C
FMC HPC J10 / FMC A
J21 / FMC F
FMCA_JTAG
FMCF_JTAG
I2C switch U37
MEM I2C
SFP1 I2C
SFP0 I2C
4x SFP0/1 control
2x SFP+ J9
4x SFP0 control
4x SFP1 control
IO expander U86
CAN_RX/TX
CAN_S / CAN_FAULT
CAN transceiver U48
CAN_H/L
Termination 2x5pol J15
9x DSUB J3

4.3 Main Components

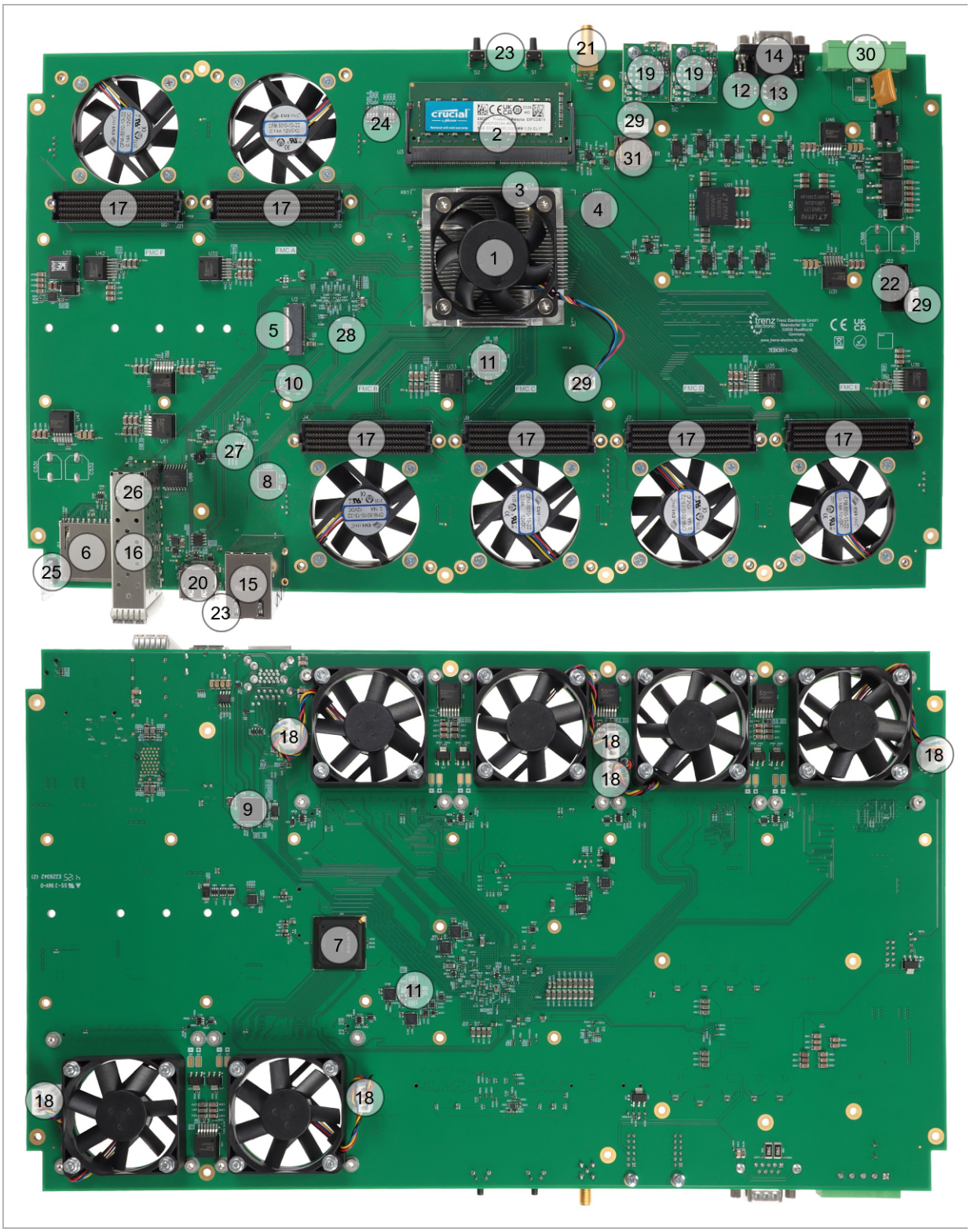


Figure 2: TEB0911 main components

1. SoC, U1
2. DDR4 SODIMM socket, U3

3. QSPI flashes U24, 25
4. eMMC U26
5. M.2 socket, U2
6. MMC SD socket, J11
7. System controller, U27
8. ETH PHY, U20
9. USB 3.2 hub, U4
10. USB 2.0 PHY, U15
11. CLK generators, U12, U17
12. CAN transceiver, U48
13. CAN termination 2x3 pin header, J15
14. CAN 9x DSUB socket, J3
15. RJ45 ETH and 2x USB 3.0 type A header, J13
16. 2x SFP+ slot, J9
17. FMC HPC connectors, J4, J6, J7, J8, J10, J21
18. FMC PWM 5/12 V fan connectors, J37, J40, J37, J38, J14, J41
19. Programming adapters (TE0790), J24, J35
20. DisplayPort, J12
21. SMA connector - CLK input to U17, J25
22. PLL I2C Header, J22
23. Buttons, S1, S2, S5
24. DIP switches, S3, S5
25. LEDs user, D13, D14, D15, D16
26. LEDs SFP+ status, D2, D3, D4, D5
27. LEDs USB 3. hub status, D17, D18, D19
28. LED SoC status, D6
29. PWM fan 12 V connectors, J2, J23, J33
30. Power Jack 24 V, J1
31. Battery Holder (CR1220/3 V), B1

4.4 Initial Delivery State

Storage device name	Designator	Content	Notes
SoC	U1	Not programmed	
System Controller	U27	Firmware	For further information see TEB0911 CPLD Firmware / TEB0911 CPLD.
QSPI Flash	U24 / U25	Not programmed	
e.MMC	U26	Not programmed	

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Storage device name	Designator	Content	Notes
EEPROM	U5	Hub configuration	**Do not overwrite**
EEPROM	U57	Not programmed	
EEPROM with MAC	U15 / U60 / U85	MAC is burned-in by the manufacturer.	
Programmable Clock Generator	U12 / U17	Not programmed	For further information see TEB0911 Reference Design.
TE0790 / Programming adapter	J24 / J35	Firmware	For further information see TE0790 TRM.

Table 1: Initial delivery state of programmable devices

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5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO count	Notes
FMC HPC	J4	IO	56x SE / 28x DIFF	
FMC HPC	J4	GTH	4x MGT (RX/TX)	
FMC HPC	J4	GTH CLK	1x DIFF	
FMC HPC	J6	IO	68x SE / 34x DIFF	
FMC HPC	J6	IO CLK	2x DIFF	
FMC HPC	J6	GTH	4x MGT (RX/TX)	
FMC HPC	J6	GTH CLK	1x DIFF	
FMC HPC	J7	IO	44x SE / 22x DIFF	
FMC HPC	J7	IO CLK	2x DIFF	
FMC HPC	J7	GTH	4x MGT (RX/TX)	
FMC HPC	J7	GTH CLK	1x DIFF	
FMC HPC	J8	IO	44x SE / 22x DIFF	
FMC HPC	J8	IO CLK	2x DIFF	
FMC HPC	J8	GTH	4x MGT (RX/TX)	
FMC HPC	J8	GTH CLK	1x DIFF	
FMC HPC	J10	IO	12x SE / 6x DIFF	

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Connector Type	Designator	Interface	IO count	Notes
FMC HPC	J10	GTH	4x MGT (RX/TX)	
FMC HPC	J10	GTH CLK	1x DIFF	
FMC HPC	J21	IO	12x SE / 6x DIFF	
FMC HPC	J21	GTH	2x MGT (RX/TX)	
FMC HPC	J21	GTH CLK	1x DIFF	
DDR4 SODIMM	U3	DDR4	76x SE and 68x DIFF	
ETH	J13	RGMII/MDI	12x SE via PHY to 4x DIFF	
USB 2.0	ULPI	12x SE		
MMC SD card	J11	SDIO	6x SE	
USB 3.2 Type A	J13	GTR	1x MGT (RX/TX)	
M.2 M Key PCIe	U2	GTR	1x MGT (RX/TX)	
DisplayPort	J12	GTR	2x MGT (TX)	
SFP+	J9A	GTH	1x MGT (RX/TX)	
SFP+	J9B	GTH	1x MGT (RX/TX)	
CAN	J3/J15	CAN	4x SE	System controller IO.
2x5 box header	J22	I2C	2x SE	

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Connector Type	Designator	Interface	IO count	Notes
TE0790 / USB 2.0	J24	JTAG	4x SE	Connected to the SoC.
TE0790 / USB 2.0	J24	UART	2x SE	Connected to the SoC.
TE0790 / USB 2.0	J35	JTAG	2x SE	Connected to the system controller.
TE0790 / USB 2.0	J35	IO	3x SE	Connected to the system controller.

Table 2: Board connectors

5.2 Test Points

Test Point	REV05			REV04 Signal	REV03/ REV02 Signal	Notes
	Top	Bottom	Signal			
TP1	x	-	DP_HOT_PLUG			
TP2	x	-	FMCA_3V3			
TP3	x	-	FMCB_3V3			
TP4	x	-	FMCC_3V3			
TP5	x	-	FMCD_3V3			
TP6	x	-	FMCE_3V3			
TP7	x	-	FMCAF_1V8			
TP8	x	-	FMCBC_1V8			

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Test Point	REV05			REV04 Signal	REV03/ REV02 Signal	Notes
	Top	Bottom	Signal			
TP9	x	-	FMCDE_1V8			
TP10	x	-	FMCF_3V3			
TP11	x	-	24V_FUSED			
TP12	x	-	SFP_SSD			
TP13	x	-	PG_3V3SB	DDR_1V2		
TP14	x	-	5V			
TP15	x	-	PSBATT			
TP16	x	-	3V3SB			
TP17	x	-	PG_VPP_SPD	PL_GT2_1V35		
TP18	x	-	DP_TX_PWR			
TP19	x	-	AVTT_L			
TP20	x	-	VPP_SPD	PL_GT2_1V05		

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Test Point	REV05			REV04 Signal	REV03/ REV02 Signal	Notes
	Top	Bottom	Signal			
TP21	x	-	AUX_L			
TP22	x	-	AVCC_L			
TP23	x	-	PL_GT_1V4	PL_GT_1V35		
TP24	x	-	AVTT_R			
TP25	x	-	AUX_R			
TP26	x	-	PL_GT_1V14	PL_GT_1V05		
TP27	x	-	AVCC_R			
TP28	x	-	PS_GT_1V14	PS_GT_1V05		
TP29	x	-	PS_AVCC			
TP30	x	-	PS_AVTT			
TP31	x	-	PS_AUX			
TP32	x	-	PS_1V8			

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Test Point	REV05			REV04 Signal	REV03/ REV02 Signal	Notes
	Top	Bottom	Signal			
TP33	x	-	USB0_ID			
TP34	x	-	PL_GT2_1V4	DCDC_2V0		
TP35	x	-	PS_PLL			
TP36	x	-	3.3V_SD		Not used	
TP37	x	-	FP_0V85			
TP38	x	-	DDR_PLL			
TP39	x	-	5V_SYS_PL			
TP40	x	-	5V_SYS_PS			
TP41	x	-	PG_1.2V	Not used		
TP42	x	-	PL_GT2_1V14	Not used		
TP43	x	-	DCDC_2V0	PL_1V8		
TP44	x	-	DDR_1V2	VPP_SPD		

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Test Point	REV05			REV04 Signal	REV03/ REV02 Signal	Notes
	Top	Bottom	Signal			
TP45	x	-	3.3V			
TP46	x	-	1.2V			
TP47	x	-	PG_PL_1V8	Not used		
TP48	x	-	PL_1V8	Not used		
TP49	-	-	Not used			
TP50	-	-	Not used			
TP51	x	-	AVDD_CORE			
TP52	x	-	VCCINT_0V85			

Table 3: Test points information

6 On-board Peripherals

Chip / Interface	Designator	Connected to	Notes
SoC	U1	• QSPI flashes U24, U25 • eMMC U26 • ETH PHY U20 • USB 3.2 Hub U4 • USB 2.0 PHY U15 • I2C • MMC SD socket J11 • ETH and 2x USB 3.0 Type A header J13 • 2x SFP+ slot, J9 • M.2 socket U2 • DisplayPort J12 • FMC HPC connectors J4, J6, J7, J8, J10, J21 • Programming adapters J24 • Optional: OSC U92 • LED status D6	

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Chip / Interface	Designator	Connected to	Notes
System controller	U27	• SoC U1 • I2C switches U13, U37 • ETH PHY U20 • USB 3.2 Hub U4 • USB 2.0 PHY U15 • DisplayPort AUX LVDS transceiver U30 • FMC HPC connectors J4, J6, J7, J8, J10, J21 • CAN transceiver U48 • I2C • Buttons S1, S2, S5 • DIP switches S3, S5 • User LEDs D13, D14, D15, D16 • SFP+ status LEDs D2, D3, D4, D5 • Programming adapters J24, J35 • Optional: OSC U87	
Programming adapters	J24 / J35	• SoC U1 • System controller U27	For further information see TE0790 TRM.
QSPI Flash	U24 / U25	• SoC U1	

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Chip / Interface	Designator	Connected to	Notes
e.MMC	U26	• SoC U1	
I2C switches	U13 / U37	• SoC U1 • System controller U27 • EEPROM U57 • EEPROM with MAC U45, U60, U85 • EEPROM for USB 3.2 Hub U5 • USB 3.2 Hub U4 • SFP+ slot J9 • SFP+ IO expander U86 • CLK generators U12, U17 • FMC HPC connectors J4, J6, J7, J8, J10, J21 • PLL I2C Header J22	
ETH PHY	U20	• SoC U1 • OSC U21 • Header J13	
USB 3.2 Hub	U4	• SoC PS GTR bank 505 • System controller U27 • USB 2.0 PHY U15 • EEPROM U5 • LED status D17 • Crystal Y3 • Header J13 • I2C	

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Chip / Interface	Designator	Connected to	Notes
USB 2.0 PHY	U15	• SoC PS • System controller U27 • USB 3.2 Hub U4 • OSC U16	
CAN transceiver	U48	• System Controller U27 • DSUB J3 • Termination header J15	
Programmable CLK generator	U12	• SoC U1 • M.2 socket • OSC U85 • I2C	For further information see TEB0911 Reference Design.
Programmable CLK generator	U17	• FMC HPC J4, J6, J7, J8, J10, J21 • I2C • Crystal Y1 • OSC U18 • SMA socket J25 • I2C	For further information see TEB0911 Reference Design.
Crystal	Y1	• Programmable CLK generator U17	54 MHz
Crystal	Y3	• USB 3.2 Hub U4	26 MHz
Oscillator	U22	• SoC U1	33⅓ MHz

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Chip / Interface	Designator	Connected to	Notes
Oscillator	U85	• Programmable CLK generator U17	25 MHz
Oscillator	U18	• Programmable CLK generator U12	25 MHz
Oscillator	U21	• ETH PHY U20	25 MHz
Oscillator	U16	• USB 2.0 PHY U15	52 MHz
Oscillator	U87	• System controller U27	Optional, 25 MHz
Oscillator	U92	• SoC U1	Optional, 100 MHz

Table 4: On-board peripherals

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7 Configuration and System Control Signals

Control signals represent hardware defined logic states, for final state consider the firmware and reference designs.

7.1 Control Signals and Buses

Signal Name	Connector.Pin	Direction [1)]	Description
PUDC_B	S3A.8	IN	Set IO pull-ups state during configuration.
JTAGENB	S3B.7	IN	Enable system controller JTAG interface.
SC_SW1 / SC_SW2	S3C.6 / S3D.5	IN	Set SoC boot source.
USR_BUT1	S1	IN	User definable.
USR_BUT2	S2	IN	System reset.
USR_BUT3	S5	IN	System reset.
M.2 (SSD1_SLEEP / SSD1_PERSTn / SSD1_CLKRQ / SSD1_WAKE)	U2.38 / U2.50 / U2.52 / U2.54	Signal dependent	
FMCB_PRSNT / FMCE_PRSNT / FMCD_PRSNT / FMCC_PRSNT / FMCA_PRSNT / FMCF_PRSNT /	J4.H2 / J6.H2 / J7.H2 / J8.H2 / J10.H2 / J21.H2	IN	FMC module presence detection.
FMCB_PG_M2C / FMCE_PG_M2C / FMCD_PG_M2C / FMCC_PG_M2C / FMCA_PG_M2C / FMCF_PG_M2C /	J4.F1 / J6.F1 / J7.F1 / J8.F1 / J10.F1 / J21.F1	IN	FMC module power good signal to carrier.

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Signal Name	Connector.Pin	Direction [1)]	Description
FANs FMC (FMCB_SENSE / FMCE_SENSE / FMCD_SENSE / FMCC_SENSE / FMCA_SENSE / FMCF_SENSE)	J37.3 / J40.3 / J39.3 / J38.3 / J14.3 / J41.3	IN	Fan speed signals.
FANs FMC (FMCB_PWM / FMCE_PWM / FMCD_PWM / FMCC_PWM / FMCA_PWM / FMCF_PWM)	J37.4 / J40.4 / J39.4 / J38.4 / J14.4 / J41.4	OUT	Fans PWM signals.
Fans system (F1_EN / F2_EN / F3_EN)	J2.2 / J23.2 / J33.2	OUT	Enable 12 V to fan.
Fans system (F1SENSE / F2SENSE / F3SENSE)	J2.3 / J23.3 / J33.3	IN	Fan speed signal from fans.
Fans system (F1PWM / F2PWM / F3PWM)	J2.4 / J23.4 / J33.4	OUT	Fan speed control signals.
IN1_P / CLK_PLL_IN	J25.1	IN	Clock input to programmable clock generator U17.
I2C (PLL_SCL / PLL_SDA)	J22.3 / J22.7	Signal dependent	
I2C (FMCB_SCL / FMCB_SDA)	J4.C30 / J4.D35	Signal dependent	
I2C (FMCE_SCL / FMCE_SDA)	J6.C30 / J6.D35	Signal dependent	
I2C (FMCD_SCL / FMCD_SDA)	J7.C30 / J7.D35	Signal dependent	

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Signal Name	Connector.Pin	Direction [1)]	Description
I2C (FMCC_SCL / FMCC_SDA)	J8.C30 / J8.D35	Signal dependent	
I2C (FMCA_SCL / FMCA_SDA)	J10.C30 / J10.D35	Signal dependent	
I2C (FMCF_SCL / FMCF_SDA)	J21.C30 / J21.D35	Signal dependent	
JTAG (FMCB_TCK / FMCB_TMS / FMCB_TDI / FMCB_TDO)	J4.D29 / J4.D33 / J4.D30 / J4.D31	Signal dependent	
JTAG (FMCE_TCK / FMCE_TMS / FMCE_TDI / FMCE_TDO)	J6.D29 / J6.D33 / J6.D30 / J6.D31	Signal dependent	
JTAG (FMCD_TCK / FMCD_TMS / FMCD_TDI / FMCD_TDO)	J7.D29 / J7.D33 / J7.D30 / J7.D31	Signal dependent	
JTAG (FMCC_TCK / FMCC_TMS / FMCC_TDI / FMCC_TDO)	J8.D29 / J8.D33 / J8.D30 / J8.D31	Signal dependent	
JTAG (FMCA_TCK / FMCA_TMS / FMCA_TDI / FMCA_TDO)	J10.D29 / J10.D33 / J10.D30 / J10.D31	Signal dependent	
JTAG (FMCF_TCK / FMCF_TMS / FMCF_TDI / FMCF_TDO)	J21.D29 / J21.D33 / J21.D30 / J21.D31	Signal dependent	

Table 5: Control signals and buses

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.
- INOUT: Bidirectional signal.
- Signal dependent: The signal direction depends on the function within the bus.

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7.2 Jumpers

Jumper	Net name / Connector.pin		
Header	**Output**	**Input**	**Notes**
J15	CAN_L / J15.3	J15.1	
	CAN_H / J15.4	J15.2	

Table 6: Jumpers

7.3 Buttons

Button		Voltage level		Function
	Signal	**Low**	**high**	
S1	USR_BUT1	pressed	unpressed	User defined
S2	USR_BUT2	pressed	unpressed	Main power reset button. Restarts power management.
S5 / J5	USR_BUT3	pressed	unpressed	Reset signal.

Table 7: Buttons

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7.4 DIP switches

DIP switch group	DIP switch	Signal name / Connector.pin	Description
S3	S3A	PUDC_B / S3.8	Determines I/O pull-ups activation during configuration.
	S3B	JTAGENB / S3.7	Enable JTAG access to the system controller.
	S3C	SC_SW1 / S3.6	Set SoC boot mode.
	S3D	SC_SW2 / S3.5	
S4	S4A	U_SW1 / S4.8	User definable.
	S4B	U_SW2 / S4.7	
	S4C	U_SW3 / S4.6	
	S4D	U_SW4 / S4.5	

Table 8: DIP switches

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8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name / Schematic Name	Description	Connector.Pin	Direction [1)]	Notes
24V / 24V_FUSED	Board supply.	J1.2	IN	
VBATT	SoC backup supply.	B1.+	IN	
12V / 12V_FMC_AF	FMC 12 V supply	J4.C35 / J4.C37 / J6.C35 / J6.C37 / J7.C35 / J7.C37 / J8.C35 / J8.C37 / J10.C35 / J10.C37 / J21.C35 / J21.C37	OUT	
3V3SB	FMC 3.3 V auxiliary supply.	J4.D32 / J6.D32 / J7.D32 / J8.D32 / J10.D32 / J21.D32	OUT	
FMCB_3V3 / FMCE_3V3 / FMCD_3V3 / FMCC_3V3 / FMCA_3V3 / FMCF_3V3	FMC 3.3 V supply.	J4.D36 / J4.D38 / J4.D40 / J4.D39 / J6.D36 / J6.D38 / J6.D40 / J6.D39 / J7.D36 / J7.D38 / J7.D40 / J7.D39 / J8.D36 / J8.D38 / J8.D40 / J8.D39 / J10.D36 / J10.D38 / J10.D40 / J10.D39 / J21.D36 / J21.D38 / J21.D40 / J21.D39	OUT	

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Power Rail Name / Schematic Name	Description	Connector.Pin	Direction [1)]	Notes
FMCB_1V8 / FMCE_1V8 / FMCD_1V8 / FMCC_1V8 / FMCA_1V8 / FMCF_1V8	FMC 1.8 V voltage supply.	J4.H40 / J4.G39 / J4.F40 / J4.E39 / J6.H40 / J6.G39 / J6.F40 / J6.E39 / J7.H40 / J7.G39 / J7.F40 / J7.E39 / J8.H40 / J8.G39 / J8.F40 / J8.E39 / J10.H40 / J10.G39 / J10.F40 / J10.E39 / J21.H40 / J21.G39 / J21.F40 / J21.E39	IN	
FAN_FMCB / FAN_FMCE / FAN_FMCD / FAN_FMCC / FAN_FMCA / FAN_FMCF	FMC fan 5 V supply.	J37.2 / J40.2 / J39.2 / J38.2 / J14.2 / J41.2	OUT	Option for 12 V via zero Ohm resistors.
12V	SoC/Systems fans 12 V supply.	J2.2 / J23.2 / J33.2	OUT	

Table 9: Power rails

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

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8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
0	-	-	-	Configuration SoM signal setup.	See Configuration and System Control Signals and chapter power from the firmware description.
1	24V	22.8 V to 25.2 (24 V ±5 %)	-	Apply board supply.	

Table 10: Power sequencing

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9 Board to Board Connectors

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10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Warning!
The listed values ONLY reflect this board. Connected Carriers / SoMs / Boards are not considered.

Power Rail Name / Schematic Name	Description	Min	Max	Unit	Notes
24V / 24V_FUSED	Board supply.	0	33.3	V	
VBATT	SoC backup supply	–0.3	6.0	V	

Table 11: Absolute maximum ratings

*) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Condition". Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

10.2.1 Temperature range

Trenz Electronic classifies modules into temperature range categories by subsumption of its component data (PCB, ICs, connectors, passive components). The temperature ranges are values for ambient air temperature and do not reflect the junction temperature of individual components.

The categories are:

- Modules with commercial (C) temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 70 °C.
- Modules with extended (E) temperature grade are equipped with components that cover at least the ambient temperature range of 0 °C to 85 °C.
- Modules with industrial (I) temperature grade are equipped with components that cover at least the ambient temperature range of -40 °C to 85 °C.

These categories do not take into account the entire custom system consisting of:

- Customer SoC design. The allowed main SoC temperature range is specified from the vendor by junction temperature using corresponding classes (C, E, I). See vendor documentation.
- Cooling solution, active and or passive cooling.
- Climate or environmental conditions besides ambient temperature range.
- Module orientation, neighbouring assemblies, neither other heat sources nor the SoC as heat source to other components.

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The temperature of individual components should not exceed the specified range due to self-heating or heating by adjacent components. The actual operating temperature range will depend on the customer design, usage, environment and cooling solution. Consult Cooling Solutions for more information.

10.2.2 Voltage rails

The following table aims to be generic for all variants. The voltage ranges are consistent across assembly variants, but exceptions are possible (custom request).

Power Rail Name/ Schematic Name	Min	Max	Units	Notes
24V / 24V_FUSED	22.8	25.2	V	
VBATT	2.2	5.5	V	

Table 12: Recommended operating conditions

10.3 Physical Dimensions

- Module size: 234.0 mm x 406.0 mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 1.946 mm ±10 %.

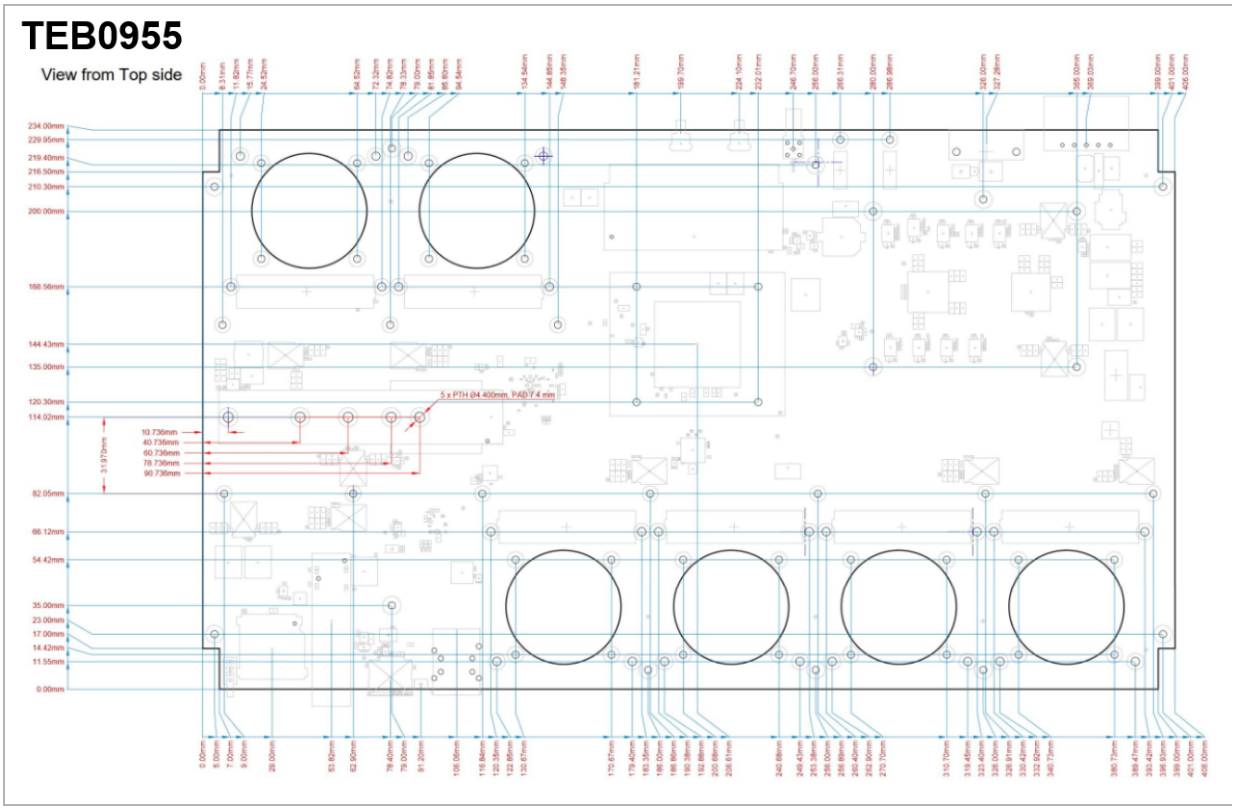


Figure 3: Physical dimension

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11 Currently Offered Variants

Trenz shop TEB0911 overview page*	
English page	German page

Table 13: Trenz Electronic shop overview

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12 Revision History

12.1 Hardware Revision History

The hardware revision number can be found on the PCB board together with the module's model number, separated by a dash.



Figure 4: Board hardware revision number

Date	Revision	Changes	Documentation Link
2025-10	05	1. DCDC U50, U84, U72, U80 were replaced with MPM3834CGPA. 2. DCDC U52, U55, U58, U62, U70, U79, U74, U64, U66 were replaced with MPM3860GQW. 3. Oscillator Y2 schematic is fixed. 4. R49, R283, R328 (4k99) replace by 100R 5. Protection diode D20 is added. 6. Change R92 to 220R (22767) 7. All FMC Fans M1 - M6 were replaced with CFM-5010-13-22 (30961) 50 x 50 mm. 8. Added connectors J14, J37 – J41 and transistors T1A – T6A . 9. Added signals FMCA_PWM – FMCC_PWM , which go from the CPLD and are intended for controlling fan speed. 10. Added signals FMCA_SENSE – FMCF_SENSE , which go to the CPLD and are intended for receiving signals from internal sensors. 11. Added parts JX1 - JX6 and contacts CONT1 - CONT24 . 12. Component S/N is removed. 13. Added pull-up R377 - R380 on MIO2 , MIO3 , MIO10 , MIO11 . 14. Added capacitors C699 - C705 to improve 3.3V_SD power rail stability. 15. Signals PHY_LED0 - PHY_LED2. LED_1A, LED_2A, LED_2B are removed from SC. 16. Renamed signals PHY_LED0 -> ETH0_LINK_ACTn, PHY_LED1 -> ETH0_LINK_MIDn, PHY_LED2 -> ETH0_LINK_MAXn. 17. Added Ethernet LED Buffers U103A - U105A . 18. Resistor R17 changed 1K -> 2.2K. 19. DDR_PG renamed to PG_DDR_1V2. 20. Added FMC Power supervisors U110 - U115 to meet FMC standard. 21. FMCA_PG_C2M - FMCF_PG_C2M disconnected from SC and connected to U110 - U115 . 22. Added signals SC_A_PG_C2M - SC_F_PG_C2M from SC to U110 - U115 to enable these supervisors. 23. Added diodes D21 - D26 to protect MR inputs of U110 - U115 .	REV05 PCN

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Date	Revision	Changes	Documentation Link
		24. PL_GT2_1V05 increased to PL_GT2_1V14. 25. PL_GT2_1V35 increased to PL_GT2_1V4. 26. PL_GT_1V05 increased to PL_GT_1V14. 27. PL_GT_1V35 increased to PL_GT_1V4. 28. PS_GT_1V05 increased to PS_GT_1V14. 29. Power_overview and Power Up Sequence pages are updated. 30. U85 , component SiT8008AI-73-XXS-25.000000E got status NRND. It is replaced with SiT8008BI-73-XXS-25.000000E. 31. NRND components U28 , U68 , U88 AOZ8808DI-03 are replaced with AOZ8S311UD4-03. 32. Connector J13 replaced with 2250576-1. The replaced transformer is corresponding to Ethernet PHY MDI interface. 33. Ethernet status LEDs are changed: J13D Yellow -> Green J13E Orange -> Yellow	

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Date	Revision	Changes	Documentation Link
2019-03	04	1. Signals C_LA27_P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC_67), C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC_67) 2. Added SDIO level translator TXS02612RTWR (U95) and 33Ω series resistors on SDIO lines from FPGA side. 3. Added user button S5 and jumper J5 (connected to U27 pin W17). 4. New fan switches U76-78/U97-99: BTS4141N. 5. New fans: AFB04512MA. Was added an option to use 5V or 12V (default) power rail. 6. Replaced EOL components: • TPS27082LDDCR -> TPS22918DBVT (U96) • ESD3V3U4ULCE6327XTSA1 -> AOZ8808DI-03 (U28) 7. New SFP+ connector: 2007492-5 instead of 1-2007492-5. 8. Resistor R65 (USB VBUS) replaced by 1K. 9. Resistors R285, R330, R226 are DNP. 10. S/N 27230 is DNP. 11. Added a battery BAT1. 12. Added quartz Y4.	REV04 PCN PCN PCN
2017-12	03	1. Signals C_LA27_P/N swapped: C_LA27_P connected to pin R10 (IO_L11P_T1U_N8_GC_67), C_LA27_N connected to R9 (IO_L11N_T1U_N9_GC_67) of U1 (XCZU9EG-1FFVB1156). 2. Flash N25Q256A11E1240E changed to N25Q512A11G1240E.	REV03

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Date	Revision	Changes	Documentation Link
-	02	1. 2 CPLDs replaced with LCMXO2-7000HC-4FG484C (U27). 2. Single SFP connector removed. MGT lanes B129_TX/RX_1 connected to FMC F. 3. DCDC U45 (power supply of 2xSFP and 1xSFP connectors) removed. 2xSFP powered by U11. 4. HDMI: lane B505_TX2 connected to DP1_TX and lane B505_TX3 to DP0_TX. 5. Supervisor U69 TPS3106E33 replaced with TPS3106E09. 6. U17 (Si5345): IN_SEL0/1 disconnected from CPLD and connected to GND. 7. Added new clock source U87 (SiT8008AI-73-XXS-25.000000E). Connected to CPLD. Not fitted. 8. I2C pull-ups R154/R155: changed from 4.7k to 1.5kOhm. 9. FAN: R285, R330, R260 changed to 27K (F*SENSE). 10. Added fuse F2 (4A). Fuse F1 (1.85A) "not fitted". 11. C354 (PWR_IN_24V/GND) deleted. 12. Removed clock loop-back OUT9P/N - IN2P/N (U17, SI5345). 13. OUT7 (P) of U17 (clock source SI5345) connected to CPLD U27 Bank 5. 14. Signal SD Card detect SD_CD connected to CPLD, MIO45 connected to CPLD. 15. Signals FMC*_PG_C2M(M2C) pulled-up to 3V3SB (was FMC*_3V3). 16. CLK_OUT U15 (USB PHY), serial resistor value R13 changed from 33 to 0 Ohm. 17. EN5311QI: Cout value changed from 22uF to 10uF. 18. BOM optimisation. 19. Added connections from CPLD to FMC A and F (x_LA06_SC - x_LA33_SC). 20. Net EN_VCCINT connected also to DCDC U31 (5V_SYS_PL) and U46 (5V_SYS_PS). 21. Added 2 2kb EEPROM (U45/U43). 22. Added power-up sequencing. 23. MIO6 connected to CPLD.	REV02

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Date	Revision	Changes	Documentation Link
		24. Signals EN_SFP was renamed to EN_SFP_SSD, 12V_FMC was renamed to 12V_FMC_AF, FMC12V_PG to FMCAF_12V_PG. 25. Nets names F_LA02/03/04 was swapped.	
-	01	Initial release	REV01

Table 14: Hardware revision history

12.2 Document Change History

Date	Revision	Contributors	Description
2026-11-13	v.188	Kilian Jahn	• Updated to TRM template 4.3.9 • Updated to hardware revision 5
2024-03-04	v.186	Vadim Yunitski	• Figure 1: fixed Zynq to FMC IO count to 14
2019-08-27	v.184	John Hartfiel	• typo
2019-05-10	v.183	John Hartfiel	• correction of J8 Pin count description
2018-07-23	v.182	Ali Naseri	• Initial document
--	all	Ali Naseri , John Hartfiel , Kilian Jahn , Lars Reinhardt , Susanne Kunath , Vadim Yunitski	

Table 66: Document change history

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