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Schematics and other handouts serve for informational purposes only!

Drawn by	*
Checked by	*
Assembly variant	D2CX4-K
Created by	VY
Modified by	VY
Modified at	2021-05-20

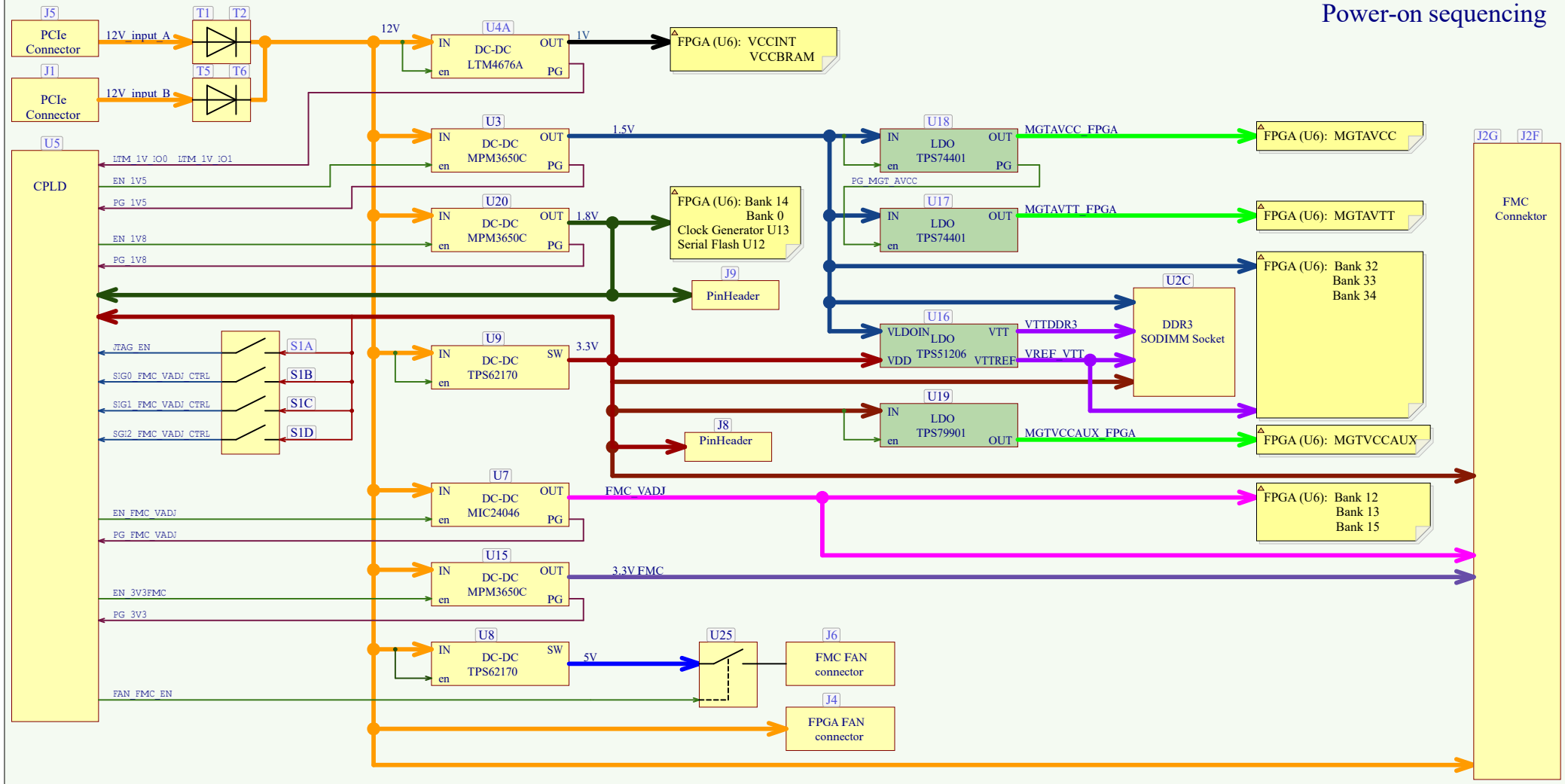


Title: TEF1001- Legal Notices		
A4	Number: TEF0001 D2CX4-K	Rev. 03
Date: 2022-06-08	Copyright: Trenz Electronic GmbH / TT	Page 1 of 34
Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	VT
-02	<p>1. Added capacitors C87 and C88, each 4.7µF.</p> <p>2. Increased the value of capacitor C154 from 27pF to 33pF.</p> <p>3. Power Input and Protection Enhancements:</p> <ul style="list-style-type: none"> - Routed 12V input from the PCIe edge connector. - Added input power protection circuits for both ATX 12V and PCIe edge connector, involving components U23 with T1, T2 and U24 with T5, T6, along with associated resistors and capacitors. - Introduced a power priority switch (T3) to prioritize ATX power. <p>4. Added switch S1 for selecting FMC_VADJ value and enabling JTAG (JTAG_EN).</p> <p>5. Added transistor T4 and resistors for reading the FMC_PRSNM_M2C signal.</p> <p>6. Added U25 and associated capacitors to support the FMC fan.</p> <p>7. Added screws for the bracket installation.</p> <p>8. Added 10 FPGA LEDs (D1-D10) controlled via level shifters (U11, U21, U22).</p> <p>9. Replaced the FAN model F455B-05MD (EOL) with F455B-05LD.</p>	<p>VT</p> <p>VY</p>
-03	<p>1. Removed the 4V power domain.</p> <p>2. Replaced U3 LTM4676AEY with the MPM3650CGQW regulator to manage the 1.5V power domain.</p> <p>3. Replaced U20 EN6347Q1 with the MPM3650CGQW regulator to manage the 1.8V power domain. The input supply switched from 4V to 12V.</p> <p>4. Replaced U15 EN6347Q1 with the MPM3650CGQW regulator to manage the 3V3FMC power domain. The input supply switched from 4V to 12V.</p> <p>5. Replaced U7 EN5365Q1 with the MIC24046YFL regulator to manage the FMC_VADJ power domain. The input supply switched from 4V to 12V. Added U26 and U27 74LVC1T45DW-7 transceivers. FMC_VADJ = 1.25V, 1.0V - 0.7V are not supported.</p> <p>6. Updated U17 and U18 TPS74401RGW BIAS supply voltage from 4V to 3.3V</p> <p>7. Updated U16 TPS51206DSQ VDD supply voltage from 4V to 3.3V.</p> <p>8. Connected U22 SN74AVC4T774RSVR pins B1 and B3 to GND to prevent floating input signals.</p> <p>9. Updated the BRx connection for board revision 03, Bank 14.</p> <p>10. CPLD Signal and Pinning Updates:</p> <ul style="list-style-type: none"> - PT12D (Pin 85): renamed net LTM_1V5_4V_IO0 to PG_1V5. - PT15B (Pin 83): removed net LTM_1V5_4V_IO1 (N/A). - PR2A (Pin 75): removed net LTM_4V_RUN (N/A). - PR2B (Pin 74): renamed net LTM_1V5_RUN to EN_1V5. - PR3A (Pin 71): renamed VID0_FMC_VADJ_CTRL to SIG0_FMC_VADJ_CTRL. - PR5C (Pin 63): renamed VID1_FMC_VADJ_CTRL to SIG1_FMC_VADJ_CTRL. - PR5D (Pin 62): renamed VID2_FMC_VADJ_CTRL to SIG2_FMC_VADJ_CTRL. - PR5A (Pin 64): reassigned LTM2_ALERT (N/A) to VOSET0_FMC_VADJ_A. - PR9B (Pin 57): reassigned VID2_FMC_VADJ to VOSET0_FMC_VADJ_DIR. - PR9C (Pin 54): reassigned VID1_FMC_VADJ to VOSET1_FMC_VADJ_A. - PR9D (Pin 53): reassigned VID0_FMC_VADJ to VOSET1_FMC_VADJ_DIR. <p>11. R33 resistor is not populated</p> <p>12. Added support for FPGA JTAG boot mode: U6 M2_0 is connected to CPLD PT15A (pin 84) via transceiver U28. Added Jumper J11 for boot mode selection.</p> <p>13. Replaced T1, T2, T5 and T6 transistors SiS444DN to SiS4604LDN.</p> <p>14. PCIe_PRSNM signal is disconnected from PCIe edge connector J1 pin B48 and connected to pin J1 B31 for PCIe x4 lane identification</p> <p>15. R31 is changed to pull-down resistor.</p> <p>16. All capacitors 100µF 10V X5R 20% 3216 (1206) changed to 100µF 6.3V X5R 20% 3216 (1206) (BOM optimisation)</p> <p>17. Changed resistor divider values R65, R71 and R77 (BOM optimisation)</p>	AH, VY, VG

	Title: TEF1001 - Revision History		
	A4	Number: TEF1001 D2CX4-K	Rev. 03
	Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 2 of 34
	Drawn by:	Filename: Revision_Changes.SchDoc	

Power-on sequencing

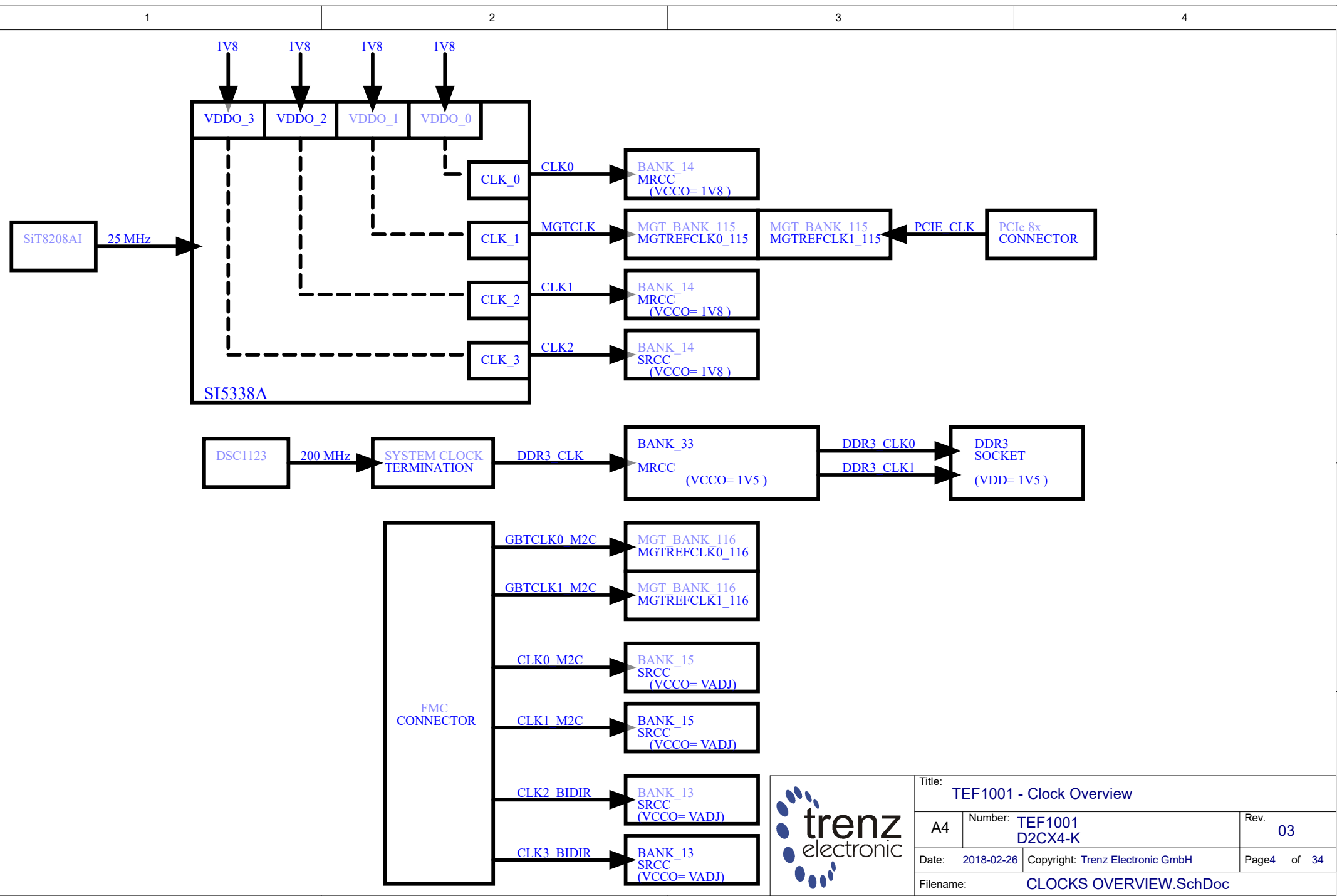


Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
12V_input_A	IN	12V	±10%	Micromodule Power	J5
12V_input_B	IN	12V	±10%	Micromodule Power	J1
1.8V	OUT	1.8V	±3%	FPGA JTAG Connector	J9
3.3V	OUT	3.3V	±3%	CPLD JTAG Connector	J8
5V	OUT	5V	±5%	FMC FAN Connector	J6
12V	OUT	12V	±10%	FPGA FAN Connector	J4



Title: TEF1001 - Power Diagram		
A4	Number: TEF0001 D2CX4-K	Rev. 03
Date: 08.01.2025	Copyright: Trenz Electronic GmbH / TT	Page 3 of 34
Filename: POWER_ENs_PGs OVERVIEW.SchDoc		

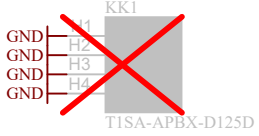


Title: TEF1001 - Clock Overview		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 4 of 34
Filename: CLOCKS OVERVIEW.SchDoc		

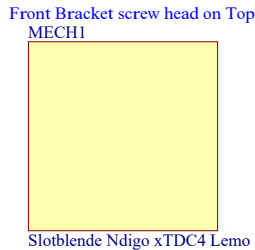
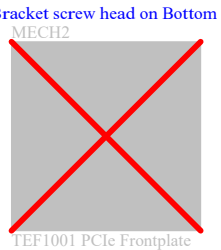
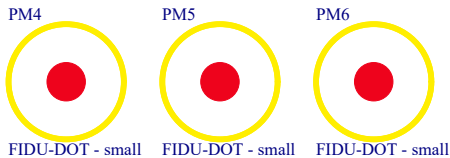
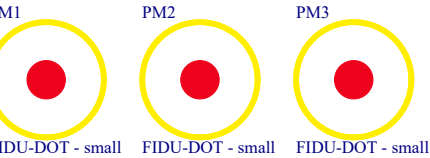
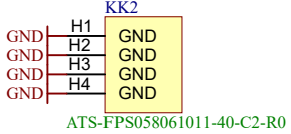
Special notes:

- U_FPGA
FPGA.SchDoc
- U_SODIMM
SODIMM.SchDoc
- U_CLOCK
CLOCK.SchDoc
- U_POWER
POWER.SchDoc
- U_CONN
CONN.SchDoc
- U_CPLD
CPLD.SchDoc
- U_CLOCKS OVERVIEW
CLOCKS OVERVIEW.SchDoc
- U_Legal Notices Modules
Legal Notices Modules.SchDoc
- U_Revision Changes
Revision_Changes.SchDoc

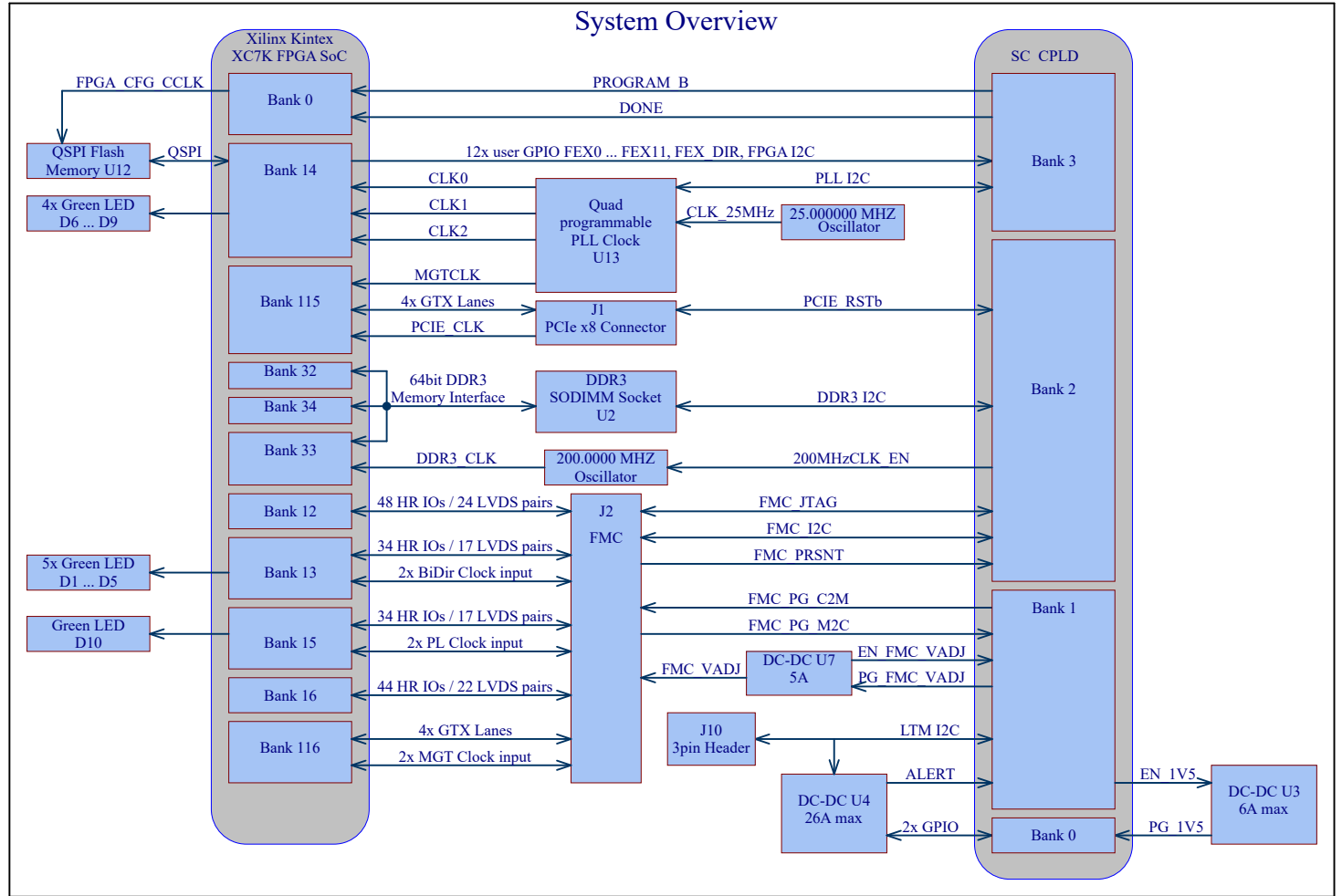
HEATSINK TYPE 1 (FPGA)



HEATSINK TYPE 2 (FPGA)



System Overview



Title: TEF1001 - MAIN		
A4	Number: TEF1001 D2CX4-K	Rev. 03
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Filename: TEF1001.SchDoc		

U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

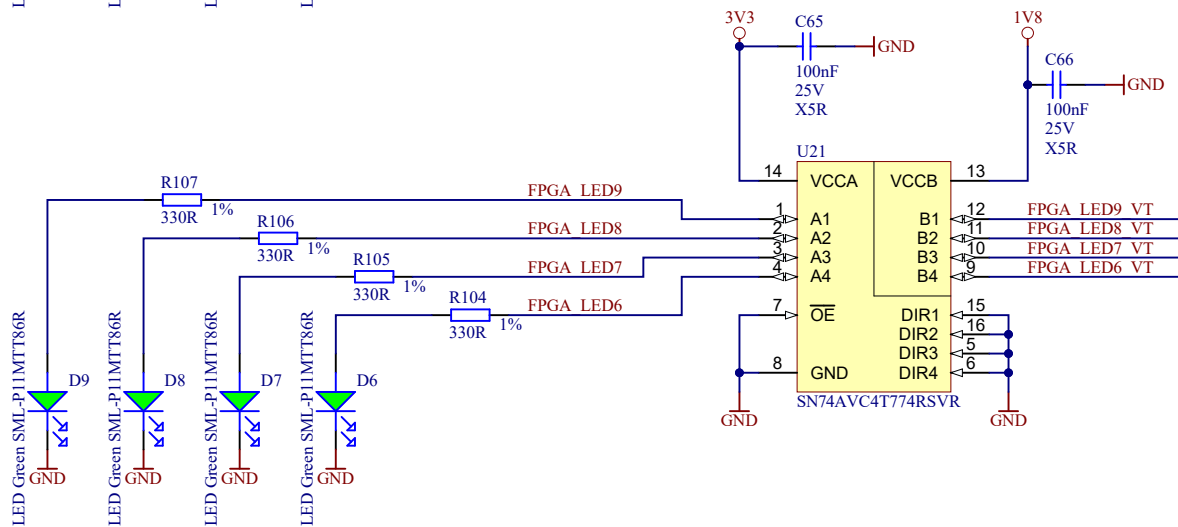
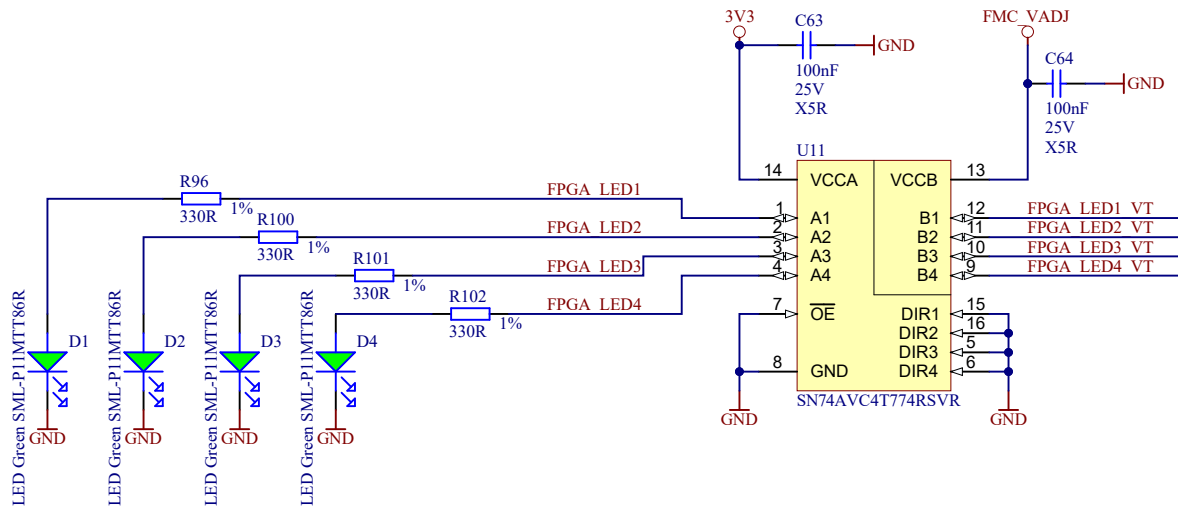
U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

U_DDR_Banks
DDR_Banks.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

U_FPGA_BANK_16
FPGA_BANK_16.SchDoc



Title: TEF1001 - FPGA		
A4	Number: TEF1001 D2CX4-K	Rev. 03
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Filename: FPGA.SchDoc		

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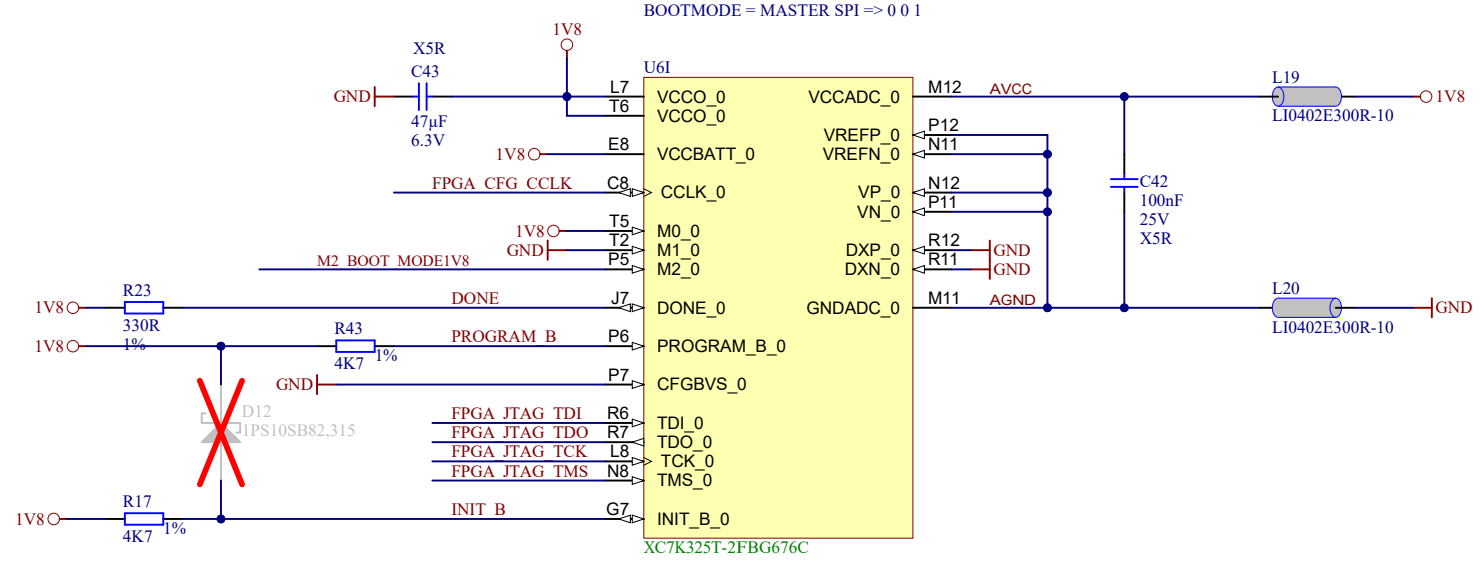
4

1

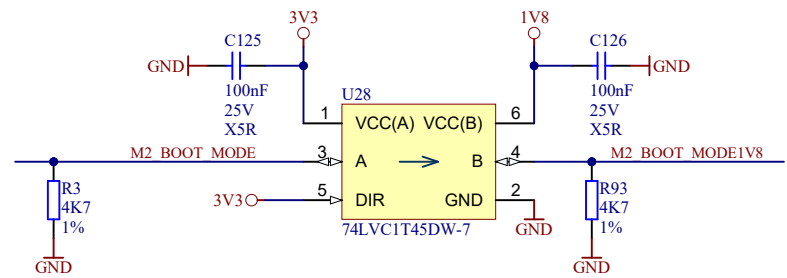
2

3

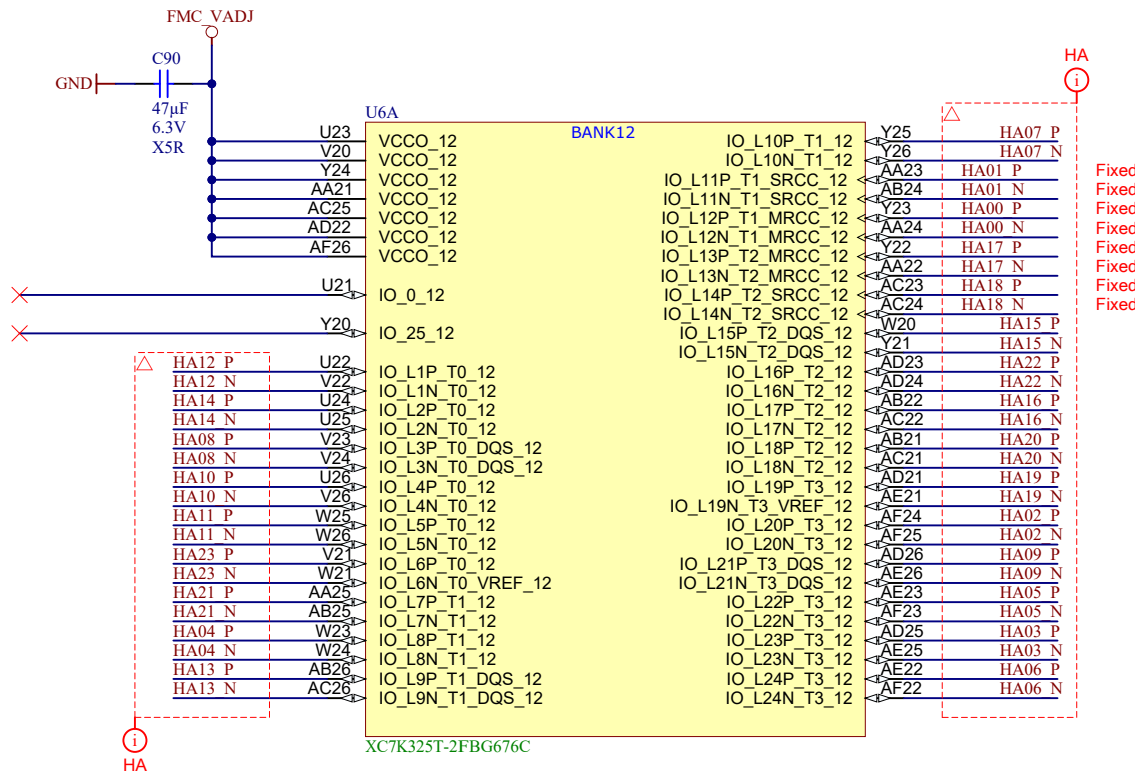
4



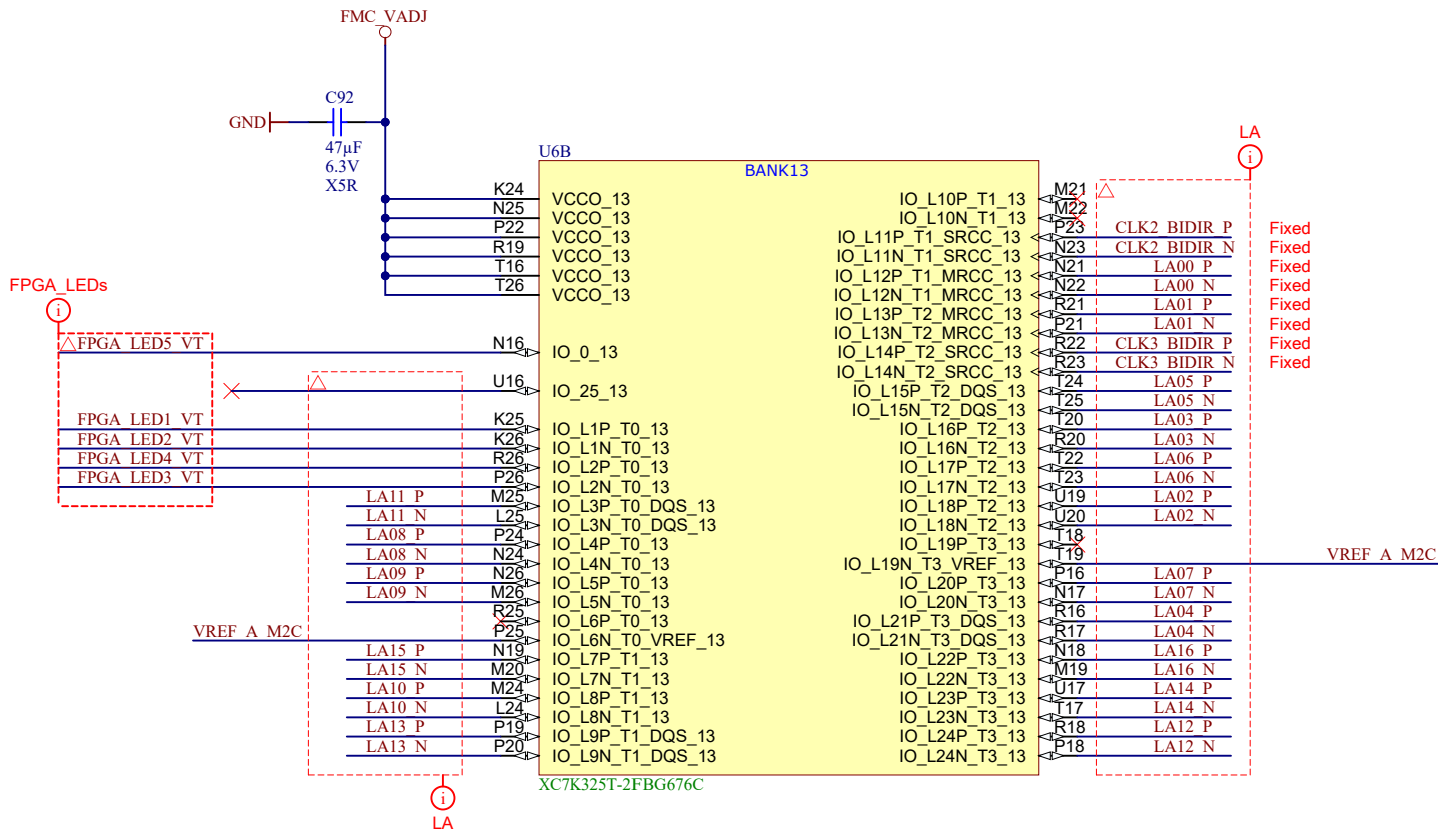
Configuration Modes	Bit M2
Master SPI	0
JTAG	1



Title: TEF1001 - FPGA_CFG		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 7 of 34
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Title: TEF1001 - FPGA_BANK_12		
A4	Number: TEF1001 D2CX4-K	Rev. 03
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Filename: FPGA_BANK_12.SchDoc		



Title: TEF1001 - FPGA_BANK_13		
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Filename: FPGA_BANK_13.SchDoc		

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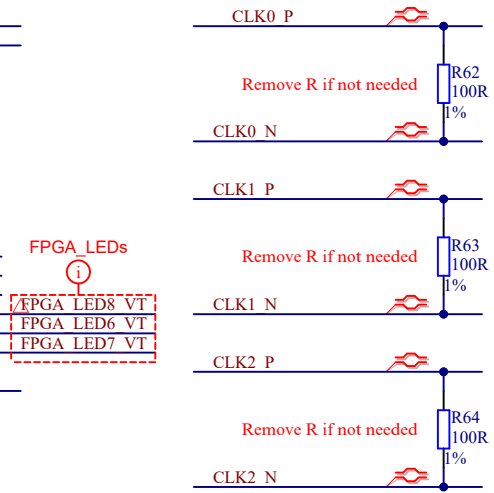
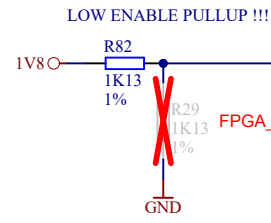
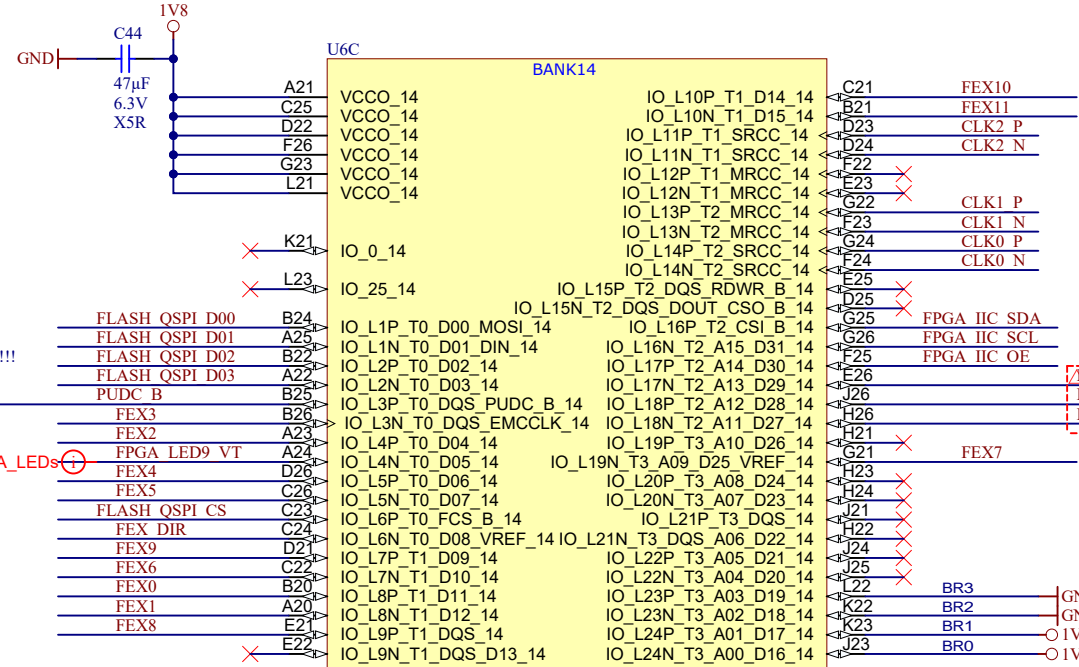
B

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C

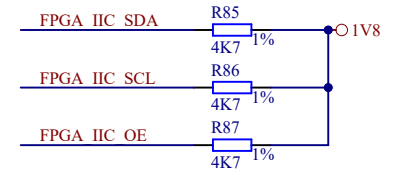
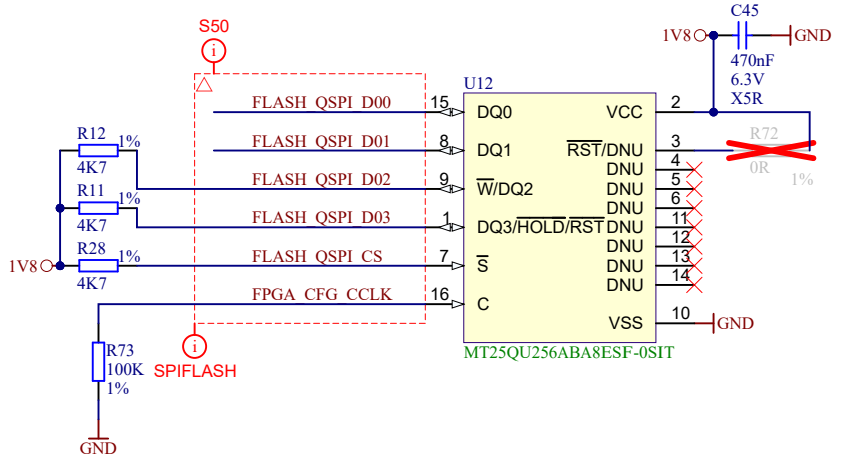
D

D



Board Revisions

BR0	BR1	BR2	BR3	
1	0	0	0	REV01
0	1	0	0	REV02
1	1	0	0	REV03



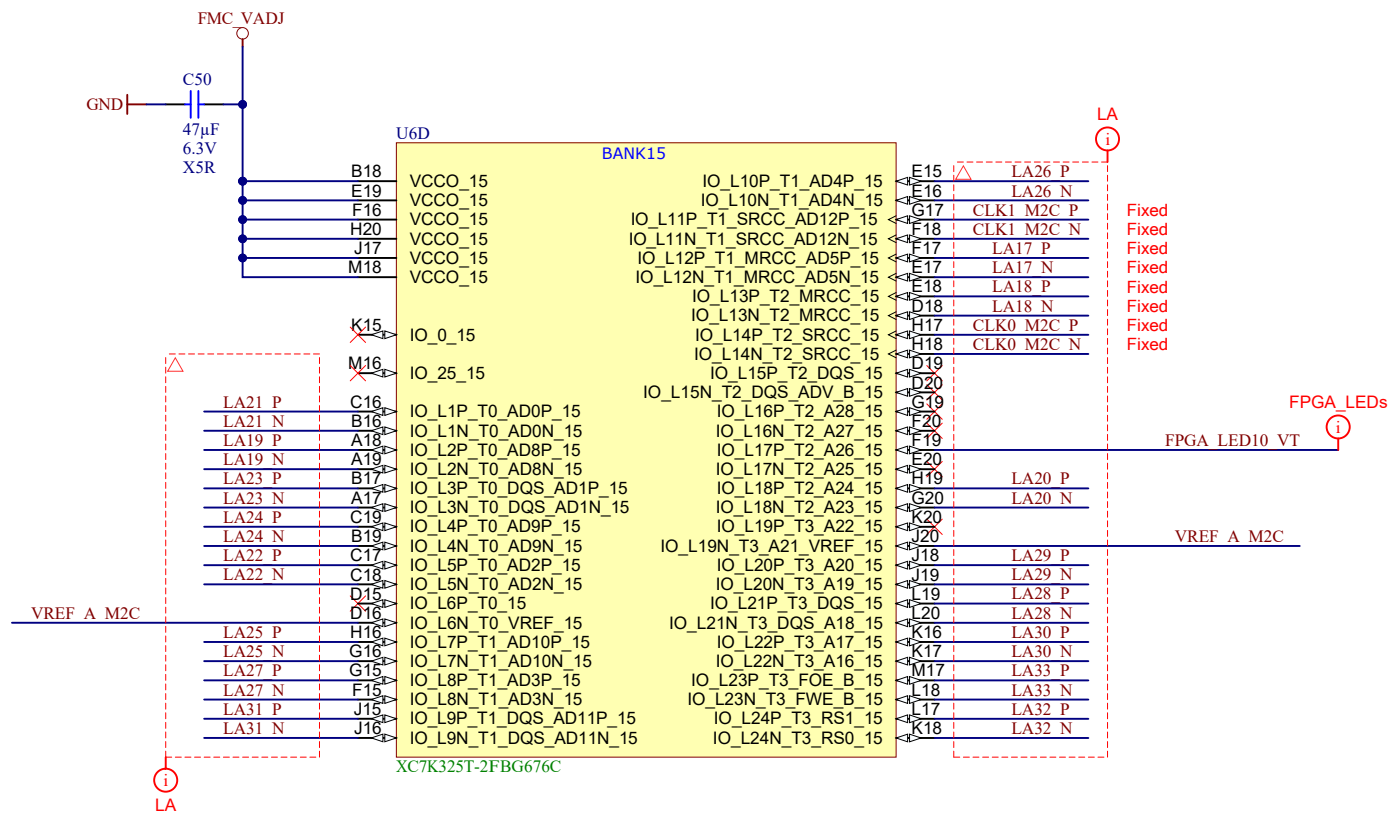
Title: TEF1001 - FPGA_BANK_14		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 10 of 34
Filename: FPGA_BANK_14.SchDoc		

1

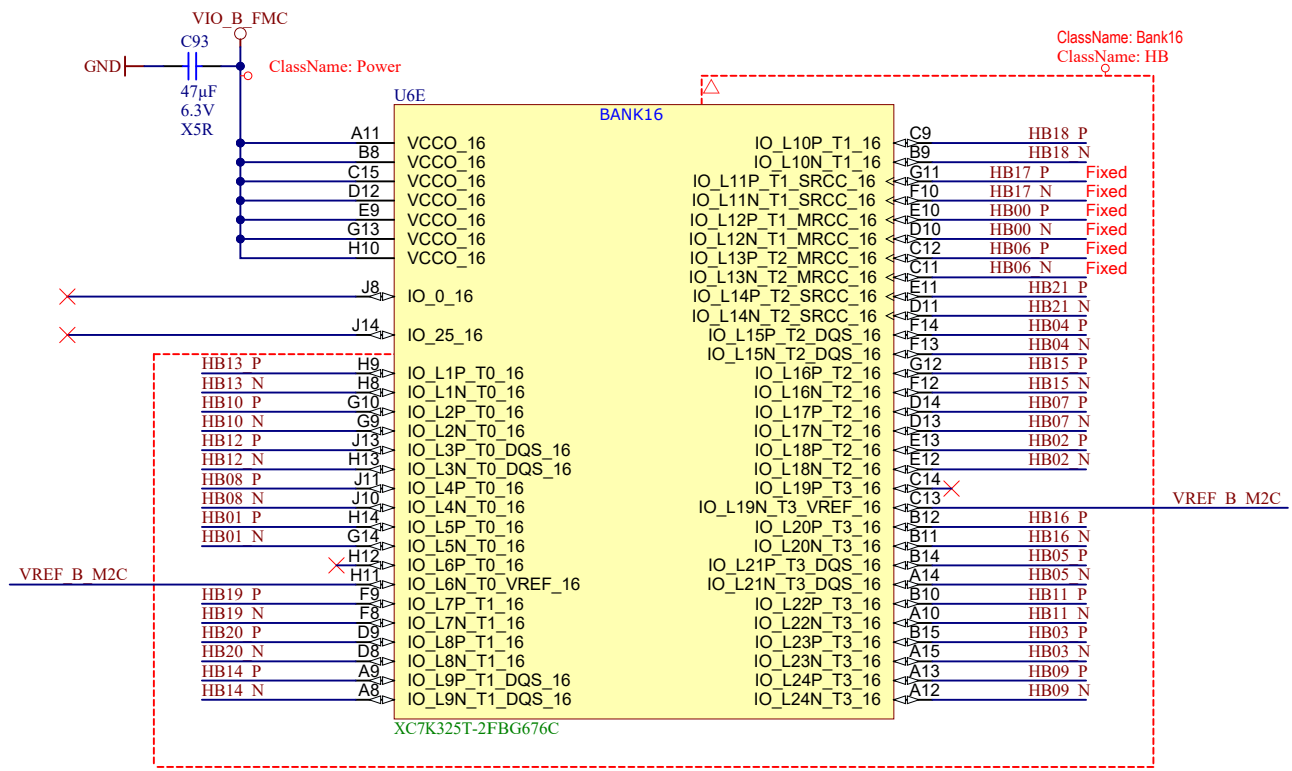
2

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4



Title: TEF1001 - FPGA_BANK_15		
A4	Number: TEF1001 D2CX4-K	Rev. 03
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Filename: FPGA_BANK_15.SchDoc		



Title: TEF1001 - FPGA_BANK_16		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 12 of 34
Filename: FPGA_BANK_16.SchDoc		

1

2

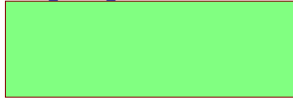
3

4

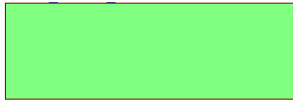
A

A

U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



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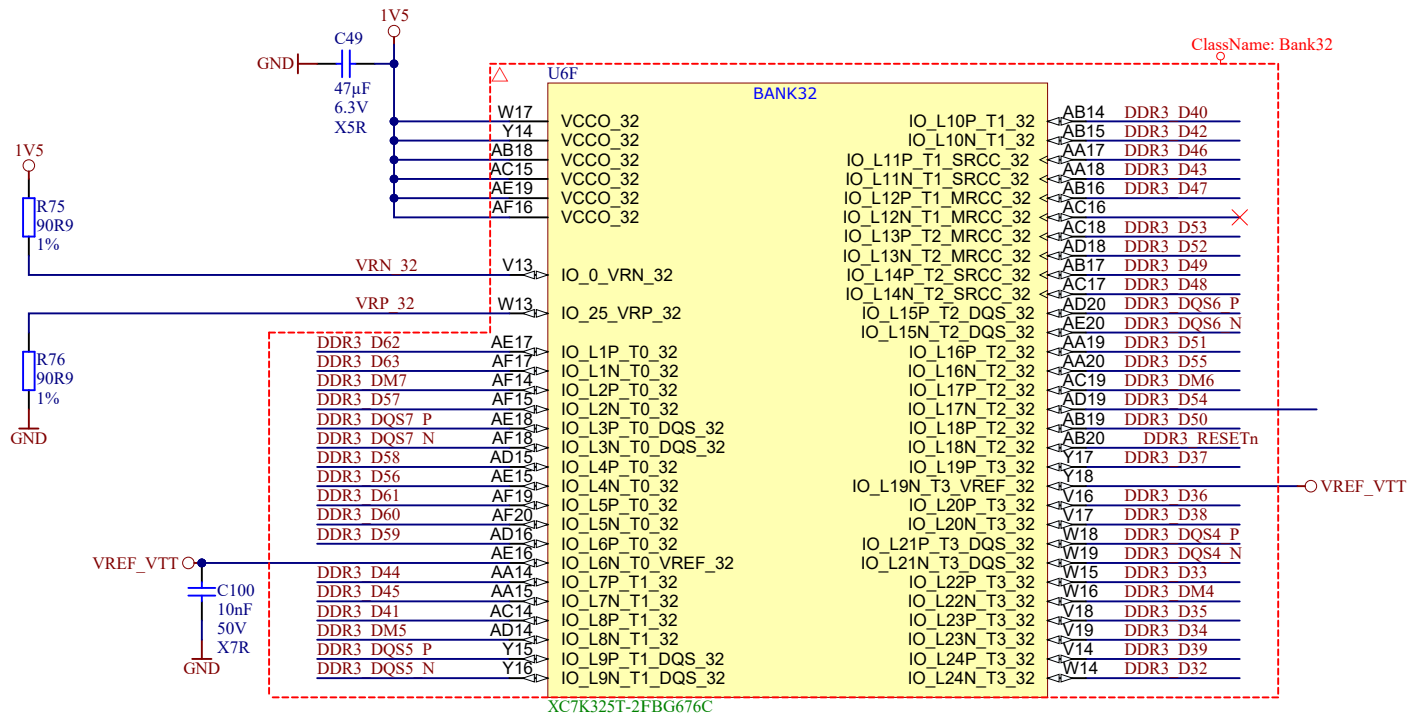
	Title: TEF1001 - DDR_BANKS		
	A4	Number: TEF1001 D2CX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 13 of 34
	Filename: DDR_Banks.SchDoc		

1

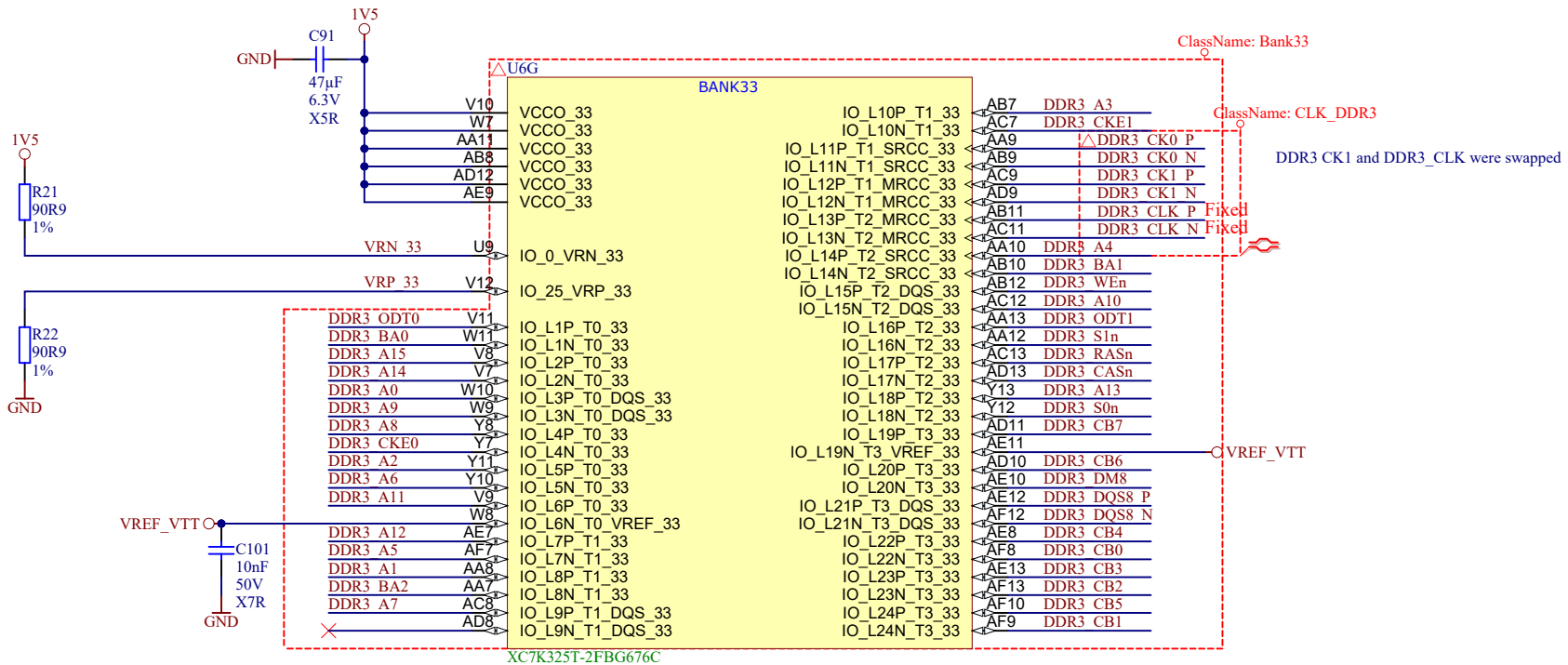
2

3

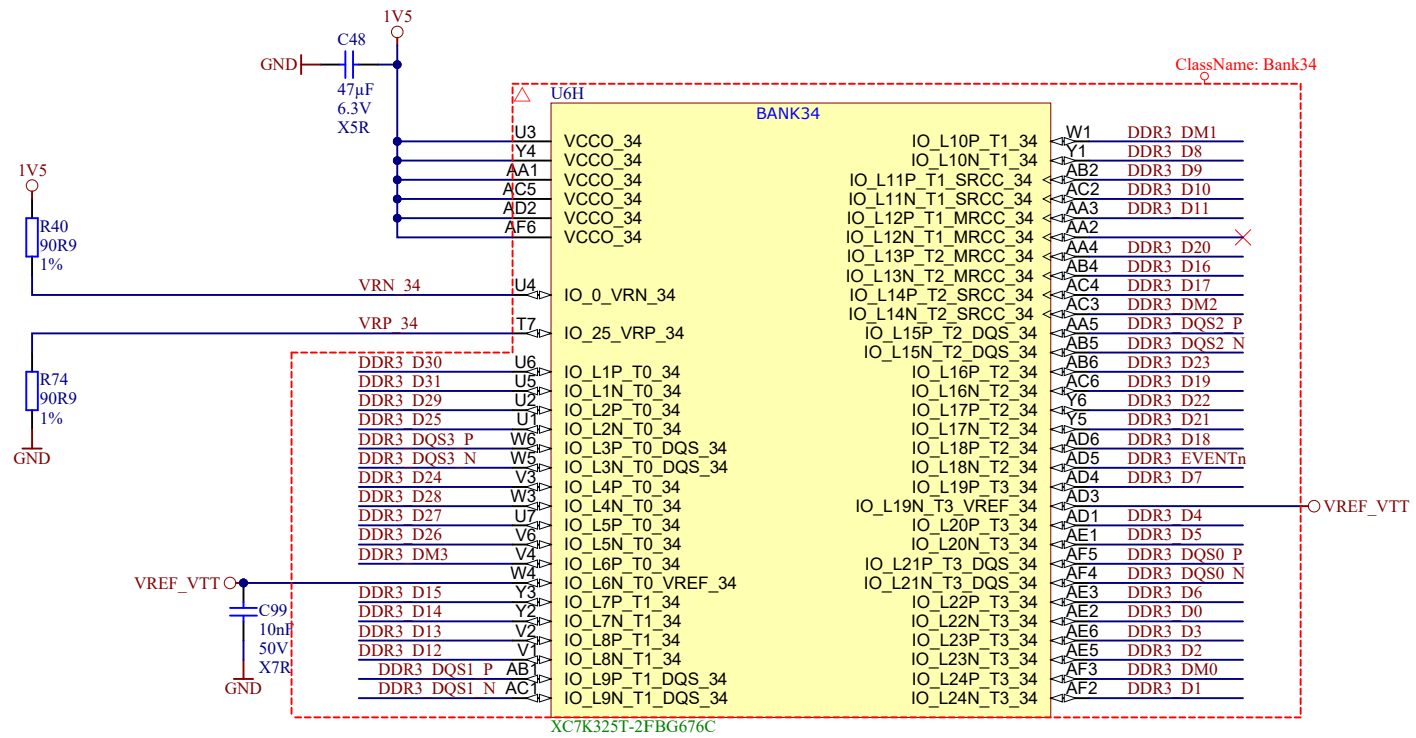
4



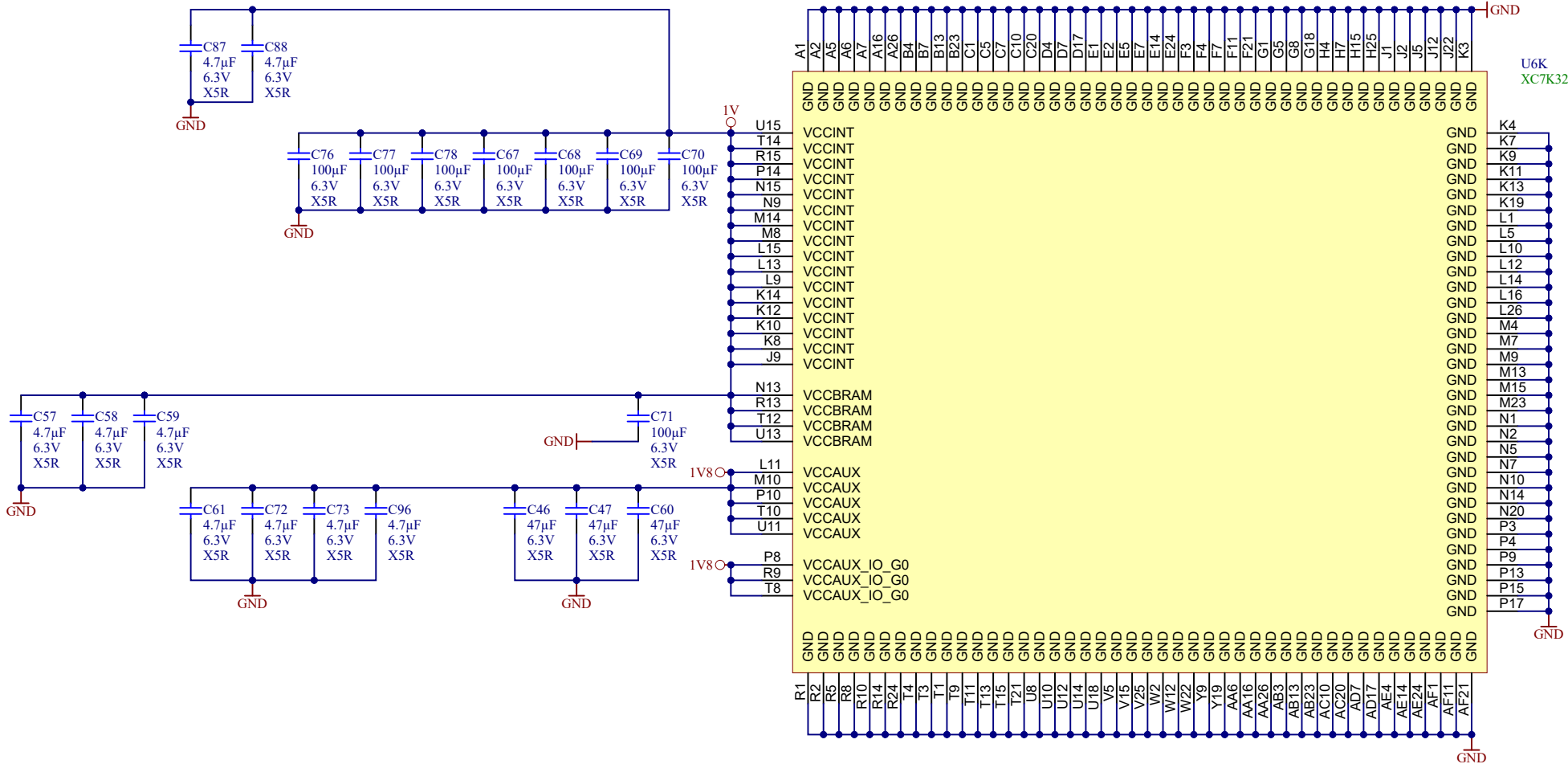
Title: TEF1001 - FPGA_BANK_32		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 14 of 34
Filename: FPGA_BANK_32.SchDoc		




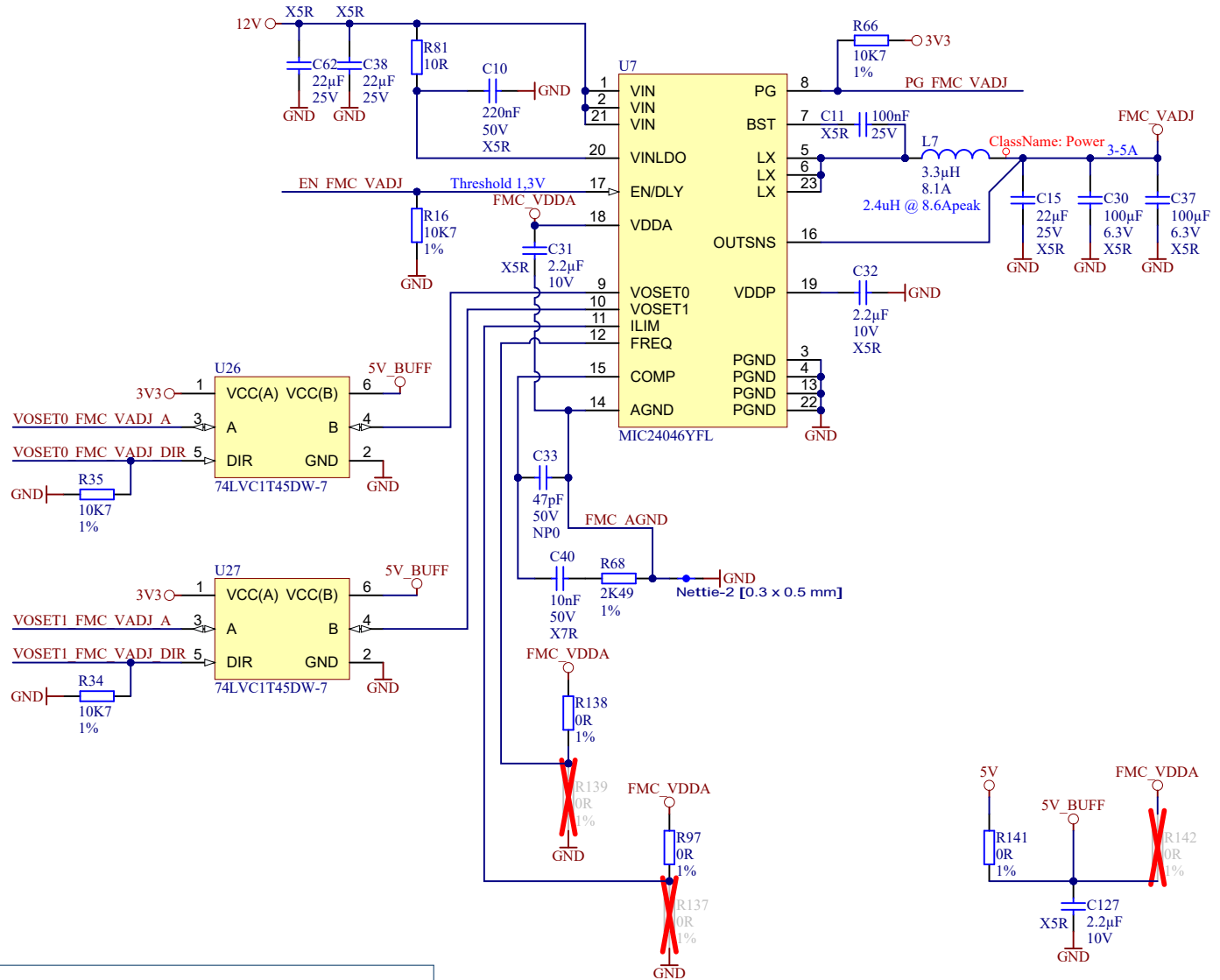
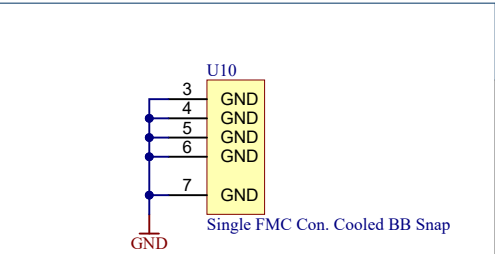
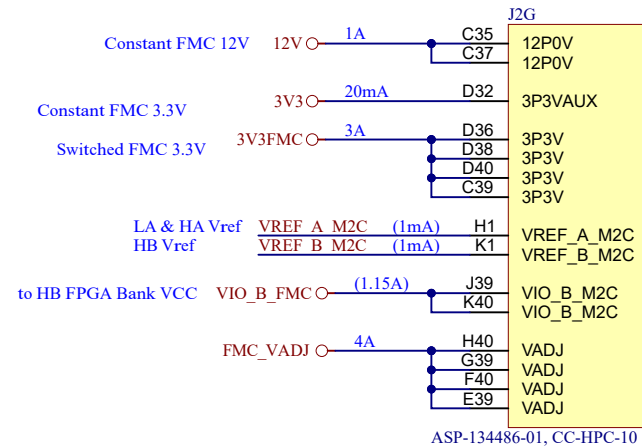
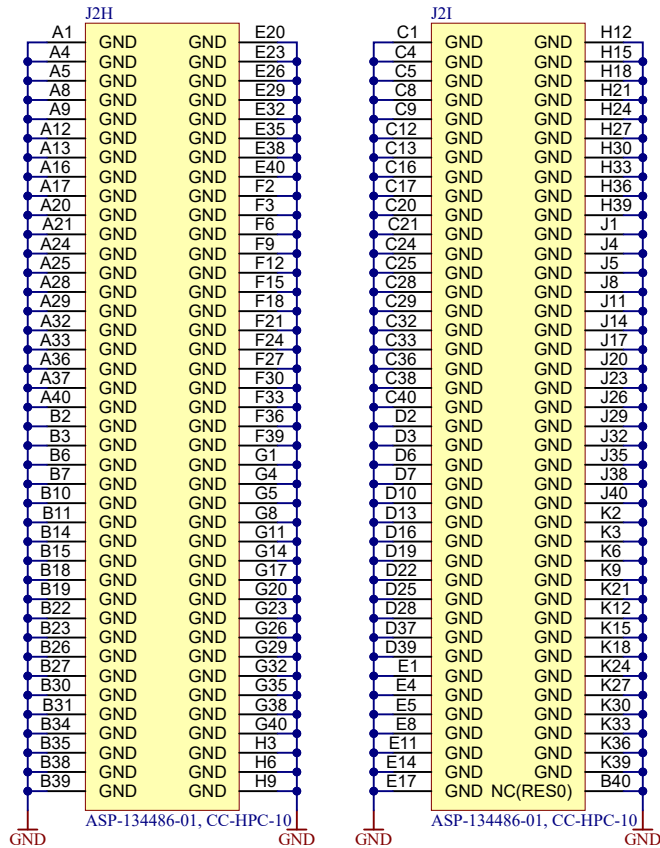
Title: TEF1001 - FPGA_BANK_33		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 15 of 34
Filename: FPGA_BANK_33.SchDoc		



Title: TEF1001 - FPGA_BANK_34		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 16 of 34
Filename: FPGA_BANK_34.SchDoc		



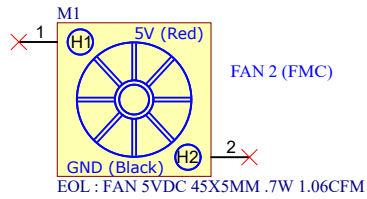
	Title: TEF1001 - FPGA_POWER		
	A4	Number: TEF1001 D2CX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 18 of 34
	Filename: FPGA_POWER.SchDoc		



Title: TEF1001 - FMC_PWR		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 20 of 34
Filename: FMC_PWR.SchDoc		

U_FMC
FMC.SchDoc

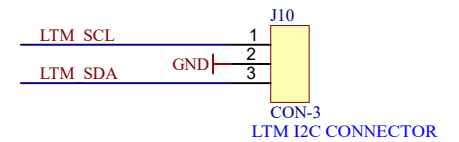
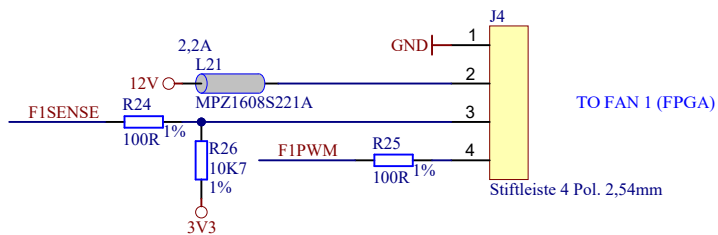
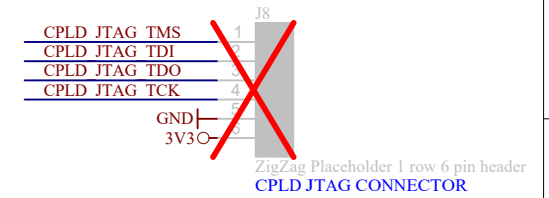
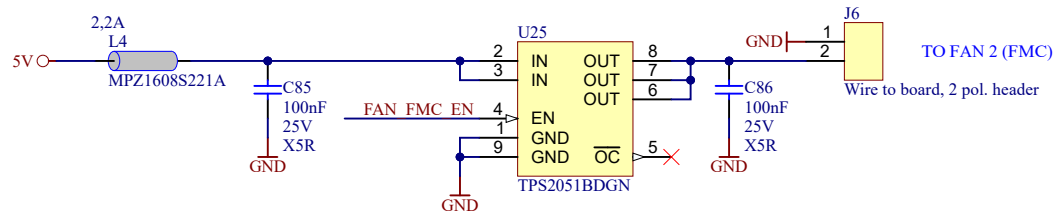
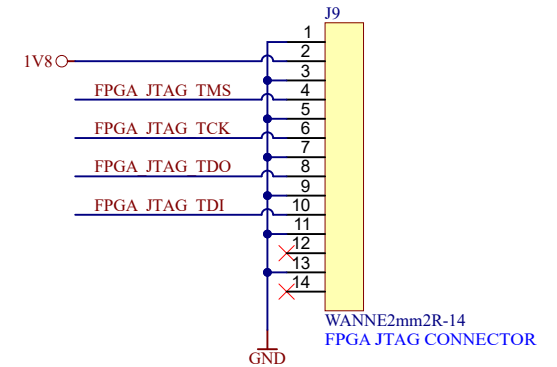
U_PCIE_CONN
PCIE_CONN.SchDoc



JX1
Wire to board, 2 pol. housing

JCT1
Crimp Terminal 4809, 22-30 AWG

JCT2
Crimp Terminal 4809, 22-30 AWG



Title: TEF1001 - CONN		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page22 of 34
Filename: CONN.SchDoc		

A

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C

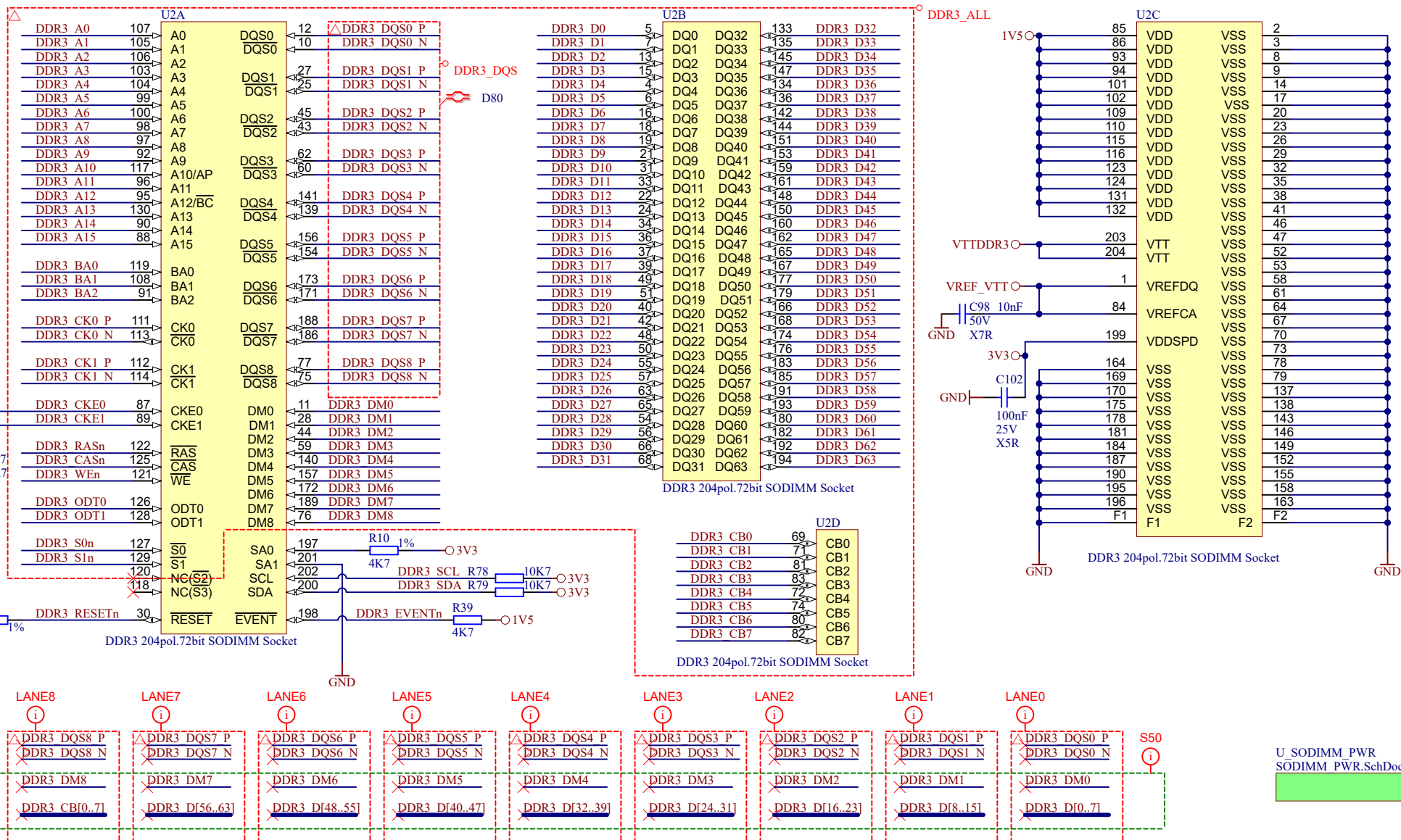
D

A

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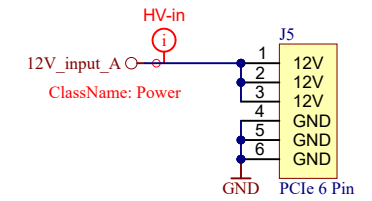
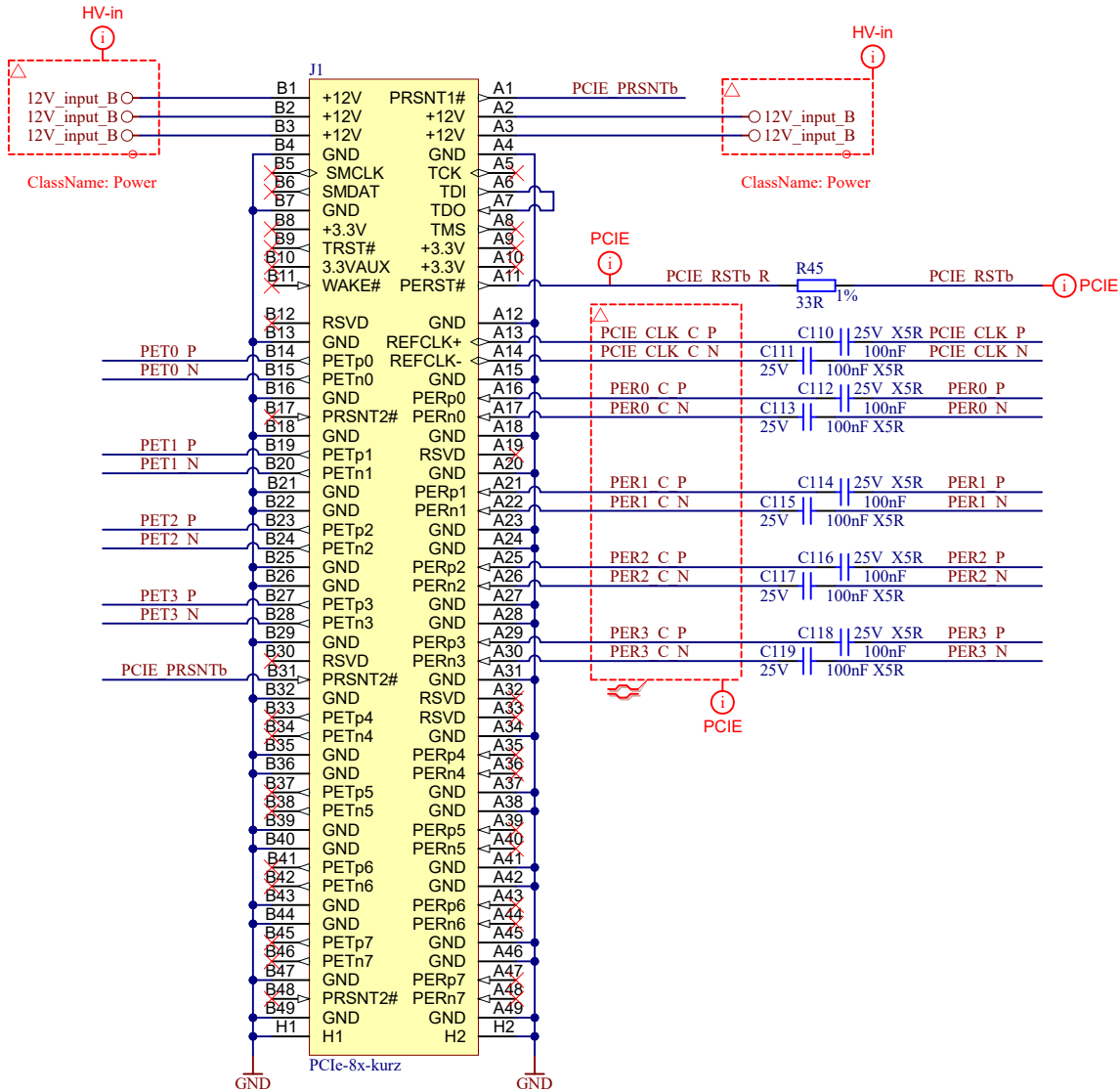
D




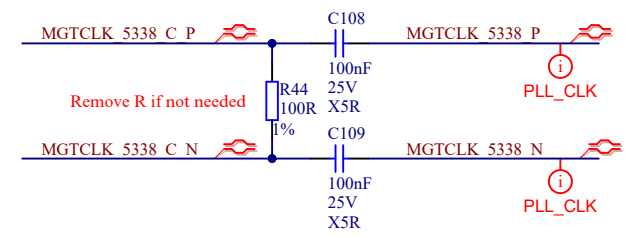
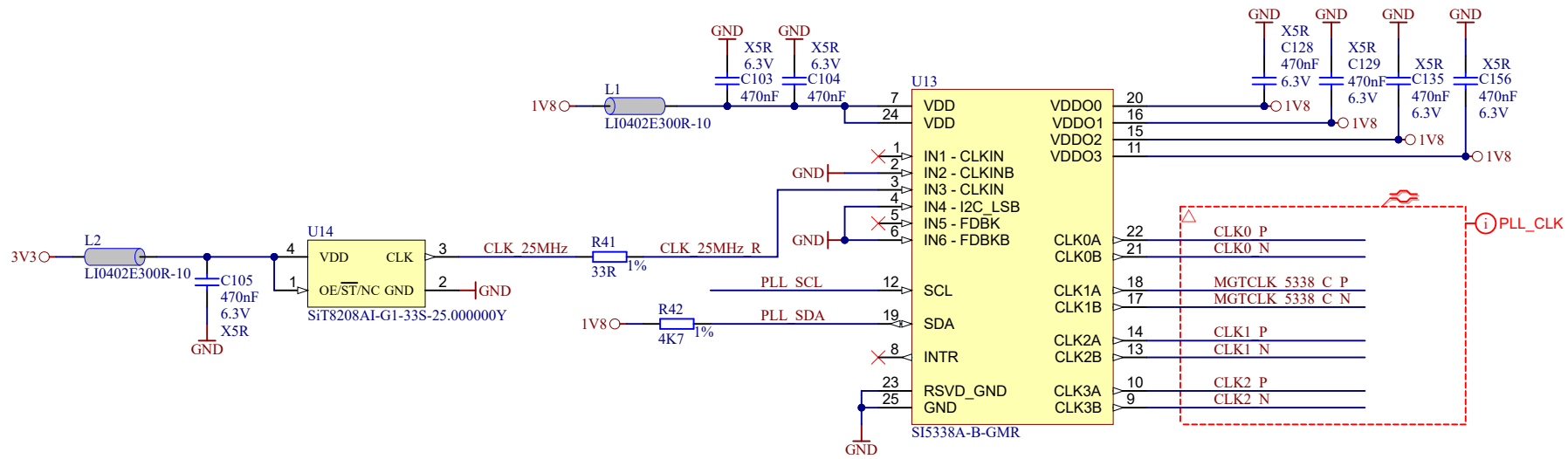
U_SODIMM_PWR
SODIMM_PWR.SchDoc



Title: TEF1001 - SODIMM		
A4	Number: TEF1001 D2CX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 23 of 34
Filename: SODIMM.SchDoc		

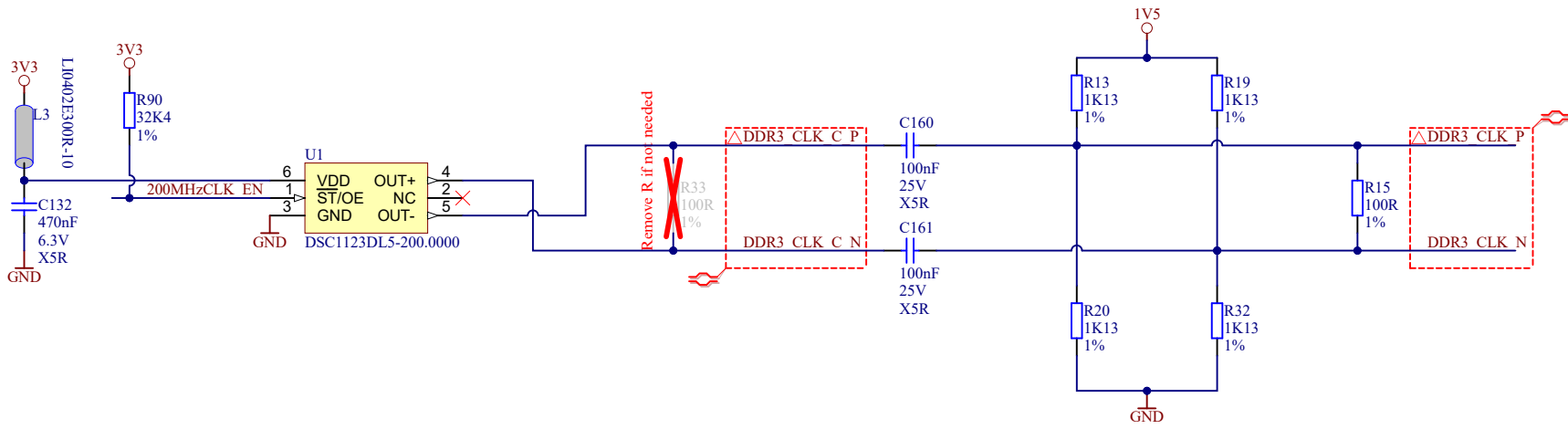



			Title: TEF1001 - PCIE CONNECTOR	
			A4	Number: TEF1001 D2CX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH		Page24 of 34
Filename: PCIE_CONN.SchDoc				



	Title: TEF1001 - CLK-SI5338	
	A4	Number: TEF1001 D2CX4-K
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH
	Filename: CLK-SI5338.SchDoc	
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U_CLK-SI5338
CLK-SI5338.SchDoc



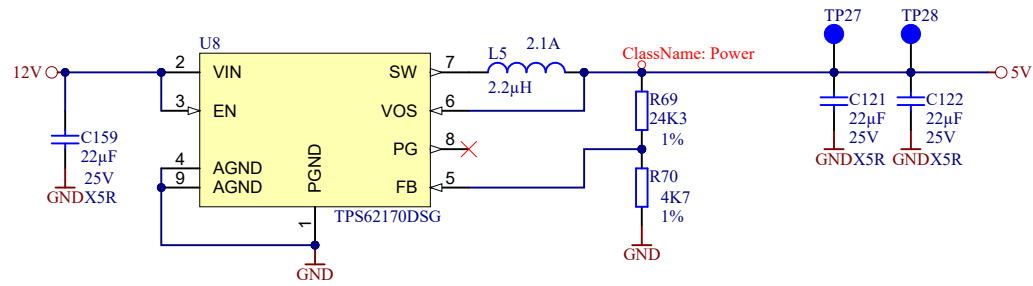
		Title: TEF1001 - CLOCK	
		A4	Number: TEF1001 D2CX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH	
Date: 2018-02-26		Page 26 of 34	
Filename: CLOCK.SchDoc			


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	Title: TEF1001 - PWR_5V		
	A4	Number: TEF1001 D2CX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page28 of 34
	Filename: PWR_5V.SchDoc		

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A

B

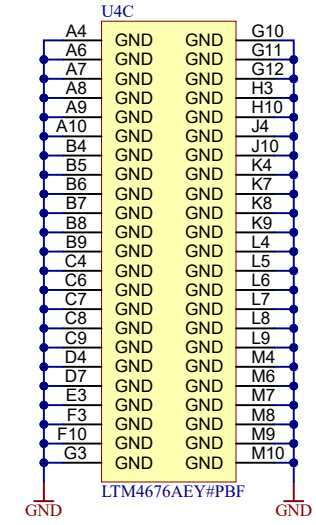
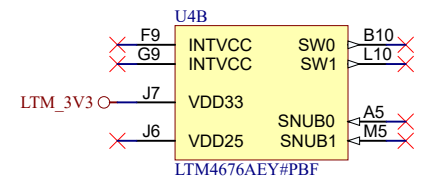
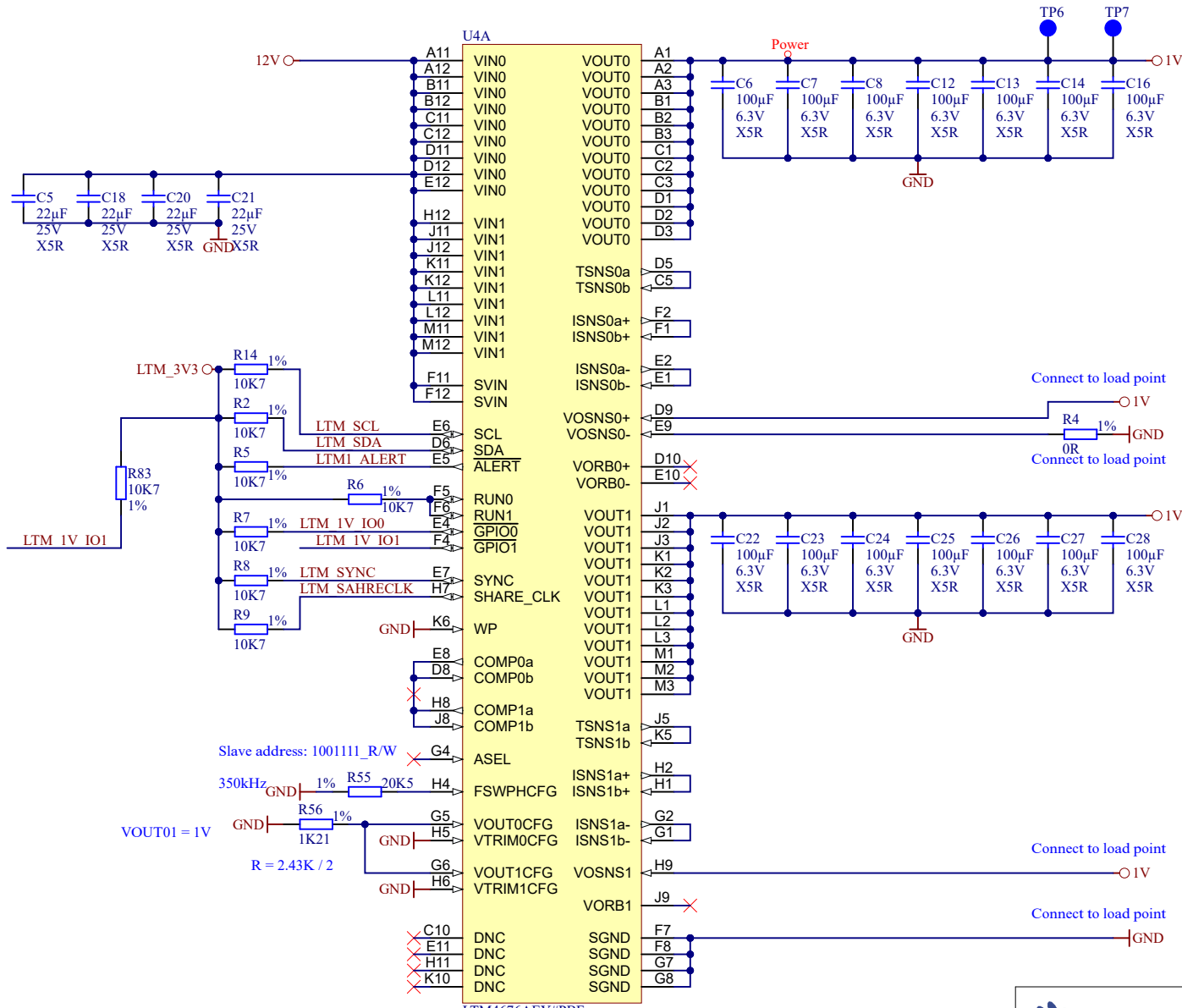
B

C

C

D

D



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1

2

3

4

A

A

B

B

C

C

D

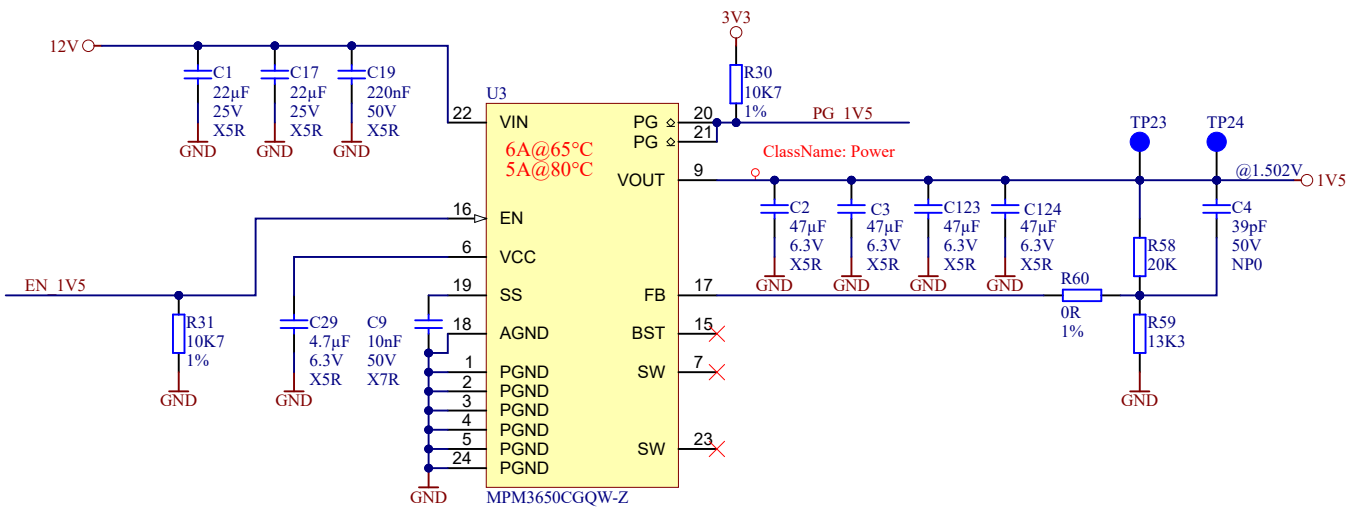
D


1

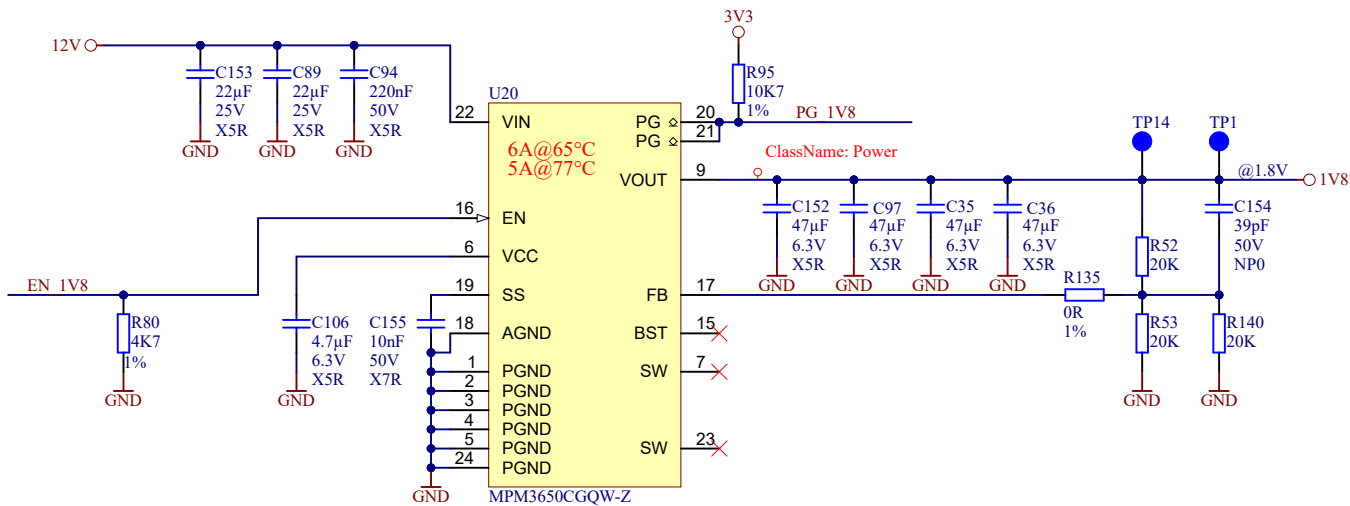
2


3

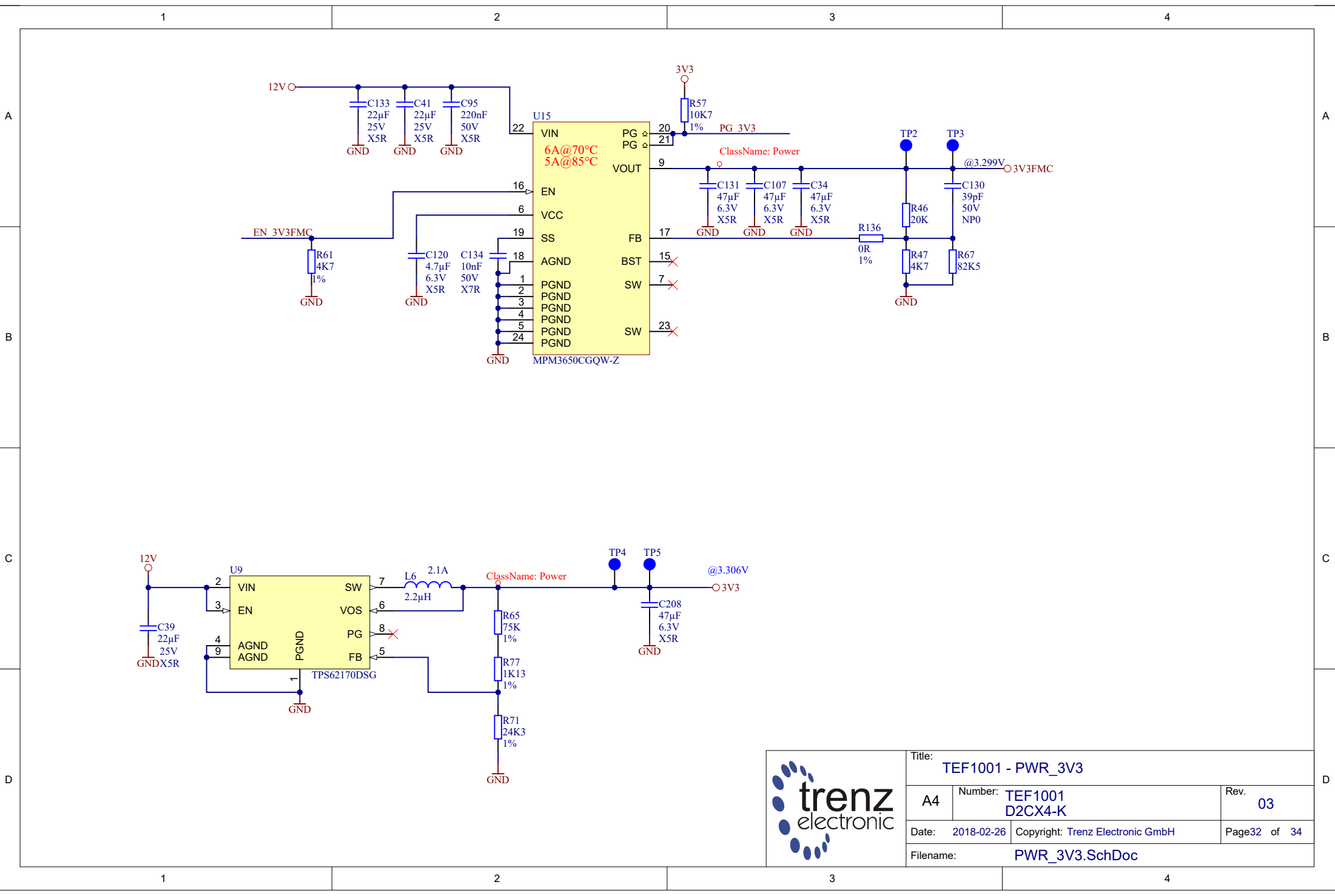
4



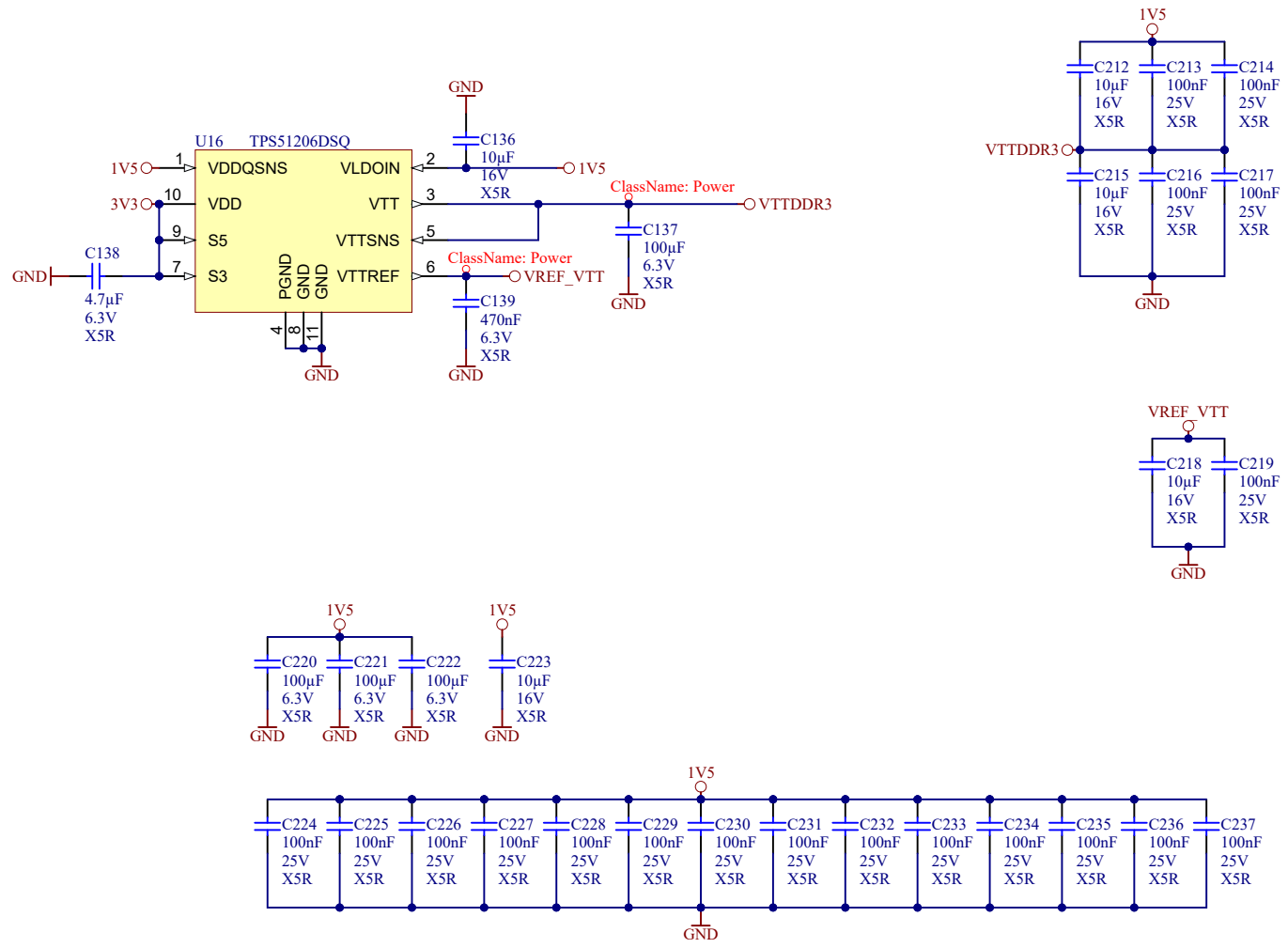
	Title: TEF1001 - PWR_12V_1V5		
	A4	Number: TEF1001 D2CX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page30 of 33
	Filename: PWR_12V_1V5.SchDoc		



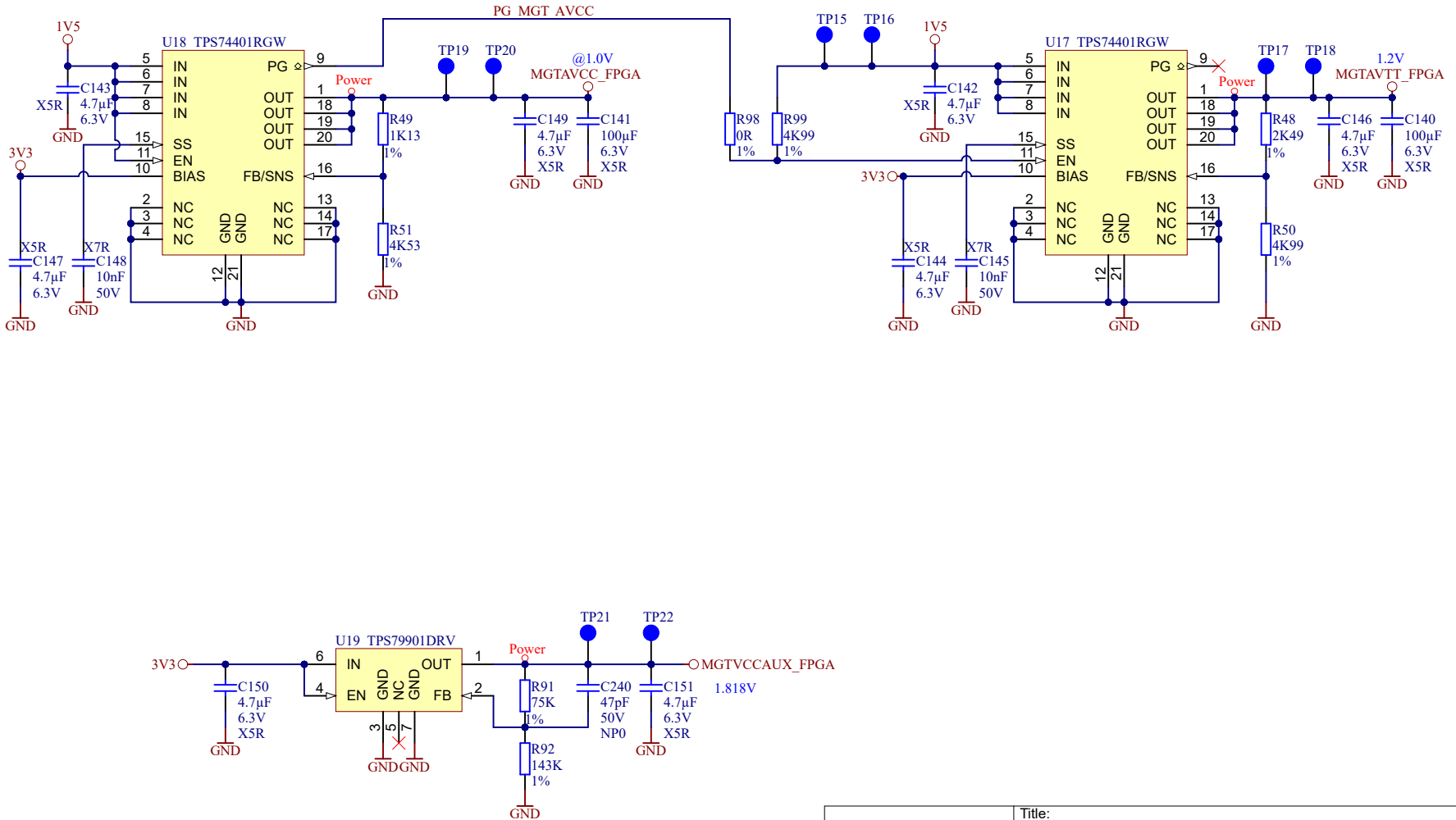
	Title: TEF1001 - PWR_1V8	
	A4	Number: TEF1001 D2CX4-K
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH
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Filename: PWR_1V8.SchDoc		



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