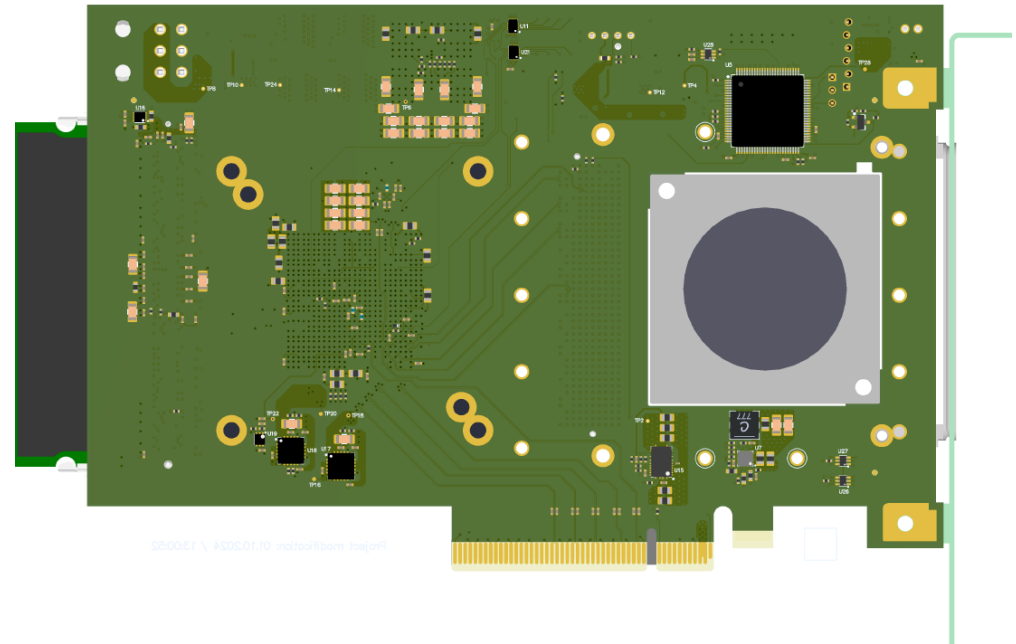


Projekt modifiziert: 01.10.2024 / 13:00:00



020007 \ \42020110 - initialform baupf!

Regarding the usage of our schematics and alike documentation for Trenz module TEF1001 .

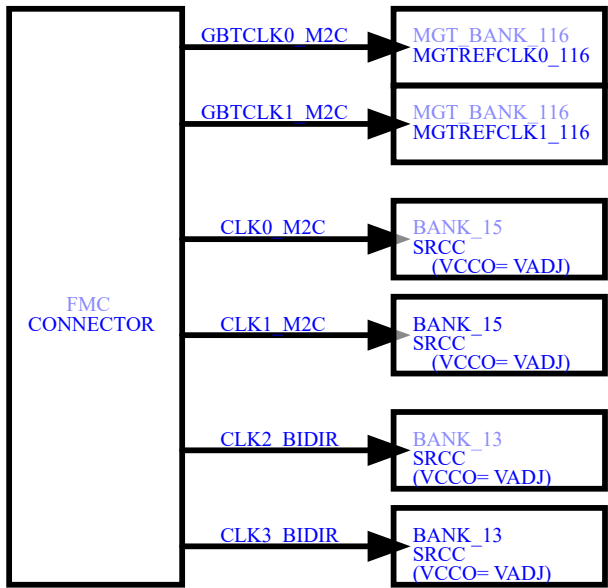
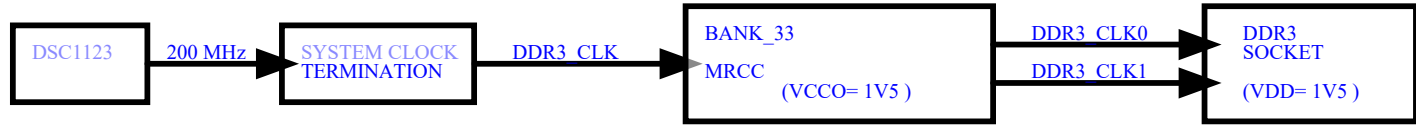
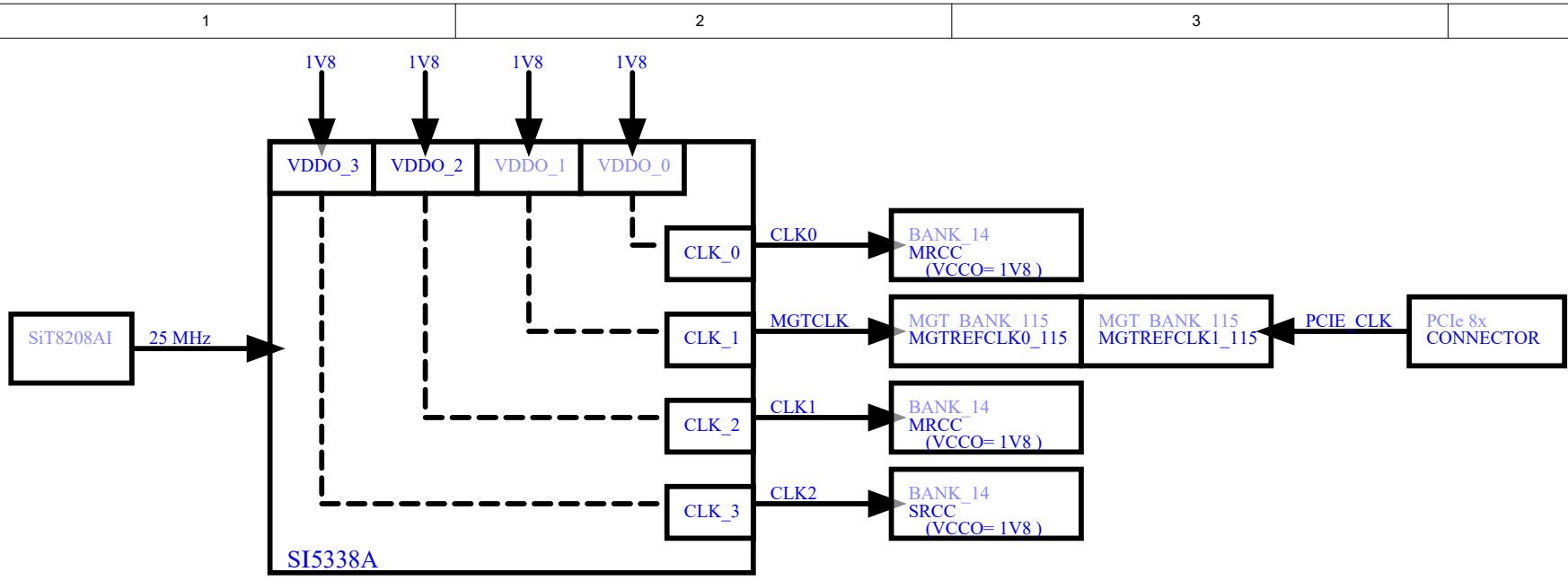
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TEF1001 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

Drawn by	*
Checked by	*
Assembly variant	G2IX4-K
Created by	VY
Modified by	VY
Modified at	2021-05-20



Title: TEF1001- Legal Notices		
A4	Number: TEF0001 G2IX4-K	Rev. 03
Date: 2022-06-08	Copyright: Trenz Electronic GmbH / TT	Page 1 of 34
Filename: Legal Notices Modules.SchDoc		

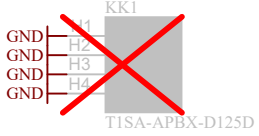


Title: TEF1001 - Clock Overview		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 4 of 34
Filename: CLOCKS OVERVIEW.SchDoc		

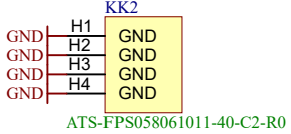
Special notes:

- U_FPGA
FPGA.SchDoc
- U_SODIMM
SODIMM.SchDoc
- U_CLOCK
CLOCK.SchDoc
- U_POWER
POWER.SchDoc
- U_CONN
CONN.SchDoc
- U_CPLD
CPLD.SchDoc
- U_CLOCKS OVERVIEW
CLOCKS OVERVIEW.SchDoc
- U_Legal Notices Modules
Legal Notices Modules.SchDoc
- U_Revision Changes
Revision_Changes.SchDoc

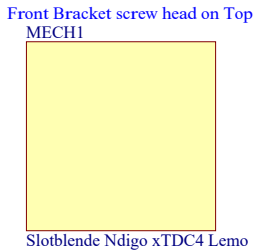
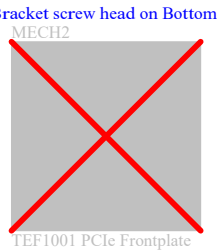
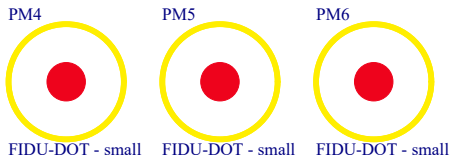
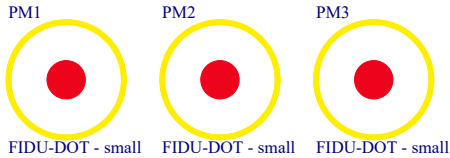
HEATSINK TYPE 1 (FPGA)



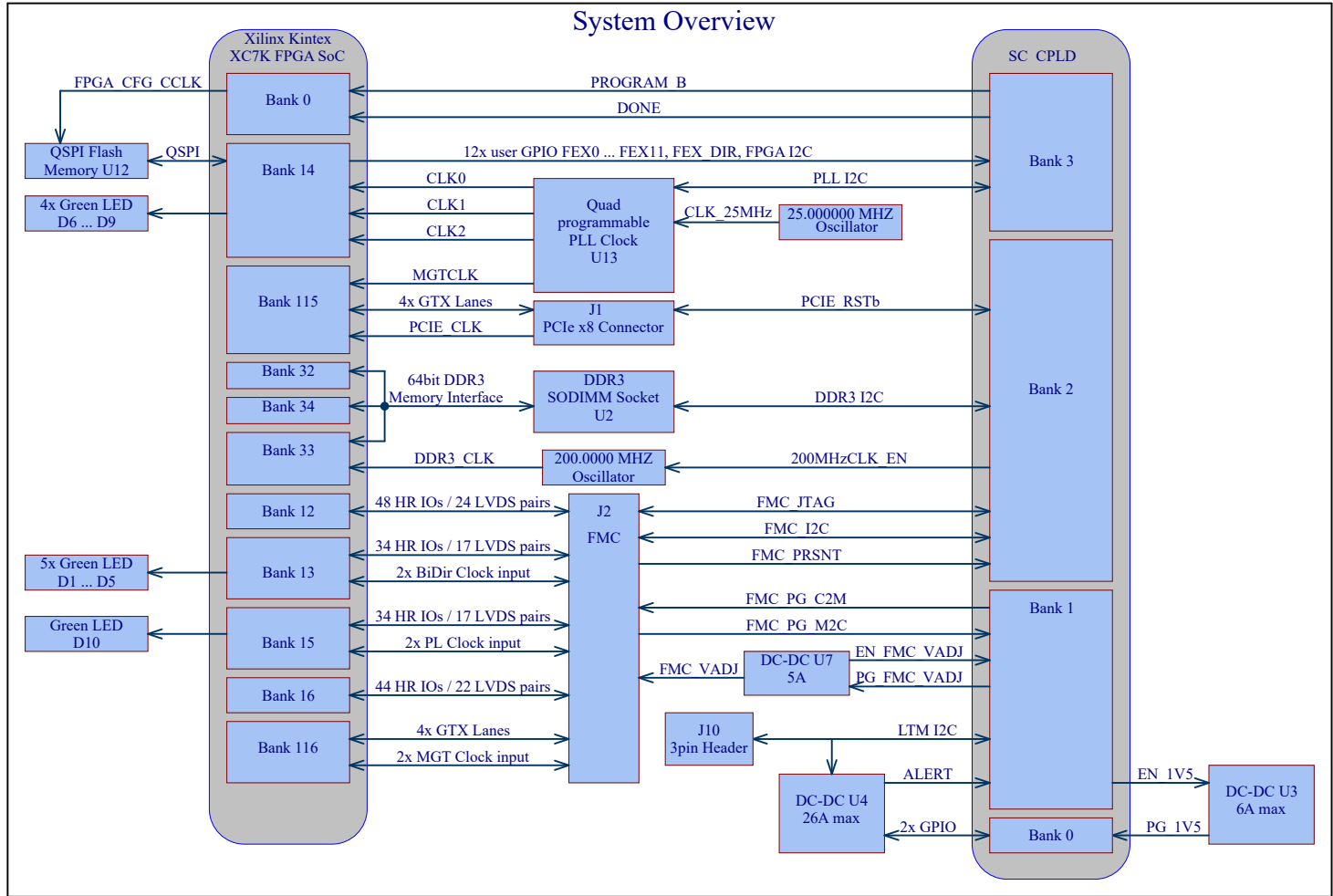
HEATSINK TYPE 2 (FPGA)



Hardware for HEATSINK TYPE 2 (FPGA)



Title: TEF1001 - MAIN		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page5 of 34
Filename: TEF1001.SchDoc		



U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

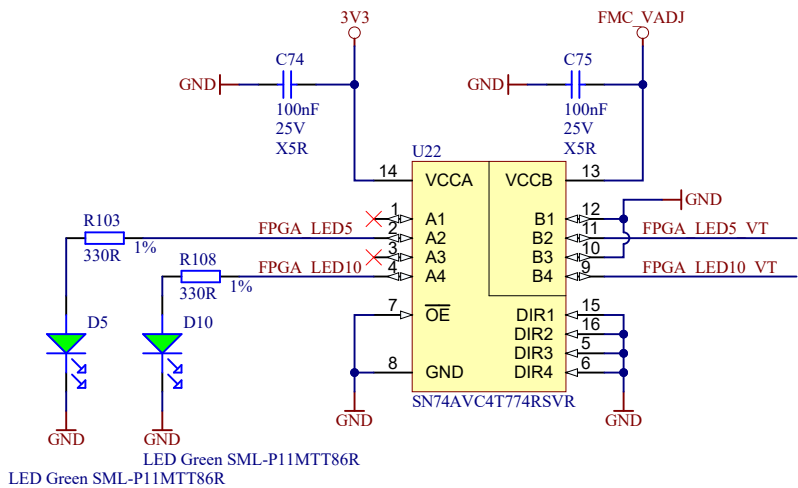
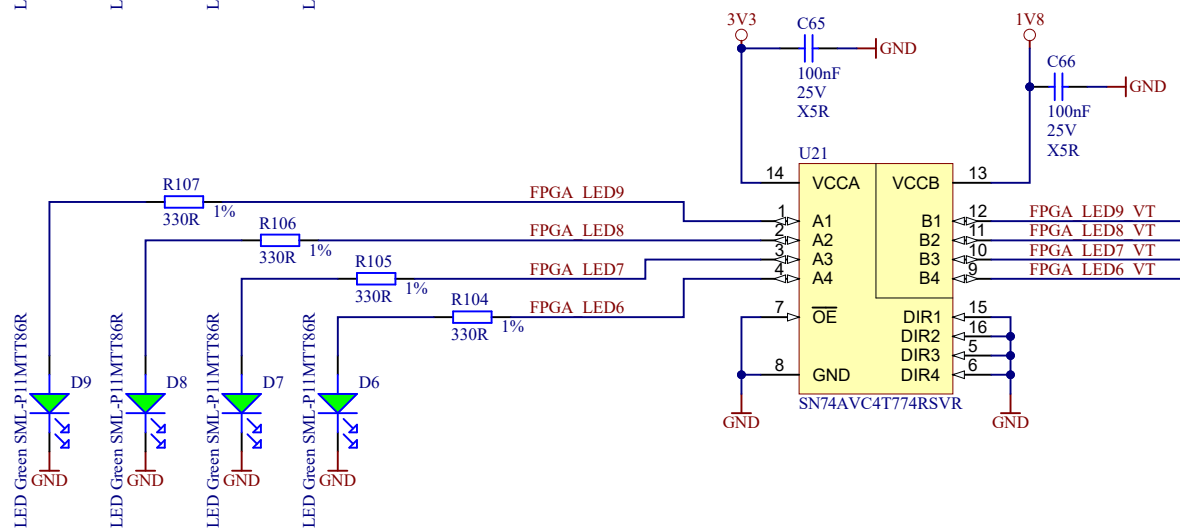
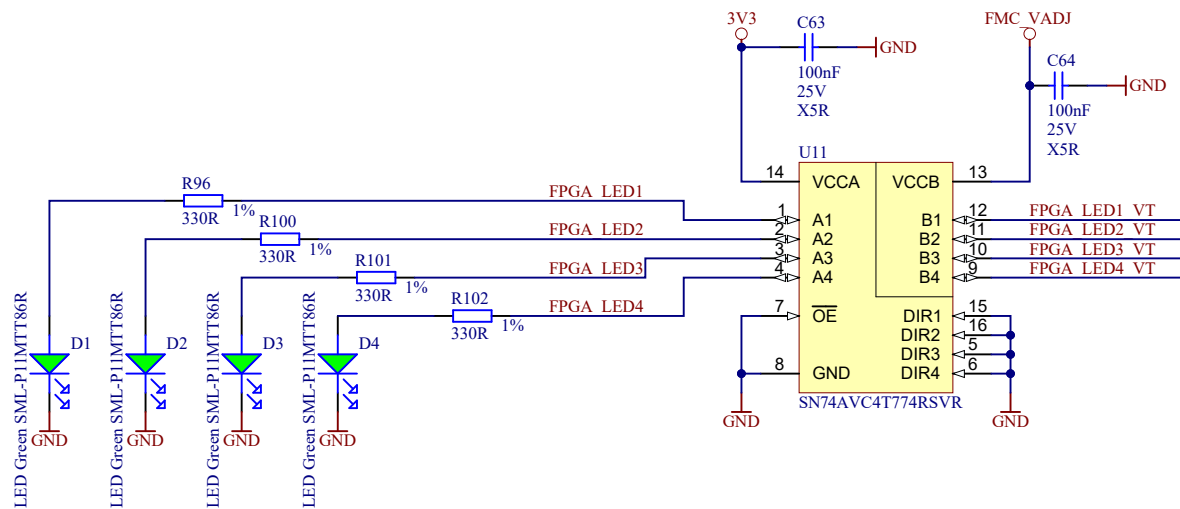
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FPGA_BANK_14.SchDoc

U_DDR_Banks
DDR_Banks.SchDoc

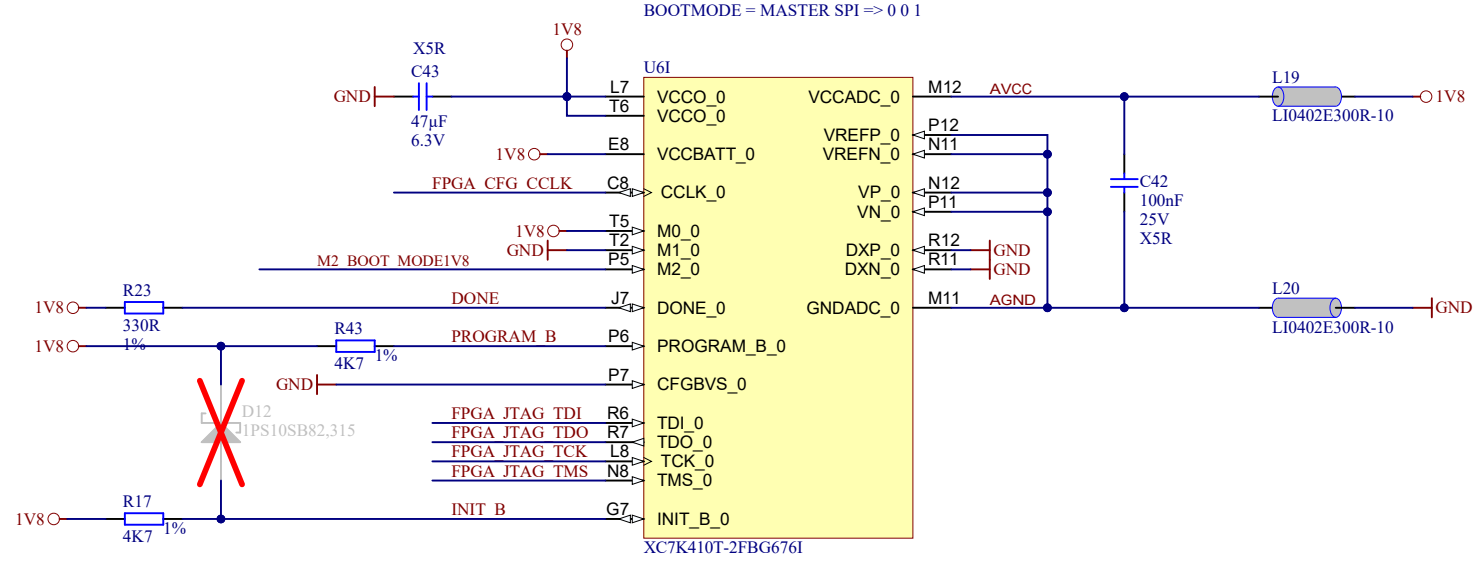
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FPGA_BANK_15.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

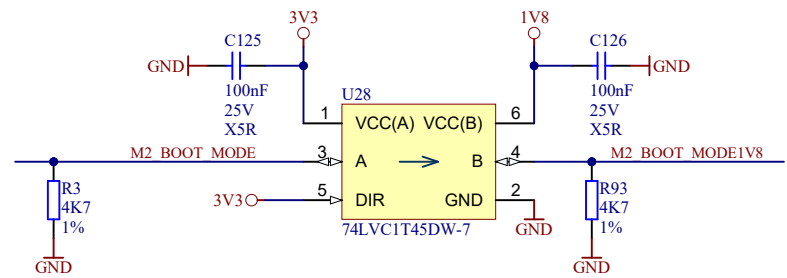
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FPGA_BANK_16.SchDoc



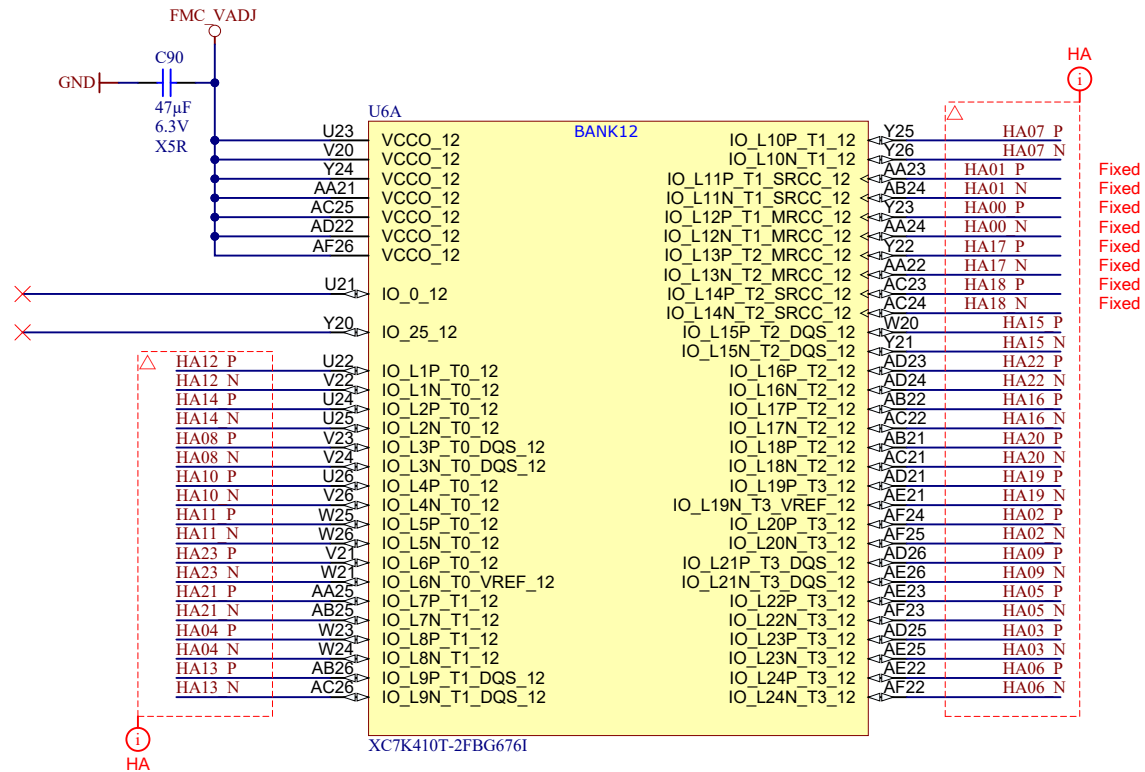
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A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page6 of 34
Filename: FPGA.SchDoc		



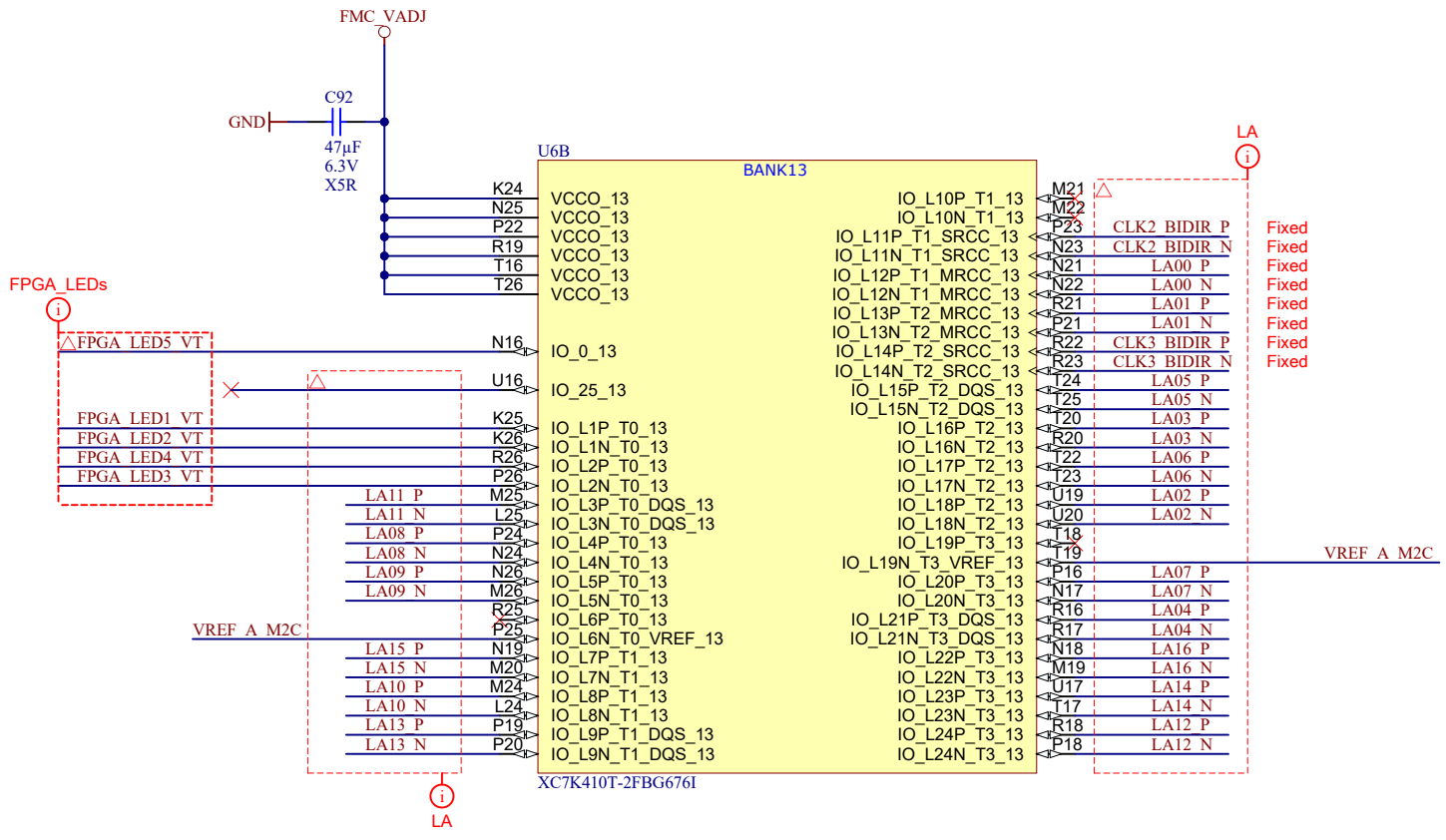
Configuration Modes	Bit M2
Master SPI	0
JTAG	1



Title: TEF1001 - FPGA_CFG		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 7 of 34
Filename: FPGA_CFG.SchDoc		



Title: TEF1001 - FPGA_BANK_12		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 8 of 34
Filename: FPGA_BANK_12.SchDoc		



Title: TEF1001 - FPGA_BANK_13		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page9 of 34
Filename: FPGA_BANK_13.SchDoc		

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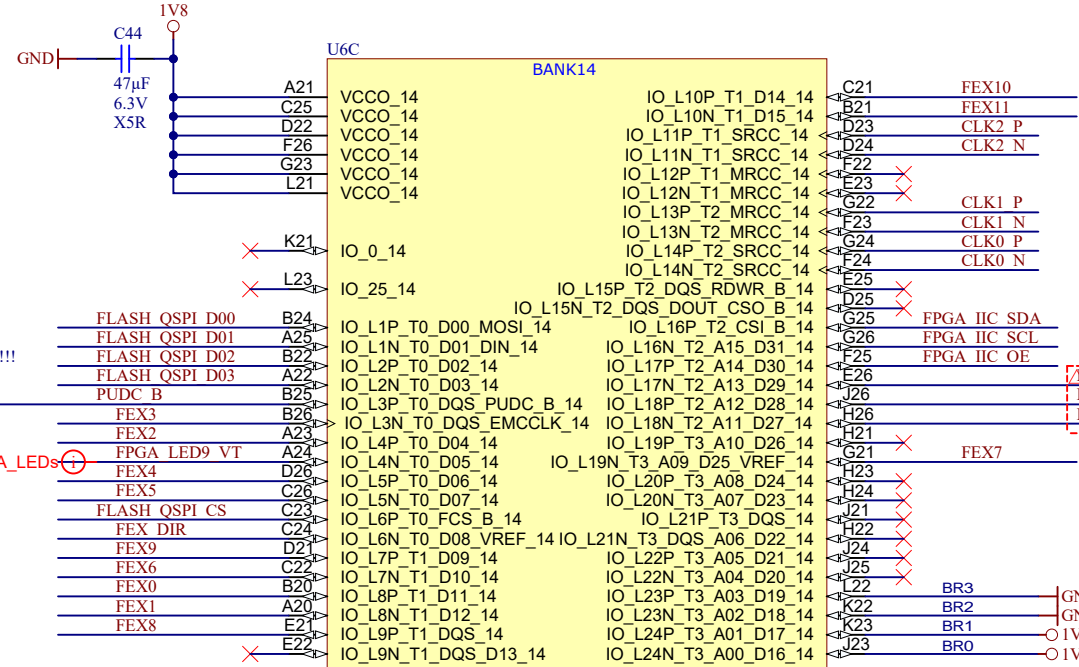
B

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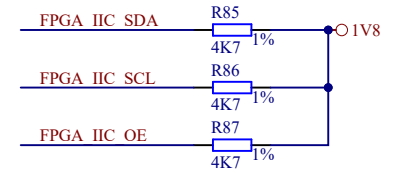
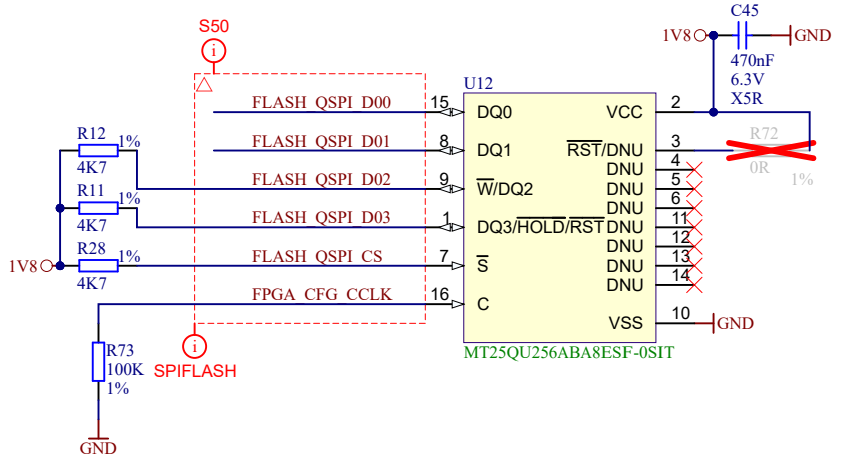
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XC7K410T-2FBG676I

Board Revisions

BR0	BR1	BR2	BR3	
1	0	0	0	REV01
0	1	0	0	REV02
1	1	0	0	REV03



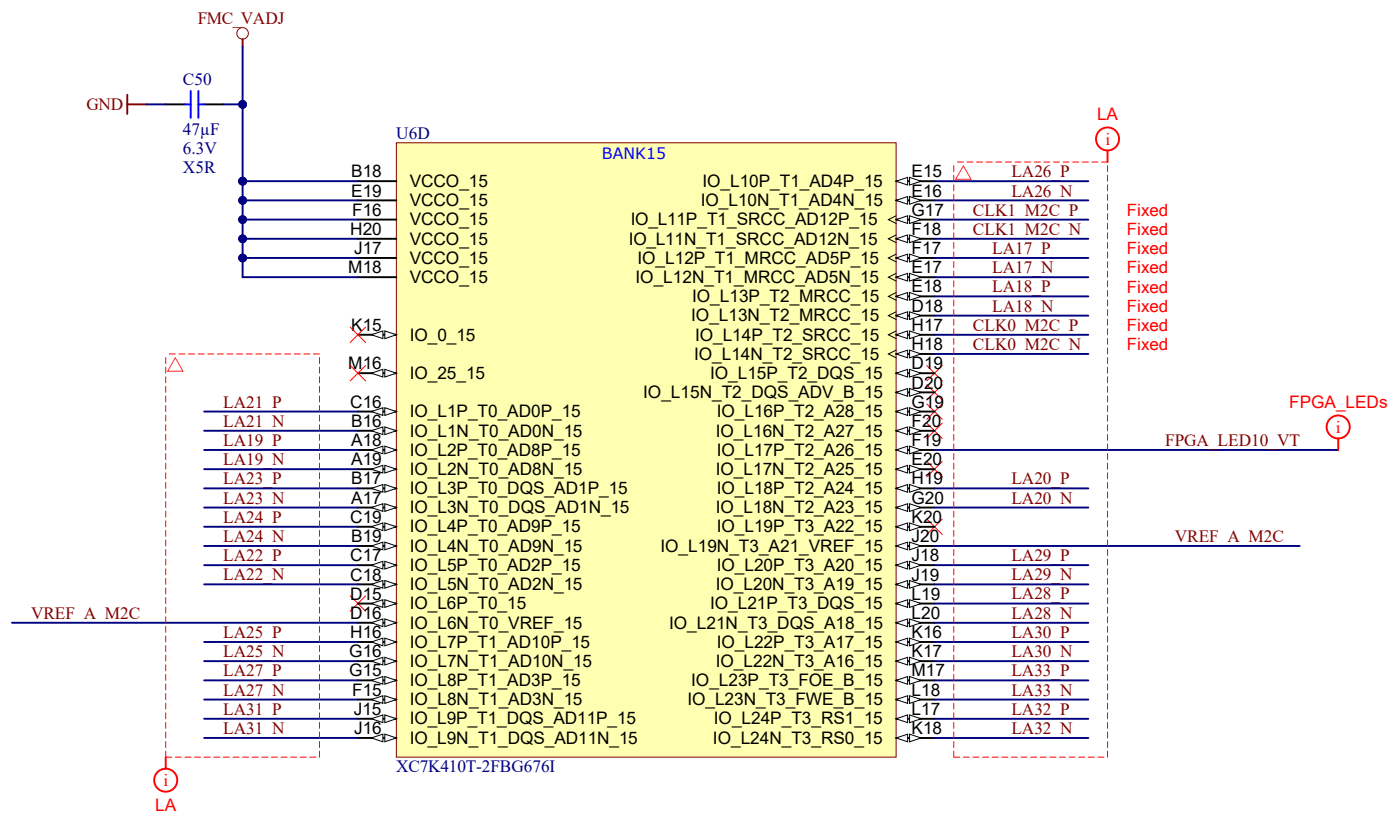
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 10 of 34
Filename: FPGA_BANK_14.SchDoc		

1

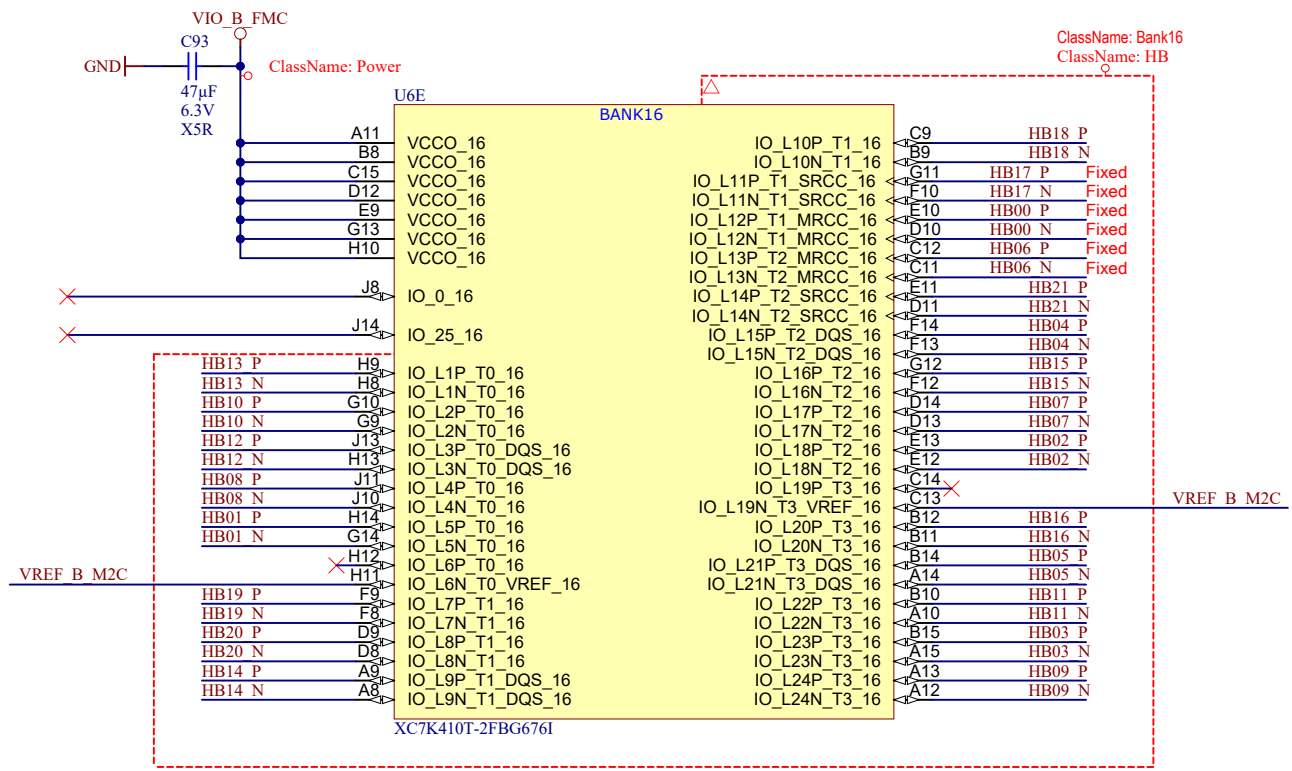
2

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A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 11 of 34
Filename: FPGA_BANK_15.SchDoc		



Title: TEF1001 - FPGA_BANK_16		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 12 of 34
Filename: FPGA_BANK_16.SchDoc		

1

2

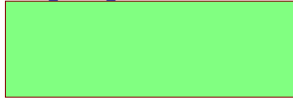
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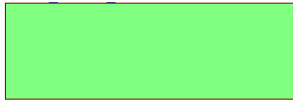
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A

U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



B


B

C

C

D

D

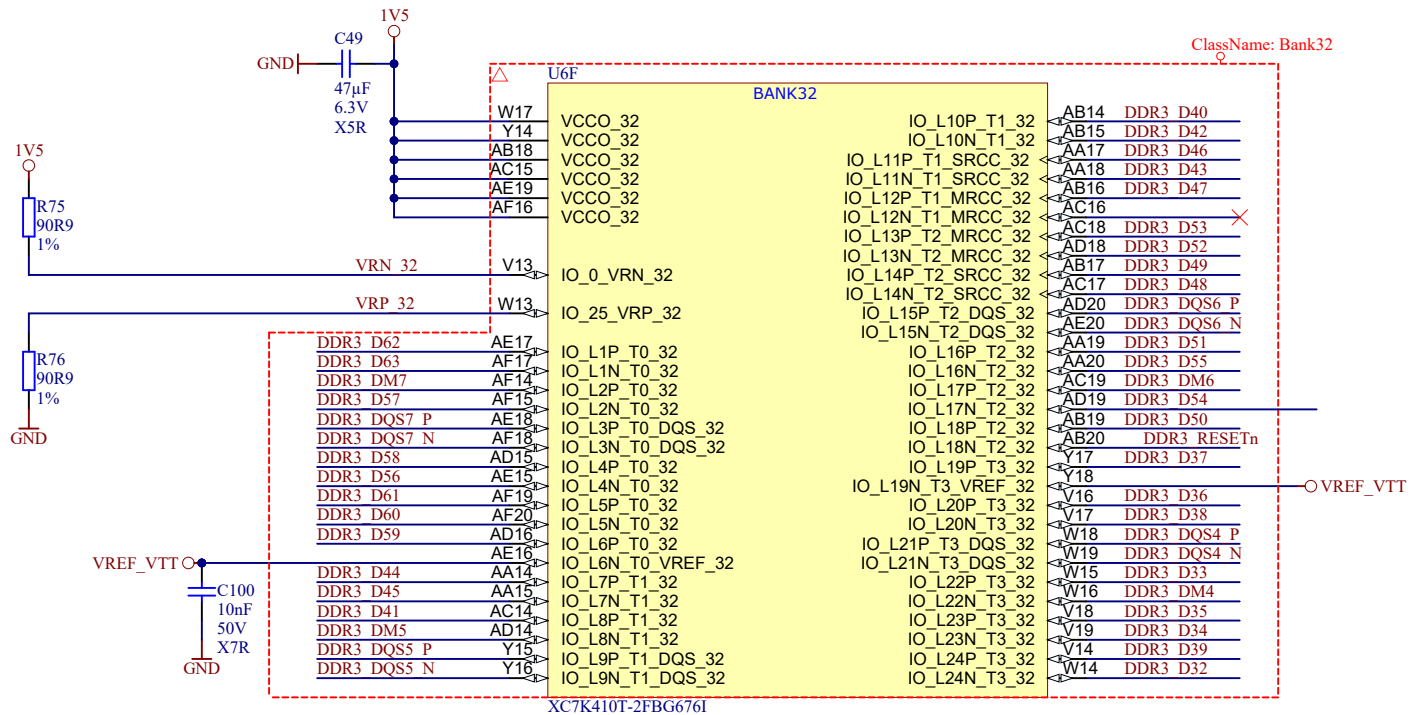
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	A4	Number: TEF1001 G2IX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 13 of 34
	Filename: DDR_Banks.SchDoc		

1

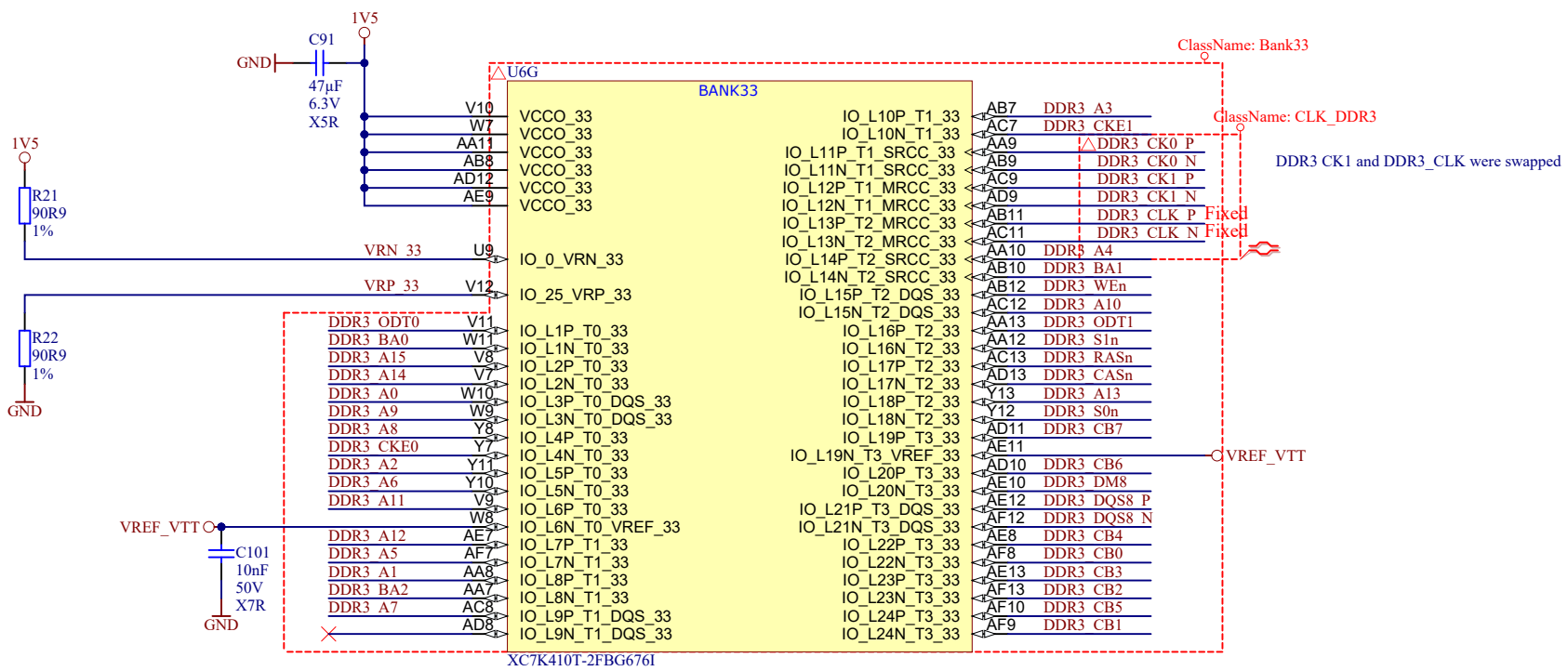
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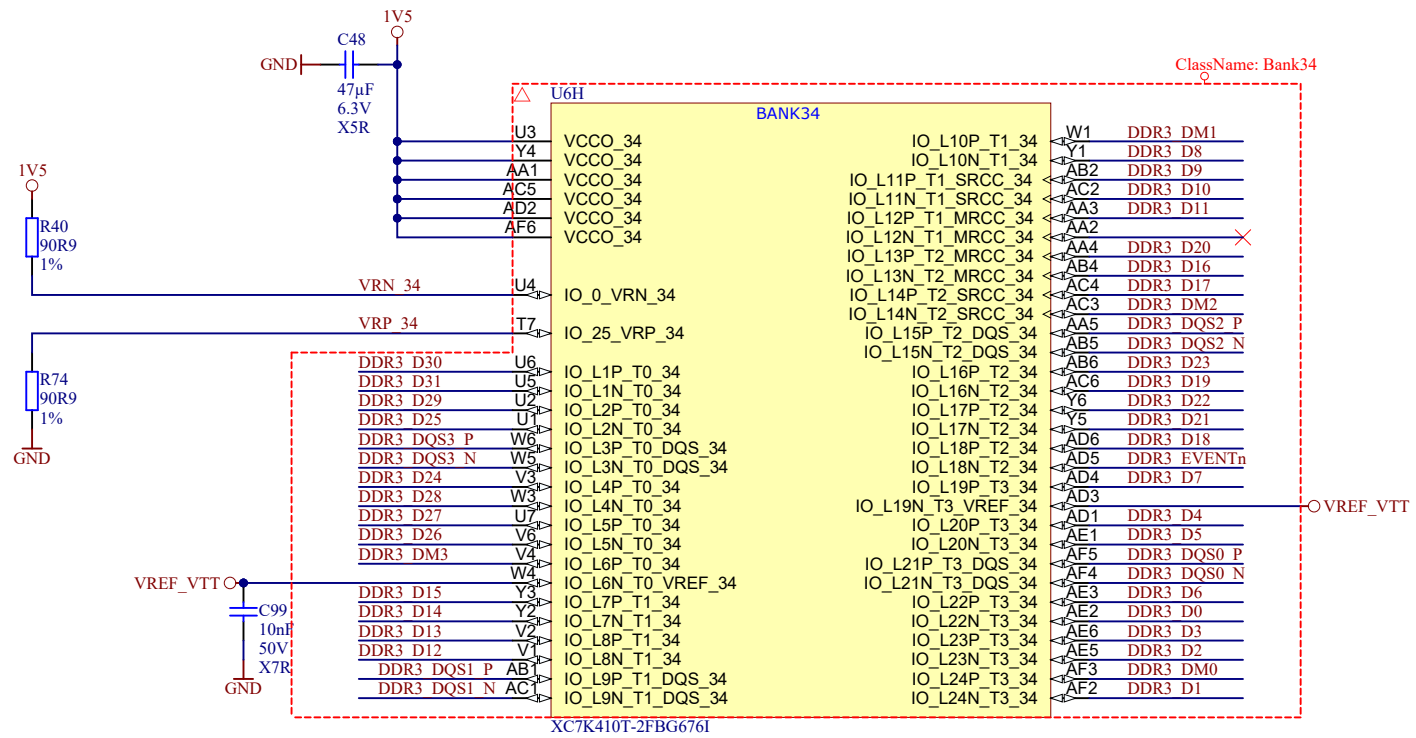
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 14 of 34
Filename: FPGA_BANK_32.SchDoc		



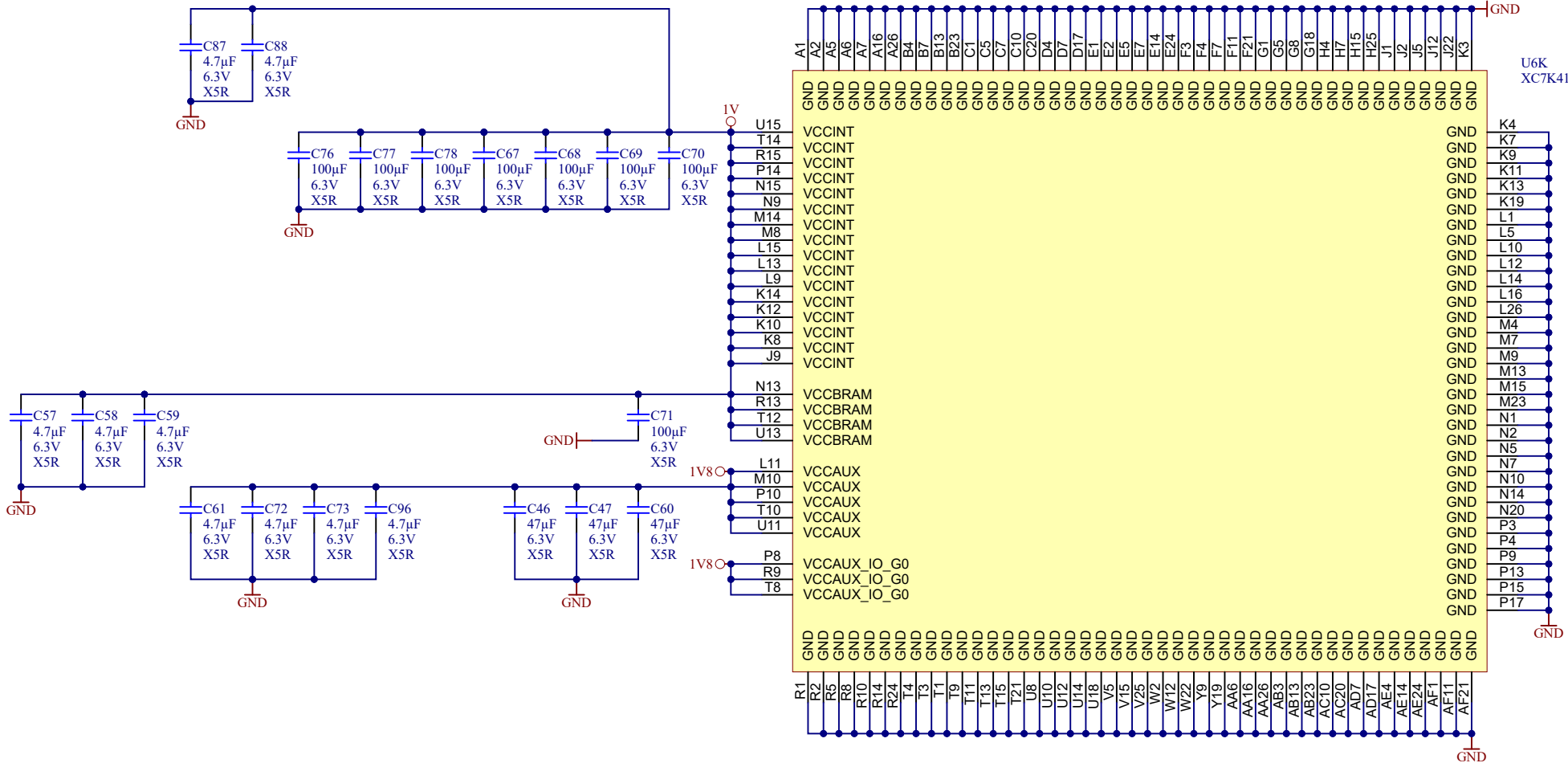
DDR3 CK1 and DDR3_CLK were swapped



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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 15 of 34
Filename: FPGA_BANK_33.SchDoc		



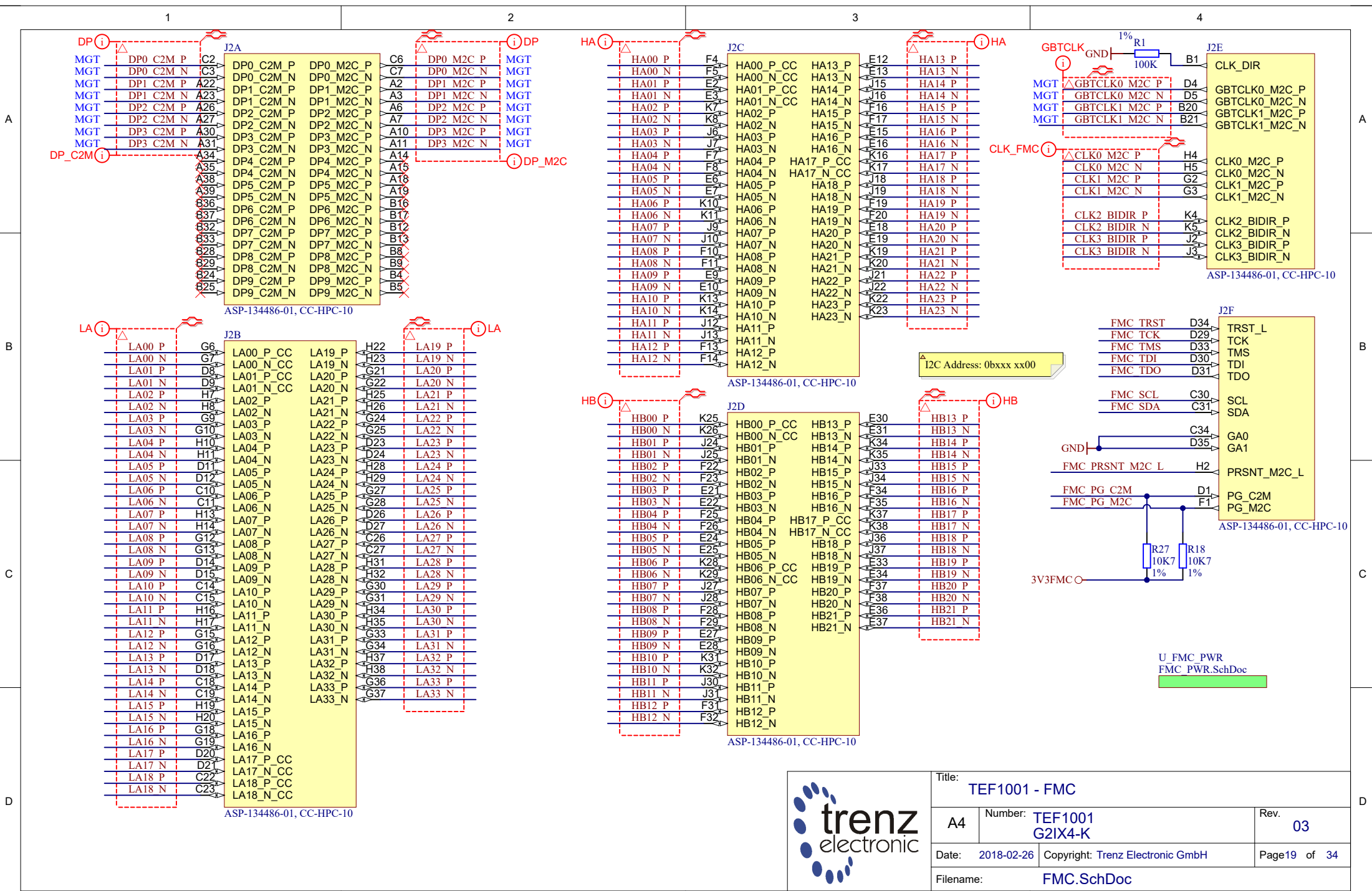
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A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 16 of 34
Filename: FPGA_BANK_34.SchDoc		



U6K
XC7K410T-2FBG6761



Title: TEF1001 - FPGA_POWER		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 18 of 34
Filename: FPGA_POWER.SchDoc		



ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10

ASP-134486-01, CC-HPC-10



Title: TEF1001 - FMC		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 19 of 34
Filename: FMC.SchDoc		

U FMC_PWR
FMC_PWR.SchDoc

1

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A

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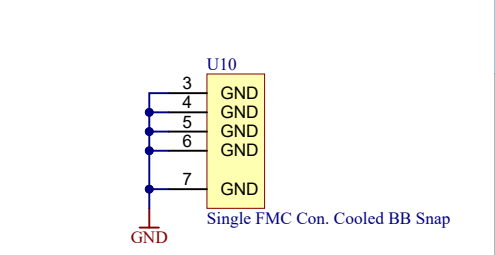
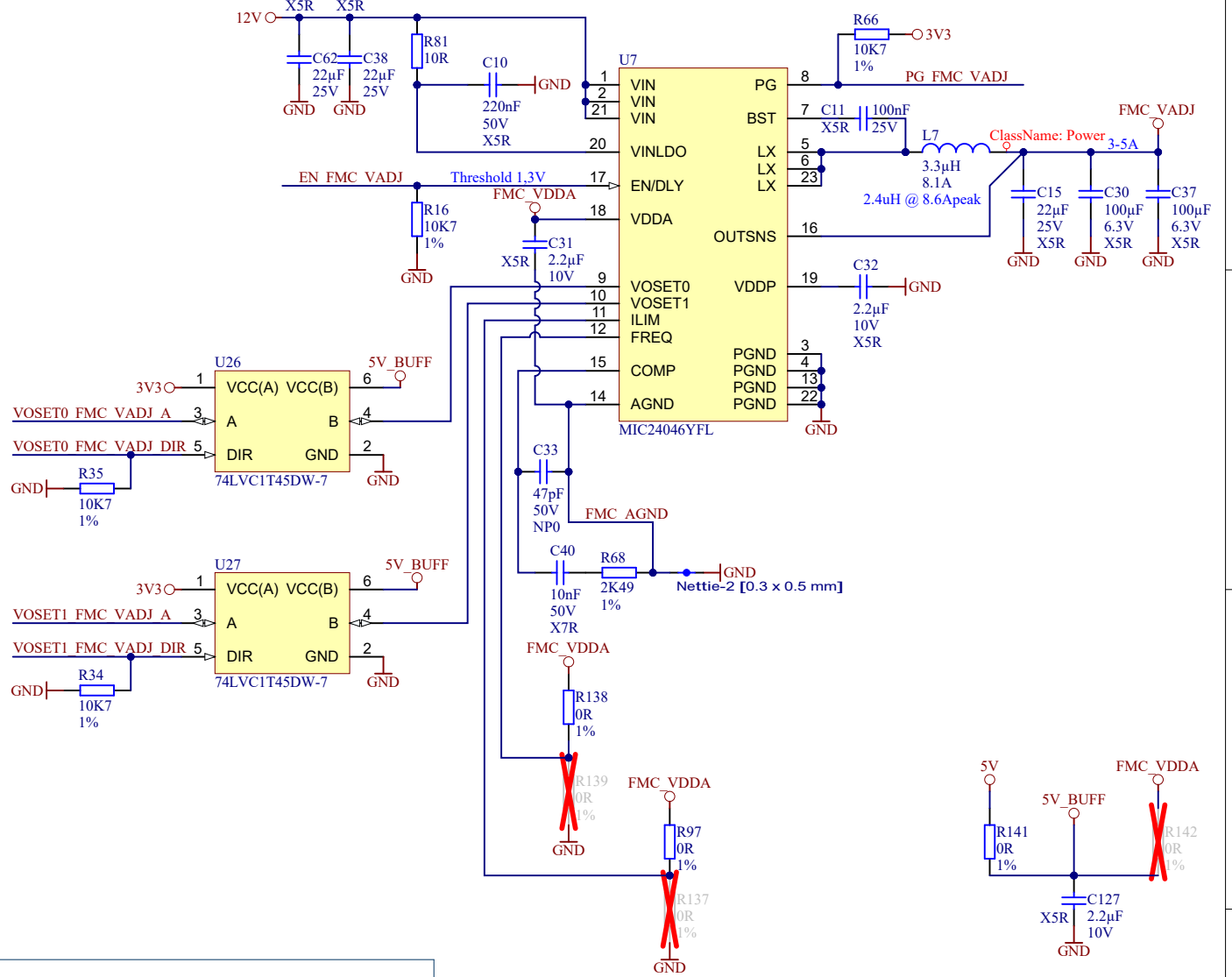
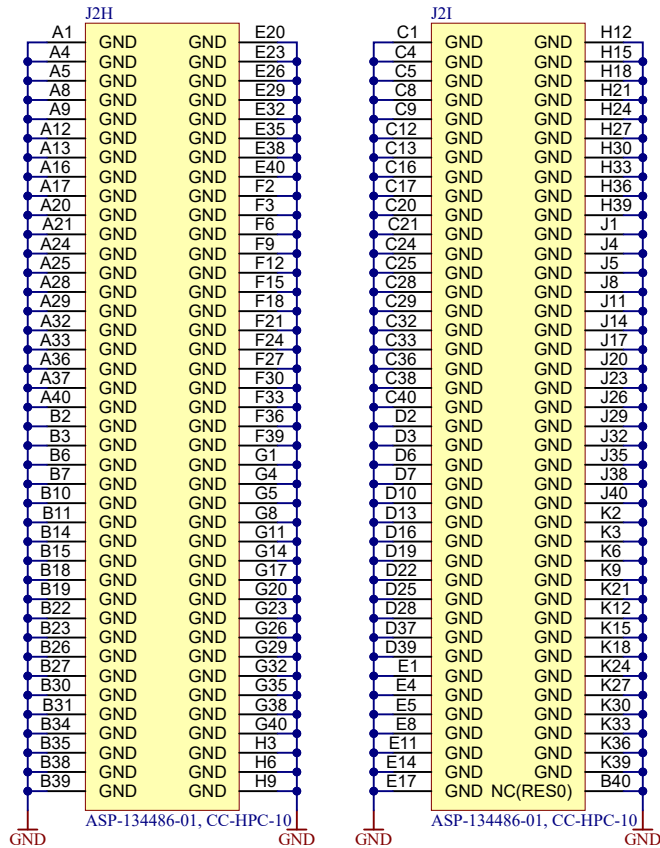
B

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C

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D



Title: TEF1001 - FMC_PWR		
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page20 of 34
Filename: FMC_PWR.SchDoc		

1

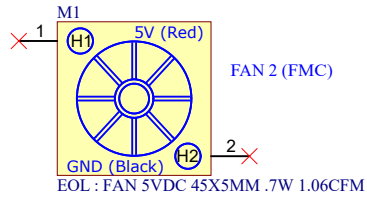
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U_FMC
FMC.SchDoc

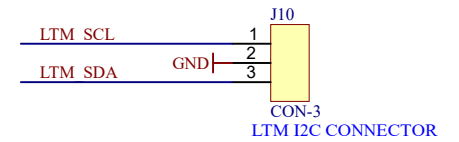
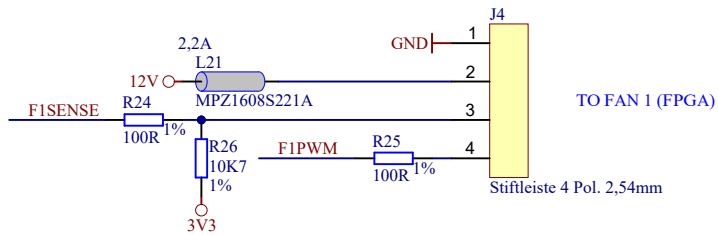
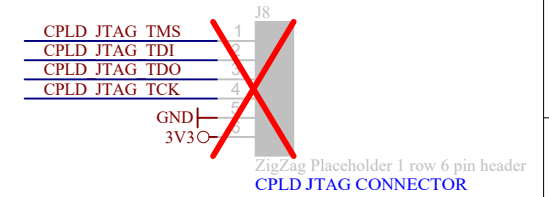
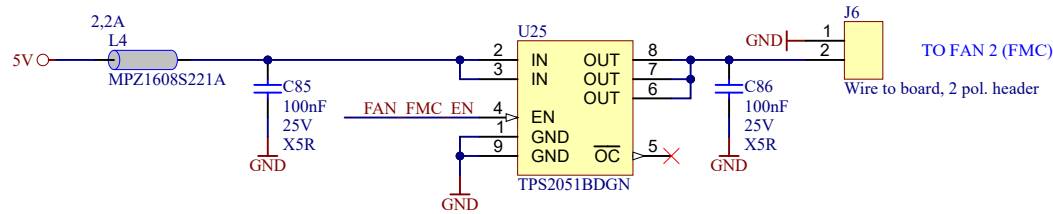
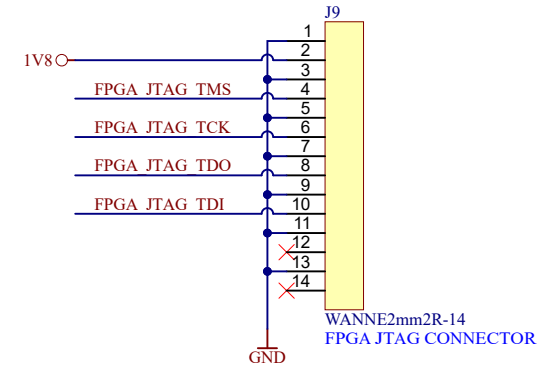
U_PCIE_CONN
PCIE_CONN.SchDoc



JX1
Wire to board, 2 pol. housing

JCT1
Crimp Terminal 4809, 22-30 AWG

JCT2
Crimp Terminal 4809, 22-30 AWG



Title: TEF1001 - CONN		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page22 of 34
Filename: CONN.SchDoc		

A

B

C

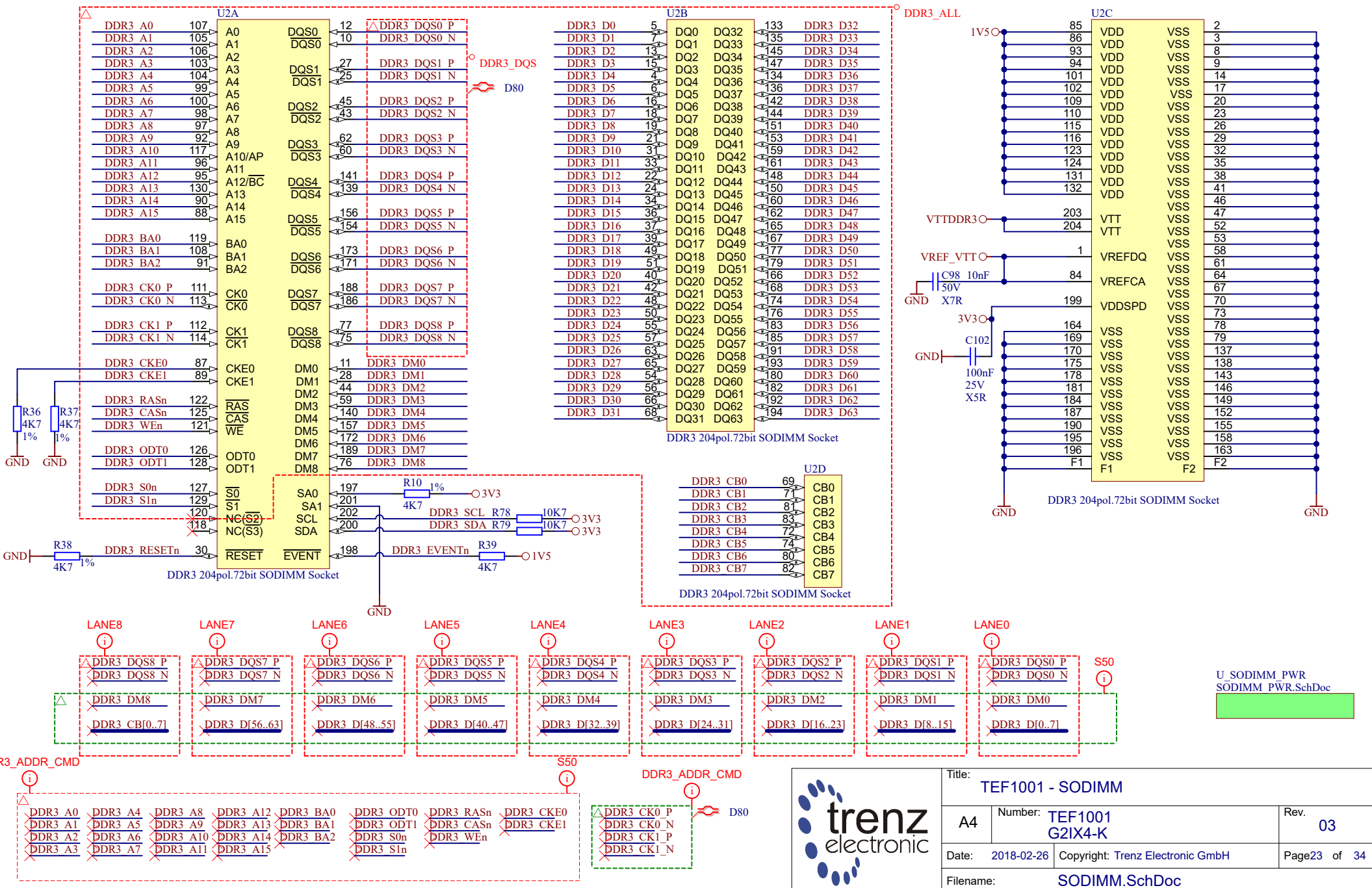
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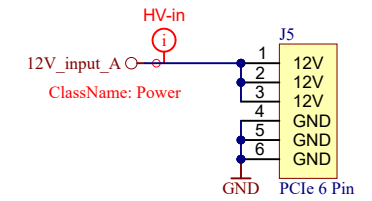
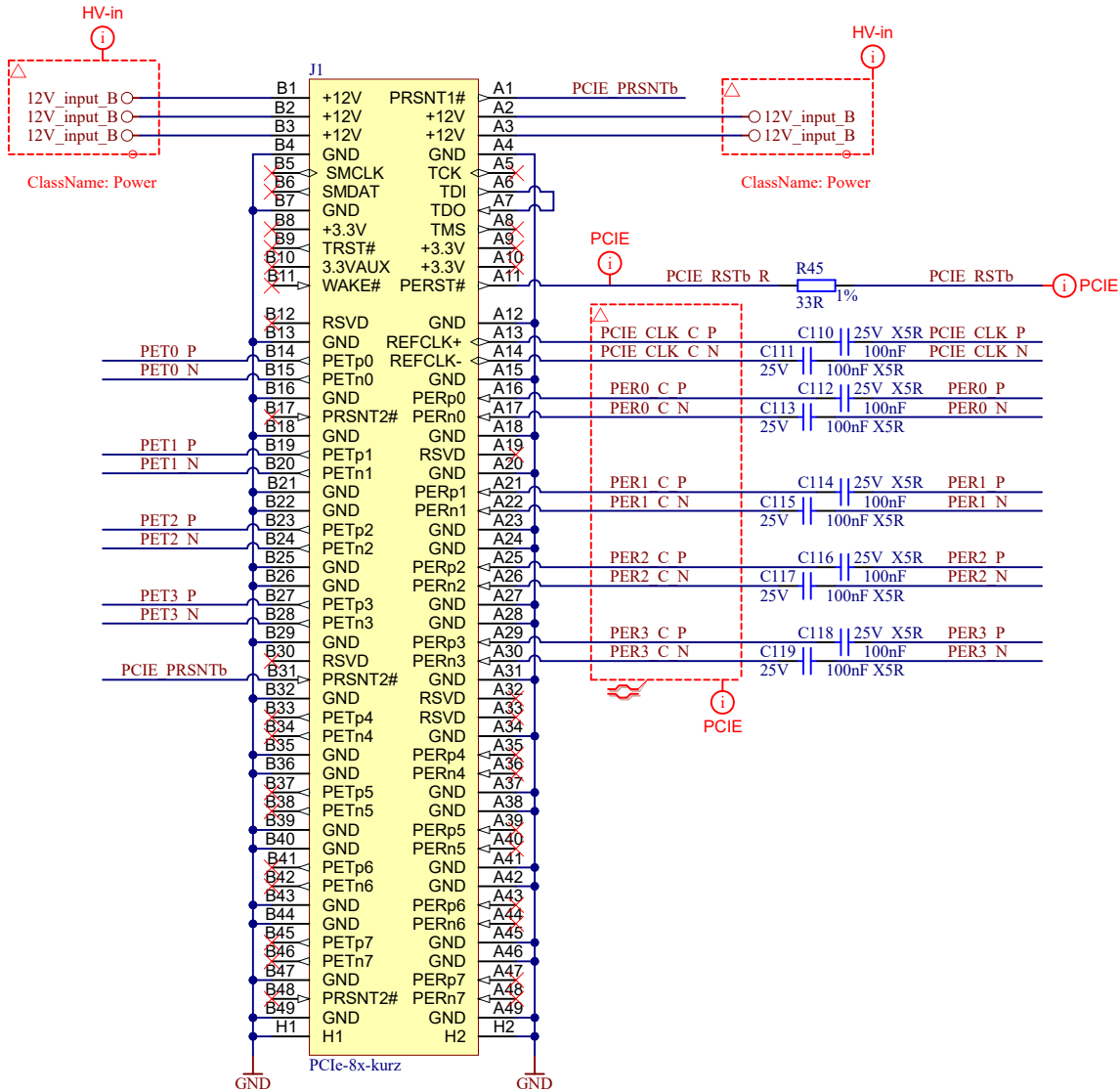
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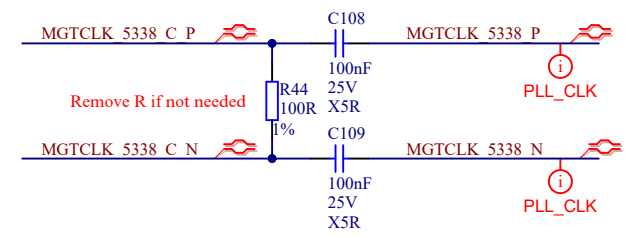
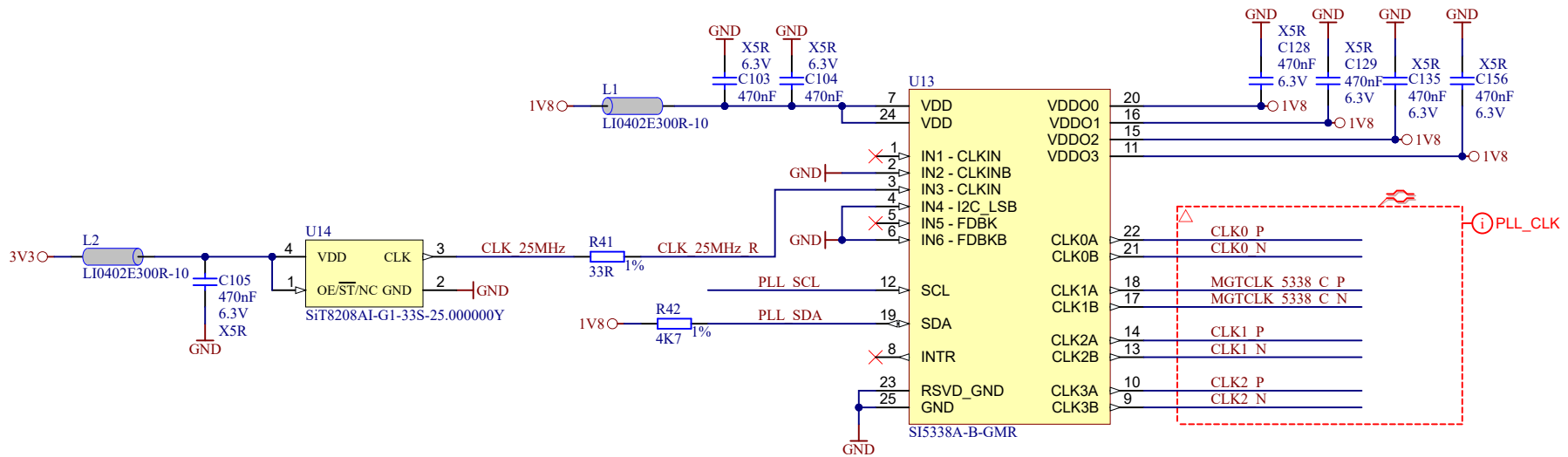
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Title: TEF1001 - SODIMM		
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Date: 2018-02-26	Copyright: Trenz Electronic GmbH	
Page 23 of 34		Page 23 of 34
Filename: SODIMM.SchDoc		

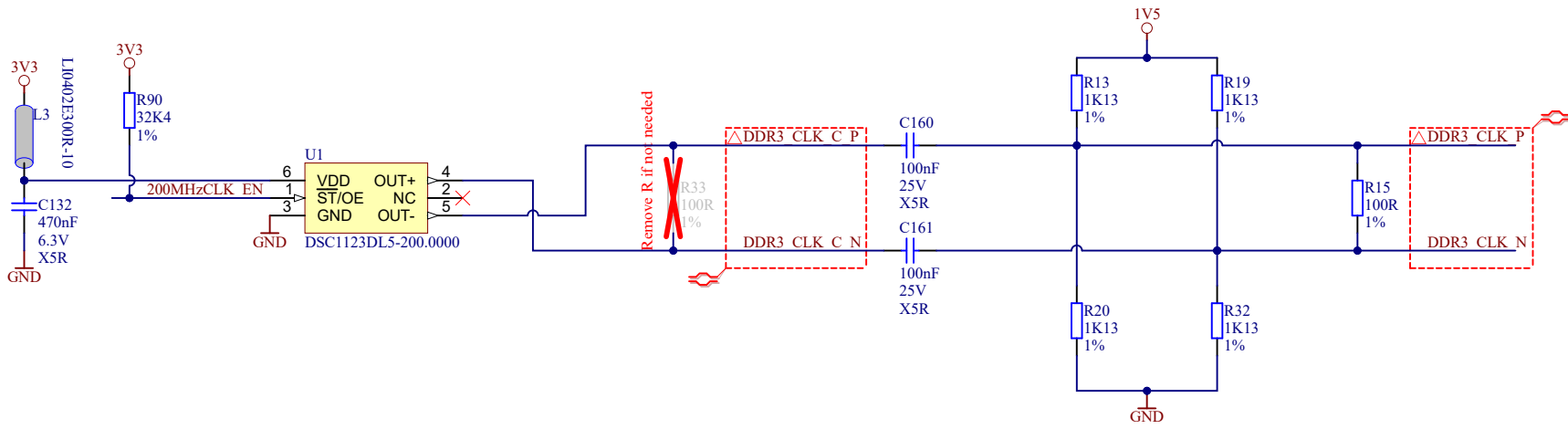



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			A4	Number: TEF1001 G2IX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH		Page24 of 34
Filename: PCIE_CONN.SchDoc				



			Title: TEF1001 - CLK-SI5338	
			A4	Number: TEF1001 G2IX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH		Page25 of 34
Filename: CLK-SI5338.SchDoc				

U_CLK-SI5338
CLK-SI5338.SchDoc



		Title: TEF1001 - CLOCK	
		A4	Number: TEF1001 G2IX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH	
Filename: CLOCK.SchDoc		Page 26 of 34	

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PWR_12V_1V5.SchDoc

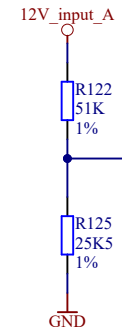
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U_PWR_1V
PWR_1V.SchDoc

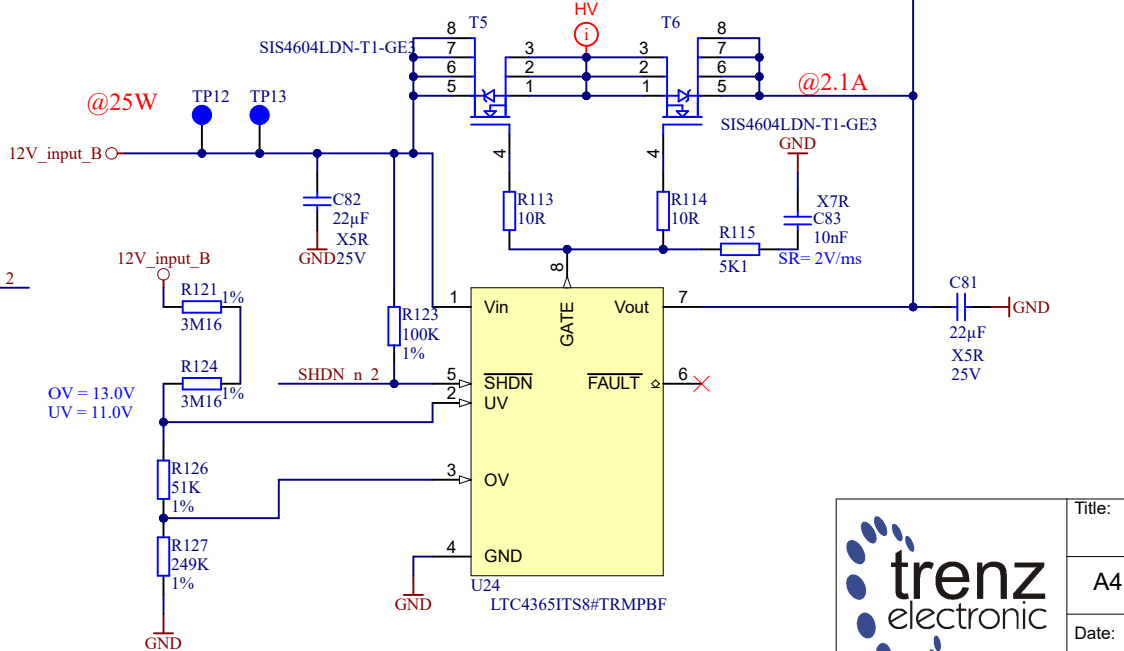
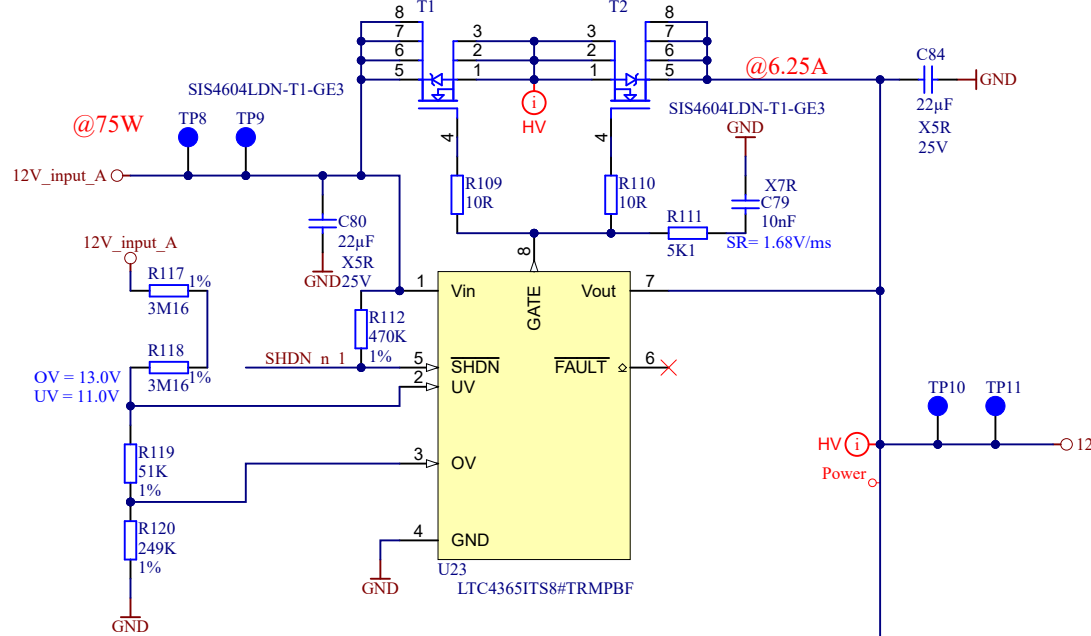
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PWR_MGT.SchDoc

U_PWR_1V8
PWR_1V8.SchDoc

U_PWR_5V
PWR_5V.SchDoc



U_POWER_ENs_PGs OVERVIEW
POWER_ENs_PGs OVERVIEW.SchDoc



FAN FPGA
FMC J2 Connector MIN11.4V MAX12.6V (Sec. 5.10. Power Supply Req.)
U4 REGULATOR 1V MIN5.75V MAX26.5V
U3 REGULATOR 4V&1V5 MINS.75V MAX26.5V
U9 REGULATOR 3V3 MIN4.5V MAX17V
U8 REGULATOR 5V MIN6V MAX17V



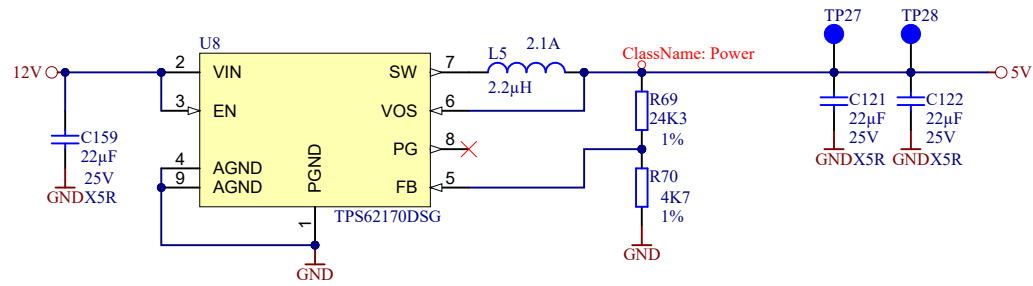
Title: TEF1001 - POWER		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page 27 of 34
Filename: POWER.SchDoc		

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Title: TEF1001 - PWR_5V		
A4	Number: TEF1001 G2IX4-K	Rev. 03
Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page28 of 34
Filename: PWR_5V.SchDoc		

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A

A

B

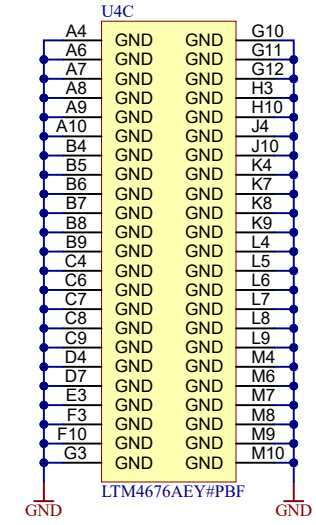
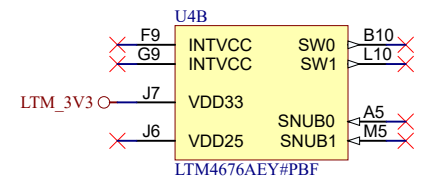
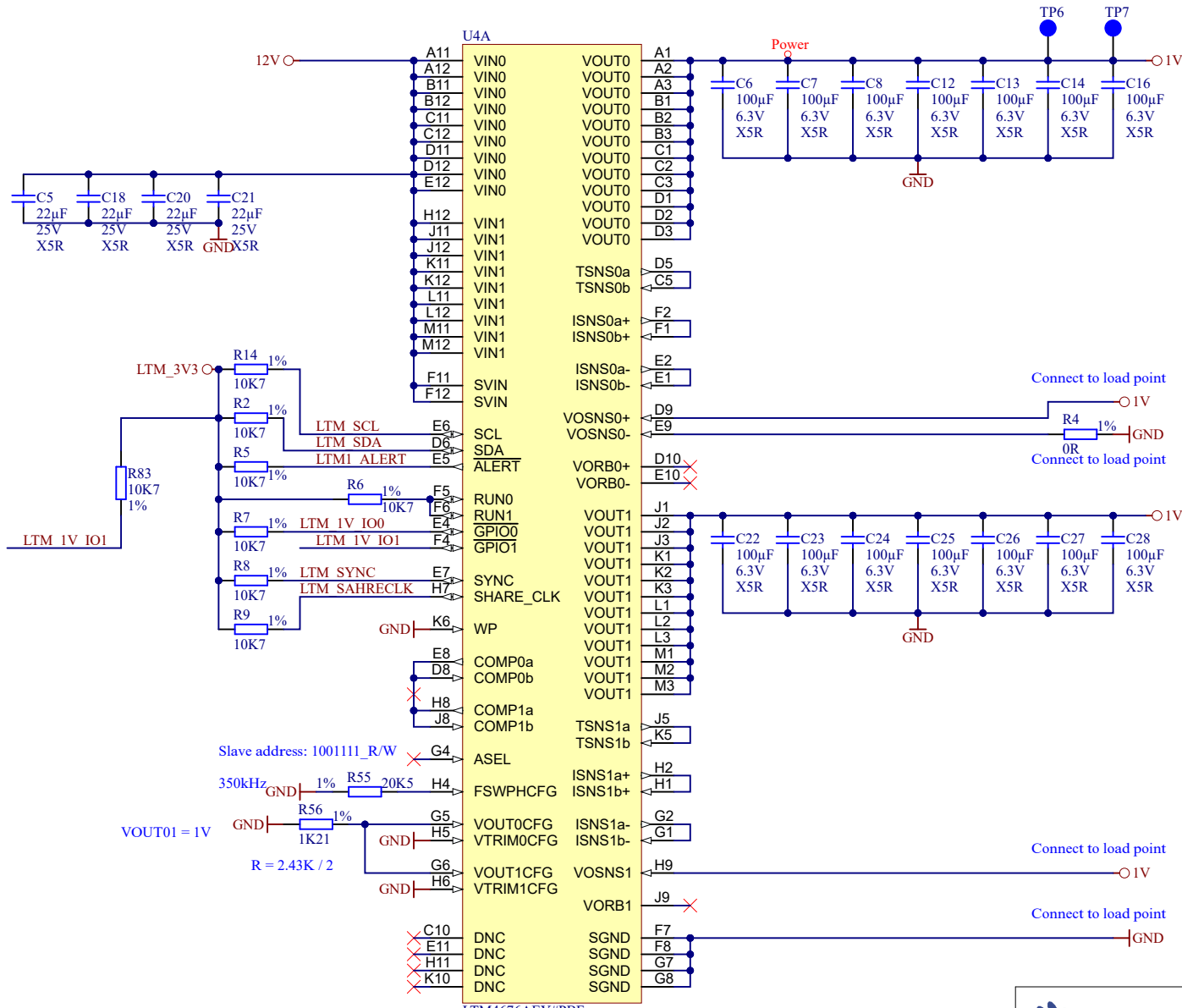
B


C

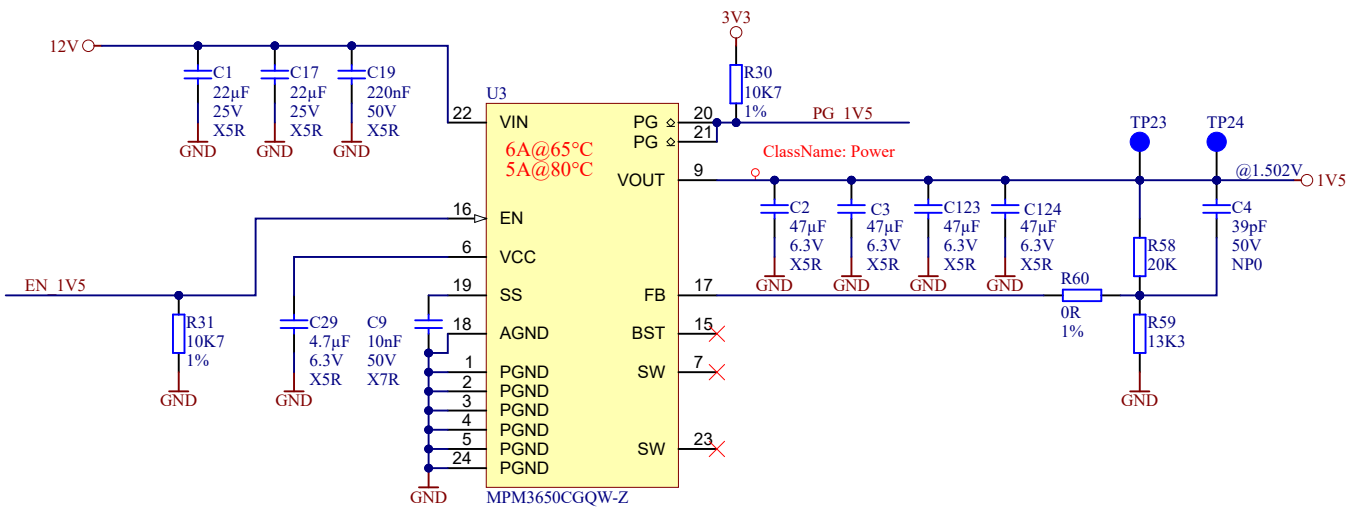
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D

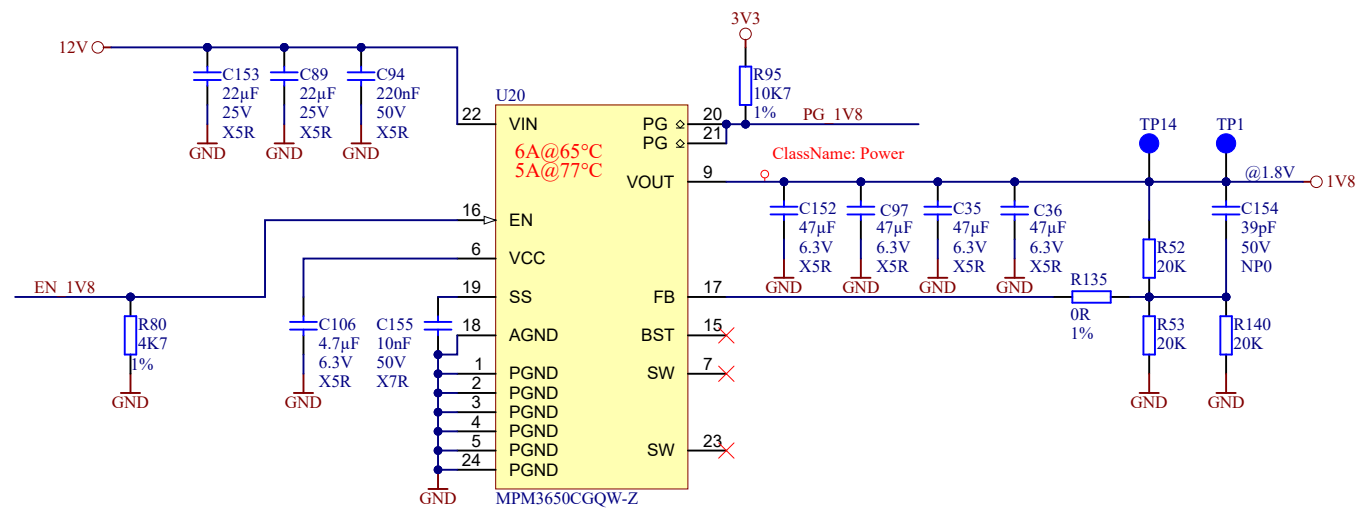
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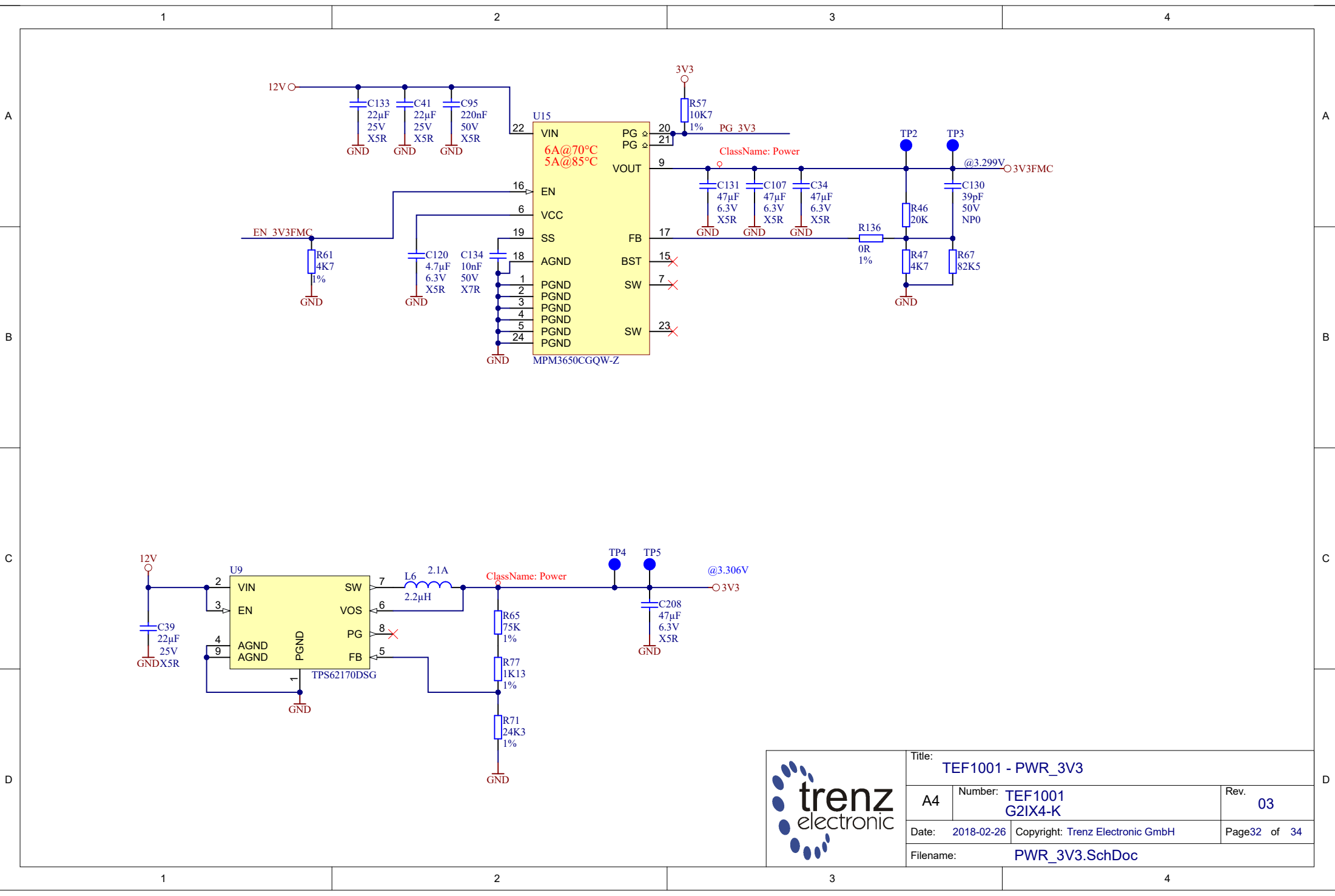

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		A4	Number: TEF1001 G2IX4-K
Date: 2018-02-26		Copyright: Trenz Electronic GmbH	
Page 29 of 34		Page 29 of 34	
Filename: PWR_1V.SchDoc			



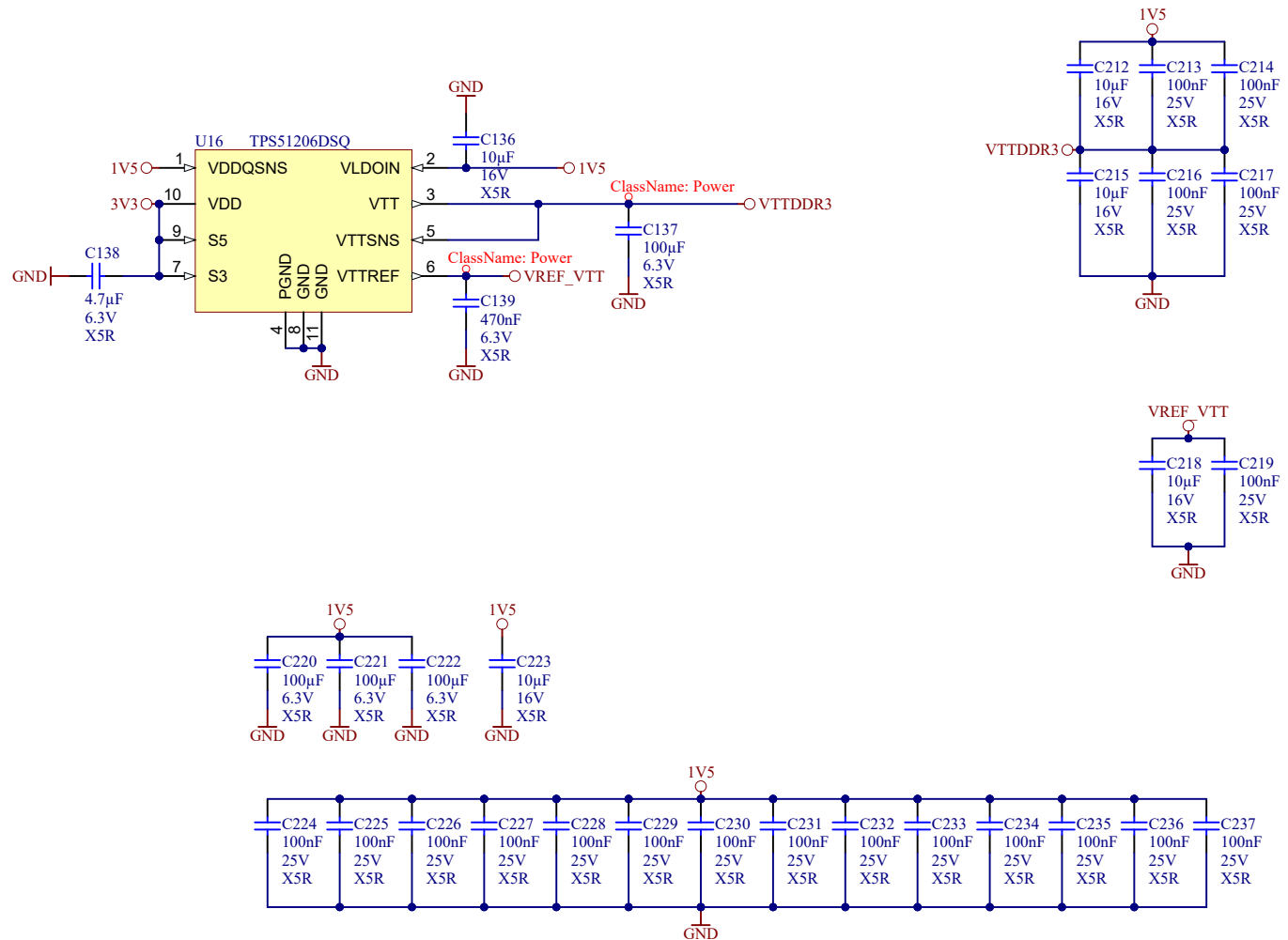
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	A4	Number: TEF1001 G2IX4-K	Rev. 03
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page30 of 33
	Filename: PWR_12V_1V5.SchDoc		



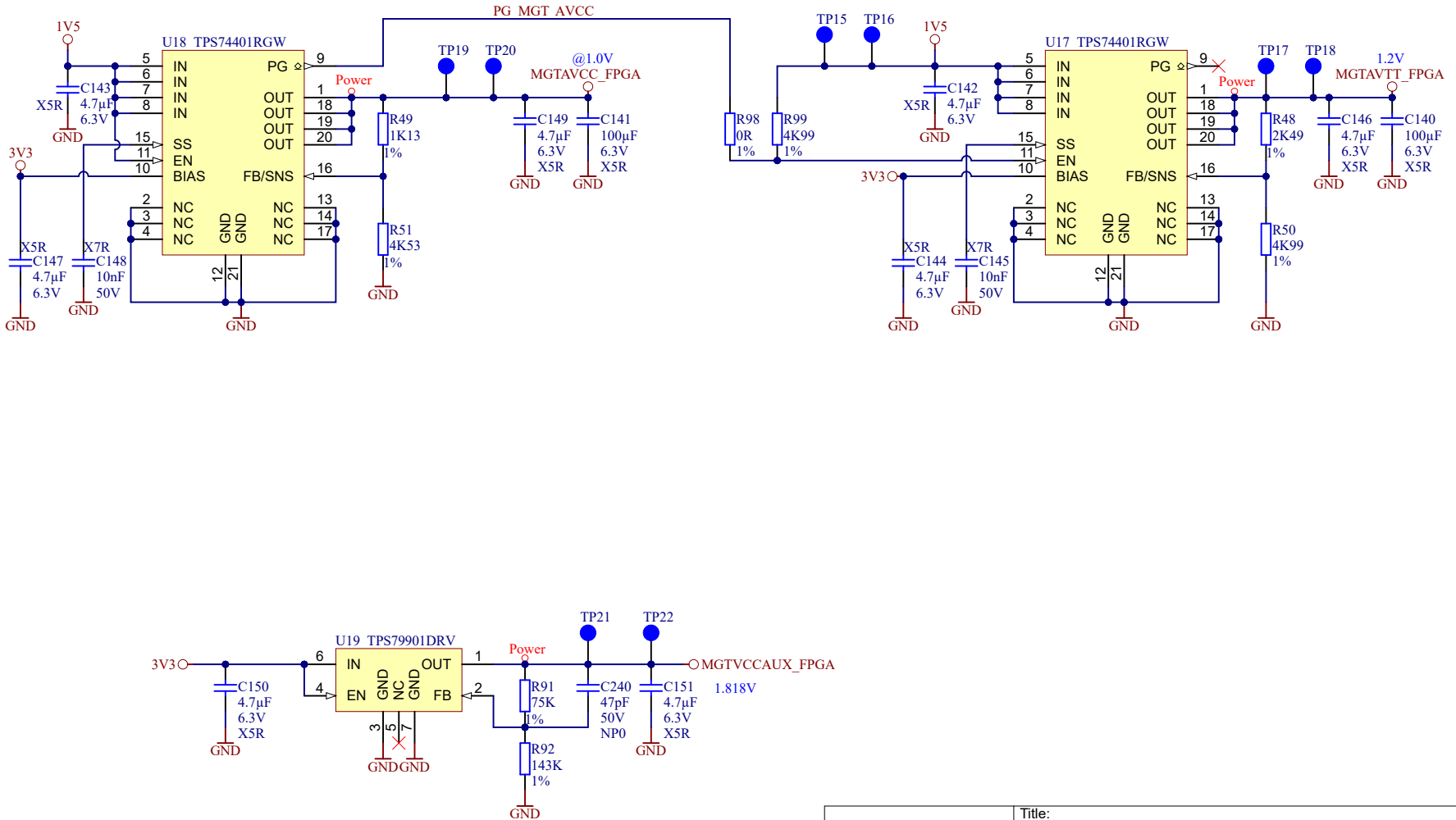
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